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LOW-VOLTAGE POWER SUPPLY DISTRIBUTION SYSTEM DEVELOPMENT IN A SCIENTIFIC SPACE MISSION

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PRESENTA:
HÉCTOR HUGO SILVA LÓPEZ

TUTOR PRINCIPAL
Dr. GUSTAVO ADOLFO MEDINA TANCO, ICN-UNAM
COMITÉ TUTOR
Dr. AUGUSTO GARCÍA VALENZUELA, CCADET-UNAM
Dr. GABRIEL EDUARDO SANDOVAL ROMERO, CCADET-UNAM

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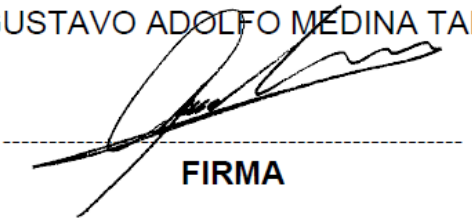
JURADO ASIGNADO:

Presidente:	Dr. Gabriel Eduardo Sandoval Romero
Secretario:	Dr. Augusto García Valenzuela
Vocal:	Dr. Gustavo Adolfo Medina Tanco
1 er. Suplente:	Dr. Jorge Prado Molina
2 do. Suplente:	Dr. Salvador Landeros Ayala

Lugar donde se realizó la tesis: INSTITUTO DE CIENCIAS NUCLEARES, UNAM

TUTOR DE TESIS:

Dr. GUSTAVO ADOLFO MEDINA TANCO



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CONTENTS

APBUS	Attached Payload Bus
ASIC	Application Specific Integrated Circuit
AWG	American Wire Gauge
BCDU	Battery Charge/Discharge Unit
CAM	Camera
CC	Contact Closure
CCB	Cluster Control Board
CLKB	Clock Board
CMOS	Complementary Metal Oxide Semiconductor
CNES	French Space Agency
COTS	Components Of The Shelf
CPU	Central Processor Unit
CW	Cockcroft–Walton
dcEL	DC Electronic Load
DDCU	DC-DC Converter Unit
DP	Data Processor
DPA	Distributed Power Architecture
DPDT	Dual Pole-Dual Throw
DSP	Digital Signal Processor
DST	Data Storage
EAS	Extensive Air Shower
EC	Elementary Cell
EF	Exposure Facility
ELS	Electronics
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPS	Electrical Power System
ESA	European Space Agency
FEE	Front End Electronic
FPGA	Field Programmable Gate Array
FR	Flame Retardant
FSE	Focal Surface Electronics
GEO	Geostationary Orbit
GND_M	Mechanical Ground
GON	Gondola
GPSR	Global Position System Receiver
GRP	Ground Reference Point
GTU	Gate Time Unit
HEO	Highly Eccentric Orbit

HK	House Keeping
HL_CMD	High Level Command
HVPS	High Voltage Power Supply
IBC	Intermediate Bus Converter
IC	Integrated Circuit
IDAQ	Interface Data Acquisition Board
IPBUS	Internal Power Bus
IPC	Institute for Printed Circuits
IR	Infrared
ISS	International Space Station
JAXA	Japanese Space Agency
JEM-EUSO	Japanese Experiment Module – Extreme Universe Space Observatory
LdReg	Load Regulation
LEO	Low Earth Orbit
LIDAR	Light Detection and Ranging
LnReg	Line Regulation
LR	Latching Relay
LVDS	Low Voltage Differential Signaling
LVPDS	Low Voltage Power Distribution System
LVPS	Low Voltage Power Supply
MAPMT	Multi-Anode Photo Multiplier Tube
MBSU	Main Bus Switching Unit
MCU	Microcontroller Unit
MEO	Medium Earth Orbit
Mfgr	Manufacturer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPU	Microprocessor Unit
NASA	National Aeronautics and Space Administration
NEMA	National Electrical Manufacturers Association
niPOL	non-isolated Point-Of-Load
NOSYCA	New Operational System for the Control Aerostats
Op-Amp	Operational Amplifier
OPT	Optics
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PDMB	Photo Detector Module Board
PMMA	Polymethyl-methacrylate
PPBUS	Primary Power Bus
PRM	Pre-Regulator Module
PSA	Pressure Sensitive Adhesive

PWM	Pulse Width Modulation
PWP	Power Pack
PWS	Power
RAID	Redundant Array of Independent Disks
RBI	Remote Bus Isolator
RF	Radio Frequency
RPC	Remote Power Controller
SATA	Serial Advanced Technology Attachment
SIREN	Système d'Interface Reseau Nosyca
SMD	Surface Mount Device
SMPS	Switching Mode Power Supplies
SPE	Single Photoelectron
SPI	Serial Peripheral Interface
SSD	Solid State Disk
SSPC	Solid State Power Controller
SSU	Sequential Shunt Unit
TDK	TDK Lambda
TES	Telescope
TH	Through-Hole
TPW	Traco Power
UHECR	Ultra High Energy Cosmic Rays
UV	Ultra Violet
V&I	Voltage and Current
VTM	Voltage Transformation Module
XPP	XP Power

A typical space flight system comprises three system segments which are coordinated and designed according to the mission objectives. These segments are related with: space, transfer and ground topics. The space segment comprises the spacecraft and its payload in orbit. The transfer section provides the transport for the spacecraft and its payload into space by a launcher (typically a rocket). Finally, a ground station is necessary in order to control and monitor the spacecraft and its payload as well as to distribute and process the payload data [1].

Mission types and payloads for spacecraft are many and varied. There are nine characteristic areas of applications for space flight missions: Earth and Weather observation, Technology testing, Fundamental research, Communication, Navigation, Military, Planetary exploration and Human space flight. Each one of these areas has its particular objectives which define the central application element of a space flight mission: the payload [1]. Successful payload operations open the door to mission success or put it in doubt. The sorts of payloads depend on the spacecraft mission, for example: radars, cameras, and sensors are essential in Earth and weather observations. But definitely, every payload needs power.

Electrical power is needed for the operation of all active spacecraft systems and subsystems. The electrical power system (EPS) of a spacecraft comprises power conversion, energy storage, regulation, power conditioning, protections, and power distribution to the various users via the on-board low-voltage power distribution (LVPD) system [1]. These stages are included in one of the following three sections: the *primary energy source* that basically converts a ‘fuel’ into electricity power, as an example a spacecraft that use a solar panel as the primary energy source, the ‘fuel’ in this case is the solar radiant energy; the *secondary energy source* that is required for storage and regulation of energy and subsequently deliver electrical power to spacecraft and its payload (when the primary system’s energy is not available); and finally, the *power control and distribution network*, that is required to deliver appropriate voltage and current levels to all spacecraft loads when required [2].

The aim of this work is to describe the research, development and validation of a proposal of LVPD system for a sub-orbital particle physic instrument, which represents a fully operational prototype for the space instrument JEM-EUSO (Japanese Experiment Module – Extreme Universe Space Observatory).

The work is comprised by five chapters. In chapter one, it’s given a concise background about near-earth space environment in order to establish the operational environmental conditions of a spacecraft. After that, is summarized the research about state-of-the-art of a spacecraft EPS.

Finally, the research will focus on the advances of LVPS architectures at industrial and telecom applications. The latter, in order to propose an optimal solution for secondary power distribution section of a spacecraft instrument in the fundamental physics research field.

The second chapter is devoted to explain the complexity of JEM-EUSO project, giving a concise description of hierarchical architecture of the instrument, as well as a brief subsystems description. Therefore, it will be justified the necessity of a reduced version test bench of JEM-EUSO instrument: EUSO-Balloon. In the final section, are explained the objectives of EUSO-Balloon instrument as well as its main components.

In chapter three, it is defined the problem statement, the research objectives and the significance of research since fundamental physics point of view and technical development. Although the fourth chapter starts with EUSO-Balloon requirements and specifications, the purpose of this chapter is to describe the development of the LVPS strategy proposed for a sub-orbital scientific mission regarding functional, environmental and communication requirements.

On other hand, chapter five describes specific tests related to electrical, data management and thermo-vacuum performance of different modules that comprise the LVPS subsystem at EUSO-Balloon instrument. The tests performed have the purpose to guarantee the safe operation of the subsystem developed at low pressure conditions.

Finally, conclusions and to do work sections are stated for improving the development of LVPD subsystems in the near-Earth space field projects.

I.1 Spacecraft Power Systems

In space, the EPS generates, stores, conditions, controls, and distributes power within the specified voltage levels to all bus and payload equipment. The protection of the power system components in case of all credible faults is also included. The basic components of the photo-voltaic power system are the solar array, solar array drive, battery, battery charge and discharge regulators, bus voltage regulator, load switching, fuses, and the distribution harness. The harness consists of conducting wires and connectors that connect various components together.

The near-Earth space environment, i.e., thermosphere and ionosphere, presents a substantial risk to space systems. The spacecraft power system must withstand the space environment and meet full performance specifications over the entire mission life, starting from the launch phase to disposal at the end of life. In that way, the environmental factors also affect the overall design of all other components of the power system [3].

I.2 Near-Earth Space Environment

A spacecraft is affected by physical conditions in space which go far beyond the well-known environmental requirements on Earth. Typical features of the space environment are high vacuum, short-wave solar radiation (electromagnetic waves), ultraviolet X-rays and gamma radiation from the galactic background, high-energy particles (electrons, protons, neutrons and alpha particles), the cold background of space, microgravity, aerodynamic drag of the atmosphere at low Earth orbits, and the influence of atomic oxygen. These conditions have to be considered during the design and realization of a spacecraft [1].

The conditions depend on the orbit of the mission. The main distinctions are:

- Low Earth Orbit (LEO).
- Medium Earth Orbit (MEO).
- Geostationary Orbit (GEO).
- Highly Eccentric Orbit (HEO).
- Interplanetary space trajectories.

LEO is approximately a circular orbit at low altitude. The International Space Station (ISS) operates in LEO. Most communications satellites operate in GEO, but some newer constellations are planned and/or placed in LEO between 350 and 2000-km altitudes and 30 to 90º inclinations (see figure 1). Being closer to the Earth, smaller and simpler satellites can be used in this orbit. On the negative side, LEO communications satellites require tracking of omni-directional antennas, and many of them are needed for wide coverage [3].

MEO sometimes called Intermediate Circular Orbit (ICO) because is the region of space between LEO and GEO. The orbital periods of MEO satellites range from about 2 to 12 hours. Some MEO satellites orbit in near perfect circles, and therefore have constant altitude and travel at a constant speed. Due this, a fleet of several MEO satellites, with orbits properly coordinated can provide global wireless communication coverage. Because MEO satellites are closer to the earth than geostationary satellites, earth-based transmitters with relatively low power and modest-sized antennas can access the system. Because MEO satellites orbit at higher altitudes than LEO satellites, the useful footprint (coverage area on the earth's surface) is greater for each satellite. Thus a global-coverage fleet of MEO satellites can have fewer members than a global-coverage fleet of LEO satellites [3].

GEO orbit is a very special geosynchronous orbit, and, in fact, is unique. It is exactly circular with a radius of 35,786km in the Earth’s equatorial plane with zero degree inclination and zero eccentricity.

A satellite placed in this orbit is synchronized with the Earth's rotation rate and direction (eastward). It does not move with respect to the Earth, and sees the same object on the Earth steadily. The orbit period is the same as that of the Earth's rotation, i.e., 23 h 56m 4.09 s. As a result, the satellite's beam-to-Earth and the ground station's beam-to-satellite are steady in position. This simplifies the design and operating requirements of both the satellite and the ground station. However, it takes more fuel to reach and maintain the geostationary orbit than any other orbit around the Earth [3].

HEO, also called Highly Elliptical Orbit Molniya, represents one specific orbit named in that way after the Molniya Soviet communication satellites which used them. The advantage of this orbit is a good coverage of the entire northern hemisphere. The disadvantage is no coverage over the southern hemisphere. Moreover, it requires more satellites and needs two tracking antennas at each ground stations [3].

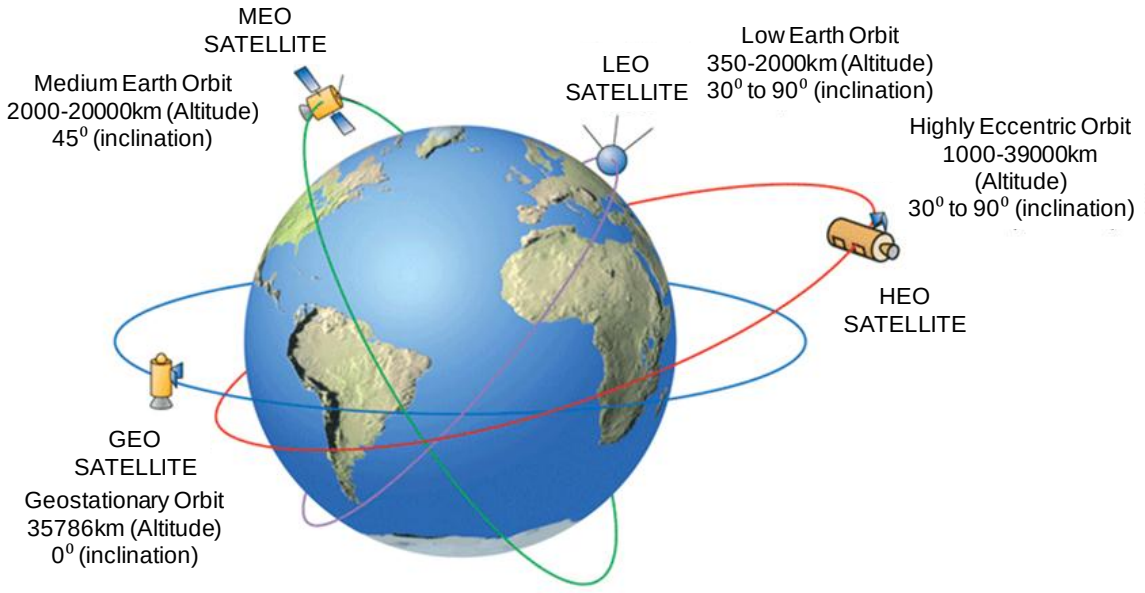


Figure1. Satellite Earth orbit map [4].

The interplanetary space trajectories have remained an activity of unmanned space flight except for the Apollo missions to the Moon. Over the decades dozens of space probes have flown to all planets (except Pluto) as well as to many asteroids and comets. In many cases these were not only fly-bys but even orbiting and landing missions. For instance, robotic vehicles have been deployed on Mars, or cometary material has been returned to Earth. Special challenges of interplanetary space flight are significant signal latency, long flight time, and navigation. Moreover, a sufficient power supply is one of the greatest problems in the outer Solar System [1].

I.3 Operational Spacecraft Environment

Spacecraft operation is characterized by its remoteness from the Earth and thus the loss of the Earth's protective shield, namely, the atmosphere. This atmosphere evidently provides a suitable stable environment in which the human species has been able to evolve. Coupled with the gravitational force of the Earth, 'the one *g* environment', it provides familiarity in design and its removal has significant and sometimes unexpected implications [1].

Before considering the environment, it should be noted that the different phases in the life of a space vehicle, namely, manufacture, pre-launch, launch and finally space operation, all have their own distinctive features. Although a space vehicle spends the majority of its life in space, it is evident that first it must survive to terrestrial conditions like dust and humidity for complete success. Whilst the manufacturing phase is not part of this work, it has an effect upon the reliability and the ability to meet design goals [1].

In the launch phase the design, manufacture and assembly of a large spacecraft, and its final integration into a launch vehicle is a lengthy process, lasting typically 5 to 10 years. Components and subsystems may be stored for months or even years prior to launch. Careful environmental control during such periods is essential if degradation of the spacecraft system as a whole is to be avoided [2]. On the other hand, during the launch phase high levels of acceleration, shock, and vibration are present. The resulting stress levels, varying with the launch vehicle, have effects on the power system design, particularly on the solar panels. For example, in transfer orbit, the solar panel is still folded, but must withstand the accelerating force at perigee and the braking force at apogee. Thermally, the outer solar panels must withstand the Earth’s heat radiation and albedo, in addition to the solar radiation, without exceeding the specified temperature limit [3].

Now then, regarding the environmental conditions, the lack of gravity and atmosphere in space has significant effects on the power system design. Zero gravity and vacuum jointly deprive all spacecraft equipment from the natural convection cooling which is normal on Earth. The thermal design in space, therefore, depends primarily on conduction cooling and, to some extent, on radiation cooling. The heat rejection to the outer space, however, must depend only on radiation cooling. On the other hand, the vacuum causes sublimation and outgassing, more in some materials than others. The subsequent condensation of the sublimed vapor on cold surfaces can cause short circuits in electrical parts. Since zinc has a high sublimation rate, and some polymers have high outgassing rates, their use in space is restricted. The solar array current collecting slip rings and brushes can experience cold welding under high contact pressure in a vacuum. The use of lubricants having low sublimation rates, or keeping them in sealed pressurized enclosures, is therefore important [3].

There are other issues that constrain the power system design like Earth's magnetic field, solar flares and solar wind, charged particles that comes with the sun's radiation, meteoroids and debris.

The Earth's magnetic field covers the magnetosphere, a doughnut shaped region of space influenced by the Earth's magnetic field. It acts on the electrons and protons coming from the space. The Van Allen radiation belts (see figure 2) are parts of the magnetosphere that contain a large number of particles. The magnetosphere normally shields the Earth from these particles. However, when a disturbance on the sun radiates an abundance of particles, some reach the Earth's atmosphere near the magnetic poles and cause a glow known as an aurora, popularly known as the northern lights (or the southern lights, in the southern hemisphere) [3].

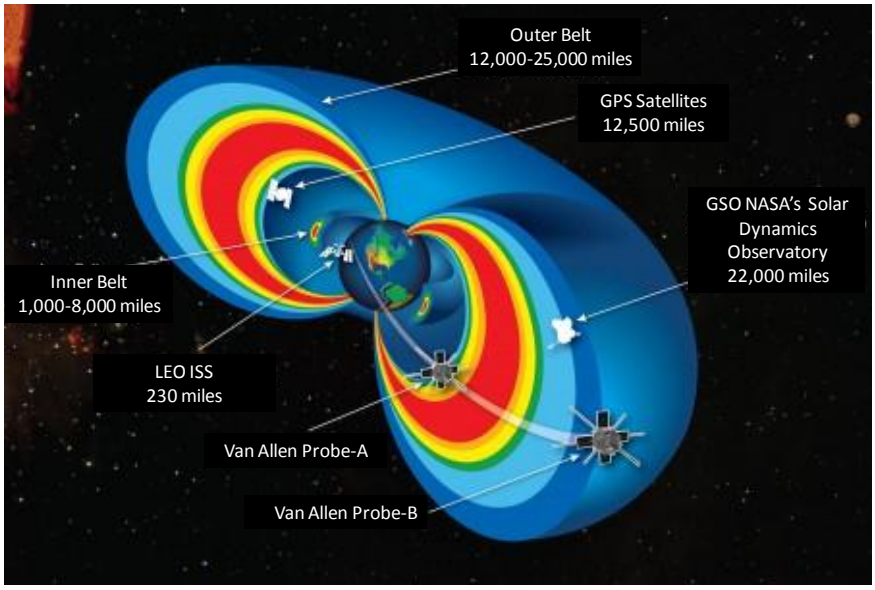


Figure2. Diagram showing the Van Allen radiation belts[6].

Besides, the sun continuously radiates energy in several forms: visible light, invisible infrared, ultraviolet, X-rays, gamma rays, radio waves, electrons, protons, and plasma (electrically charged hot gas). The abundance of charged particles that come with the sun's radiation makes space a hostile environment. The common sources of charged particles in the space environment are as follows:

- Solar radiation, consisting of mostly electrons and protons from the sun.
- Solar wind brings bursts of charged particles in addition to the normal radiation from the sun. It is primarily made of protons and some electrons radiating from the sun.
- Cosmic radiation comes mostly from the outer space and some probably from the sun. It consists approximately of 85% proton, 12% alpha particles, and 3% electrons.

In addition to the last total dose effects, which are caused by deposition of energy by many particles, there is a set of phenomena that are caused by single particles, called single event effects. The first one, single event upset occurs when a heavy ion is incident on the sensitive area of an integrated circuit, producing sufficient charge in the form of electron-hole pairs to cause a change in the logic state of the device. This type of error is known as a 'soft' error since it is reversible and causes no permanent damage. However, if it occurs in critical circuitry such as a control system or decision-making logic, then it can have serious consequences on the spacecraft operation generating false commands [2].

A single-event latch-up occurs when the passage of a single charged particle leads to a latched low impedance state in a parasitic PNPN devices in bulk complementary metal oxide semiconductor (CMOS) material, and it can result in burn-out. A more serious effect is single-event burn-out which occurs when an incident ion produces a conducting path-in a metal oxide semiconductor field effect transistor (MOSFET), for example, that causes the device to latch-up; if this condition continues for a sufficiently long time then the device could be completely burnt out and destroyed [2]. Finally, single-event-induced dark current is caused by the passage of a particle which causes displacement damage in a single pixel. Tests must be conducted at the subsystem and at the total system levels to ensure the tolerance levels are met and that catastrophic failure is impossible. Error correction techniques applied at the systems level include: redundant units, self-checking circuits, error-detecting and error-correcting codes, breakpoint reasonableness testing, and repetitive execution and watchdog timers (time-related solutions) [5].

There are another two factors that contributes to electronic systems damage in space, solar wind and solar flares. A continuous stream of protons, electrons, and ionized gas leaving the sun and sweeping the solar system is called solar wind. It is very thin, containing approximately 5 charged particles per cubic centimeter of space. The solar wind streams constantly, but not evenly. When these particles flow past the Earth, some get trapped in the Earth’s magnetosphere. On the other hand, a solar flare is a gush of ionized gas with charged particles spewed out by the corona, the sun’s glowing outer shell. It is associated with dark sunspots bounded by intense magnetic fields that come and go in 11-year cycles. The flare can cause auroras and disturb radio signals on Earth. The ionized gas is extremely hot, such that atoms of hydrogen and helium are homogenized into diluted plasma, composed mainly of negatively charged electrons and positively charged protons (see figure 3). Although this constitutes a million tons of matter moving at a million miles per hour, its density is so low that it is still considered a vacuum. Therefore, their energy levels and the corresponding probabilities that must be considered in designing the power system are mutually agreed upon by the satellite customer and the manufacturer [3].

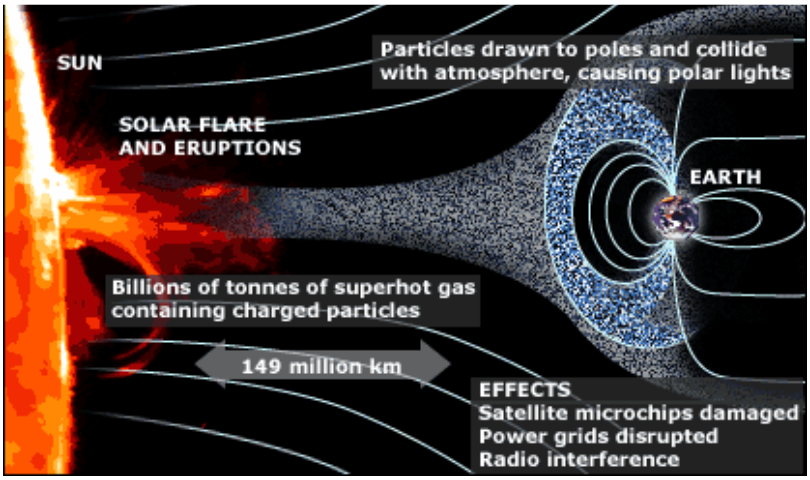


Figure3. Solar activity and its effects on Earth[7].

Major effects of solar flares and geomagnetic storms on the spacecraft power system are:

- Rapid degradation of the solar array power generation. This is a life shortening, not a life threatening, effect.
- Common-mode electromagnetic interference (EMI) noise entering the electrical power system components through exposed cables. This can upset the power system possibly causing a permanent damage.

Another important aspect and related with solar array degradation is the atom oxygen which is present in LEO. It severely erodes some materials, such as silver, which is extensively used in the solar array construction. Similar erosion is also seen in some electrical insulation such as Kapton and silicon rubber. The erosion comes not only from the chemical activity, but also in large part by the atoms travelling at several km/s velocities relative to the spacecraft. In addition to the erosion (surface recession), atomic oxygen can also form stable oxides on the metal surface. For these reasons, exposed bare silver in solar arrays and silicon or Kapton insulation on electrical wires are undesirable [3].

Therefore, all these phenomena affect in some way to spacecraft systems. As a result, different electronic devices manufacturers develop ICs that were submitted to very well planned tests simulating similar space environmental contingencies. In the next section, it is given a concise description about state of the art, in the research, of EPS on-board scientific space missions. The later will help to understand the goal of this work, which is focused in the conditioning and distribution of low-voltages levels at different loads on the spacecraft.

1.4 State-of-the-art of Spacecraft EPS

Different space agencies, for instance, NASA (National Aeronautics and Space Administration), ESA (European Space Agency), JAXA (Japan Aerospace Exploration Agency) and CNES (Centre National d'Études Spatiales) are constantly developing new philosophies about next generations of spacecraft power systems regarding specific key points in future missions. Some of these issues, addressed by ESA in [8], are focused on higher power demand and system efficiency, reusability, adaptability and flexibility, decrease in system mass, size and cost, as well as modularity and standardization. The later will help to meet the main goal of EPS, for a determined space mission, which is to ensure reliable delivery of electrical power and prevent failure propagation, under all foreseeable conditions, during all mission phases.

Power requirements in very early satellites were several watts. In today's communications satellites, it is several Kilowatts and is growing. Furthermore, some strategic defense spacecraft power requirements are estimated to be in hundred of Kilowatts and some concepts require hundreds of Megawatts of burst power [3]. Owing solar radiation represent the only external source of energy available in space, any spacecraft power system needs a solar array structure in order to achieve that energy; if there is not such structure, it must carry its own source of energy.

Therefore, in a very general way figure 4 shows the basic block components of the spacecraft power system. They are the primary energy source, energy conversion, power regulator, rechargeable energy storage, power conditioning, distribution and protection, to be acquired by user's equipment (load) in power utilization block.

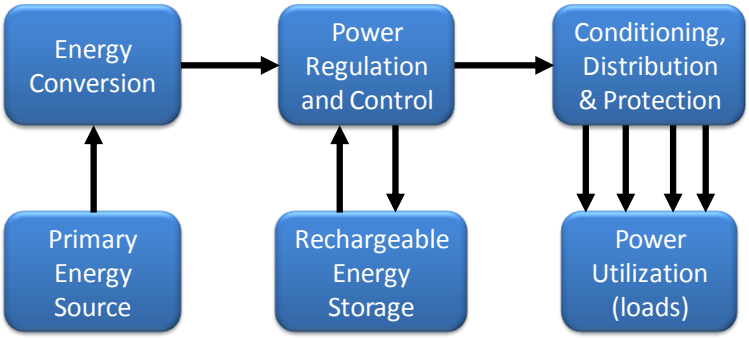


Figure4. Basic block components of EPS on spacecraft.

Within the candidates for the primary energy source are: solar radiation, radioisotopes, nuclear reactors and electrochemical fuel. The block of energy conversion may be photovoltaic, thermoelectric, dynamic alternator, full cell or thermionic. Finally, energy storage is typically electrochemical, although flywheel technology was also used at NASA Glenn research center [3].

On the other hand, the block of conditioning, distribution and protection provides bus voltage conditioning converting unregulated battery voltage into a semi-regulated low voltage line; meanwhile distribution section distributes the different voltage to the payload and experiments. Within this block, the third very important task is the power system protection provided against faults and short-circuits in the subsystems and bus circuitry.

Therefore, the figure 4 shows the basic block diagram of EPS in a spacecraft; these blocks are comprised by several modules depending on target mission. In the case of microsatellites development, as example Tsinghua-1 [9], the power system design reflects the need for autonomous operation, independent of all other systems, as is practiced and described on EPS of small satellites [10]. Autonomy is obtained using converter regulation methods and through total redundancy when mass issue is not a critical constraint. The redundant systems automatically switch to the other system in the event that a fault is detected. As reference, figure 5 shows the components included in EPS of micro-satellites.

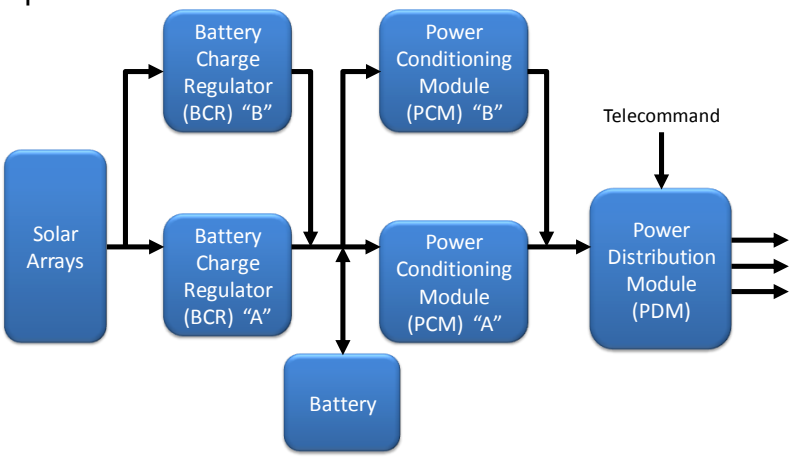


Figure5. Micro-satellite power system block diagram.

In figure above, and for the particular case of Tsinghua-1 micro-satellite, the redundant system is comprised by two identical BCR's capable of deliver full power from solar panels to the battery and for the rest of spacecraft. Meanwhile, the two PCMs ensure regulated power through convert the raw battery voltage into a regulated voltage line for other subsystems. Both modules (BCRs and PCMs) are equipped with control and regulation circuitry; furthermore, are capable to detect faults and also to switch the cold redundant systems for reliable and safe operation.

On the other hand, the area of solar panel plays a very important role in determining the total power the solar panel should give. The parameters involved on such calculation are the power budget, orbit, placement and packing. Equations 1-3 help to calculate the power that solar panel should generate (P_S), the effective solar area that must meet (A_S), and the area of each panel (A_P), respectively as is described in [9].

$$P_n * \left(1 + M_p\right)/E_p = P_S * I_i * I_S * e^{-fN} \quad (1)$$

$$A_S * 1353 * U = P_S \quad (2)$$

$$A_P = P_n/(1353 * I_i * I_S * e^{-fN} * T * P_a * U \quad (3)$$

In equation 1, are involved power and orbit parameters like P_n as power budget, E_p as efficiency of power system, and M_p as the power margin. Meanwhile, orbit parameters are I_s which is the sunlight factor (typical 1/3 of eclipse time), I_i used as illumination factor (typical value of 0.7) and the degradation rate, e^{-fN}, where N represents the life time and f have typical value of 0.025. In equation 2, is required the efficiency of solar cells (U) which values are 14% in case of Si, and 18% for GaAs. Therefore, from the data above it can be obtained the effective area of solar panel, A_S. Finally, in order to calculate the area of each panel equation 3 is used. In this equation, T depends of shape solar array, in the case for Tsinghua-1, shape like a box is considered, thus a factor of 1.25*A is used (A: section area of one surface). P_a is a factor (80%) utilized when cannot be used the total area of solar panel to place solar cells.

As a last block, the PDM has the task to distribute the different voltages to the payload and experiments. A second very important task of this block is to protect the power system against faults and short-circuits in the subsystems and bus circuitry. Furthermore, the distribution can be performed in three different ways, as is described in [9]. The first one is by Hard Wired, this means that the subsystem is directly connected to the EPS. The second one is by fused lines, the subsystem is connected to EPS via a fuse protecting the power system from short-circuits down the line. However, in [9] is stated that the most flexible way of distribution is via power switch. The last has two main functions; is possible to switch the subsystems On/Off by tele-commnads (TC), and also can be considered as electronic fuse that automatically switches off when the current drawn, by the subsystem, becomes larger than a pre-programmed value.

Now then, all above described was based on the utilization of the most common used power source in space, solar radiation. However, some surveillance satellites have considered and compared different power sources, as a part of its EPS, as is showed and evaluated in [11]. The three sources selected were a PV concentrator and two fission reactors which were evaluated for their compatibility with payload operation. Figures 6, 7 and 8, show the block diagrams of proposed EPS architectures for the three sources. Note that these sorts of satellites will consist of: A power control & distribution unit (PCDU) which contains monitoring and fault protection capabilities for all spacecraft power. Two, or more batteries for energy storage. A battery charge controller (BCC) and voltage converters or regulators, as required by the particular power source.

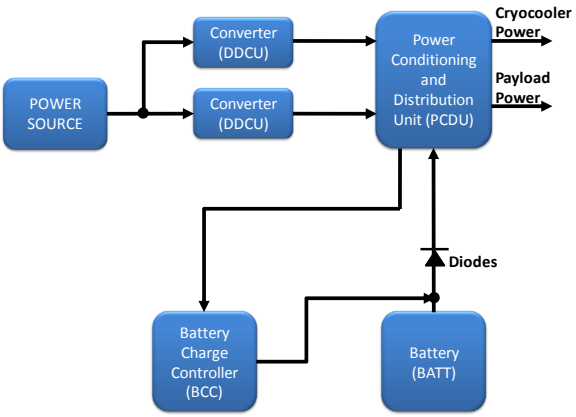


Figure7. Star-C EPS architecture.

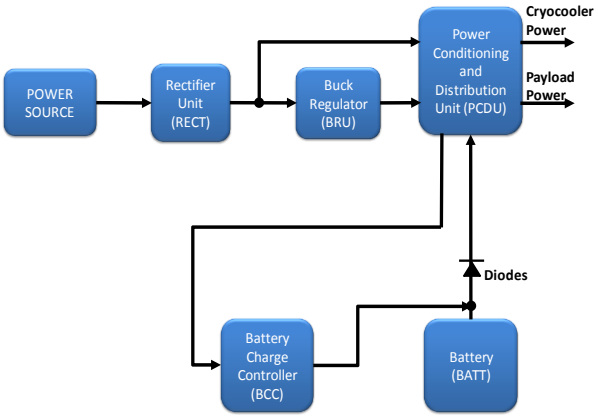


Figure8. SNAP-DYN EPS architecture.

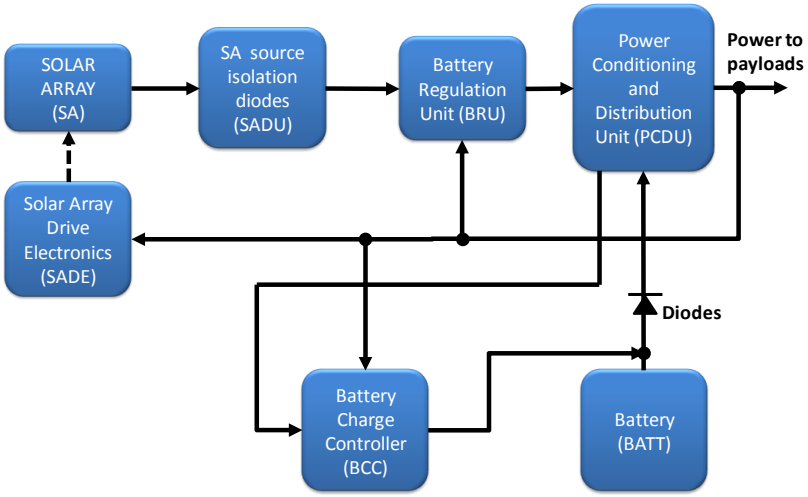


Figure6. Solar array EPS architecture.

The above three architectures are quite similar. The main difference is that for solar array source, isolation diodes for solar array (SADU), solar array drive electronics (SADE) and a bus regulator unit (BRU) are added. On the other hand, radiation is the major concern with reactors; they are mounted on booms to reduce the spacecraft dosage. This in turns increases weight and complicates the spacecraft attitude control system. Furthermore, electronics parts of spacecraft still require additional shielding.

As conclusion for surveillance satellites in [11], states that solar array architecture meets with the main constraints, weight and compatibility with payload operation, but possibly not meet some of the survivability requirements. The reactors are compact, but relatively heavy. However, appears like that, with development will meet weight limits [11].

Another kind of application, in satellites, is those based on radar payload on a space-based radar (SBR) satellite. The major issues are founded in generating and distributing power, specifically, in the power distribution and control system, as is stated in [12]. The EPS of SBR differs from existing systems in three major ways. First, it is required tens of kW of dc from radar payload. Second, the antenna would contain many solid-state transmit/receive modules feeding than 30,000 radiating elements distributed over a large area. Finally, the radar will demand critical transient response from dc power supply.

The principal challenges in designing at [12], are the average of dc power supply, orbit, and number of loads. The last, represents the principal constraint for power conditioning and distribution system. Fundamental power architecture distribution to be implemented (radial, trunk, ring, etc.) is another very important task to be defined, as well as, location of various elements and modules (constrained by presumption as to the basic geometry of the spacecraft), and component technology to be used are fully related.

On the other hand, the choice of bus voltages is a question of compromise. Meanwhile, high voltage had the advantage of reducing the conductor mass and the power loss. Against this, was the need to limit the voltage to prevent plasma leakage and breakdown, and reduce the stresses in semiconductor devices used in the associated converters and regulators.

Finally, and regarding management and control autonomy, implementation of on-board control circuitry for data management becomes financially feasible when volume of data involved is relatively small. So caution must be exercised regarding number of on-board elements in control systems are considered. As a conclusion, in this sort of satellites, power conversion and conditioning scheme result in a major concern. A principal design choice is whether to use central or local conditioning. In central approach lightweight and efficient (>85%) converters in the 5 to 10kW range would need to be develop using maybe individual converters rated over 100W each one. On the other hand, local conversion at the T/R module level would need small converters rated, maybe, up to 5W and efficiencies of 90 to 95%. However, it is necessary to assure enough space inside each transmit /receive module.

Now then, taken as example larger spacecrafts as reported in [13], the power requirements of last have increased from tens of watts up to the present programs requiring powers in the range of 10 to 300kW in space stations. In these cases spacecraft power systems require special attention mainly because of two reasons. First, due to high power demanded and inevitable subsystem weight; and second, for its aim, which is the efficient transformation of the available energy into electrical power. Besides, properly distributed architecture to other systems and payloads has to be selected.

For large satellites, in applications as Earth-orbiting [14], the EPS is composed of solar arrays, batteries for provisional energy storage, power conditioning and harness for energy transformation and distribution, as is showed in figure 9. The power conditioning block associated with spacecraft power system has been the "heart and mind" of the system itself [13].

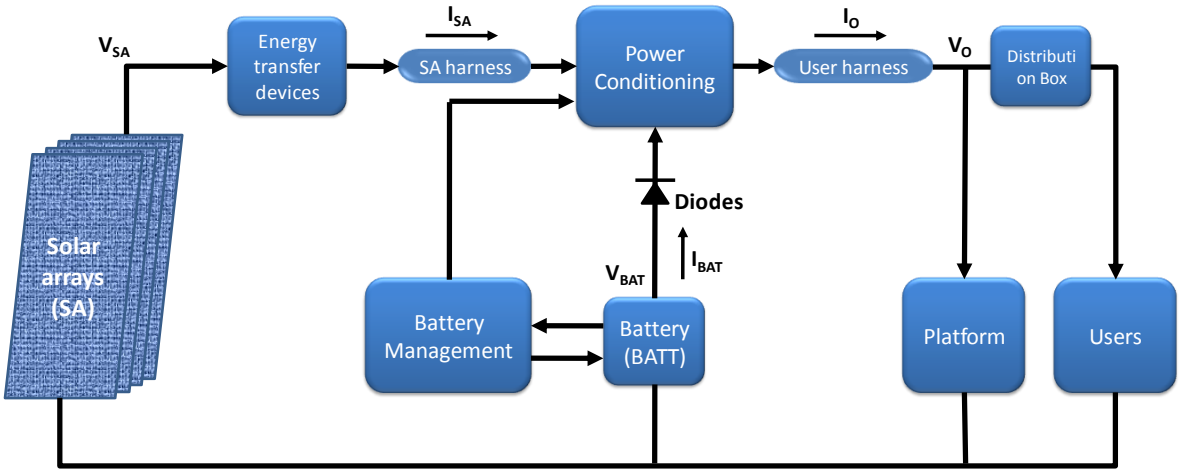


Figure9. General power system configuration of Earth-observing satellite.

The power conditioning system converts the requested energy into an electrical form (V_O), distributed to the users network through one or several bus bars, and guarantees the reliable working of the system. According to the adopted power system topology, the voltages of the solar array (V_{SA}), the battery (V_{BAT}) or the bus bars (V_O) may be identical or independent. The power system is responsible for the correct operation of the payload internal power conversion and distribution network. This system is composed of several functions which are supplied under a centralized or decentralized form via dc/dc or dc/ac converters connected to the distribution box unit (DBU) [13]. On the other hand, the platform is responsible for spacecraft in-orbit servicing functions as attitude control, thermal, housekeeping, and data handling, as well as the energy supply of the complete satellite.

Thus, the basic components of PV-battery system (as showed in figure 9), are extremely important in selecting the power system architecture that is most suitable for the mission. The following architectures represent the EPS configurations that would optimize the system performance for a given mission.

I.4.1 Direct Energy Transfer (DET) architecture

Here, the solar power is transferred to the loads with no series component in between. The necessary exceptions are: the *slip rings*, which provide a rotary joint between the Earth-facing spacecraft body and the sun-facing solar array; and the power distribution unit (PDU), consisting of load switching relays and fuses to protect the power system from faults in the load circuits.

The DET can be further subdivided into three classes: the fully regulated bus, the sunlight regulated bus, and the unregulated bus voltage power system. The components and operation of these busses are similar, except that the latter has no battery discharge converter (or regulator) in the power regulator unit (PRU).

Figure 10 shows the fully regulated bus DET architecture. In the fully regulated bus the typical bus voltage variations is ±2% to ±5% of the nominal voltage. This architecture in normal operation maintains the bus voltage between the specified upper limit and the lower limit.

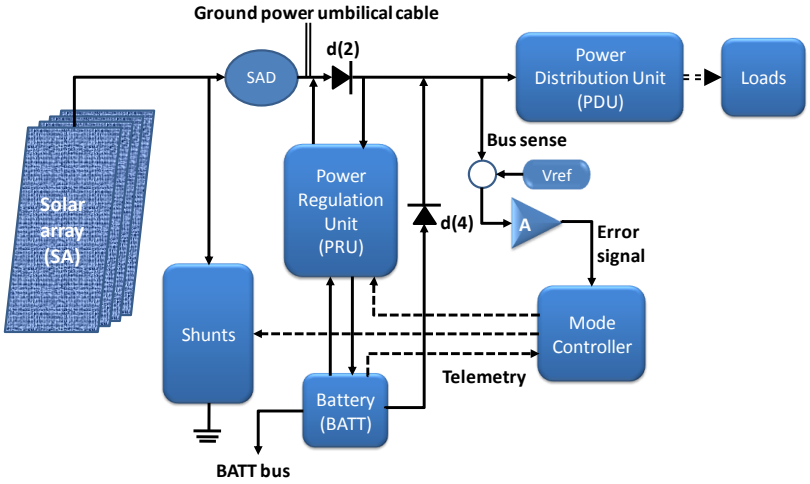


Figure10. Fully regulated bus direct energy transfer architecture.

The components and its description are as follows. The solar array is generally divided into many parallel circuits (strings), each with isolation diodes so that a failed string would not draw power from the healthy ones. These diodes may be located inside the PRU for protection, or on the back of the solar array exposed to the environment. The electrostatic discharge induced transient voltage suppressing snubber capacitors may be located inside or outside. The bus diodes pair d(2), typically Schottky diodes, prevents loss of the bus voltage in case the battery charger gets an internal fault, which may clear after some time. Those diodes are usually implemented in defense meteorological satellites.

The solar array drive (SAD) continuously orients the solar array to face the sun for generating the maximum possible power during the entire sunlight period of the orbit. Shunt component dissipates power that is unwanted after meeting the load power and the battery charge power requirements. The battery stores energy in an electrochemical form to supply power to the loads during eclipse periods over the entire mission life. The PRU provides an interface between the solar array bus and the battery. Due to the widely voltage variation of battery, the discharge converter in the PRU boosts the battery voltage to the bus voltage during an eclipse and the charge converter bucks the array voltage to the battery voltage during sunlight.

The PDU ensures that all loads, except critical and essential loads, are powered through switches and fuses. The fuses are not to protect the loads as much as to protect the power system from faults in the user equipment. The bus voltage controller consists of the bus voltage sensor, the reference voltage and the error signal amplifier. The amplified error signal output of the bus controller enters the mode controller, which in turn sends command signals needed to regulate the bus voltage within required limits. The mode controller automatically changes the EPS mode in response to the error signal as follows: *shunt* mode which during sunlight dissipates the excess in power. *Charge cut-back* mode controls the battery temperature cutting back the charge rate when battery is approaching to full charge. *Discharge* mode maintains the bus voltage through PRU which automatically increase the duty ratio of the discharge converter as the battery voltage decays. And in *PRU bypass* mode, the battery is instantly connected to the bus by the bypass diode quad d(4), which quickly delivers the battery energy to the fuse in case of fault, and blocks power flow to the battery at all other times.

The battery bus is essentially a tap point directly from battery, regarding that during launch and ascent phases the PV array is not deployed, and the battery meets all the energy needs. The power ground cord preserves the battery power during pre-launch testing and final checks before lift-off. Finally, the battery telemetry consists of the battery voltage, current, temperature, individual cell voltages and the internal pressures of selected cells.

On the other hand, figure 11 shows the sun regulated bus DET architecture. The aim of this architecture is to minimize complexity distributing power from sources like solar array and battery, directly to the load. Although, this DET bus is sometimes misinterpreted as unregulated bus, the bus voltage is regulated by shunt control during sunlight, and is unregulated only during an eclipse. For this reason, this sort of bus is also known as the partially regulated bus, sunlight regulated bus, or sun-regulated bus.

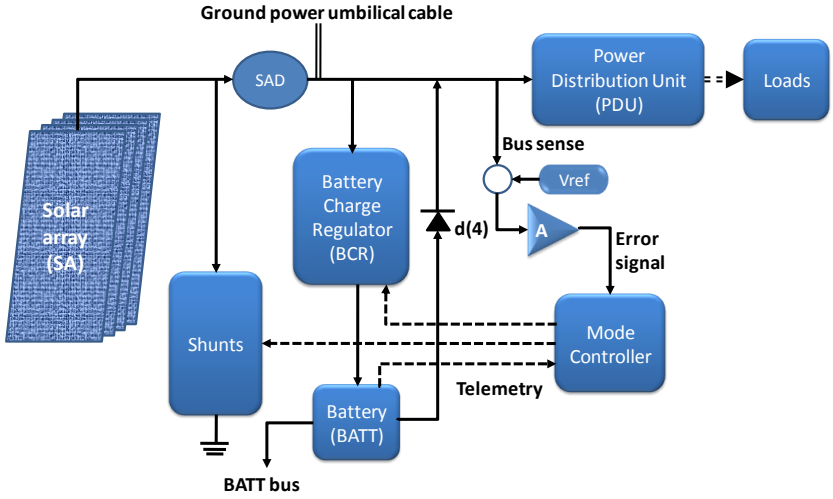


Figure11. SRB direct energy transfer architecture.

The sun-regulated bus has the usual battery charge regulator to regulate the battery charge rate during sunlight as commanded, but does not have the battery discharge converter. Instead, the battery discharges directly to the bus during eclipse through diode ‘d4’, called battery discharge diode. It only allows discharge from the battery, but blocks any uncontrolled charge current coming directly to the battery, leaving the charging function to the charge regulator. Thus, the battery is disconnected from the bus during sunlight when the shunt controller is regulating the bus voltage. Therefore, the voltage regulation during sunlight is achieved by shunt control circuits. However, since the battery is directly connected to the bus without a discharge converter in between, the bus voltage is the same as the battery voltage. Therefore, the bus voltage falls as the battery discharges during eclipse, and rises as it gets recharged during sunlight. This architecture would be most beneficial in multiple battery systems in GEO where the sunlight duration is long and the eclipse is short [3].

Finally, the figure 12 shows the unregulated bus DET architecture. The last, basically connects the batteries directly to the solar cells through power switch unit, and provides the lowest level of bus regulation. The bus voltage will vary with varying solar conditions and battery state-of-charge. The main challenge with this topology is matching the battery voltage to the solar panel voltage such that the panel's operating point is close to its maximum power point. As the battery voltage varies, the operating point will move away, giving reduced solar panel efficiency [15].

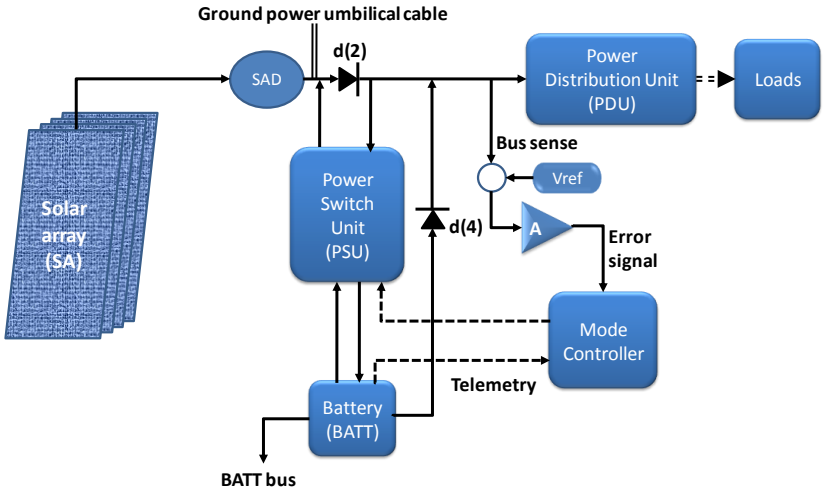


Figure12. URB direct energy transfer architecture.

I.4.2 Peak Power Transfer (PPT) architecture

Here, the solar array output voltage is always set at the value which results in the maximum power transfer from the array to the load. A series power converter between the array and the load matches the load voltage requirement and the array output voltage. For this architecture to be cost effective, the power loss in the

PPT converter must be less than the gain in operating the system at the peak power point all the time [3]. Figure 13 shows the PPT architecture for a mission with wide variations in solar flux and temperature.

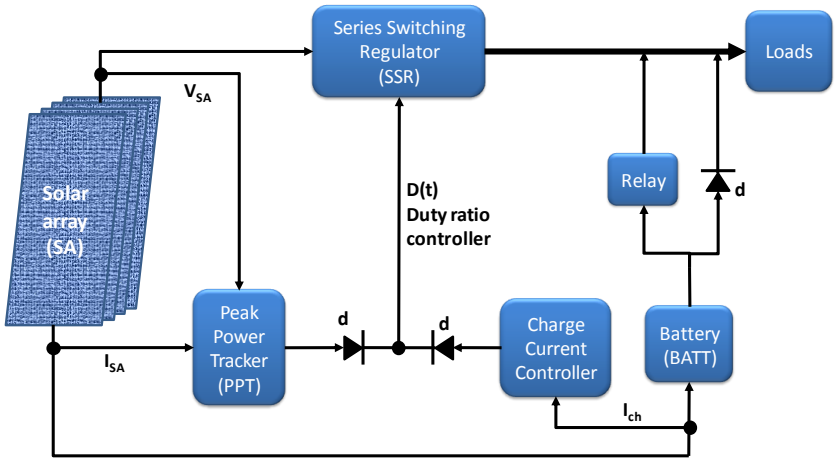


Figure13. PPT architecture in a mission with wide variations in solar flux and temperature.

In this architecture, a switching regulator between the solar array and the load remedies the main disparity between the voltage produced at maximum power and the constant load voltage. The series regulator input voltage is then maintained at the maximum power producing level by the PPT block, and the output voltage is stepped down to a constant load voltage by varying the duty ratio as required. The PPT is activated only when the battery needs charging or the load demand exceeds the solar array output. Otherwise, the excess power is left on the array raising the array temperature. The battery relay is opened up when the battery is fully charged.

The PPT architecture is particularly useful in applications where the additional weight, power loss, and cost of adding such an assembly can be justified, as happens in small satellites where solar array is not always oriented towards the sun. Furthermore, in satellites having solar radiation and array temperature varying over a wide range is also applied [3]. The last definitively implies a variation in array voltage.

The main advantages of the PPT are that it maximizes the solar array output power all the time, and it does not require the shunt regulator and the battery charge regulator. On the other hand, it results in poor system efficiency due to power loss in the PPT converter. Moreover, since these losses are dissipated inside the spacecraft body, it negatively impacts the thermal system.

Once studied the different alternatives on EPS architectures in different sort of space missions. The research will focus on the low-voltage levels distribution unit, as a part of secondary power distribution system of photo-voltaic EPS spacecraft in order to provide power to the network users through one or several busses, and guarantees the reliable working of the system.

I.4.3 Secondary power distribution

At the beginning of 1988 the experience in designing dc EPS for spacecraft was limited to the heritage got from relatively low power of less than a kW to several kW. As some examples, most American spacecraft have used the NASA standard 28Vdc bus. Both regulated and unregulated 28Vdc designs have been flown. The specification for unregulated dc buses permit voltages as high as 42Vdc. European have used a 50Vdc regulated bus in several spacecraft including the European telecommunication satellite series with an 800W and Olympus with a 4kW capacity [17]. On the other hand, General Electric with Radio Corporation of America has built the satellite television corporation which is a direct broadcast satellite spacecraft with a 2kW capacity and a 100Vdc bus [18].

Until now, most spacecraft have used 28Vdc and 50Vdc distribution buses. However, as spacecraft size and power increased, it is inevitable that distribution voltages would increase because of mass considerations. Therefore, as the spacecraft power and bus lengths increase, higher bus voltages could be used to reduce cable mass, to improve power conditioner efficiency, and to reduce EMI [19].

The voltage selection is based upon constraints imposed by space environments and the availability of components. For example, under space vacuum conditions, electrical discharge (corona) can cause shorting between conductors and subsystems at voltage levels above 280Vdc [20]. In LEO, often power loss occurs because of plasma acting as shunting resistor across the PV arrays. This power loss increases with voltage, and becomes noticeable for PV arrays, above 160Vdc [19]. All these factors generate voltage stress in certain critical parts that are voltage-limited as tantalum capacitors, semi-conductors, and power devices. Although, actually designs parts and design methods have been improved and overcome the voltage limitations, it is highly recommendable to stay bellow 160Vdc for a selected bus voltage [21].

As example of above mentioned, figure 14 shows a simplified block diagram of ISS EPS [22]. All blocks involved, already described in previous sections, provide a primary distribution regulated 160Vdc bus. Voltage conversion is accomplished by dc-dc converter units (DDCUs) which feed a secondary distribution voltage of 120Vdc and provide isolation.

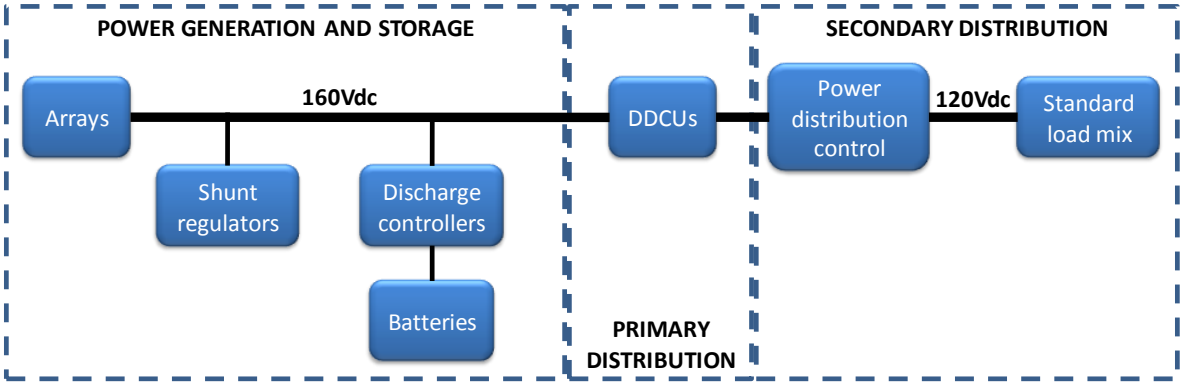


Figure14. Baseline of EPS on ISS.

Figure 15, shows a simplified block diagram of a typical secondary power distribution system [24]. This figure illustrates all of the essential elements of the secondary distribution power supplied to typical loads.

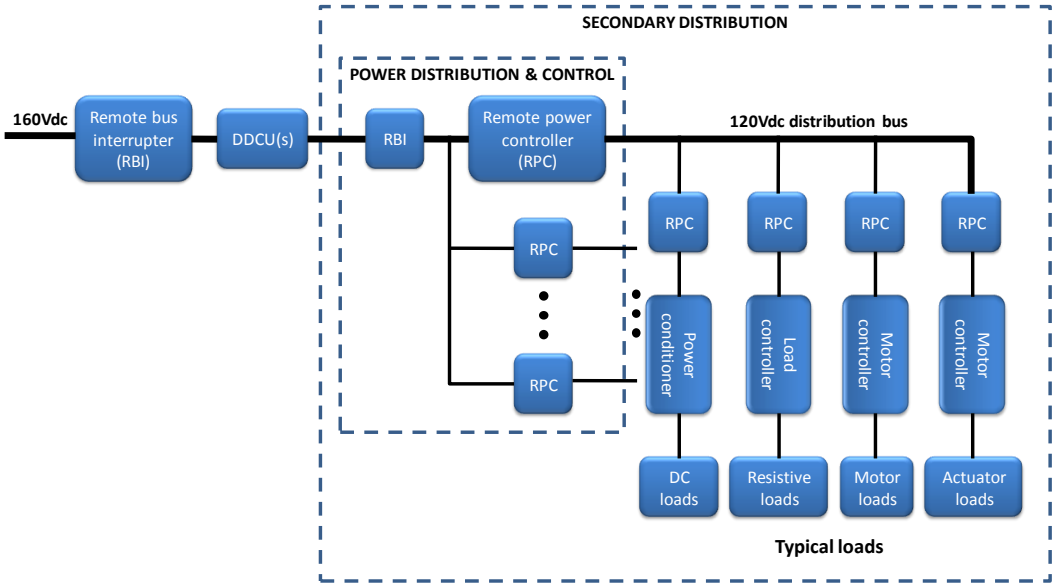


Figure15. Typical secondary power distribution system.

On the other hand, the typically bus voltage levels for secondary power distribution section are: 28V (up to 2.5kW), 50V (up to 8kW), 100V and 125V (above 8kW). It is recommended that bus voltages should not be selected below 20Vdc and not exceeds 125Vdc. Bus voltage below 20Vdc might lead unwieldy current densities, while bus voltage above 125Vdc might easily generate dangerous potential gradients leading to ionization of air molecules (plasma) causing coronal and electric arc discharges, in particular during tests in partially pressurized environments. Furthermore, is necessary to consider that the biggest selection of components-of-the-shelf (COTS) is compatible for operating voltages between 24 and 50 Vdc [2].

The secondary power distribution system often results quite complex because of large number of different type of loads, as well as the control in their interactions. Topics as fault tolerance, safety, and high reliability are no less important.

The typical loads in a spacecraft are varied and usually are depending on space mission target, but generally those are comprised by small motors, pumps, induction heaters, battery circuitry, transmitters and semiconductors electronic devices proper to sort of mission. Typically, the dc voltage levels supplied for this sorts of loads are in the range of 5Vdc to 3.3Vdc (even less) for logic circuits, ±15Vdc and ±12Vdc for control electronics, and 28Vdc for instruments based on motors and actuators.

In the next section, of this research, is described the state of the art of the low-voltage level generation in secondary power distribution section: low-voltage power supply.

I.4.3.a Low-voltage power supply (LVPS)

As semiconductor technology increase in functional densities and processing speeds of electronic system, is mandatory to minimize power consumption. Therefore, to allow higher processing speeds reducing power consumption, supply voltages had been reduced in new logic families. With the simultaneous increase in power demand and decrease in supply voltage level, new challenges arise for the power system.

According to international technology roadmap for semiconductors every 18 to 24 months integration scale of transistor in ICs is doubled, as well as clock frequency [25]. As a result, higher performances ICs like microprocessor units, memories, and application specific integrated circuits (ASICs) are produced to benefit a wide range of ground level applications which basically are implemented in sectors as telecom, computer, industrial, and military systems. However, regardless application field, these ICs in a circuit board requires several regulated supply voltages to function properly. Furthermore, the ICs digital cores may run at lower voltage while their input/output and analog sections operate with a higher supply voltage. Consequently, on-board LVPS systems must provide features as:

- Very low output voltage levels (≤1V).
- High output currents (≥10A).
- Efficient thermal management.
- Multiple outputs regulation.
- High power density and efficiency.
- Low-profile (mass and dimensions) and costs.

Unfortunately, the on-board power supplies not always meet these features because of several constraints, some of those, related to PCB area, conductions losses and degraded voltage regulation at point-of-load (POL).

Therefore, the current stage of LVPD architectures, as well as system integration, have been developed and improved on industrial, telecom and computer systems. In next paragraphs, the most important architectures on these fields are explained and considered, in order to find and optimal and innovative solution for low-voltage power distribution on a scientific space mission.

The figure 16 shows a block diagram of centralized power system. In a centralized power architecture all power is performed in one bulky power supply which provides the final voltage(s) required at the POL(s) [26]. In other words, this power distribution architecture converts the bus line voltage to the number of DC voltages needed in the system to the appropriate load.

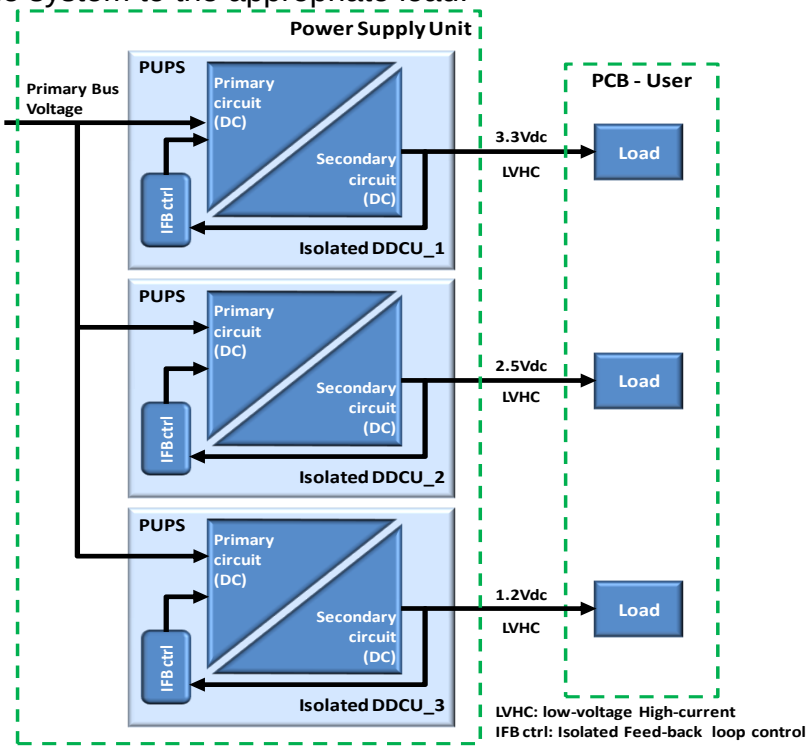


Figure16. Centralized LVPD architecture.

The strategy above is very cost effective. It doesn't consume precious board real estate at the point of load with the power conversion function. It's relatively simple to manage thermal behavior and EMI. It is fairly efficient because it avoids serial power transformations. This architecture, in general, works well when the power requirements, once defined, are not likely to change and space is not an issue. However, the most obvious problem is how to distribute hundreds of amps common with low output voltages. Furthermore, in this power distribution strategy the power supply must be sized to handle system of maximum configuration, which could put the small configurations (many low-voltages) at a cost disadvantage [27].

On the other hand, the remoteness of the supply from the load, which could be consider as another drawback, can negatively impact the ability of the supply to react to a rapidly changing load (i.e., transient response). Also thermal management, although relatively simple, could become in a special challenge owing the excess heat generated which could concentrate hundreds of watts in a centralize area. The last implies large heat-sinks and fans structures implemented to keep-out the power supply from becoming overheated. Finally, these system hotspots are a source of reduced system reliability [27].

To solve some addressed shortcomings of centralized power architecture, figures from 17 to 20 show the conventional distributed point-of-use power supply architectures [XIX-XXI], which are decentralized power distribution architectures consisting, in the simplest form, of a DDCU serving post regulators, non-isolated Point-of-Load (niPOL) converters, or a mix suited on-board users. The DDCU might provide intermediate DC voltage with certain level of regulation, isolation, noise suppression, and power factor correction. Therefore, this intermediate voltage is converted by post regulators located at the point of the load they serve. The last improves dynamic response, a better distribution of low voltages as well as heat distribution through the system eliminating the need of heat sinks or high velocity airflow structures. Distributed point-of-use power supply architectures, nevertheless, can be more expensive because isolation, regulation, transformation, EMI filtering and I/O protection are all done at every brick [27].

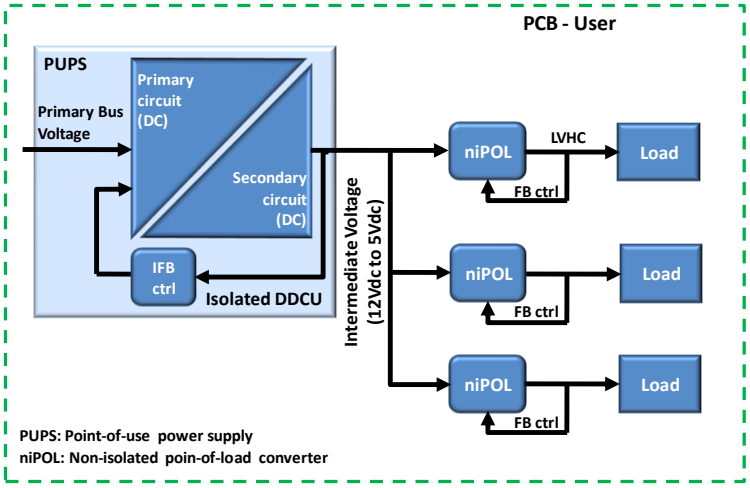


Figure17. IBC architecture.

In figures 17 and 18, both intermediate bus converter (IBC) architectures, isolated and non-isolated, are widely used in telecom and computer systems. The DDCU converts the power from the system bus into a relatively lower intermediate voltage, which is normally between 12 to 5 volts [25]. Then the power is distributed at this intermediate voltage and converted the second time by the post-regulators into the required low voltage at the POL. The two-stage dc-dc power conversion for each output gives good regulation at POL, nevertheless reduces the

overall efficiency, and due to additional power components employed, the cost as well as the physical size of the power supply is increased [27].

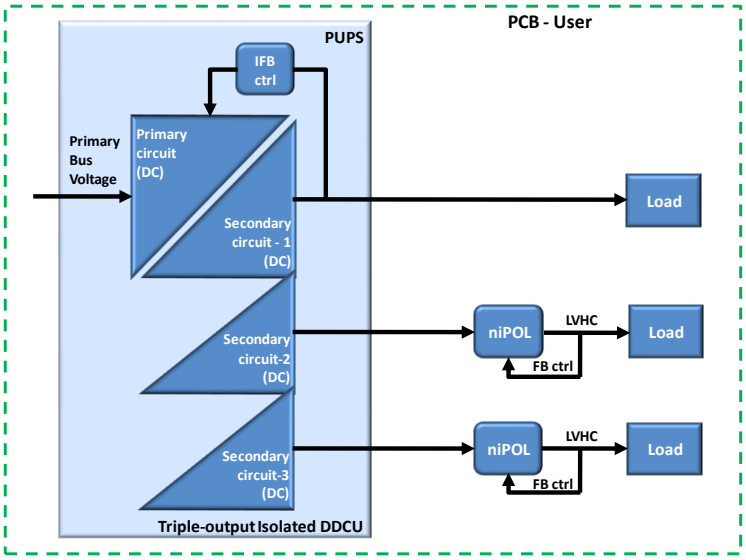


Figure18. IBC multiple outputs architecture.

Furthermore, because the intermediate voltage is lower than main bus voltage, the power distribution is done with a relatively higher current over a long distance on the PCB. This will cause a significant conduction loss [25]. The conduction lost (P_{loss}) in a PCB track is determined by equation 4, where ρ is the copper resistivity, *l, w* and *h* is the length, width and thickness of the track, respectively, which is used to distribute an rms current of I_{rms} [30]. Therefore, in order to minimize losses many layers of PCB must be used to distribute the power; consequently, PCB real estate utilization is greatly reduced for routing the high-speed signals.

$$P_{loss} = \rho \frac{l}{w \times h} I_{rms\_distr}^2 \tag{4}$$

On the other hand, in figure 19 the cross-regulated multi-channel architecture employs fewer power components for multiple outputs than the IBC architectures do. However, it is rarely used in telecom and computer systems, because precise regulation in multiple outputs is not obtainable owing to exacting matching and coupling of the magnetic elements [25]. Furthermore, the internal loop control on DDCU multiple outputs is usually associated to single or positive output making them tightly regulated, nevertheless this put it in total dependence the tight regulation of the other outputs.

Finally, in the figure 20 is shown the multi-module architecture which frequently is put it in practice at industry. Here, several point of use power supplies are used each independently producing a finely-regulated supply voltage.

It is efficient, especially when several low-voltage high-current loads are located at different points on the circuit board. It is because each point of use power supply can be placed close to its load, thus the power can be delivered to these locations at the level of the bus voltage, and it is converted into the required low voltage at the point of load. Therefore, high current only, travels a very short distance reducing conduction losses on the PCB. However, this approach is rather expensive because of the high costs of point of use power supplies, thermal management in critical sections of board, and it takes much of the valuable on-board space [25].

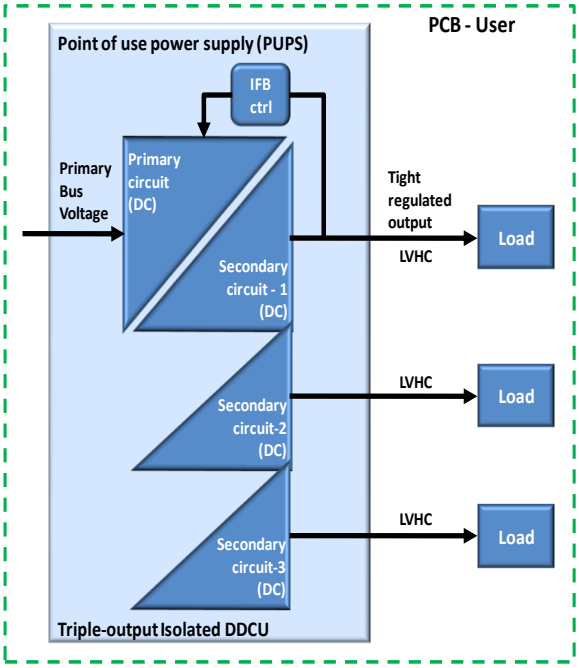


Figure19. Cross-regulated multichannel architecture.

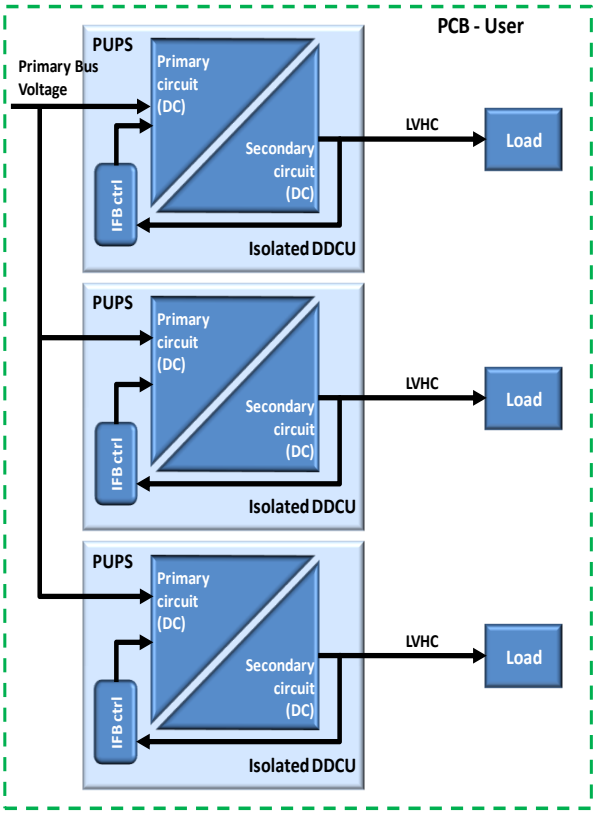


Figure20. Multi-module architecture.

Currently, the introduction of new modular and high density power converters did make faster and easily the migration to distribute point of use power supply architectures, and overcame some of the problems of centralized architectures. However, with each new generation of processors, memories, DSPs, FPGAs and ASICs, the trend is toward lower voltages, higher currents, higher speeds and more on-board voltages. Consequently, system designers are challenged to contend with a proliferation of lower voltages; provide ever-faster transient response; improve overall power system efficiency; and do it all using less board area [31]. The last, cause that for some applications distribute point of use power supply solutions required increase the number of power modules affecting subsystem development, in terms of board space and cost.

One of the key objectives of factorized power architecture, which is showed in figure 21, is to maximize the competitiveness of a power system by providing the highest degree of system flexibility, power density, conversion efficiency, transient responsiveness, noise performance, and field reliability [31]. All these features are meeting by separating conventional converter functionality in two power building blocks: a *pre-regulator Module* (PRM) and a *voltage transformation module* (VTM). Therefore, the load regulation function is accomplished by a non-isolated converter with high efficiency (97%-99%), the PRM. The later works with an input line range of 36V to 55V, and outputs a *factorized bus* that can range from 0V up to 55V [32]. After that, a voltage transformation stage is enabled by a *voltage transformation module* (VTM), designed to convert the factorized bus to the voltage levels required by loads with efficiencies as high as 97%. Furthermore, VTM provides effective current multiplication and isolation.

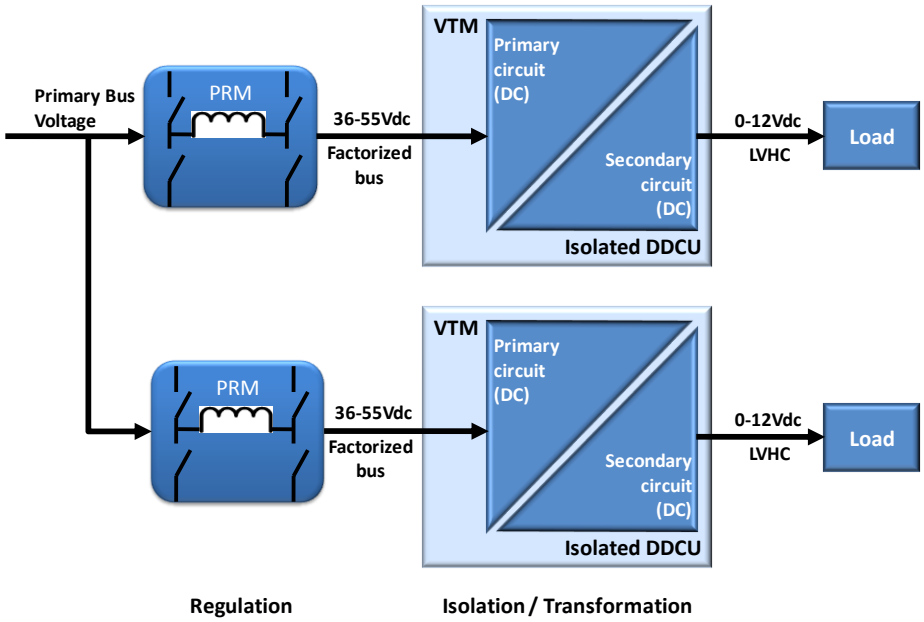


Figure21. Factorized power architecture.

The very important issues of this architecture are that factorized voltage bus is normally maintained above 40V, the last reduce losses and cross-section requirements on the main board. The load voltage can be regulated has a wider range, given the factorized bus range and the availability of various VTM transformer ratios [32]. And, PRMs and VTMs are power components ICs which are enabled to do power conversion in a small (≤ 4 cm^3) and light (<15gr) power ball grid array or J-level package, with power densities over 800W/in^3 which represent good thermal management.

The combination of factorized power architecture and IC power blocks give the power designer the flexibility to use only what is needed where it is needed [28]. Furthermore, this architecture also take advantage of the state-of-the-art in designing switching mode power supplies (SMPS), by implementing zero-voltage switching and zero-current switching topologies on VTMs to provide wide voltage range input and high efficiency voltage transformation [31]. However, the main inconvenient (at the designing phase of this work) lies that this architecture enables an efficiently power conversion only for process over 200W of power demand [27]. The last issue, is an inconvenient for low power ranges application resulting in high cost architecture.

Once stated the most important aspects in the research about LVPS architectures on industrial, telecom and computer fields; is necessary to put in context the complexity, for distributing low-voltage levels, in a very large and innovative instrument on high energy particle detection within a scientific space mission development. All advances reached, by above architectures, represent potential different possible solutions for distributing low-voltage levels in space environment. However, the constraints in electronic design at this environment make every mission a very particular scenario. Then, power designer has to innovate according to scenario requirements of scientific mission being considered, in order to find an optimal solution for its LVPD system [29]. Therefore, in next chapter will be described the Extreme Universe Space Observatory (EUSO) instrument, onboard Japanese Experiment Module (JEM). This instrument, represent a scientific space mission in fundamental physics research field. Moreover, due to the complexity of the instrument, a large scale comprehensive prototype is mandatory: EUSO-Balloon instrument is such prototype, and also will be described.

II.1 JEM-EUSO project

In general, space scientific missions are conducted with small, medium and large satellites, as well as space stations. Its targets could be one or more different topics related with Earth's observation, weather study, fundamental research, etc. The latter, typically suits purpose of studying astronomical objects or physical phenomena in the context of cosmology or analyses in relativistic physics [2]. In that way, ultra high energy cosmic rays (UHECR) detection has attracted the attention of a big scientific sector in Physics. The reason is that Cosmic Rays (CR) provides a unique probe of the most energetic processes in the universe. Therefore, in order to innovate in CR detection, a space telescope is proposed and can be extremely large and complex as is the case of JEM-EUSO mission.

JEM-EUSO is a worldwide collaborating effort of approximately 75 research groups from 13 countries. The instrument consists of a large telescope with a wide field-of-view (±30°), to be mounted on ISS JEM. It is the first space mission to explore the universe at extreme energies through the detection from space of UHECR (≥10^20eV) impinging the Earth's atmosphere. Such interactions produce an extensive air shower (EAS), a huge number of charged particles, mainly electrons and positrons travelling through the atmosphere along the original direction of the incoming UHECR. These particles excite the atmospheric N_2, which immediately decays by fluorescence producing UV photons with wavelengths between 300 and 400 nm. Furthermore, the electrons and positrons are super-luminal inside the atmosphere producing UV Cherenkov radiation. Both radiations are observed by JEM-EUSO from LEO at 400 km of height. Since electrons and positrons travel all at roughly the same speed, essentially that of light the net effect is that, from the point of view of the telescope, an EAS is observed as a light spot moving at the speed of light, thus defining a track on its focal surface. It is worth to notice that Cherenkov photons are emitted along the propagation direction of the particles in the EAS, i.e., downwards (see figure 22). Therefore, those photons are only observed because of scattering in the atmosphere or after diffuse reflection on the top of optically thick clouds or on the ground. The latter produces a strong Cherenkov mark signaling the impact point of the EAS and it is extremely important for data reconstruction [33].

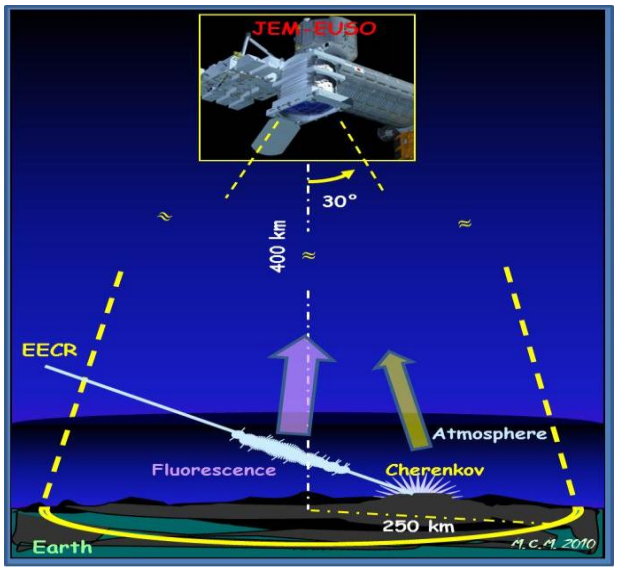


Figure22. JEM-EUSO will use the Earth atmosphere as a giant detector of UHECR [34].

In a beginning, EUSO was originally selected by ESA as a mission attached to the European Columbus Module of the ISS. Then, Phase-A study has been successfully completed in June 2004 under ESA. However, ESA postponed the start of phase-B, so Japanese and U.S. teams redefined EUSO as a mission attached to exposure facility on JEM (JEM/EF) of ISS. Therefore, the mission was

renamed as JEM-EUSO and continue with extensive simulations, design, and prototype hardware developments that significantly improved mission profile, targeting the launch in 2017 by H2B rocket and conveyed by the HTV (H-II Transfer vehicle) to ISS [35].

JEM-EUSO instrument is designed to operate for more than 3 years on board the ISS. Then, in next section it will be given a brief background of ISS as well as its EPS. Also, are described the subsystems that comprise this complex instrument, plus the conditions and constraints to be consider during work's development.

II.2 International Space Station

As mentioned above, the most standard space missions are based on satellites due to the fact that reach the stage of being economically viable. As examples, we have several satellites for communications, weather and navigation purposes, as well as those for monitoring Earth's resources, health of its crops and pollution. However, there are some special missions that requires more complex and biggest structure for serving to scientific community on issues related to Earth's environment, solar system and universe [1]. The International Space Station represents a very good example.

The ISS, as showed in figure 23, is truly the largest and most complex structure ever built wider than the length of a football field, with sixteen international partners. The complete assembly weighs 450 tons and the total interior space comprises six laboratories equal to two Boeing 747 aircraft. The ISS is located at an altitude range of 335 to 500 km, in LEO, with a 90 min orbit period and 35 min of eclipse [3]. The experiments planned for its on-board laboratories are targeted to enhance our understanding in Earth's observation, exposure of micro-gravity on humans and producing new medicines and materials.

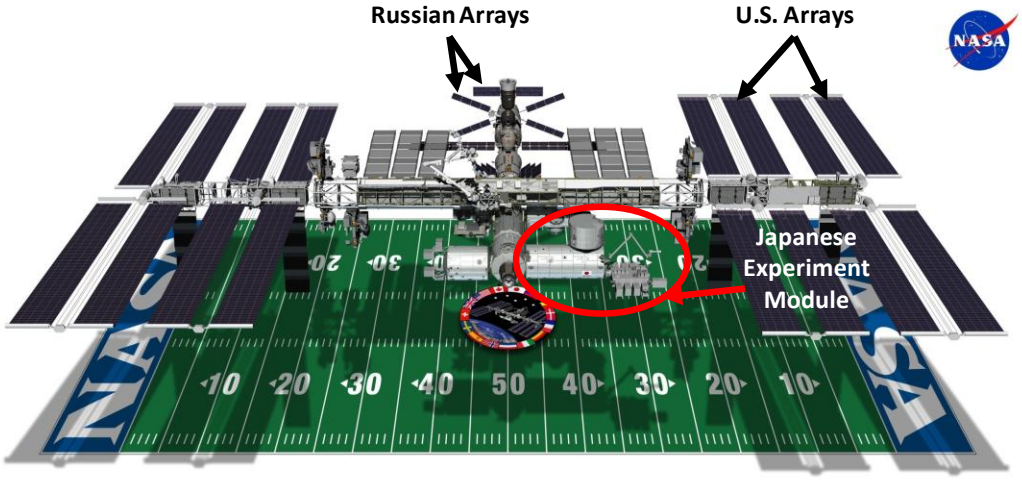


Figure23. International Space Station [36].

II.2.1 Utilization: JEM/Kibo-Exposure Facility

As can be seen in figure 23, ISS utilization could be subdivided in different modules from different countries. For this work, JEM is targeted. Experiments in JEM/Kibo focus on space medicine, biology, Earth observations, material production, biotechnology, and communications research [37]. *Kibo* (translated as hope) experiments and systems are operated from the Mission Control Room in the Space Station Operations Facility at the Tsukuba Space Center in Ibaraki Prefecture, Japan, just north of Tokyo. The Earth observation payloads are accommodated in the external JEM/Kibo-EF.

The JEM-EF is an external platform for conducting scientific observations, Earth observations, and experiments in an environment exposed to space. The JEM-EF/payload interface on the JEM-EF side is the Exposed Facility Unit (EFU). There are a total of 12 EFUs on the JEM-EF, nine of which are available for users. The other three EFUs are used for the JEM-experiment logistics module-exposed section (ELM-ES) and for temporary storage. Figure 24, is a general view of the JEM/Kibo facility; meanwhile figure 25, is a block diagram of the EFU locations on the JEM-EF. In general, the JEM-EF services its EFU payloads with electrical power, data, and active thermal control [37].

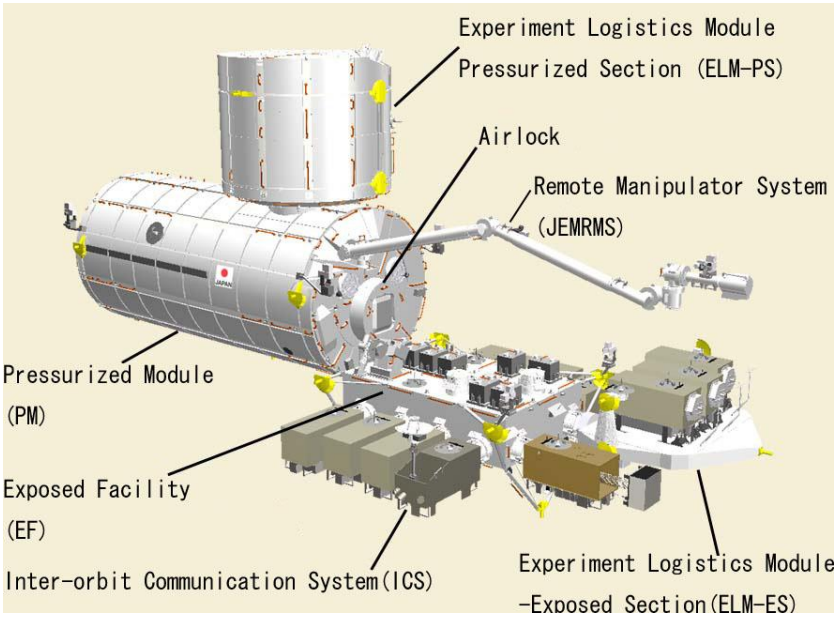


Figure24. General view of JEM/Kibo-EF [38].

As stated above, nine EFUs are available for users. Figure 25, shows the experimental payloads already mounted on these EFUs: MAXI (monitor of all sky X-ray image), SMILES (superconducting sub-millimeter-wave limb-emission sounder), ICS (inter-orbit communication system), SEDA (space environment data acquisition equipment), and HREP (HICO-RAIDS experiment payload).

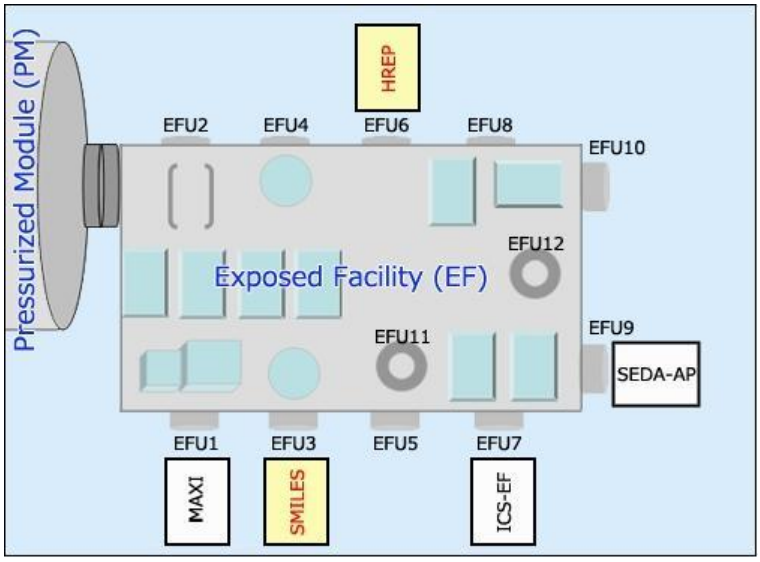


Figure25. EFU locations in the JEM-EF [37].

On the other hand, each EFU has a built-in attached payload BUS (APBUS) unit. The APBUS was developed to service the *Kibo*-EF payloads. Each experiment/payload is mounted onto the *Kibo* Exposed Pallet, grasped by the *Kibo* remote manipulator system, transported to the predetermined position, and then installed at the predetermined port of the *Kibo* EF.

The various handling logistic task-launch, on-board transportation, and installation require the payloads to be equipped with special attachment: the payload attach mechanism-payload unit (PAM-PU), the grapple fixture, and/or payload interface unit (PIU). All attachments are subject to accurate alignment/interface requirements for installation. Therefore, JAXA developed a mission interface structure to satisfy all interface requirements for the payloads to be handled. This resulted in two types of support structures: box structure (BStr) and pallet structure (PStr) showed both in the figure 26 bellow.

Figure26. Mission interface support structure: BStr (left) and PStr (right) [37].

The subsystems needed for APBUS BStr or PStr service provision are: the heater control equipment (HCE), the attached payload remote terminal (APRT), the power distribution box for attached payload (PDAP), and the extension mechanism assembly (EMA).

Figure 27, shows HCE at left and APRT at right. HCE detects experiment equipment temperature and keeps experiment equipment warm by providing electrical power to the heater in case the sensor detects a determined temperature [39]. HCE has a mass of 2 kg, power: 330mA (supply current), and a controllable temperature range of -44ºC to 1ºC. On the other hand, APRT converts signals of experiment equipment to the *Kibo* specific communication protocol (MIL-STD-1553B) to perform experiments on *Kibo* [39]. APRT has a mass of 6 kg.

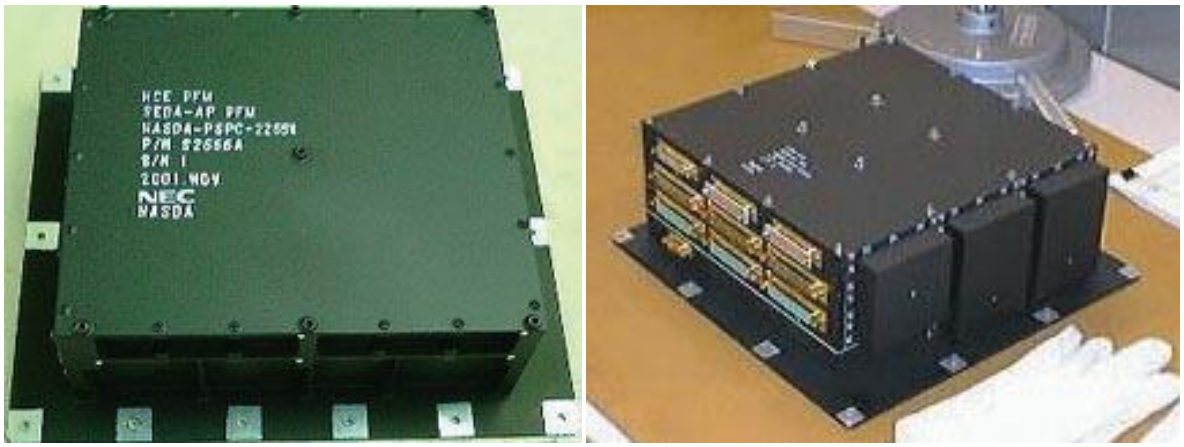


Figure27. HCE at left, and APRT at right [39].

Considering the EPS of ISS which distributes a 120V electrical power supply line, through the *Kibo*-EF, experiment equipment must satisfy specific interface conditions (e.g. load characteristics) to connect to the *Kibo*-EF. PDAP can meet above conditions and transform electrical power to 28 V that is easy for experiment equipment to use [39]. Besides, PDAP can distribute electrical power to multiple lines (12 channels max). PDAP has a mass of 7 kg.

On the other hand, some *Kibo*-EF experiments need an extension from the main structure. EMA was developed for this purpose. EMA can extend up to 1 m with the experiment equipment on the tip of an extendable mast [39]. Also, EMA can stow the extendable mast within the mission structure as required. For that purpose, EMA is equipped with LLM (Launch Lock Mechanism) to positively fix the extendable mast during launch and landing (Shuttle requirement), and to release the extendable mast to perform experiments on the *Kibo*-EF [39]. Figure 28 shows PDAP at left and EMA to the right.

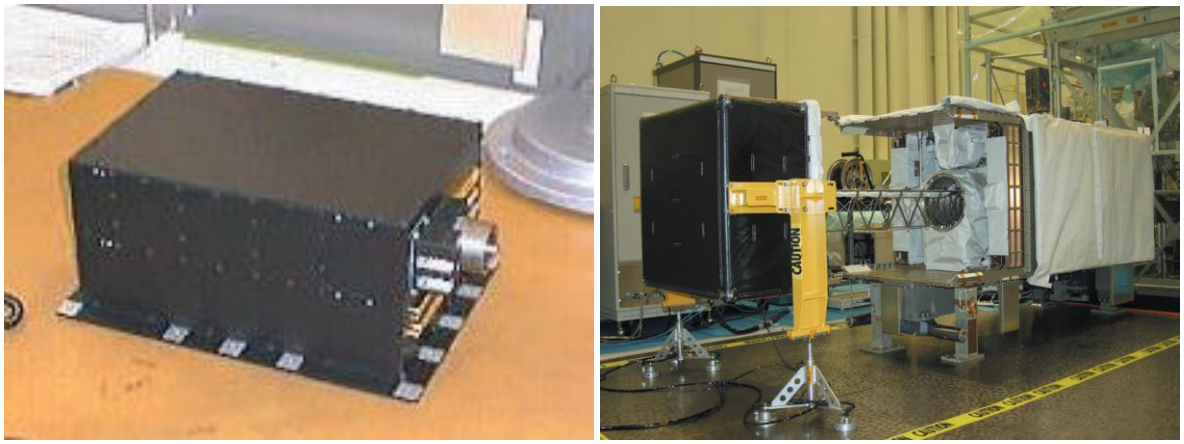


Figure28. DPA at left, and EMA at right [39].

In principle, through PDAP component, ISS will provide a nominal power of 1kW to JEM-EUSO instrument by generating 28V bus voltage level. However, about 600W are devoted to focal surface electronics instrument in order to supply power to several subsystems allocated over focal surface structure. Now, before get in detail on instrument description, it will be described the major segments of EPS on ISS.

II.2.2 Electrical Power System

The EPS of ISS consists of a hybrid mix of two major segments: a 120-Volt US built portion, and a 28-Volt and 120-Volt Russian built portion. The two systems are generally independent, but are interconnected via DDCUs to allow mutual transfer of power depending on availability and system demand [40].

The U.S. segment utilizes a 120-Volt channelized, load-following network of extensive solar arrays, batteries, voltage converters, remote controlled switchgear, and cables to route power to users in the U.S., European, and Japanese Modules. Figure 29 shows a top-level representation of the power flow through the U.S. power segment, and indicates the interconnections with the Russian system by the Russian functional cargo block (FGB). For the US segment, the four independent solar power modules will deliver a total of 76 kW of continuous power under normal conditions. Additionally, the Russian segment will provide a generating capacity of at least 29 kW, giving the Station a total projected capability of 105 kW [40].

The EPS of U.S. portion is divided into a primary system, which generates, stores, and distributes power over a network regulated anywhere between 173V and 115 Volts, and a 120-Volt secondary system, which is a tightly regulated network that feeds power to user loads throughout the station. The main elements of the U.S primary system are: the four solar power modules, the sequential shunt units (SSUs), the batteries which are designed for a 6.5 years useful life, the bidirectional battery charge/discharge units (BCDUs), the dc switching unit (DCSU), and the associated cooling system pumps and thermal radiators.

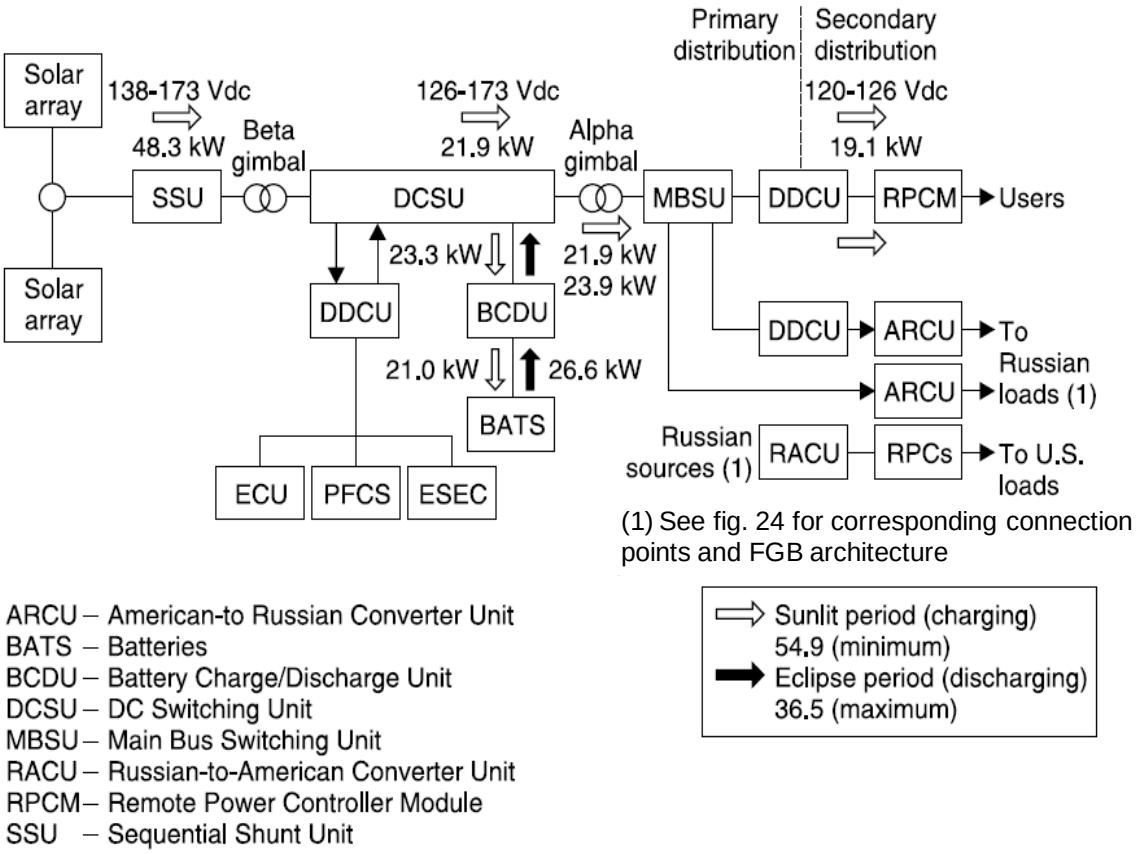
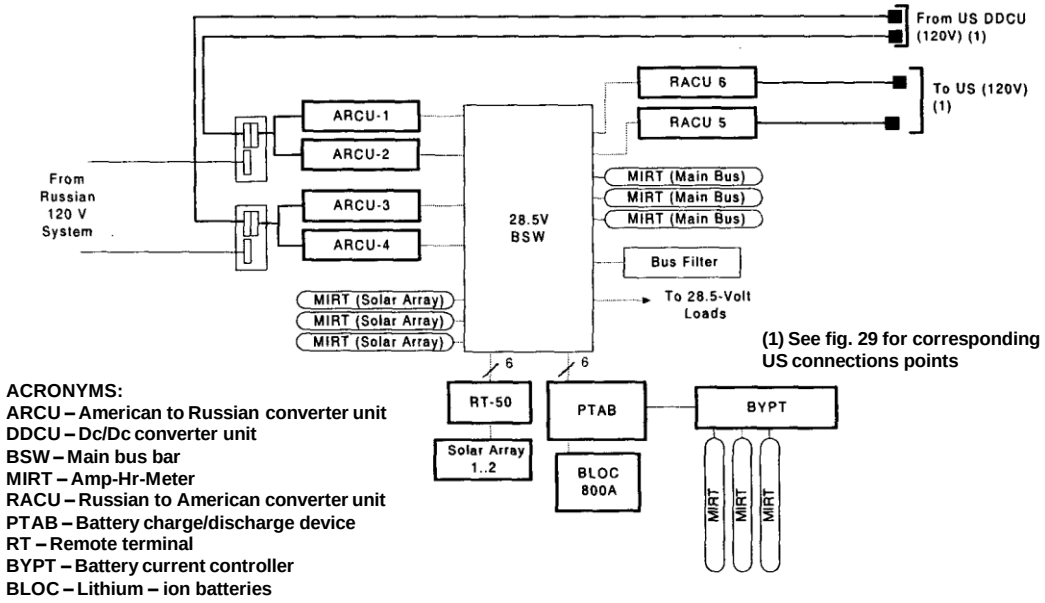


Figure29. U.S. channel top-level power flow diagram [41].

Rotating structural connections at the base of the arrays (denoted as beta gimbals) provide one axis of rotation for solar pointing. The larger alpha gimbals (or solar array rotary joints-SARJs) provide the other axis of rotation and connect the power modules to the main truss structure of the Station. More detailed information about these elements is given at [40].

On the other hand, the Russian channel power systems can be divided into two basic categories; a 28.5-Volt system and a 120-Volt system. The FGB and Service Module (SM) each contain 28.5-Volt systems rated at 3.5 kW and 4.4 kW, respectively. The 120-Volt system is distributed in the science power platform (SPP) and Universal Docking Module (UDM).

Figure 30, shows a block diagram of the FGB Power System. The following devices are included: solar arrays, solar array regulators (RT-SOS), American to Russian converter units (ARCUS), lithium ion (Li-ion) battery cells, battery charge/discharge devices (PTABs), battery current controllers (BYPTs), Amp-Hr Meters (MIRTs), main bus bar (BSW), bus filter (BF). More detailed information about these elements is given at [40].



ACRONYMS:
ARCU – American to Russian converter unit
DDCU – Dc/Dc converter unit
BSW – Main bus bar
MIRT – Amp-Hr-Meter
RACU – Russian to American converter unit
PTAB – Battery charge/discharge device
RT – Remote terminal
BYPT – Battery current controller
BLOC – Lithium – ion batteries

Figure30. Russian channel FGB power flow diagram [40].

Finally, as two important challenges to be addressed related with plasma environment of space, the possibility of the 160-Volt array current arcing to the ambient space plasma is precluded by means of the plasma contactor unit (PCU). The later is mounted on the exterior truss structure, and operates by creating a plume of ionized Xenon gas constituents, which acts as a low impedance, conductive bridge between the station and plasma environment. This protects the arrays and other conductive surfaces from arcing, pitting, and erosion by ion bombardment. Therefore, in case of fault, protection is achieved by solid-state remote power controllers (RPC) in six ratings from 3.5 to 65A in both current limiting and non-current limiting designs. The RPC trips at different set points of over-current, over-voltage, and under-voltage to isolate faults, as close as possible, to the faulted equipment [3].

The power system stability is also a serious concern because the loads on the station are constantly changing as new scientific experiments are brought on board. As a result, the output impedance of the DDCUs and the input characteristic of the loads have been specified to ensure stability with any combination of the expected loads. The power flow balance between major segments of the station is coordinated by the on-board command and control systems, which also provide interface control between the segments [3].

Once was given an overview of considerations and constraints about EPS of a very complex space structure, ISS, in the next section it will be described the different subsystems that comprise JEM-EUSO instrument.

II.3 JEM-EUSO instrument description

JEM-EUSO is an instrument of 2.6m of diameter and 2m length divided in four parts; those are optics, focal surface (FS) detector, focal surface electronics (FSE) and telescope structure (see figure 31). Optics focuses the UV lights (330nm-400nm) incident to the front lens onto the FS with the angular resolution of 0.1 degree. This resolution corresponds approximately to 0.75-0.87km on Earth's surface. The FS detector converts the photon energy to an electric pulse with the duration of 10 ns. The electronics counts-up the number of the electric pulses in the period of 2.5μs and record them according to the brightness of a pixel. When it finds a signal pattern coming from EAS, it issues a trigger signal. It starts a sequence to send all the brightness data close to the triggered pixels stored in memory to the ground operation center. Structure encloses all the parts of the instruments and keeps them out from the outer harmful environment in space. It also keeps the lenses and focal surface to the preset place [35].

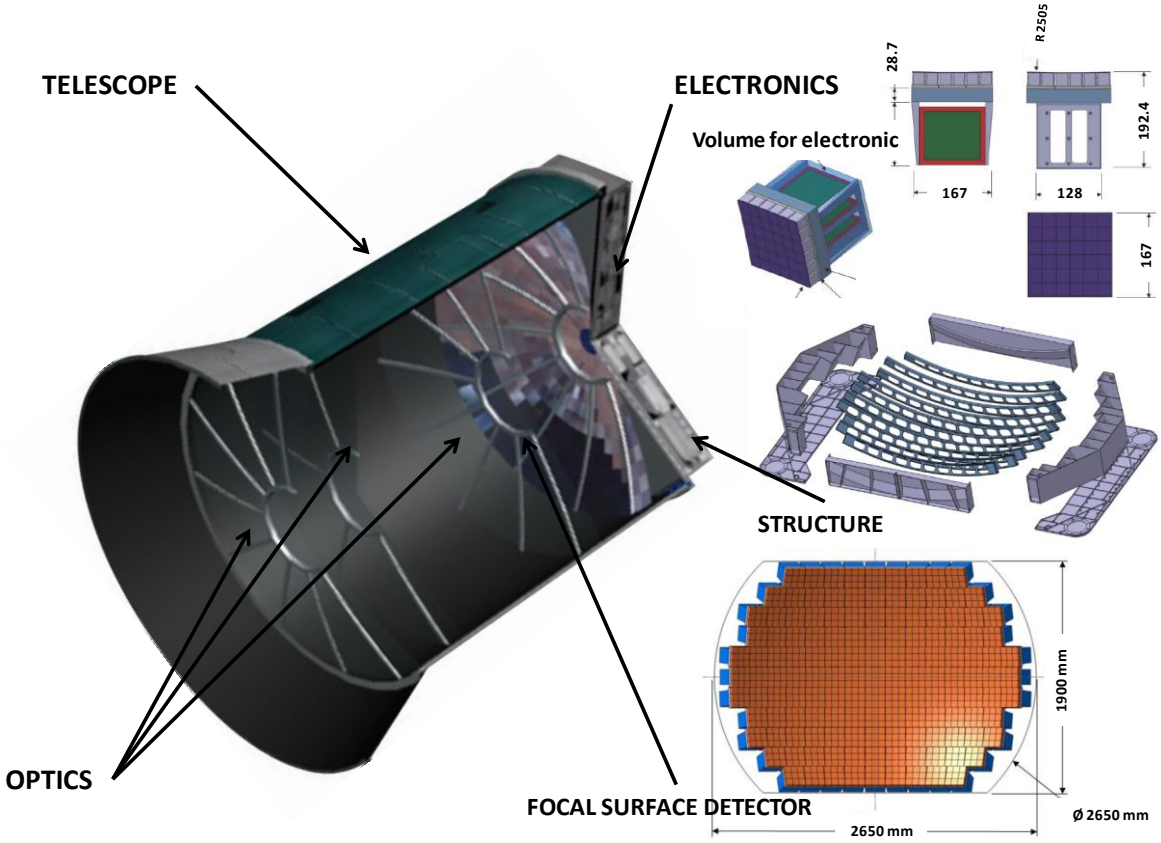


Figure31. JEM-EUSO instrument systems.

This work focuses in electronic part behind the FS detector, FSE. Then, one of the key subsystems of the telescope is the FS which is comprised about 6000 multi-anode photomultiplier tubes (MAPMT) to detect the UV photon emission, they all have its respective readout electronics subsystems arranged in a hierarchical tree to achieve an optimal discrimination of the random events that take place in the

atmosphere, only the data generated by the most energetic events are significant to be tracked and recorded by the instrument for further analysis on Ground [34].

II.3.1 Focal Surface

The FS of JEM-EUSO has a curved surface of about 2.5m in diameter covered by MAPMT manufactured by Hamamatsu. The FS detector is comprised by several Photo-Detector Modules (PDMs), each of one consisting of 9 Elementary Cells (ECs). The EC is comprised by 2x2 MAPMTs array. Therefore, about 165 PDMs are arranged on the whole focal surface. The last trigger is performed by a cluster comprised by 8 PDMs resulting in 20 cluster control boards (CCB). The figure 32, describe hierarchical disposition of FS.

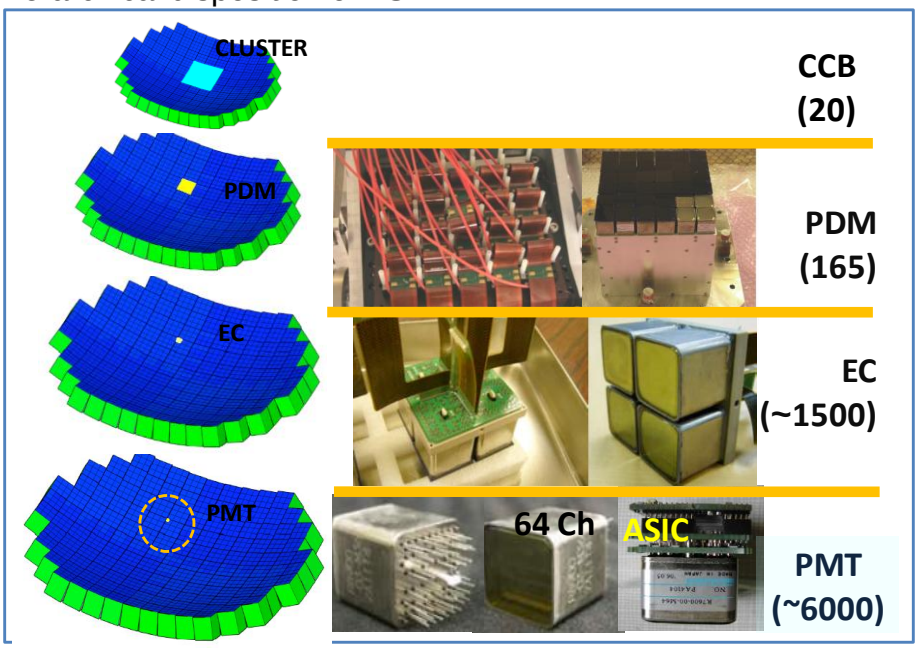


Figure32. Hierarchical diagram of FS.

The JEM-EUSO FSE is composed of four-level hierarchies: PMT sensor, EC electronics, PDM control electronics, and cluster control electronics. JEM-EUSO extensively employs FPGA's, even for the readout and control boards, to perform a sophisticate trigger algorithm without losing flexibility and to reduce power consumption. Designers plan to use FPGA's or DSP's for this trigger electronics to match with computational requirement within power budget. Figure 33, shows the data flow of readout electronic. The trigger levels carried out by the devices mentioned above are as follows:

- Readout process will be executed by ASIC's. One ASIC performs the readout from each PMT related to the counting of photons and integrated charge transduced by the PMT.

- 1st trigger level, will be executed by FPGA in PDM board. The numbers of photoelectrons counted by the front-end electronics (FEE) on EC are collected by every PDM.
- 2nd trigger level, will be executed by FPGA in a CCB. A cluster is composed of eight PDM's and has a cluster control electronics to process the event triggered by the 1st trigger level logic inside a PDM.
- 3rd trigger level, will be performed by micro-processor unit on CPU subsystem. The control of the operating state and the data flow, decentralized processing, is done with the micro-processor on the focal surface control electronics. Then the CPU control board communicates with the master data processor.

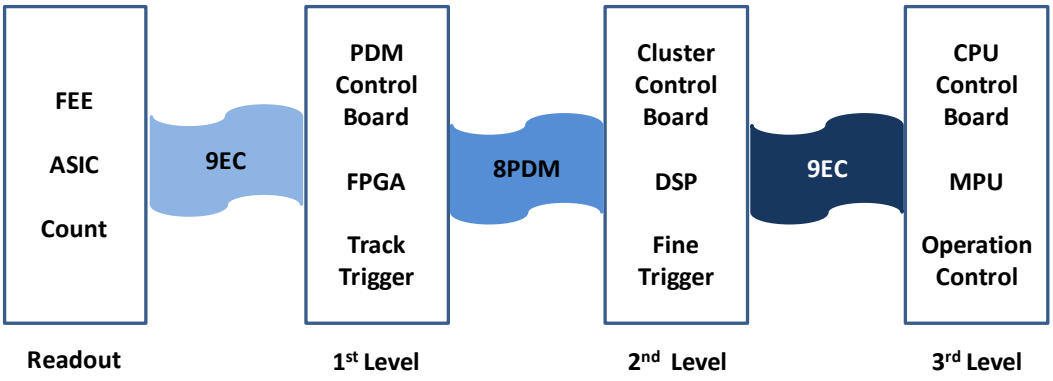


Figure33. Outline of readout process.

Finally, is important to state that the trigger system has to be selective in order to tag the EAS-produced signal while rejecting the background in an efficient way.

II.3.2 Elementary cell subsystem

The heart of EC subsystem is ASIC SPACIROC, which processes the anode signal converting the anode current into a digital number. The ASIC's work in parallel in two different modes: in single photo-electron mode, for low photon flux; and charge integration mode, for high photon flux. For communications purposes, ASIC's use a 40MHz operation frequency for serialized bit readout, and 400Hz to all data readout. Regarding power consumption, ASIC's must perform readout process with biasing levels of 3.3V (analog and digital) and 1.5V voltage levels with tolerances of ±3%. The EC boards mass shall not exceed the 200g mass.

Regarding electromagnetic compatibility (EMC), the MAPMTs and EC components are the most susceptible elements, of entire FS, to EMI. Therefore, it is planned that ASIC's packages shall be correctly located and potted on the EC subsystem boards [42], as is shown in figure 34b. The EC subsystem is comprised by four different EC boards: EC-Dynode, EC-Anode, EC-HV and EC-ASIC, as is showed in figure 34c. EC-Dynode It shall transmit fourteen high voltage values between 20V to 1000V to the corresponding MAPMT pins. Then, EC-Anode It shall collect the MAPMT anodes signal and transmit them to the EC-ASIC Boards. These signals shall be isolated with a proper ground, at the level of the connector, and go directly to PDM board (PDMB). Meanwhile, EC-HV board it shall distribute the voltage from the HV box to the MAPMT dynodes.

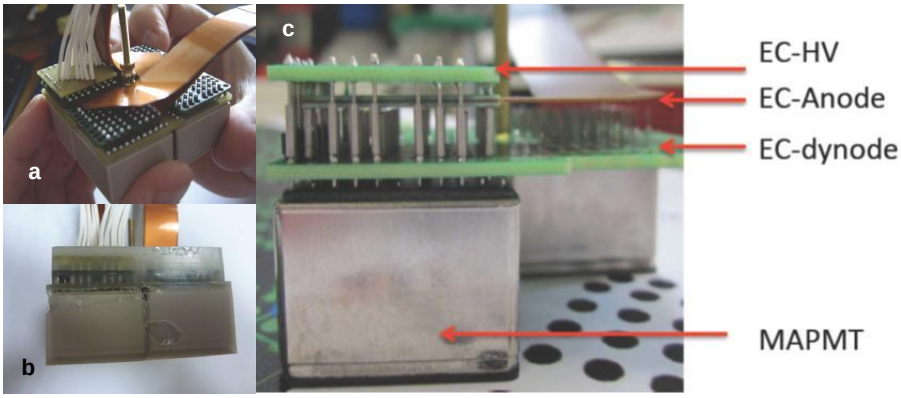


Figure 34. a) EC unit before potting, b)EC unit board potted and c) EC unit boards assembly [43].

The upper part of EC assembly it's an interface board which purpose is hold the ASIC's flexible cables, as can be appreciated in figure 34a, interfacing EC-Anode and PDMB. Figure 35 shows, EC-ASIC board top (a) and bottom (b) view in which can be appreciated ASIC's 68-pins connectors, also it can be observed 120-pins PDMB interface connector.

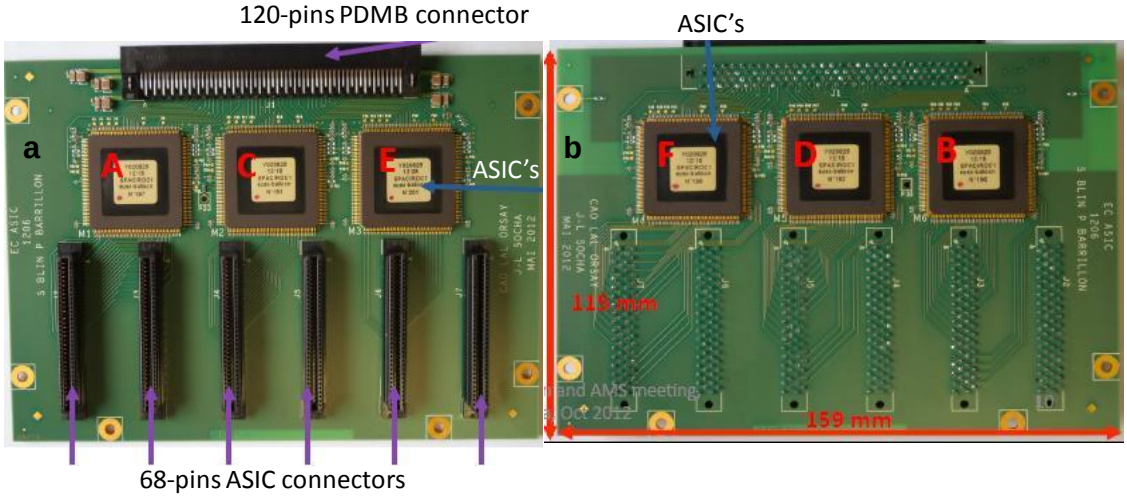


Figure35. EC-ASIC a) top view and b) Bottom view [43].

II.3.3 High Voltage Power Supply subsystem

One unit of high voltage power supply (HVPS) is set on every PDM in order to provide 1kVdc bias voltage for the MAPMT. The HVPS subsystem shall distribute voltages to 4x12 dynodes of each MAPMT to achieve a nominal gain of 10^6, with possibility of fine adjustment from 10^5 to 10^7.The HVPS current design baseline for JEM-EUSO is a Cockcroft–Walton (CW) circuit, commanded by a microcontroller unit (MCU) in order to adjust the high voltage (MAPMT gain). The CW circuit has a 100kHz/60V sine wave input. The later is then multiplied at all dynodes, up to reach 1000Vdc. CW circuit is based on voltage multiplier circuit from low voltage AC or pulsing DC input. Figure 36 shows engineering model of CW circuit.

Therefore, the CW output voltage level can be adjusted, in order to modify the gain of each MAPMT. One DAC is used to perform an output voltage variation from 0-3.3Vdc from power source of 3.3Vdc. On the other hand, the 100kHz oscillator is driven by 5Vdc power supply. Furthermore, another power source of 28Vdc is needed for the switch section. The high voltage switches implemented shall protect MAPMT's against strong light while allowing strong signals to be measured. MAPMTs gain shall be commanded and changed by control switch module in less than 2.5 μs and within the interval gain levels of: 10^6, 10^4, 10^2 and 30 [42].

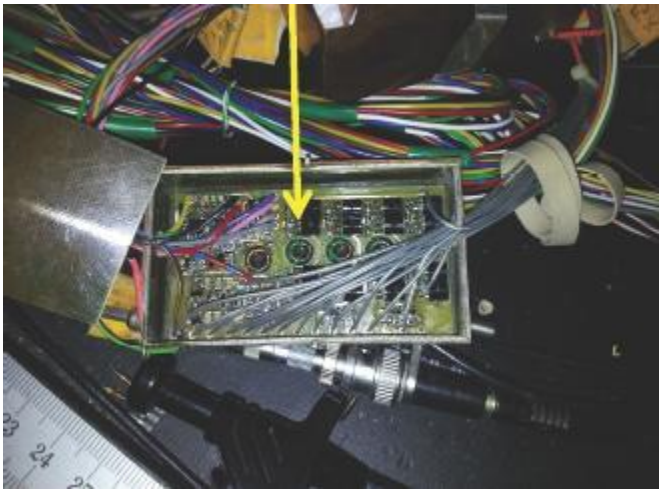


Figure36. Engineering model of CW circuit [43].

Finally, in order to provide noise immunity, MAPMT dynodes and HVPS-CW circuit section were potted. Furthermore, a magnetic interface 1:1 was suggested for providing isolation from main bus.

II.3.4 Photo Detector Module subsystem

The PDM electronics receive digitalized data from ASIC's, for performing the first trigger level algorithm, and transmit to CCB through high speed data protocol. PDM's are independent each other, and there is no communication between them. So, system clock, configuration of ASIC's, overall control data transfer and slow control should be made for higher level system like CCB or Housekeeping (HK) subsystems.

The main key device within PDM electronic hardware is an FPGA, which interface with ASIC's and CCB. These interfaces require a large number of pins in order to meet communications requirements of subsystems involved. But definitively, the main constrain comes from power budget consumption which is planned to be 1W per PDM. Furthermore, the FPGA needs for a properly performance 3.3V, 2.5V, 1.8V, 1.5V and 1V voltage levels with tolerances of ±3%, and not exceed a mass of 700g.

The figure 37, shows top and bottom layers of PDM board prototype, at left and right respectively. In top layer it can be observed FPGA and PROM circuits, also 120-pins interface connectors with 6EC-ASIC's. Furthermore, MDM connectors of 51, 15 and two 9-pins interfacing CCB, HK, HVPS and LVPS subsystems, respectively. Regarding low-voltage levels constraints, for LVPS subsystem was recommended implement five on-bard POL converters. Two converters are foreseen to provide 3.3V to FPGA core and I/O banks; meanwhile, the remaining three converters provide 3.3V (digital and analogue) to EC-ASIC boards. Finally, to lower voltage levels it was suggested to implement linear regulators.

Figure37. PDM board prototype, top-layer at left, and Bottom-layer at right [44].

In the next section, the subsystem in charge to perform the second trigger level is described from the electronic point of view, CCB subsystem.

II.3.5 Cluster Control Board subsystem

The CCB shall classify 8-PDM data according to acquisition mode, priority and data type. Then, shall perform second trigger level filtering in case of a potentially good event, and transmit data to the CPU through interface data acquisition board. CCB subsystem shall also provide data on temperatures, voltages and currents to the HK subsystem. At first instance, CCB subsystem had planning to use a DSP as a heart of the subsystem. However, for the first tests a FPGA was considering, keeping flexibility in the design.

Due to the level of interaction with other subsystems, CCB requires the use of at least three different communication protocols in order to perform data management. CCB shall interface the PDM board through 8 bit parallel running at 40 MHz. It shall use SPI standard running at 1 MHz for sending commands to PDM, and also to receive information from HK subsystem. Furthermore, shall transfer and receive commands, as well as processed data to CPU via standard Spacewire at 200 Mbits/s [42].

The figure 38 shows, CCB engineering model board containing a XILINX FPGA which for properly accommodation, into a determined data processor (DP) rack, shall meet a standard 3U EUROCARD dimensions of 100mmX220mm. The CCB subsystem power consumption shall not exceed 5W, and a mass less than 300gr. The CCB biasing levels specifications states that voltage levels of 3.3V and 2.5V are needed as auxiliary voltages and also for I/O banks, respectively. Furthermore, CCB requires a 1.8V, 1.5V, and 1.2V levels for FPGA core. Tolerances expected of biasing levels are about ±2%.

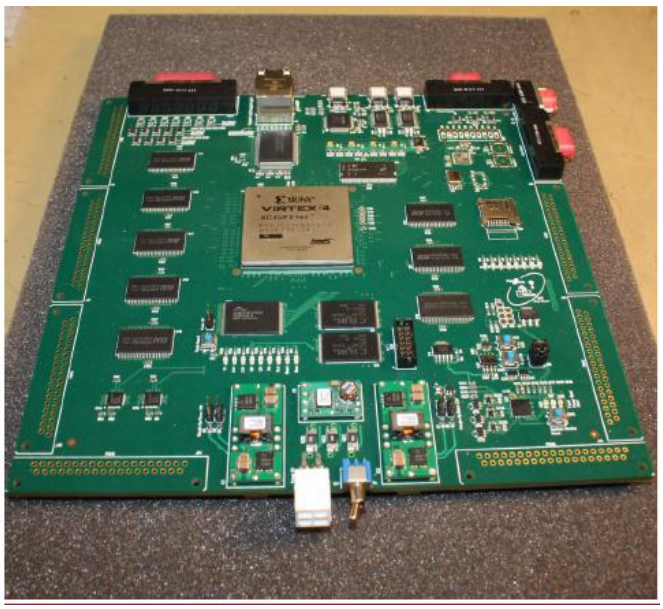


Figure38. CCB engineering model [45].

II.3.6 Housekeeping subsystem

The overall purpose of HK is to monitor and activation, by telemetry and high level commands (HL_CMD) respectively, of several subsystems that constitute JEM-EUSO instrument. The HK subsystem is subservient of CPU subsystem, and all its activities are defined as slow control, i.e., with reaction time scales typically larger than a second [42]. It is planned to use an FPGA as control device in order to give flexibility to monitoring system. However, as preliminary design was consider a less expensive device, but no less powerful like microcontroller.

Then, to perform the first test, HK subsystem is based on a commercial Arduino microcontroller development board. The later, requires 12V level as main input for on-board linear regulator which supply 5V to microcontroller. Furthermore, HK distributes tele-commands (e.g. HL_CMDs) in order to perform ON/OFF functions. At same time, ON/OFF status based on contact closure (CC) signals are reported, and telemetry information in the form of temperatures, voltage and current (V&I) are monitored from several subsystems of the instrument in order to generate alarms. Additionally to status monitoring and analogue V&I measurements, HK subsystem, in cooperation with CPU, will transmit parameters settings to other subsystems. Figure 39 shows the engineer model of HK subsystem, as well as assembly disposition.

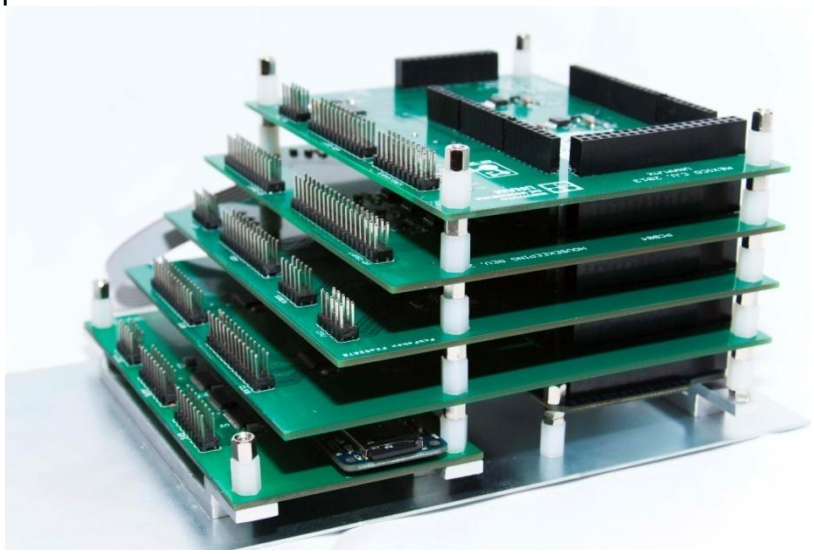


Figure39. HK subsystem assembly disposition [43].

Therefore, for performing all tasks mentioned above HK subsystem is comprised by several boards, in order to do acquisition, conditioning and digitalization of measurements. The disposition showed in figure 39, was decided in order to fit into Eurorack structure. The HK power supply requirements states the necessity of ±12V, 5V and 3.3V in order to bias different ICs devices, memory, DAC's, MUX's, MOSFET drivers, LVDS, etc. The power consumption expected is 6W and 300gr of mass.

II.3.7 Central Processor Unit subsystem

The CPU shall manage data packets transmitted not just by CCB, also by other clients like the clock board (CLKB) through an appropriate interface (SpaceWire to Gbit-Ethernet/PCI). Furthermore, shall interface the *Système d'Interface Reseau Nosyca* (SIREN) which is basically a network system interface to transmit data to ground, in real time, and receive tele-commands according to payload specification given in [42].

On other hand, CPU shall control the HK subsystem collecting HK-data through RS232/RS422 port using a serial protocol. Also, as an advanced option for future flights, CPU shall control the infra-red camera (IR-CAM) for atmospheric monitoring purposes through an USB or RS232 port. Therefore, in order to perform all its tasks CPU subsystem design team has proposed an Arbor iTX MPU, which needs 5V and 3.3V biasing levels with tolerances of ±10%. Figure 40, shows both, CPU board based on Arbor iTX at the left, and SpaceWire PCI Mk2 card at the right.

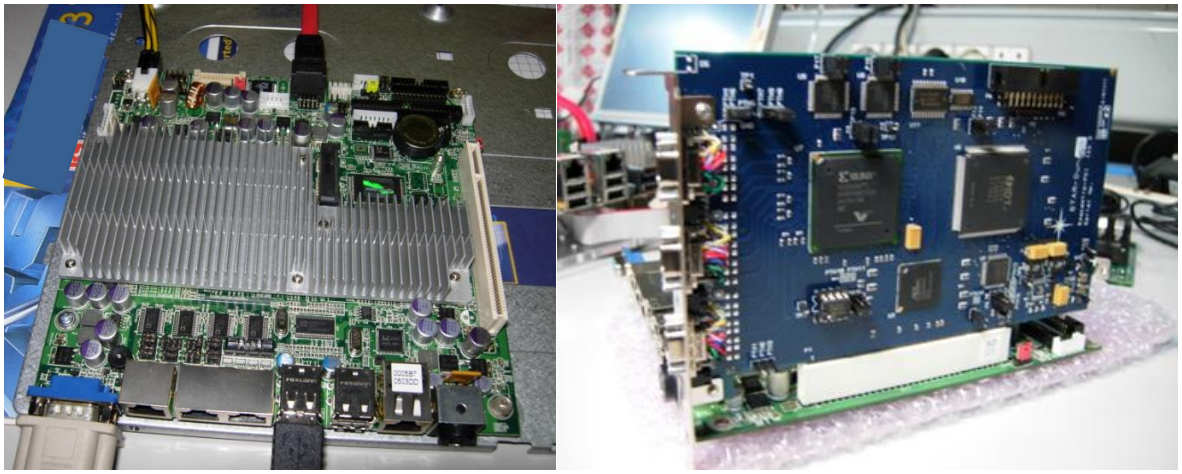


Figure40. CPU subsystem based on Arbor iTX (left) and SpaceWire PCI Mk2 card (right) [46].

Additionally, CPU shall also manage the mass memory subsystem, in order to store science and telemetry data received from the CCB, and from the on-board sensors and transducers. For that purpose, CPU shall procure two serial advanced technology attachment (SATA) ports, which is a common data transfer interface between PCB's subsystem and mass memory storage platforms. The CPU subsystem shall not exceed a standard 6U-EUROCARD board dimensions. The power consumption expected is 15W and a mass less than 1kg.

II.3.8 Data storage subsystem

The Data Storage (DST) shall record the data collected by the CPU from the FSE, via CCB, global position system receiver (GPSR), and CLKB, as well as from the HK subsystem. DST subsystem shall have storage capacity not less than

512 Gbytes, and it should sustain a data transfer rate from CPU up to 150 Mbits/s. Furthermore, in order to fulfill the requirements on data transfer and redundancy, two solid states disks were proposed to be disk fault-tolerant and operate in redundant array of independent disks (RAID) mode. RAID-1 level has to be supported, at least, according to [42]. Figure 41, shows the two OCZ 1TB solid states disks that conform DST subsystem.

Figure41. Two OCZ 512GB solid states disks from DST [46].

Therefore, the DST power consumption expected is 18W providing a voltage level of 5V ±10%. The mass shall be less than 0.6 kg, and will fit into 6U-space of Euro-rack structure.

II.3.9 Clock Board subsystem

The CLKB subsystem is in charge to distribute the clock signals to all the electronic devices of FS, and has to measure the fractions of live/dead time of the instrument. Also, it shall provide the interface with GPSR in order to record the position and the absolute time of each recorded event. In that way, a signal system clock of 40 MHz with 50% duty cycle, and gate-time-unit (GTU=2.5μs) clock of 400 kHz with 98% duty cycle, are generated.

On other hand, CLKB shall receive command from CPU and shall transmit data to the CPU according to the SpaceWire communication protocol. Also provides data values, concerning to temperatures and voltages, via a serial protocol to HK subsystem. The device used for this purposes is a Virtex5 FPGA from Xilinx. The voltage levels required for properly operation are 3.3V, 2.5V and 1.8V ±3%. Meanwhile the power consumption shall not exceed the 4W. The CLKB will be hosted in a standard 3U-Eurocard space. Figure 42 shows the CLKB engineering model.

Figure42. The CLKB engineering model [46].

II.3.10 Global Position System Receiver subsystem

The GPSR subsystem, is based on the SiRFstarIII™ 20-channel GPS compact module/receiver, and shall provide the coordinated universal time (UTC) with accuracy of 1μs. Furthermore, data and signals like position of the payload with an accuracy of 10m during the flight at height up to 42km above sea level also shall be provided. Figure 43, shows GPSR mounted and tested in a 3U-Eurocard box.

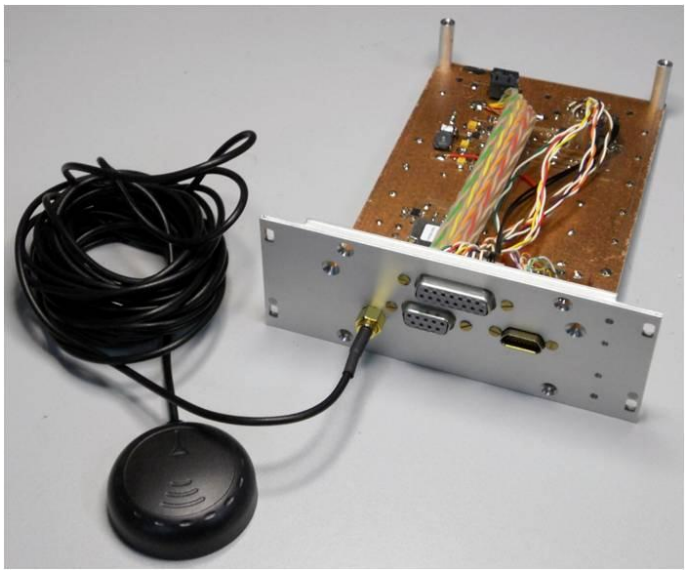


Figure43. GPSR mounted and tested [46].

The voltage level required for properly operation is 5V ±10%. Meanwhile the power consumption expected is 1.5W with 300gr of mass.

II.3.11 Atmospheric monitoring

As a part of mission main objectives, an atmospheric monitoring system was included. Since the intensity and the atmospheric transmittance of the fluorescence and Cherenkov emissions strongly depend on the atmospheric conditions, especially on parameters like cloud amount and cloud-top altitude, a light detection and ranging (LIDAR) instrument was considered. The later, has the capability to shoot a laser beam on event direction, just after EAS was detected. On other hand, an IR-CAM imaging instrument is used to detect the presence of clouds, and to obtain the cloud top altitude during the observation period of the JEM-EUSO telescope. Since the measurement shall be performed at night, the cloud top height shall be based on cloud IR emission [35].

Now, once described the most relevant JEM-EUSO subsystems is time to put in context the complexity for distributing power to low-voltage levels over all the FS.

II.4 Power distribution at JEM-EUSO instrument

JEM-EUSO instrument, it is the first of its kind in space environment within the UHECR detection field. The JEM-EUSO objectives and dimensions make it unique and very ambitious. The low-voltage power distribution over such kind of instrument represents a great challenge to power engineers. Figure 44, shows the current scenario of power distribution in JEM-EUSO. The diagram starts from 120Vdc electrical power supply line provided by *kibo*-EF [47]. This primary power bus (PPBUS) is received by APBUS through PDAP, which step down the voltage to 28Vdc through several channels, this conforms the secondary power bus. After that, an optimal LVPS architecture must be implemented in order to satisfy requirements and specifications of payload instrument.

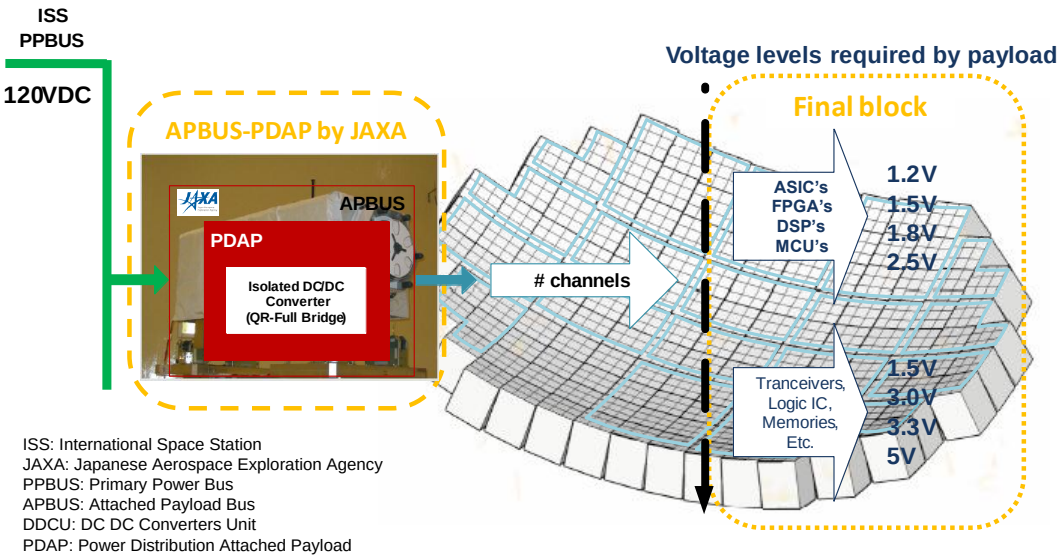


Figure44. Current scenario of power distribution at JEM-EUSO.

In principle, APBUS development will be under supervision of JAXA or another project leader space agency. Usually, the PDAP component comprises a block of isolated DDCUs which will provide a nominal power of 1KW, for JEM-EUSO, through PPBUS. However, about 600W are devoted to FSE. All this power has to be properly distributed along 165 PDMs located over all FS through appropriate harnesses. The harnesses have to comply, at first instance, with military standard specifications (M22759 spec55) which have a space qualified section.

During an internship at Japan, a proposal based on three different ways to distribute power to FSE was stated. The first one was based on punctual distribution strategy which implies a power distribution per PDM structure. The latter consist on several harnesses spread from APBUS component. Those harnesses would travel directly to a power supply board allocated inside of each PDM structure. These boards will be in charge to supply low-voltage levels to subsystem inside of this structure. The same strategy will be applied to CCB, HK and CPU subsystems. Figure 45 shows the proposal based on punctual power distribution.

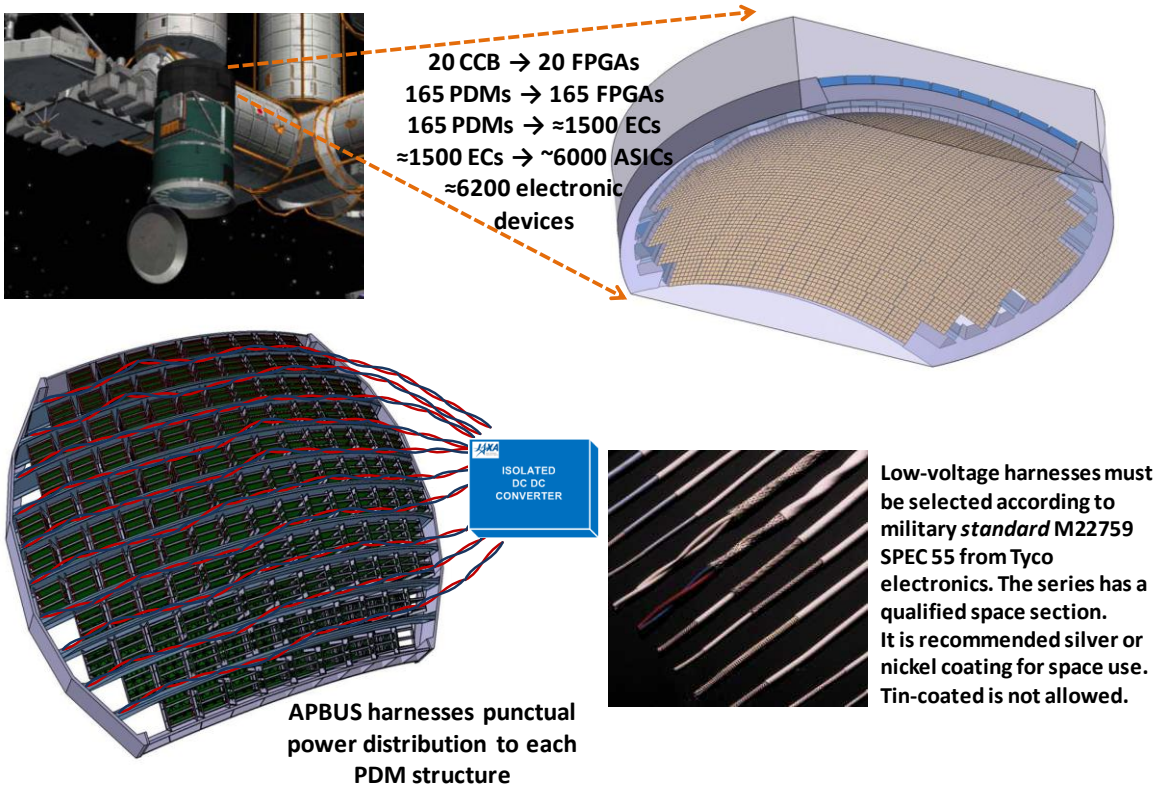


Figure45. Low-voltage power distribution at PDM level.

As can be observed in the figure 45 above, several drawbacks are identified in this proposal the most important are: mass and length cables, space available in PDM structure, thermal management, high cost due to the several power devices and

high levels of radiated emissions. On the other hand, efficiency could be acceptable, and in case of fault events just a PDM area could be lost.

The second proposal was based on divide FS, in such way, that the number of sections generated will match with the CCB subsystem units (18 or 20). Therefore, same number of power supply modules will be created. Figure 46 shows the power distribution from PDAP to each power supply module, and the harnesses coming out from each power supply module to PDM subsystems.

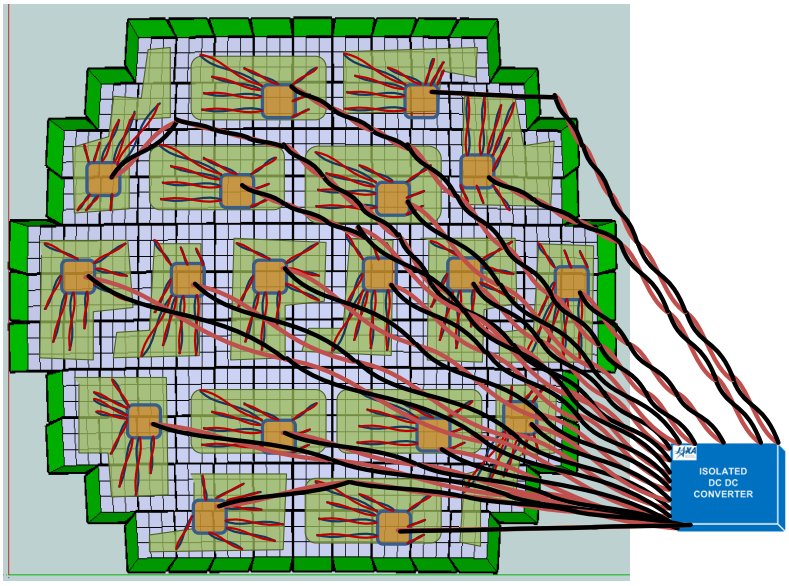


Figure46. Low-voltage power distribution at cluster level.

In the figure 46 above, the harnesses from PDAP of APBUS are reduced. Also, main source of EMI are removed from PDM structure. However, it will be required to accommodate power supply modules at each cluster, and provide the harnesses required in order to distribute low-voltage at cluster level. The latter implies increase the mass over the mechanical structure of focal surface.

The third proposal was based on the idea to decrease the mass over FS structure. The latter will be reached taking the advantage of CCB boxes location. There are planned four boxes, as is showed in figure 47, which its purpose is to house five CCBs per box, and the same time the focal surface data management is divided in four parts. On the other hand, thermal management is concentrated on theses boxes, and heat could be conducted over all structure box directly to the focal surface.

The main drawback about this proposal is propagation of failure event. In JEM-EUSO the propagation failure is not allowed. In case of failure event occurs, by PDM subsystems, cannot be propagated far than CCB boxes. A solution could be implement latch current limiters in PDM, as well as CCB subsystems.

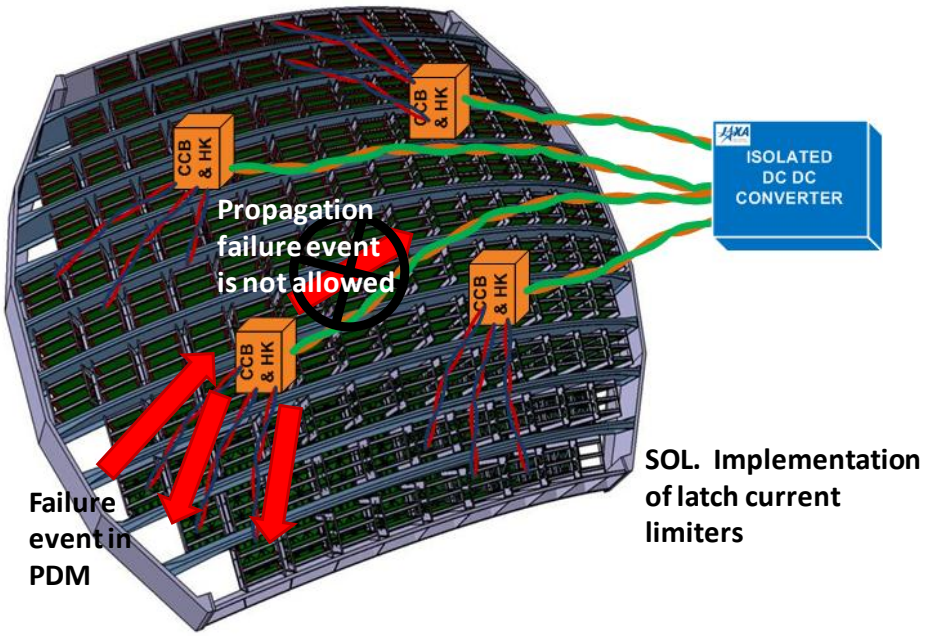


Figure47. Low-voltage power distribution at CCB boxes.

Therefore, the necessity to distribute low-voltage levels over the focal surface comprised by ~6200 programmable electronic devices inside PDMs structures, plus the EMC constraint imposed by EC components, demonstrates the complexity for distributing power at low-voltage levels in JEM-EUSO instrument. Furthermore, the mechanical dimensions of the focal surface structure and boxes location of additionally electronic represented by CCB, GPSR, CLKB and CPU, make a more difficult scenario to identify the best suited power distribution architecture to implement. Thus, the LVPS subsystem development that involves, such kind of instrument, represents a very complicated challenge due to hierarchical and mechanical structure instrument.

Regarding all above stated, it was necessary to propose a preliminary project in order to demonstrate three main objectives. The first one was to prove the capability to perform the first detection of EAS, by looking from above atmosphere, using the chain detection proposed at JEM-EUSO. The second one was to perform full end-to-end test of hardware selected for JEM-EUSO, in a reduced version of the later, resulting in the instrument qualification model of JEM-EUSO. And finally, perform critical measurements of UV background. The project to demonstrate, before stated, is called EUSO-Balloon and represents the case of study of this work.

II.5 EUSO-Balloon instrument

EUSO-Balloon instrument has been designed and built by a consortium led by French Space Agency (CNES), and comprised by laboratories from France, Germany, Italy, Japan, Mexico, Poland, South Korea and Spain. The instrument is a fully operational prototype of JEM-EUSO, a scaled version of that instrument, and still comprises all the subsystems of the main mission. The instrument idea is based on a stratospheric balloon which will operate at an altitude of 40km, during the night, and measure photons in the UV range with a time resolution of 2.5μs with a field of view of 12ºx12º and a large dynamic range (1 to 10^4 photo-eV per GTU). The Figure 48 shows the altitude and orbital speed comparison between both instruments, JEM-EUSO and EUSO-Balloon. The EUSO-Balloon also has the potential to detect for the first time a cosmic ray atmospheric shower from above, marking a key milestone in the development of UHECR science, and paving the way for any future large scale, space-based UHECR observatory, including of course JEM-EUSO [48].

Figure48. Comparison in operational conditions of both instruments.

The main objectives of the EUSO-Balloon instrument are:

a) Perform a full end-to-end test of JEM-EUSO qualification model pointing out its technical readiness level.
b) Measure critical and terrestrial UV background components and,
c) Perform the first detection of air-showers by looking from above the atmosphere.

EUSO-Balloon instrument consist, firstly, of a Fresnel optic array comprised by tree polymethyl-methacrylate square lenses for UV transmitting. After that, a focal plane detector composed of 36 MAPMT's with 64 pixels each representing 2,304 pixels, called PDM is included. The last implies a 2x2 MAPMT's array, called EC, has its ASIC, high voltage supply (HV) and HV switches.

The 15 x 15 cm PDM and the 100 cm x 100 cm Fresnel lenses provide a field of view of ± 6° and shall observe in “nadir mode” that can be varied, in principle, during later flights in a range between 0° to 30°.

Therefore, the UV light entering in optics system is imaged on PDM. The later normally works in single-photoelectron mode; however, it can also extend its dynamic range in order to observe intense light signals thanks to the implementation of gain switches. The signal from each MAPMT is processed by the FEE (based on the ASIC) and preliminary processed in the so-called PDM board, which is inside of PDM structure where the first-level trigger is performed. Data are then transferred to the DP subsystems where the second level trigger is first applied by the CCB, after those data are prepared to be sent as a part of telemetry information. Data management and storage, instrument control and commanding are managed by CPU board inside of DP structure which represents third trigger level.

The Figure 49 shows the main components of the EUSO-Balloon instrument.

1) Telescope (TES).
2) Optics (OPT).
3) Electronics (ELS).
4) Power (PWS), and
5) The camera (CAM).

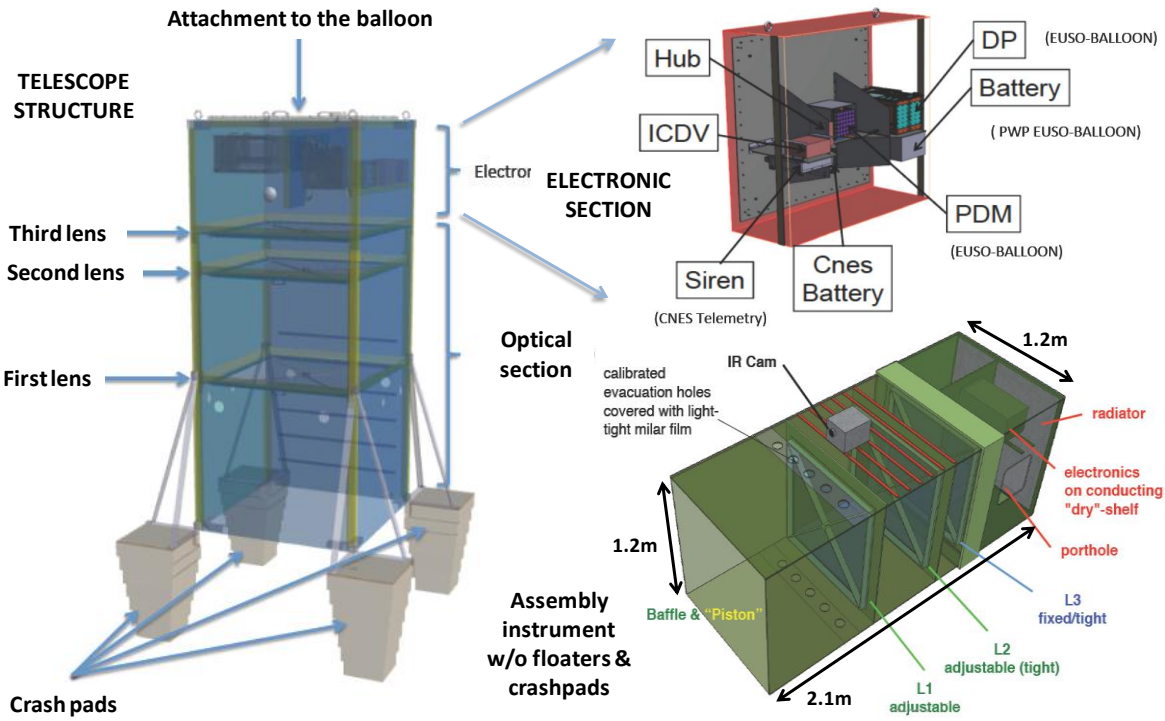


Figure49. Main components of EUSO-Balloon instrument [43].

As stated before, this work focuses on the electronic of FS detector. Therefore, in EUSO-Balloon ELS is divided into two main structures: PDM and DP. The PDM plays the role of FS of the instrument and includes the FEE that performs signal acquisition, digitization, and the first level trigger selection. The DP structure includes the digital electronics of the instrument, controls FEE, and performs level trigger filtering. On the other hand, the power pack (PWP) includes batteries assembly and protection circuitry [42]. As it can be observed in the figure 49, there are other components which have specific functions on the performance instrument, but their description goes beyond the scope of this work.

Therefore, EUSO-Balloon will serve as an evaluation test-bench for JEM-EUSO mission, as well as any future mission dedicated to the observation of EAS from space. Through a series of stratospheric balloon flights, all the components and subsystems that comprise EUSO-Balloon should demonstrate the right performance of the instrument at three levels.

Level-A, should demonstrate that all the key technologies and instrumentation of JEM-EUSO can be calibrated and validated during its performance on cosmic ray acquisition. The level-B, should demonstrate the proper operation of on-board hardware and software algorithms involved in the triggering and recognition of cosmic-ray initiated EAS. And finally, level-C should demonstrate that JEM-EUSO mission is a feasible project, by the success of precursor mission: EUSO-Balloon project. The latter by performing the first detection ever of air-shower looking downward from space [42].

Table 1, shows ELS and PWS components as well as elements that conform balloon instrument. As can be observed, EUSO-Balloon comprises all PDM electronics, not in amount but in sort of elements, plus one unit of remaining subsystems. Furthermore, in table 1 is denoted the country responsible of procurement the requirements and specifications, as well as delivery of various equipment on instrument. This list becomes in a very important issue, regarding interaction level, during integration phases of the instrument.

Component	Structure	Subsystem	Acronym	Country
ELS	PDM	Elementary Cell –ASIC	EC-ASIC	France/Germany
		High Voltage Power Supply	HVPS	Poland & France
		PDM Board	PDMB	South Korea
		LVPS for PDM subsystems	LVPS-PDM	México
	DP	Cluster Control Board	CCB	Germany
		Clock Board	CLKB	Italy
		GPS Receiver	GPSR	
		Data Storage	DST	
		Central Process Unit	CPU	
		Housekeeping	HK	Mexico
		LVPS for DP subsystems	LVPS-DP	
PWS	PWP	Battery	BAT	Japan

Table1. Political and technical responsibilities in the procurement and delivery of various subsystems of EUSO-Balloon instrument.

The description of subsystems listed in table 1 is more and less the same of JEM-EUSO instrument description section. Some changes on power consumption are due to the sort of technology used. The figure 50 shows the block diagram of the instrument. As can be observed, the tree main components of PDM structure are: EC, HVPS, and PDMB. The cores of these components are based on ASIC's and FPGA's, which perform signal acquisition and digitalization as a part of readout process and first trigger level detection, respectively. On the other hand, the DP structure comprises the CPU, DST hard disks, CCB, CLKB which dictates the system master clock, GPSR, and the HK. The latter monitors the instrument; generate alarms, reset signals and powers on/off every other subsystem at the request of either the CPU or ground station. As in the PDM structure, the cores of all DP components are FPGA's and MPU which have tight constraints about voltages levels requirements. A first approximation of the power distribution system is based on one LVPS module for each structure: LVPS-PDM & LVPS-DP.

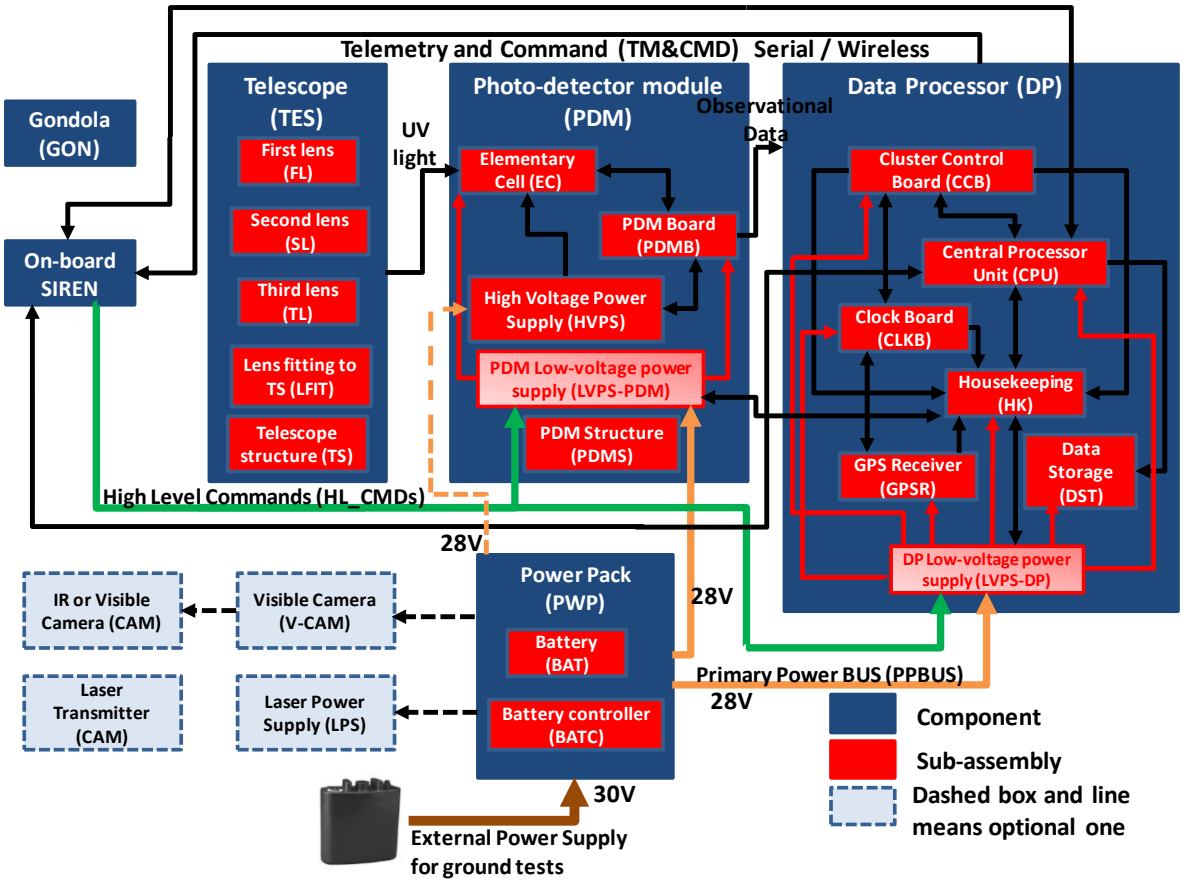


Figure50. Functional block diagram of EUSO-Balloon instrument.

As can be observed in the figure 50 above, an external power supply is used during ground tests in order not to degrade the flight battery array.

EUSO Balloon PWP is designed to maintain constant power of 225 W for the phone-booth during 24 hours flight. The power bus, supplied by the battery cell array, is 28V with a current capability of 192.7Ah during operation duty of 24h. The operation range temperature goes from -40ºC to 70ºC at 40km of height. The dimensions of the PWP envelope are 500mm x300mmx170mm and the weight is about 30kg. As main component of the battery in EUSO-Balloon was selected the lithium G62 from SAFT manufacturer which were arranged in 6 of 10 cell series batteries. The expected cell array voltage excursion goes from 28V to 18V due to battery discharge. As it can be seen in the figure 51, the battery pack includes not only the battery array, but also control and protection components, like electrical and thermal fuses [49]. Additionally, there is an external power source intended to use during ground tests, a switch to select main power line, either the EUSO battery array or the external power source, is also foreseen.

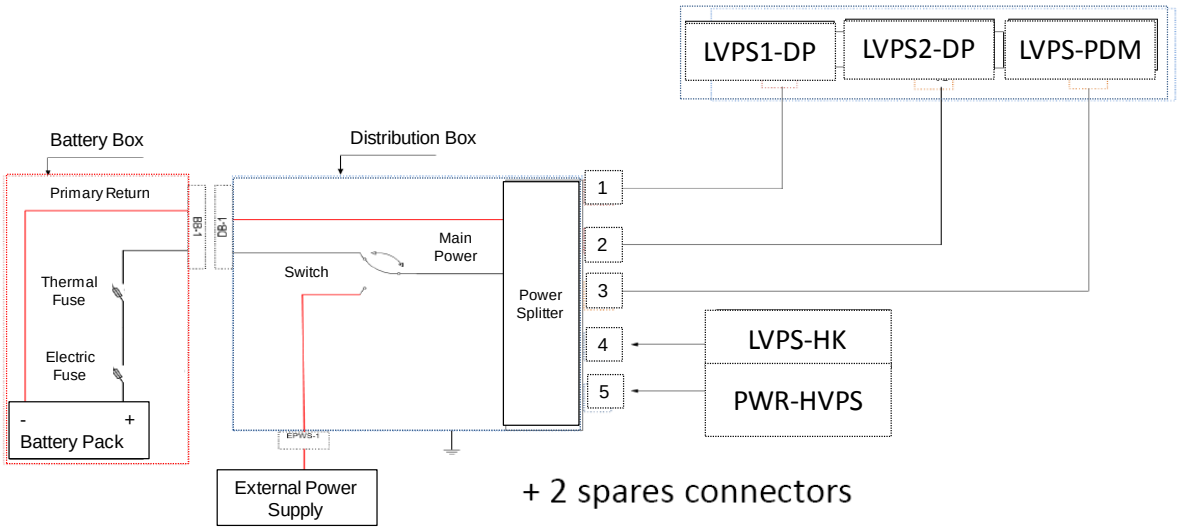


Figure51. Battery pack connection diagram [49].

The PWP will be attached to the GONDOLA and will provide power to LVPS modules and HVPS subsystem. In the figure 50, the external source provides the nominal 30V primary power bus without load (brown arrow). Once payload is attached a 28V bus (orange arrows) is distributed to LVPS modules (LVPS-PDM & LVPS-DP) and to HVPS subsystem (orange dashed line). After that, is planned that LVPS modules distribute low-voltage levels (red arrows) to its respective payload according to subsystems requirements and specifications.

Finally and once stated the JEM-EUSO description and complexity; in the next chapter, main objectives and scope of this work will be stated, and after that the case of study will be addressed by requirements and specifications definition.

III.1 Problem statement

Although theoretically sound, the Earth's observational principle of UHECR has never been tested from space. JEM-EUSO will lead against considerable uncertainties with regard to the intensity of the Earth up-going UV background produced by the atmosphere and the ground due to both, the Moon and terrestrial sources, as well as the UV diffuse reflectivity of different types of ground (sand, snow, ice, clouds, vegetation, oceans, etc.) which can affect the reconstruction efficiency and the effective duty cycle of the instrument. Furthermore, the instrument is very complex, owing a high density of EAS that has never been observed yet from space. Therefore, a large scale comprehensive prototype is mandatory: EUSO-Balloon instrument is such prototype.

As is well known, in every space mission the power budget is limited, so the PDS must be designed in such way that efficiency is as high as possible regarding the several operational modes of the mission. The problem of power distribution at payload level lies on requirements and constraints imposed from various

equipment by the large amount of subsystems which, in turn, are comprised of various nature electronic devices each (analogue and digital circuitry).Therefore, the aim of this work is to research, propose and develop the low-voltage power supply subsystem for a JEM-EUSO fully operational prototype: EUSO-Balloon instrument.

III.2 Research objectives

The main objectives and contributions of this work can be stated as follows:

- To perform a research based on the state-of-the-art of low-voltage power supply distribution architectures implemented in space environment on large scale instruments.
- Propose the best suited strategy for distributing low-voltage levels on a large scale comprehensive and fully operational prototype: EUSO-Balloon instrument. Furthermore, the strategy proposed will serve as a basis for designing LVPS subsystem of a unique and novel large scale instrument, JEM-EUSO, in the context of cosmology or analyses in relativistic fundamental physics research.
- Develop the LVPS subsystem proposal. The later means design, manufacture, validate and implement the LVPS strategy proposed, according to requirements, specifications and constraints imposed from various subsystems of the instrument.

III.3 Significance of the research

Reviewing the previous chapters of this work, it is relatively easy to detect various space projects development referenced, involving radar, surveillance, communications, and Earth observing satellites, as well as huge projects like ISS. These spacecrafts serve as host entities to house several experiments with different aims and objectives. The experiments usually are comprised by payloads with technology according to its targets. In that way, several research groups around the world in fundamental physics field had been devoted to develop large UHECR ground detectors. A very good example of later is the Pierre Auger Observatory.

The Pierre Auger Observatory is a hybrid detector, located on the vast plain known as "*The Pampa Amarilla*" (yellow prairie) in the western of Argentina. This observatory employs two independent methods to detect and study the UHECR. One technique detects high energy particles through the interaction with water inside surface detector tanks. The other technique tracks the development of air showers by observing ultraviolet light emitted in the Earth's atmosphere [50].

Therefore, in order to perform the two detection methods the observatory uses 1600 water tanks (of 3.5m of diameter and 1.5m of height) and six optical detectors. The water tanks and optical detectors conform an UHECR detection network that covers a 3000m^2 of ground surface. However, in the development of such kind of detectors, scientists face a very complex challenge because the UHECR are extremely rare. Cosmic Rays with energies of over 10^{20}eV have an estimated arrival rate of just 1 particle per square kilometer per century [50]. The last issue implies that UHECR ground detectors, in order to record a large number of these remarkable events, will need a huge ground surface detection area.

Consequently, JEM-EUSO instrument becomes in a novel an ambitious project within the UHECR detection, because offers the opportunity for the first time to perform UHECR detection from space, by using a detector of 2.6m diameter composed by more than 6200 electronic devices. The detector will provide, in nadir mode, ~200,000km^2 of observational area increasing in such way the ground detection surface. Therefore, is mandatory the right performance of all subsystems comprised by this large scale detector. Then, LVPS subsystem plays a very important role on instrument performance regarding operational environment, thermal management, number of subsystems involved, cost technology, mass and EMC issues.

In next chapter, instrument requirements and specifications of EUSO-Balloon instrument will be stated according to instrument performance. Based on later, best suited strategy will be given in order to meet the relevant requirements and specs. Furthermore, design, manufacturing and validation process will be described towards the production of the flight model.

IV.1 Requirements

In order to produce a good design, many questions should be asked prior to the beginning of the design process. Moreover, this will help to state the most essential information to meet the main objective of a project. In engineering field, the requirements are used as input data of a design stage. The requirements should establish WHAT the system performance must be? But NOT necessarily HOW it will achieve such performance? In other words, the *requirements document* is a statement that identifies a necessary attribute, capability, characteristic, or quality of a system (or subsystem) in order to provide value and utility to a user.

The LVPD system requirements will define, to a certain extent, the interaction level with other subsystems. In order to establish the best suited strategy, requirements were divided in four sections.

IV.1.1 Functional

- The LVPS shall supply power in a reliable way to PDM and DP structures.
- The LVPS subsystem shall consist, at least, of two different power distribution modules: LVPS-PDM and LVPS-DP.
- The LVPS modules shall provide isolation interface between the 28V bus of PWS and all other payload subsystems.
- The isolation stage will comprise isolated DDCU's with efficiencies equal or higher than 80%.
- The DDCU's shall provide wide input voltage range in order to withstand input voltage variations from nominal values due to discharge of the battery power pack (PWP).
- The regulation stage shall be performed directly at load, or as close as possible, for best performance.
- The tight regulation stage will comprise niPOL converters with efficiencies higher than 90%.
- Propagation failures inside of LVPS modules should be confined. If any failure event occurs, it cannot propagate to either the primary or secondary sides of the isolation stage.
- The LVPS modules shall provide remote ON/OFF functionality in order to be controlled either from the ground through SIREN, or on-board from HK.
- The DDCU's shall provide input circuit protection function in order not to damage circuitry attached to the main bus by some abnormalities.
- The DDCU's shall provide over-current output protection function.
- Input and Output EMI filters should be considered in the design of the LVPS modules.
- The maximum PCB dimensions shall meet the 3U EUROCARD standard size board.
- The weight of LVPS subsystem, including casing and harnesses, must not exceed the 5kg.

IV.1.2 Environmental

- The electronic components of LVPS must withstand temperature variations within the range -20°C to +50°C during operation.
- The electronic components must accept storage temperature of -40°C.
- The instrument (including components) shall withstand vertical acceleration equal to 10Gs, and horizontal acceleration equal to 5Gs.
- All the elements of LVPS must able to operate at a low residual atmospheric density equivalent to 3 mbar of pressure.

IV.1.3 Interface

- Tele-commands shall be used for turning On/Off LVPS modules remotely.
- The On/Off status by contact closure (CC) signal shall be provided from LVPS modules.
- Telemetry information about V&I levels shall be generated on-board LVPS modules and transmitted to the HK subsystem.

IV.1.4 Schedule

- The model development philosophy is according to following sequence: bread board model, engineering model, qualified model and flight model.
- The flight model must be delivered on December 2013.
- The first flight of stratospheric balloon is programmed on August 2014.

Once the general requirements are defined, it is important to provide the necessary detailed information based on the specific requirements. This explicit information describes the technical characteristics of a product or system, and is often stated at the *specifications document*.

IV.2 Specifications

The LVPS requirements stated in the previous section define, to a certain extent, the interaction level with other subsystems. On the other hand, the specifications describe the technical subsystem features. This explicit information provides the procedure to be followed for determining whether the requirements are met [51].

The table 2 summarizes the EUSO-Balloon subsystem specifications which will help to propose the best suited strategy for low-voltage power distribution architecture. This table contains those subsystems which interact with LVPS subsystem. In the table 2 can be observed key parameters like power consumption expected as well as the power consumption plus a safety factor, voltage levels, tolerances, operating temperature range, and mass expected from each subsystem.

Main Subsystem	Component	Element Subsystem	Electronic Device	Power Expected (W)	Power + SF (W)	Voltages (V)	Output Tolerance (%)	Temp (ºC)	Mass (kg)
PWS	PWP	Battery	N.A.	100	225	28	+7 above -36 down	-40 to 70	30
ELS	PDM	EC	ASIC's	10	15	3.3_A, 3.3_D, & 1.5	±10	-30 to 50	0.5
		PDMB	FPGA	10	15	3.3, 2.5, 1.8, 1.5 & 1			0.7
	DP	CCB	FPGA	5	6	3.3, 2.5, 1.8 & 1.5		-40 to 100	<0.3
		CPU	MPU	12	15	5 & 3.3	±25	-20 to 70	<1
		DST	SSD	15	30	5	±10	0 to 70	<0.6
		CLKB	FPGA	4	5	3.3, 2.5 & 1.8		-40 to 85	<0.3
		GPSR	GPS	1.5	2	5		-40 to 80	0.3
		HK	MCU	0.5 & 5	8 & 2	±12, 5 & 3.3	+10 above -50 down	-40 to 40	0.3

Table2. Summarize subsystems table specifications.

In next section, is described the LVPS distribution proposal and development regarding the most relevant requirements and specifications stated during this chapter.

IV.3 Constraints in the design

The power supply assumes a very unique role within a typical system. In many aspects, it is the mother of the system. It gives the system life by providing consistent and repeatable power to its circuits. It defends the system against the harsh world outside the confines of the enclosure and protects its wards by not letting them do harm to themselves. If the supply experiences a failure within itself, it must fail gracefully and not allow the failure to reach the system [52].

The latest high-performance FPGAs, ASICs and MPU require increased high performance on voltage levels from power supply. Typical requirements include low voltages (sometimes less than 1V), high currents (up to 3A), tight regulation (less than 1%), fast transient response, and even supply voltage sequencing. Meeting the latest issues becomes more difficult for small configurations, understanding the last term as the necessity to supply many low-voltages leading to a proliferation of converters, increasing in that way cost and board space demand. Therefore, a trade-off study must be performed considering the following constraints:

- Number of payloads involved
- Operational environmental conditions
- Efficiency
- Dynamic response
- Thermal management
- EMC (emissions and susceptibility)
- Reliability
- Power technology intended to use
- Electrical interfaces
- Development cost
- Mass and mechanical dimensions
- Instrument subsystems integration
- Development time

The constraints above stated play a very important role on LVPS subsystem design. In the next section, it is shown the current subsystems interactions on instrument.

IV.4 Low-voltage power distribution architecture

Many are the issues that play an important role in determining the best power distribution architecture on a determined instrument. These factors help not only in selecting the most suitable strategy for power distribution architecture development, but will also constitute a basis for selecting the most appropriate power technology.

The first conception on instrument hierarchical components and subsystem disposition is shown in functional block diagram of figure 50. However, due to the number of interactions occurring with DP subsystems, an alternative block diagram is proposed in figure 52. Here, all DP and PDM subsystem interactions are shown through different communication protocols: SPI, RS422, RS232, SpaceWire and USB. Also, two LVPS blocks are showed, one housed inside the DP box (black dotted line) which is LVPS-DP, and other housed inside the PDM box, LVPS-PDM.

However, taking into account mechanical constraints as heat distribution, thermal coupling, and power consumption requirements specified in table 2; three different LVPS modules (blue squares) are proposed, instead of a single one, in order to power DP subsystems, as shown in figure 53: LVPS1-DP, LVPS2-DP and LVPS-HK. The latter will represent an isolation and transformation stage between PWS and payload components.

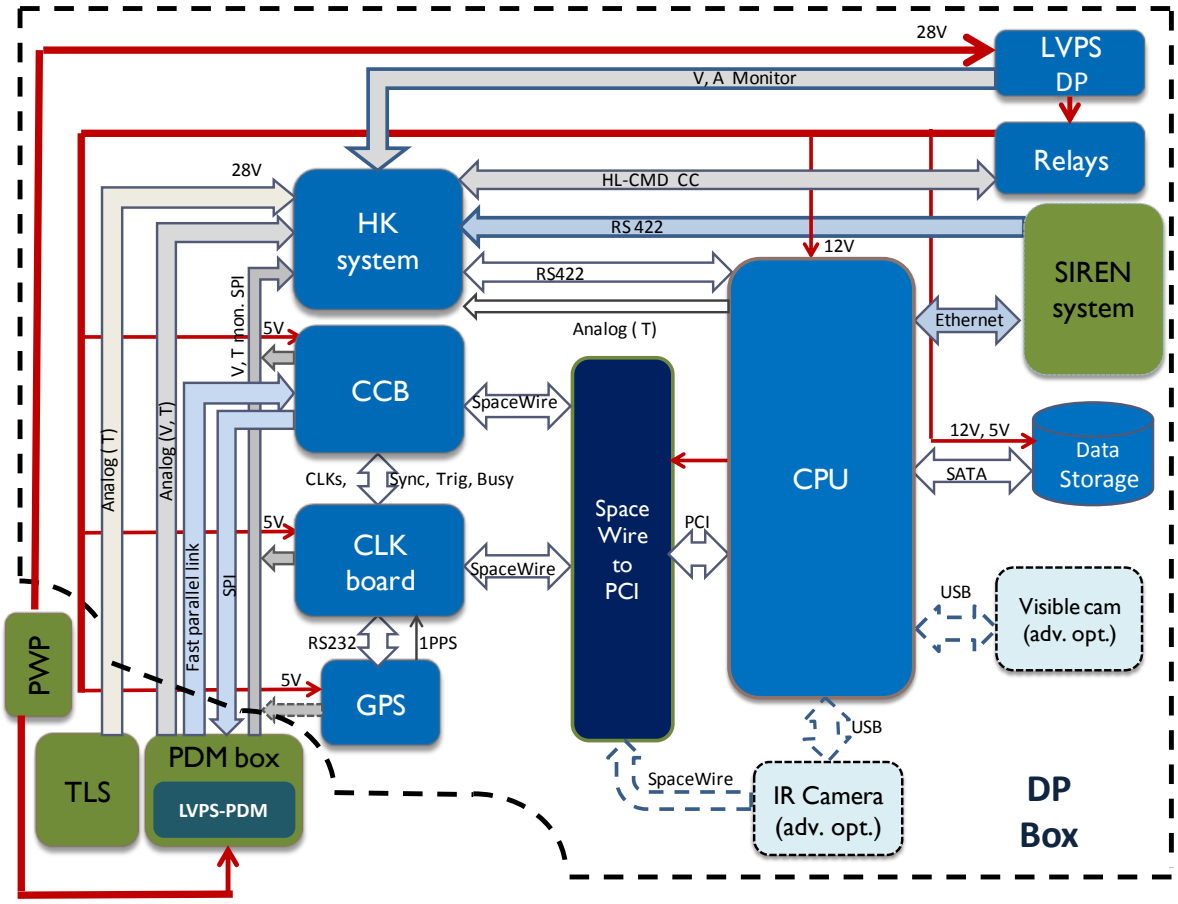


Figure52. DP and PDM subsystem interaction block diagram.

The proposal to increase the number of LVPS modules, up to three, obeys to following reasons: to prioritize the subsystems involved according to importance on instrument performance, to avoid ground loop disturbances by sharing line returns, to identify subsystem critical dynamic response, and a better heat distribution as well as thermal coupling.

On the other hand, in order to avoid radiated and conducted EMI generated within the PDM detector structure, which in principle has the most EMI-susceptible components, it was decided to install the LVPS module of PDM (LVPS-PDM) inside of the DP rack as well, as can be seen in figure 53 (green square).

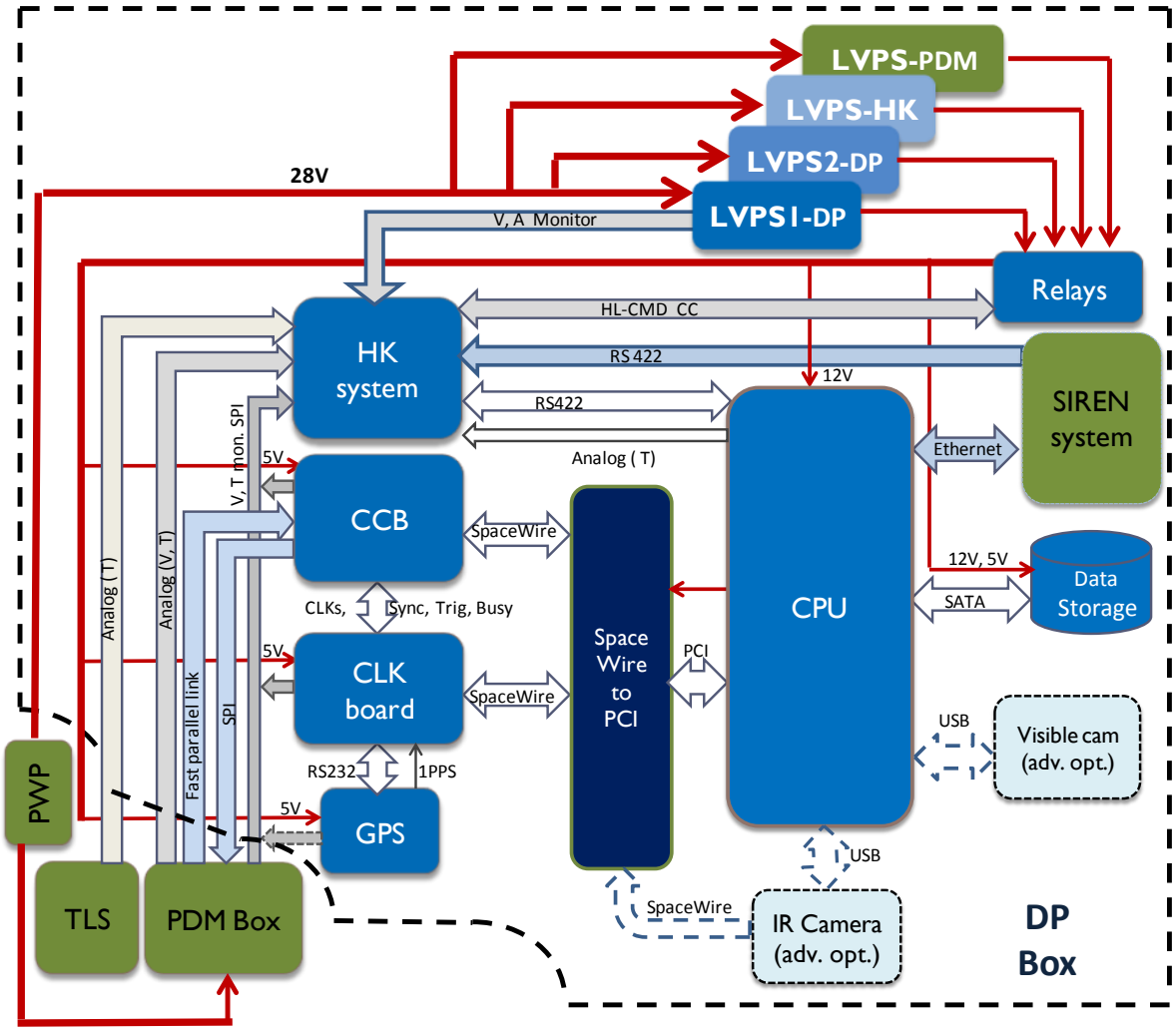


Figure53. EUSO-Balloon power distribution architecture proposed.

This strategy obviously increases number of LVPS modules, which cause the undeniable disadvantage of pushing up costs and complexity; nevertheless, it improves heat dissipation, system reliability, while decreasing EMI disturbances by ground loops generated due to ground planes sharing of different voltage levels subsystems.

Therefore, from the system performance point of view, it is a won't paying added cost. In the case of LVPS modules devoted to DP components, it is important to highlight that modules were planned and disposed according to hierarchical importance and criticality on the instrument performance. This strategy also facilitates heat dissipation and increases the overall reliability of the instrument. Regarding efficiency, the later is decreased due to tight regulation stage added by the implementation of niPOL on-board subsystems. However, this recommendation improves load and line regulation parameters, as well as fewer losses of PCB tracks due to the possible high current levels demanded.

Summarizing, the power distribution architecture proposed is based on four LVPS modules arranged according to hierarchical importance and criticality on performance instrument, which its aim is to provide isolation and transformation stage. The modules proposed and its subsystem clients are listed in table 3.

LVPS module	Subsystem clients
Low-voltage power supply for the Housekeeping (LVPS-HK)	Powers the different PCBs, disposed in stack assembly, of monitoring subsystem.
Low-voltage power supply 1 for Data Processor (LVPS1-DP)	Powers the subsystems in charge of second trigger level, master clock signal, and UTC parameter in recorded events, CCB, CLKB & GPSR respectively
Low-voltage power supply 2 for Data Processor (LVPS1-DP)	Powers the master processor unit, and the operative system storage on hard disks, CPU & DST respectively.
Low-voltage power supply for PDM (LVPS-PDM)	Powers elementary cells of PDM array, as well as PDMB

Table3. LVPS modules proposed.

As stated at the beginning of this section, once the power distribution architecture is defined, it is important to starts a methodology in order to select the most appropriate power technology to be used on the implementation of the design.

IV.5 Selecting appropriate power supply technology

Once that the instrument and subsystem overview, as well as distribution architecture has been achieved, the proper power supply technology within the system must be selected. The most important issues that influence this stage of design are:

- Cost
- Efficiency
- Heat generated
- Input power source(s)
- Noise tolerances
- Number of outputs and its characteristics
- Weight and dimensions (low-profile)
- Components obsolescence
- Procurement time scales

For this work, three major power supply technologies were considered: linear regulators, PWM SMPS and high efficiency resonant SMPS. Each one of these technologies excels in one or more of the system considerations mentioned above, and must be weighed against the other considerations to determine the optimum mixture of technologies that meet the needs of the final product [52].

IV.5.1 Linear regulators

Linear regulators are used predominantly in ground-based equipments where the generation of heat and low efficiency are not a major concern, and also where low cost and a short design period are desired. They are very popular as on-board level regulators in distributed power systems where the distributed voltage is less than 40VDC. For off-line (plug into the wall) products, a power supply stage ahead of the linear regulator must be provided for safety in order to produce dielectric isolation from the ac power line. Linear regulators can only produce output voltages lower than their input voltages and each linear regulator can produce only one output voltage [52].

IV.5.2 PWM SMPS

These devices are much more efficient and flexible in their use than linear regulators. One commonly finds them used within portable products, aircraft and automotive products, small instruments, off-line applications, and generally those applications where high efficiency and multiple output voltages are required. Their weight, on systems implementation, is less than that of linear regulators since they require less heat-sinking for the same output ratings. They do, however, cost more to produce and require more engineering development time [52]. The major drawback of this sort of supplies lies on the EMI emissions conducted and radiated provided to entire system.

However, these devices are used in critical field applications as military and space programs receiving power from a main power bus and regulate their outputs to a narrow voltage range. Usually, the satellite power bus voltage can range from 20Vdc to 120Vdc. Meanwhile, payload electronic and bus system typically require 3.3Vdc to 28Vdc although at present the voltage requirements are decreasing towards 1Vdc and less for digital loads [53]. Taking into account the high cost of these missions and the impossibility of repairs, the DDCU must comply with general requirements as reliability tests, good efficiency, good load and line regulation, low output ripple, meet EMC standards and input/output protections.

IV.5.3 High efficiency resonant switching mode power supply

This variation on the basic PWM switching power supply finds its place in applications where still lighter weight and smaller size are desired, and most importantly, where a reduced amount of radiated noise (interference) is desired. The common products where these power supplies are utilized are aircraft avionics, spacecraft electronics, and lightweight portable equipment and modules. The drawbacks are that this power supply technology requires the greatest amount of engineering design time and usually costs more than the other two technologies.

Therefore, it was decided to use the PWM SMPS as power technology for isolation and transformation stage. This technology was selected considering topics as manufacturer variety suppliers, reasonable costs, and relatively shorts procurement time scales (a month at best case) for isolated board mounted modules, as well as diversity regarding converter type package and relatively easy pin-out replacement. Also, and not less important, the experience achieved in designing SMPS along this development project. Moreover, linear regulators are admissible (as on-board level regulators) in those places which constraints as space and heat dissipation are not key factors.

IV.6 Developing power system design by specifications

The *design specification* document acts as the performance goal that the ultimate power supply must follow in order to meet its overall performance over entire instrument. Therefore, once that the summarized specifications in table 2 were frozen, certain precautions were considered regarding power consumption. The later led us to add about 25% to 50% safety margin to the output current capabilities of power supply during design process in order to accommodate subsystems eventualities. However, this sort of precaution shall not compromise the assigned space to allocate the power system modules, as well as project schedule development. Moreover, since the power system is a support function within the product, its design will be subject to constant modifications in reaction to design issues within the other sections of the product. This will always make the power supply design the last circuit to be released for production [52].

Before starting the LVPS modules description, it is important to quantify some important parameters, according to performance instrument, for using them on the selection of SMPS. In the following section are defined and quantify, in tables, some of those parameters.

IV.6.1 Electrical parameters

In table 4 are shown the input nominal voltage $Vin_{(nom)}$ at which the LVPS modules shall to operate during flights development. Also, the lowest anticipated operational input voltage $Vin_{(low)}$ at which the subsystem can perform emergency tasks, as well as the highest anticipated operational average input voltage $Vin_{(hi)}$. All these parameters are dictated by output's battery. Furthermore, in the same table are stated some observations regarding these parameters.

Other parameters, but dictates by subsystems, are the nominal output voltage $Vout_{nom}$ (ideal) at which operation of client subsystem should properly works during experiment. The output voltage below which the load should be inhibited or turned off, often called minimum output voltage $Vout_{(min)}$. In similar way, the maximum output voltage under which normal operation of the load circuits can operate, it is called maximum output voltage $Vout_{(max)}$.

Regarding current consumption, the maximum average current that will be drawn from an output $Iout_{(rated)}$, according each subsystem, is called output current rated. In similar way the minimum current that will be drawn from the output of the LVPS module, during normal operation, is called minimum output current $Iout_{(min)}$.

Abbreviation	Parameter	Value	Comments
Vin_{nom}	Input nominal voltage	28V	These voltages correspond to battery output voltages conditions.
Vin_{low}	Lowest operational input voltage	18V	
Vin_{hi}	Highest operational input voltage	30V	
Vo_{nom_EC}	Nominal output voltage for EC	5.5V	In these cases the nominal output voltage was proposed according to OB converters for lower voltages distribution. Meanwhile the overall current demand was dictated by each subsystem.
Vo_{min_EC}	Minimum output voltage for EC	4.5V	
Vo_{max_EC}	Maximum output voltage for EC	9V	
Io_{rated_EC}	Maximum current drawn by EC	2A	
Io_{min_EC}	Minimum current drawn by EC	0.6A	
Vo_{nom_PDMB}	Nominal output voltage for PDMB	5.5V	
Vo_{min_PDMB}	Minimum output voltage for PDMB	4.5V	
Vo_{max_PDM}	Maximum output voltage for PDMB	9V	
Io_{rated_PDMB}	Maximum current drawn by PDMB	2A	
Io_{min_PDMB}	Minimum current drawn by PDMB	0.6A	
Vo_{nom_CCB}	Nominal output voltage for CCB	5V	
Vo_{min_CCB}	Minimum output voltage for CCB	4.5V	
Vo_{max_CCB}	Maximum output voltage for CCB	5.5V	
Io_{rated_CCB}	Maximum current drawn by CCB	1A	
Io_{min_CCB}	Minimum current drawn by CCB	0.3A	
Vo_{nom_CPU}	Nominal output voltage for CPU	12V	In some cases, due to the tight schedule development project, the nominal output voltage was settled according to development board used by each subsystem to perform its main task. Meanwhile the overall current demand was dictated by each subsystem.
Vo_{min_CPU}	Minimum output voltage for CPU	9V	
Vo_{max_CPU}	Maximum output voltage for CPU	15V	
Io_{rated_CPU}	Maximum current drawn by CPU	1A	
Io_{min_CPU}	Minimum current drawn by CPU	0.3A	
Vo_{nom_DST}	Nominal output voltage for DST	5V	
Vo_{min_DST}	Minimum output voltage for DST	4.5V	
Vo_{max_DST}	Maximum output voltage for DST	5.5V	
Io_{rated_DST}	Maximum current drawn by DST	3A	
Io_{min_DST}	Minimum current drawn by DST	1A	
Vo_{nom_CLKB}	Nominal output voltage for CLKB	5V	
Vo_{min_CLKB}	Minimum output voltage for CLKB	4.5V	
Vo_{max_CLKB}	Maximum output voltage for CLKB	5.5V	
Io_{rated_CLKB}	Maximum current drawn by CLKB	0.8A	
Io_{min_CLKB}	Minimum current drawn by CLKB	0.3A	
Vo_{nom_GPSR}	Nominal output voltage for GPSR	5V	
Vo_{min_GPSR}	Minimum output voltage for GPSR	4.5V	
Vo_{max_GPSR}	Maximum output voltage for GPSR	5.5V	
Io_{rated_GPSR}	Maximum current drawn by GPSR	0.3A	
Io_{min_GPSR}	Minimum current drawn by GPSR	0.2A	
Vo_{nom_HK}	Nominal output voltage for HK	±12V & 3.3V	
Vo_{min_HK}	Minimum output voltage for HK	±9V & 3V	
Vo_{max_HK}	Maximum output voltage for HK	±15V & 3.6V	
Io_{rated_HK}	Maximum current drawn by HK	±0.23A & 0.15A	
Io_{min_HK}	Minimum current drawn by HK	±0.15A & 0.1A	

Table4. Electrical parameters specifications at which LVPS must operates.

On the other hand, due to the different instrument operation modes all subsystems will perform several tasks at different processing speeds. The later will result on variations of power consumption, and also in the possibility of loads that may be removed from or added to the system as part of overall system architecture. This inconvenient point out other very important parameters like: *Line regulation* which refers to the percentage change in the output voltage(s) in response to a change in the input voltage [52], such relation is represented by equation 5.

$$Ln_{reg}(\%) = \frac{Vo_{Hi-In} - Vo_{Lo-In}}{Vo_{Nom-In}} \times 100 \quad (5)$$

Where $Vo_{Nom\text{-}In}$ is the output voltage at the nominal input voltage. Meanwhile, $Vo_{Hi\text{-}In}$ and $Vo_{Lo\text{-}In}$ are the output voltage when input voltage is at allowed highest and minimum value, respectively. In similar way, *load regulation* is defined as the percentage change in the output voltage in response to a change in load current, from full-load $Vo_{full\text{-}load}$ to one-half rated load $Vo_{half\text{-}load}$ divided by voltage output at ideal rated load $Vo_{rated\text{-}load}$ [52]. The relationship is represented by equation 6.

$$Ld_{reg}(\%) = \frac{Vo_{Full-load} - Vo_{Half-load}}{Vo_{rated-load}} \times 100 \quad (6)$$

The *overall efficiency* will help to determine how much heat will be generated within the instrument [52], and whether any heat-sinking will be needed as a part of mechanical design. The *overall efficiency* is described by equation 7 below.

$$Eff(\%) = \frac{P_{out}}{P_{in}} \times 100 \quad (7)$$

Additionally, is important to take into account the power dissipated by those components which allocation is critical within instrument subsystems. The later makes reference to the power dissipated of internal devices of DDCU [52]. The power dissipation is expressed by equation 8 bellow.

$$P_D(W) = \left(\frac{1}{\eta} - 1\right) P_{out} \quad (8)$$

Other very important topics are the protections against different eventualities which could represent a catastrophic event for ELS system of balloon. Therefore, due to the criticality level of mission and the impossibility of access for repairing actions, LVPS modules should provide circuit protections interface for avoiding propagation of failures. The most relevant are devoted to protect against input/output over-current due to short circuit and over loading, under-voltage lockout on input, output over-voltage trip limits, and thermal shutdown in over-temperature failure. Furthermore, during mission development it has to be considered meet some regulatory standards based on special functionalities of power supply.

These safety standards are mainly devoted to prevent abnormalities in fields related to EMC, vibration and Electrical/Electronic products. The range limits are very well predefined within these standards. Therefore, due to the lack of information, about these topics, and having in mind that LVPS modules are the major EMI generators in the instrument, some standards were proposed in order to not exceed certain levels about emissions, ESD, radiated and conducted immunity, as well as vibration and thermal shock. The latter represent special EMC requirements which must be provided by power electronic technology selected.

Then, once stated a good basis about requirements and specifications, the LVPS modules will be described through a block diagram based on functional and interface requirements. After such description, schematic is presented in following sections to be discussed technically.

IV.7 Low voltage power supply module description

As was stated in the section of power distribution architecture, four LVPS modules to be hosted inside DP rack, were proposed: LVPS1-DP, LVPS2-DP, LVPS-PDM and LVPS-HK. As an example, figure 54 shows a block diagram of LVPS module intended to be developed.

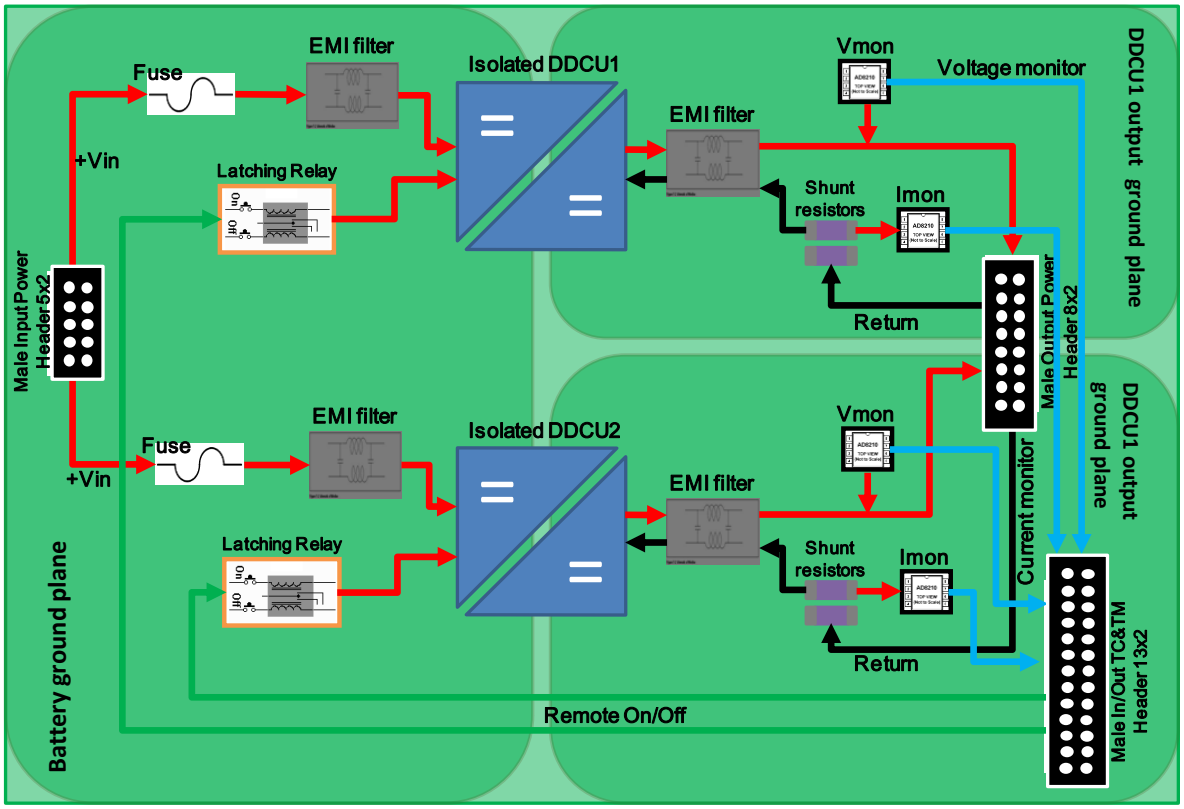


Figure54. Functional block diagram of LVPS board.

Regarding functional requirements stated at the beginning of this chapter, each LVPS module provide the isolation and transformation stage by the use of isolated DDCUs, represented by blue opposite triangles in figure 54. These isolated converters were selected in order to withstand input voltage variations due to battery discharge on PWP, as well as not allow failure propagation in case of event occurrence. Furthermore, the use of step-down converters were suggested to PDM and CCB subsystems for performing on-board tight regulation stage, as well as part numbers of different niPOL converters suppliers. On the other hand, in order to provide instrument flexibility and reliability, a remote On/Off section was implemented by the use of dual-pole-dual-throw latching relay (DPDT-LR), showed as orange squares frames in the figure 54. In such way, the internal coils of LR are controlled by signals commanded either from the ground SIREN, or on-board from HK (green arrows).

Regarding EMC issues, LC and pi-filters at input/output DDCU's were implemented (denoted as EMI filters in figure 54) in order to offer protection to EMI conducted by PCB traces, cables or conductors wires of other equipments. In the same way, LVPS modules were housed into the metallic boxes for reducing radiated emissions. On the other hand, V&I monitor circuits based on dedicated operational amplifiers (op-amp) integrated circuits were implemented. The later, in order to produce telemetry information related to voltage and current (by using shunt resistors) consumption levels by each subsystem, labeled as V_{mon} and I_{mon} in the figure 54 above.

Taking into account criticality of the mission, fuses at each input converter were located for inrush energy and maximum dc input current protection. It is important to mention that several balloon flights are planned using the same hardware. The later implies to preserve, as much as possible, the hardware integrity of each subsystem. Furthermore, in order to keep isolation at board level between main power bus and payload secondary side, three different ground planes were planed during PCB design. The later issue also helps for avoiding ground loops and less contamination between subsystems.

Finally, at least three male header terminal connections were implemented in order to manage main power bus, as well as all information received and sent to HK. In the next section, LVPS modules design considerations are presented based on schematics.

IV.8 Low voltage power supply design considerations

As stated at the beginning of this chapter, the power supply subsystem assumes a very important role within any system; it gives power in a consistent and reliable way to circuits system. Furthermore, protects the system against electrical abnormalities like a transients and short circuits events.

The latter led us to put in practice special design considerations, according to application field, as a part of LVPS development process. Consequently, in the next paragraphs four different subsections are developed in order to describe technically design considerations applied in the LVPS modules development: DDCU selection, EMC, PCB design and Thermal management. In order to have a better understanding during the explanation, LVPS1-DP and LVPS2-DP schematics are used along the next four subsections. The first subsection is related to DDCU's selection process which represents a challenge regarding the environment operational conditions at 40km altitude flight. The second subsection focuses in EMC constraints imposed by application field; meanwhile third subsection presents the PCB design considerations applied to board development. Finally, fourth subsection is devoted to thermal management analysis performed to LVPS2-DP module.

IV.8.1 DC-DC converters selection

This section describes the design trade-offs presented on DDCUs selection process to be used in space applications. The DDCUs intended to be used in space have to deal with radiation effects, vacuum environment, shock, vibrations and comply with EMI requirements. To cope with these string requirements several considerations have to be taken. Selection of the proper converter topology, for a particular application, suitable to support radiation effects is of major importance [54]. Therefore, component selection to withstand radiation, mechanical dimensions and thermal analysis on vacuum conditions are key parameters to achieve a high reliability levels.

In space environment, the requirement to obtain very high reliability levels, led to the use of heritage designs, i.e., the use of components that have already been used on-board of spacecraft [54]. The disadvantage lies in that these components are typical several years old, resulting in larger, heavier and less competitive power supplies than current practice. Furthermore, space qualified parts are usually much more expensive than the COTS counterpart, and the parts are usually considered military grade. The later imposes another problem, the need to get and approval to import the parts, which make the design more expensive and the design cycle longer [54]. Another possibility is the qualifications of new parts, this approach results very expensive due to the specific nature of the tests.

In the particular case of balloon flights, at 40km of height, the environment is also called under the term "near-space". The later means that the space constraints are not as critical as in the LEO orbit. Thus at 3mbar conditions, the losses are performed mainly by radiation, through good thermal coefficient materials, and by the "air". The latter, although not enough existing for natural convection performing, but still helping for conducting heat in a very reduced way. Furthermore and not less important, this reduced amount of "air" could serve as interface for arcing event occurrence.

Therefore, the first step of the design is choosing the appropriate power supply topology. Converters which have a direct short circuit path from a low impedance source to ground through switches (MOS or Bipolar transistors) will always be sensitive to single event upset due to possible latch-up [54]. These converters include the half-bridge, full-bridge, voltage-fed push-pull and active clamp forward. All single-ended converters such as the Forward or the Flyback are acceptable [54]. Therefore, considering low-voltage power distribution strategy proposed, step-down voltage converters topologies were selected. In isolation and transformation stage either Flyback or Forward topology converter will be suited; meanwhile, buck converters will be preferred for tight regulation on-board.

Considering two important facts: the tight agenda of EUSO-Balloon and the required time to design a SMPS. It was decided to acquire isolated board mounted DDCUs from different suppliers on market. The later leads other benefits related to saving board space, less EMI contamination, and better heat path dissipation. On the other hand drawbacks about cost, non-standard pin-out parts, and uncertainty about modules performance at determined altitudes were carefully handled minimized by most convenient manufacturer selection. Then, the following topics were considered to proper selection of isolated DDCUs.

- Power range
- Component availability
- Cost
- Procurement time scales
- Efficiency
- Input voltage range
- Output voltage level (fixed, or adjustable)
- Remote On/Off feature
- EMC regulatory standards
- Environmental features
- Component replacement
- Mass and dimensions

It is important to state that isolated board mounted DDCUs are based on different power topologies. The term *topology* refers to the arrangement of the power components within the package of DDCU. This arrangement has a large bearing on which environment the supply can operate in safely, and how much power the supply can provide to the loads. Each topology has its relative merit. One topology may have a low parts cost, but can only provide a limited amount of power; another has ample power capability, but costs more, and so on. Table 5 shows a comparison of different SMPS topologies implemented within isolated DDCU. The table 5 dictates where various topologies are used according to power region application.

Topology	Power Range (W)	Vin(dc) Range (V)	I/O Isolation	Typical Efficiency (%)	Relative Parts Cost
Buck	0-1000	5-40	No	78	1
Boost	0-150	5-40	No	80	1
Buck-Boost	0-150	5-40	No	80	1
1T Forward	0-150	5-500	Yes	78	1.4
Flyback	0-150	5-500	Yes	80	1.2
Push-Pull	100-1000	50-1000	Yes	75	2
Half Bridge	100-500	50-1000	Yes	75	2.2
Full Bridge	400-2000+	50-1000	Yes	73	2.5

Table5. The SMPS topologies according to the power range [52].

Regarding the cost of military power modules as well as large scale times to import parts. This work proposes the use of industrial power modules, in order to lower costs, which comply with EMC basic, generic and product standards. The last means that the purpose of EMC systematized standards is to protect electrical/electronic devices from being subject to various interferences (including lightning and static electricity) or damage, by minimizing hazards found in their operating environments [55]. In that way, the DDCUs selected comply with at least two of the following EMC major international standards shown in table 6.

EMC standard	Part	Performance criteria	Testing and measurement techniques about
International Electro-technical Commission (IEC)	IEC EN 61000-4-2	Class A	Electrostatic discharge (ESD) immunity
	IEC EN 61000-4-3		Radiated, radio-frequency, electromagnetic field immunity
	IEC EN 61000-4-4		Electrical fast transient (EFT)/burst immunity
	IEC EN 61000-4-5		Surge immunity
	IEC EN 61000-4-6		Immunity to conducted disturbances induced by radio-frequency fields
	IEC EN 61000-4-8		Power frequency magnetic field immunity
Comité International Spécial des Perturbations Radioélectriques (CISPR)	CISPR 11	Rev. 4.1	Emissions test methods and limits on industrial, scientific, and medical radio-frequency equipment. Electromagnetic disturban-ce characteristics
	CISPR 22	Rev. 6.0	Emissions test methods & limits of radio disturbance characteristics on informa-tion technology (IT) equip.
Euro Norm or European standard (EN)	EN55022	Class A & B	Unwanted conducted emis-sions of radio disturbance characteristics on IT equip.

Table6. EMC international standard.

On the performance criteria column are shown two classes. In immunity testing there are four classes by which equipment passes or fails tests process. The equipment always will fail if: in class “A” loss of function or performance due to the testing occurs, in class “B” temporary loss of function or performance occurs (self recoverable), in class “C” loss of function or performance which needs intervention to restore occurs, and class “D” permanent loss of function or performance due to damage occurs. The previous scenarios always represent a failure [56].

Therefore, in order to achieve electronic parts with lower costs and procurement time scales, isolated board mounted DDCUs from three different manufacturers were considered: TDK Lambda, Tracopower (TPW) and XP-Power (XPP). The table 7 shows a specification summary of the selected DDCU’s according to each subsystem.

Parameters	LVPS1-DP		LVPS-PDM		LVPS2-DP		LVPS-HK	
DDCU Manufacturer (Qty)	TDK (1)	TPW (2)	TPW (2)		TPW (1)	XPP (1)	XPP (2)	
Subsystem target	CBB	CLKB & GPSR	EC-UNIT & PDMB		CPU	DST	MCU & LVDS	
Input Voltage Range (V)	18 to 36				9 to 36			
Output Power (W) with safety factor	6	5 & 2	15 (each one)		15	30	8	2
Secondary Bus Voltage (V)	5	5 & 5	5.5	5.5	12	5	±12	3.3
Line&Load Regulation (%)	0.2~1		0.2~0.3		0.2~0.5		0.2~0.5	
Efficiency @ full load (%)	80~82		84		87~91		80~86	
Operating temperature range (ºC)	-40 to 85						-40 to 100	
EMC standards	Safety stds: UL60950-1 IEC60950-1 EN60950-1 CISPR 11, 22 Conducted noise: EN55022 Class A and B, FCC part 15				Safety stds: UL60950-1 IEC60950-1 EN60950-1 Conducted noise: EN55022 Class A and B, FCC part 15 ESD, Radiated and Conducted Immunity: EN61000-4-2, 4-3, 4-6 respectively.			
Mechanical & thermal shock and Vibration test	According to MIL-STD-810F test conditions						---	
Protections	Under Voltage Lock Output Under Voltage Shutdown Input Short circuit Over Temp Shutdown Output Over current Short circuit (hiccup and foldback) Output Over Voltage							
Package	Through Hole (TH)	TH & SMD	TH (both)		TH (both)		TH (both)	
Weight	5.8	18.5	21 (each one)		15	30	24.5	

Table7. Main specifications of DDCUs selected.

As can be seen in table 7 above, each DDCU has an input voltage range able to withstand output battery variations which goes from 28V to 18V. Furthermore, 25% to 50% safety factor to power consumption was added to DDCUs for preventing eventualities in such parameter.

On the other hand, the secondary bus voltages row (output voltages of power modules) were selected in order to match with those voltages at which LVPS subsystem must operate, and at the same time, the nominal voltages expected by payloads. The last information is stated and highlighted in yellow at table 4. Additionally, the selected DDCUs fulfill, by far, with -20ºC to 50ºC operating temperature range environmental requirement.

Regarding vibration test levels, the DDCUs comply with mechanical and thermal shock, as well as vibration test conditions stated in MIL-STD-810F. The methods for such tests are: method 516.5 for mechanical shock test, method 514.5 for Vibrations tests, and method 503.4 for thermal shock test. In method 516.5 the equipment under test (EUT) is tested during power-on state by applying terminal-peak saw tooth pulse shape with pulse duration of 11ms. The impact acceleration is 40Gs distributed in 18 shocks (3 shocks for each face). On the other hand in method 514.5, random vibration waveform is applied on EUT in power-on state during 1hr for each axis (X, Y & Z). Finally in method 503.4, 20 cycles within temperature range from -55ºC to 105ºC with duration exposure of 1hr in each temperature extreme are applied to EUT in power off state [57].

In the terms of efficiency, the selected DDCUs meet the functional requirement which states that efficiency (at full load) of SMPS shall be major or equal to 80%. It is important to note that datasheet specification about DDCU efficiency, as well as line and load regulation parameters are measured directly at converter pin terminals with a resistive load. Now, in the next section will be described all EMI design constraints during LVPS modules development.

IV.8.2 Electromagnetic compatibility

The EMC topic is always considered as very particular issue within a project development. In that way, EMC is defined as the ability of electrical or electronic equipment to function in the intended operating electromagnetic environment without causing or experiencing performance degradation due to unintentional EMI. On other hand, EMI is electromagnetic energy that adversely affects the performance of electrical/electronic equipment by creating undesirable responses or complete operational failure [58]. Thus, regarding that SMPS are major contributors of high voltage and current switching waveforms that generate EMI, the influence of electrical noise in a system must be minimized. Therefore, in order to provide the proper ability to LVPS subsystem for performing its function without causing or experience performance degradation to or from other subsystems, the selected DDCUs comply, as in table 7 can be observed, with international EMC standards. Those standards usually recommend the implementation of LC or pi-filter at input converter for EN55022 class “A” & “B” compliance. The figure 55 shows the schematic of LC-filter recommended at input of DST converter.

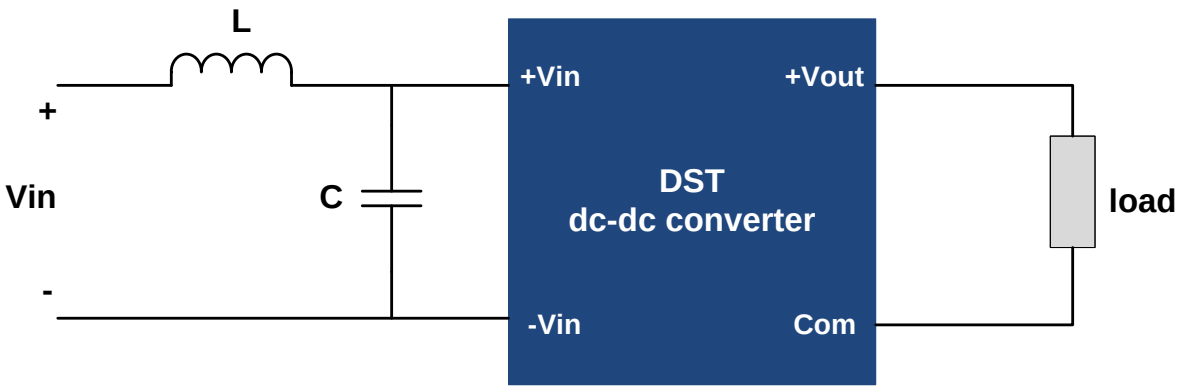


Figure55. Recommended filter for EN55022 class “A” conducted and radiated emissions compliance on DST converter input.

Although such filter represents the manufacturer recommendation on most selected converters, a complementary analysis during this research was performed in order to confirm stability of the DDCU performance. Until now, many articles address the topic of system instability in [XXXII, XXXIII and XXXIV]. Most of the articles states that to guarantee system stability the magnitude of source impedance, Z_S, should be small compared to the magnitude of the DDCU input impedance, Z_I. Although the $|Z_S|<<|Z_I|$ requirement is a relative well known “rule of thumb” in the industry, It is not always easy to implement. The latter is due to mainly two reasons; the first one is due to very few DDCU manufacturers provide $|Z_I|$ in their data sheets, and the second one is because is not clear how much smaller $|Z_S|$ must be compared to $|Z_I|$.

The DDCU input impedance is affected by a positive incremental change in the input voltage (V_{IN}), which results in a negative incremental change in the input current (I_{IN}), causing the converter to look like a negative resistor (R_N) at its input terminals [59], as is expressed in equation 9.

$$R_N = -\left(\frac{V_{IN}}{I_{IN}}\right) \tag{9}$$

The latter also is affected by the inclusion at the converter’s input of different sort of filters including a relatively large electrolytic capacitors. The equivalent series resistance (ESR) of this capacitor provides the positive resistance (R_P) needed to compensate for the destabilizing effects due converter’s negative resistance. Also, is important to note that at full load and at the lowest input voltage (WC condition) the magnitude of R_N is the smallest. Then, for the particular case of DST converter with 5Vout, 6A at 91% efficiency will drawn an input current of 1.8A when its input voltage is 18V. Under this condition R_N=9.8Ω. And at the nominal input voltage of 28V, the full load input current is 1.2A and R_N=23Ω.

Actually, reviewing $|Z_I|$ vs frequency specification data from other converters, usually converter's input impedance appears as negative resistance only at low frequencies. At higher frequencies the impedance is influenced by the converter's own internal filter elements and of its feedback loop [60]. Therefore, this behavior can be modeled as a capacitor "C" in parallel with R_N. Now then, following the last assumption, the circuit shown in the figure 55 can be approached as is shown in figure 56.

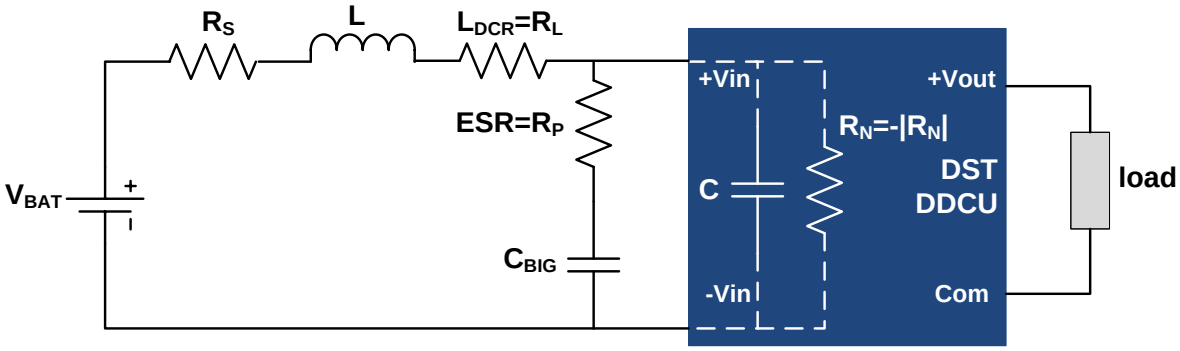


Figure56. The model approach to system stability.

The figure above show the most common input filter design used in power field. The manufacturer recommends this filter, where C_{BIG} and the resistor R_P represents the ESR of the electrolytic capacitor. The advantage here is that the capacitor does not dissipate dc power. The important here is to determine how large R_P must be to ensure a stable system. Therefore, is necessary to find the characteristic equation of the complete network shown in figure 56. In that way, to obtain the characteristic equation is necessary to develop the next calculations about series and parallel elements. The equation 10 shows parallel simplification of internal C and R_N elements resulting in Z_I. Meanwhile, series simplification of C_{BIG} elements is shown in equation 11 resulting in Z_{BIG}. After that, parallel simplification of latter gives Z_{EQ} in equation 12. Regarding output internal impedance of DC source, equation13 shows series simplification of output source resistance (R_S), inductance (L) and its DC resistance (R_L) resulting in Z_{SL}.

$$Z_I = Z_C \| R_N = \frac{R_N}{1+sCR_N} \tag{10}$$

$$Z_{BIG} = Z_C + R_P = \frac{1+sC_{BIG}R_P}{sC_{BIG}} \tag{11}$$

$$Z_{EQ} = Z_{BIG} \| Z_I = \frac{R_N(1+sC_{BIG}R_P)}{s^2CC_{BIG}R_PR_N + s[C_{BIG}(R_P+R_N)+CR_N] + 1} \tag{12}$$

$$Z_{SL} = Z_S + Z_L + R_{DCR} = sL + (R_S + R_{DCR}) = sL + R_{SC} \tag{13}$$

Therefore, the equation14 shows the transfer function using equations above.

$$\frac{V_{OUT}}{V_{BAT}} = \frac{Z_{EQ}}{Z_{EQ}+Z_{SL}} \tag{14}$$

After several reductions, the characteristic equation of the complete network shown in the figure 56 gives, in this case, a third-order equation which is expressed at equation 15.

$$s^3 LCC_{BIG}R_P + s^2\left(\frac{LC_{BIG}R_P}{-R_N} + LC_{BIG} + LC + CC_{BIG}R_P R_{SC}\right) + s\left(\frac{L}{-R_N} + \frac{C_{BIG}R_P R_{SC}}{-R_N} + C_{BIG}R_{SC} + CR_{SC} + C_{BIG}R_P\right) + \left(\frac{R_{SC}}{-R_N} + 1\right) \tag{15}$$

However, considering that values of R_S and R_{DCR} are significantly lower to be omitted. Consequently, the equation 15 is simplified in the equation 16.

$$s^3 LCC_{BIG}R_P + s^2 L\left[C_{BIG}\left(1 - \frac{R_P}{R_N}\right) + C\right] + s\left(C_{BIG}R_P - \frac{L}{R_N}\right) + 1 \tag{16}$$

Then, it is necessary that the coefficients of this third-order equation have the same sign to be stable. The later statement yields the following constraints which are shown in equations 17 and 18.

$$R_P < |R_N|\left(1 + \frac{C}{C_{BIG}}\right) \tag{17}$$

$$R_P > \frac{L}{(C_{BIG}|R_N|)} \tag{18}$$

Furthermore, these constraints become sufficient for stability if C_{BIG}>>C. A factor of five between these two capacitance values is usually enough for meet the constraints [60]. Consequently, and substituting the following values in constrains above: C_{BIG}=100μF, C=20μF, L=12μH, and with a minimum value of R_N=10Ω. The results in constraints give for R_P the following range that will give a stable system in 0.012Ω<R_P<12Ω.

Taking into account the range in which R_P must be to ensure stable system, the electrolytic capacitor recommended by manufacturer, C_{BIG}, has to be selected with the proper ESR to fit in such range. In that way, an electrolytic capacitor with an ESR=0.3Ω was selected. With this value of R_P, the poles of characteristic equation occur at: s_1=-176820 and $s_{2,3}$=-9089.8±26511.4i. As can be seen, the poles lie in the left-hand plane.

On the other hand, since LVPS modules contains DDCU which provide high voltage and current switching waveforms that generate EMI, in both conducted and radiated emissions, enclosure and grounding during low-voltage development subsystem become a very important issue [61]. Usually, shields it is used to contain electromagnetic fields, if the shield is surrounded by the noise source. The last configuration provides protection for all susceptible equipment located outside the shield. However, a shield may also be used to keep electromagnetic radiation out of a region. This technique provides protection only for the specific equipment contained within the shield. From an overall systems point of view, shielding the noise source is more efficient than shielding the receptor [62].

Therefore, in order to minimize radiated emissions the LVPS modules were housed (shielded) by an aluminum 19” plug-in units which serve accommodation of up to two PCBs. The mechanical dimensions comply with the IEC-60297-3-102/IEEE 1101.1/11 standard. The figure 57 shows the LVPS modules box type plug-in unit enclosure and also the different plug-in unit parts. This plug-in unit matches with 3U Euro-card standard requirements.

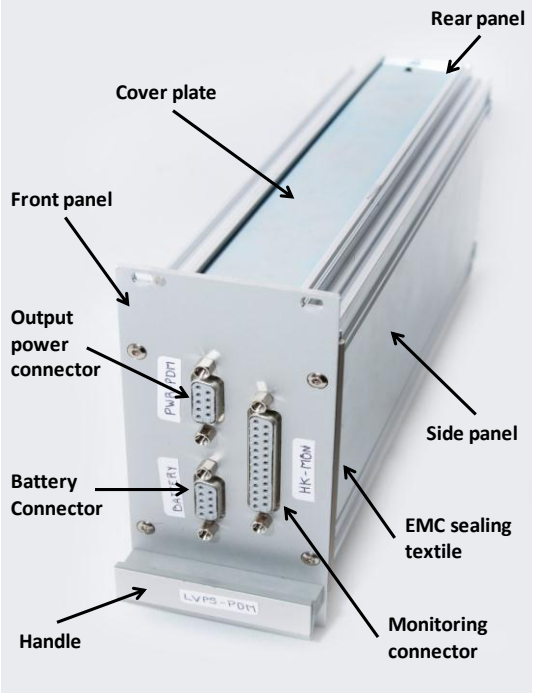


Figure57. LVPS module inside of 3U plug-in unit.

Additionally, aluminum plug-in unit includes a conductive foam EMI gasket consisting of a polyester textile yarn uniformly platted that provides high shielding performance (60-100dB), high level of flame resistance (UL94-V0), mounted using pressure sensitive adhesive (PSA) and is able to operate at higher frequencies due to no gaps on their construction.

Additionally, these plug-in cabinets are fitted into metal chassis DP rack that serves as a shield structure for all the subsystems housed inside it. The figure 58 shows the DP rack with most of the sub-systems installed and interconnected.

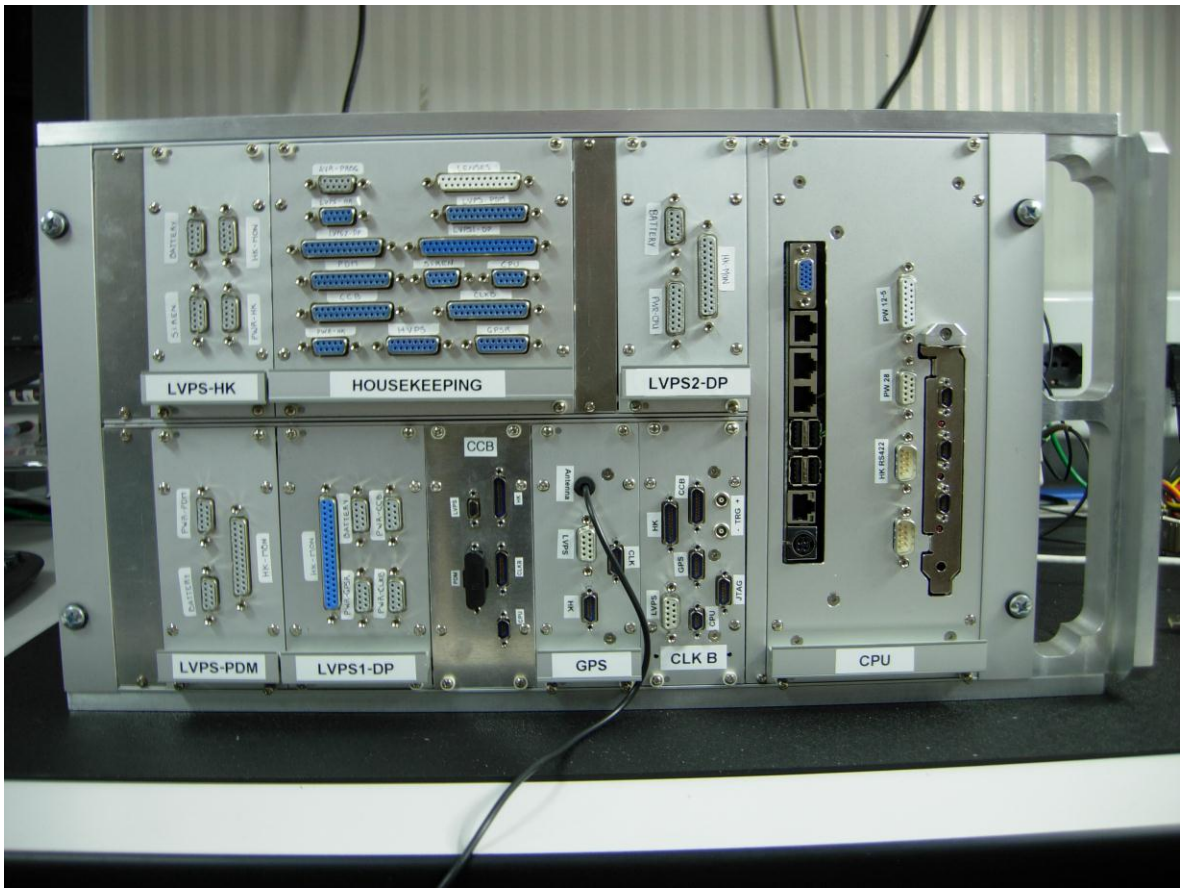


Figure58. DP rack shielded box with almost all subsystems fitted [46].

In the next section are described all issues involved in the PCB design of the LVPS modules.

IV.8.3 Layout and grounding

As previously stated four LVPS modules, instead of the two envisaged in the preliminary version were proposed according to hierarchical importance, and criticality on performance instrument, providing isolation and transformation between PPBUS and payload. Additionally, all the LVPS power modules were housed in individual aluminum 19” plug-in units and located inside DP rack box in order to minimize, as much as possible, radiated and conducted EMI to entire subsystems. However, it’s a well-known fact that a high energy spectrum is created as a result of switching current within a PCB.

These currents are created by a product of digital components, as well as, switching behavior of analog components. The latter means that each logic transition state produces a transient surge within the power distribution system [63]. The stated above implies a carefully PCB design considering many aspects of circuit and system design. The first is to define the base material intended to use, the number of layers and the layout accommodation.

Consequently, it was decided to use a NEMA base material FR-4 grade of 1oz (35µm) of conductor material. For this project were consider two classification schemes: NEMA grades (National Electrical Manufacturers Association) and IPC (Institute for Printed Circuits) of Association Connecting Electronics Industries standards. TheFR-4 material is by far the most commonly used material for printed circuits. The outstanding electrical, mechanical, and thermal properties of FR-4 have made it an excellent material for a wide range of applications including computers and peripherals, servers, telecommunications, aerospace, industrial controls, and automotive applications. Besides, FR-4 provides a flame retardant feature.

On the other hand, number of layers becomes in critical issue during PCB development. A Single, double or multi-layer PCB design is justified by the nature and number of signals. The nature of signals in a circuit could be classified in those signals that come from power components, small signals which can be digital or analog, critical signals which magnitude and integrity are very important to performance system, ground returns (planes) and DC voltage signals. However, there are two parameter, regarding manufacture process, which are cost and volume production. For LVPS PCB designs, as first instance, was proposed a four-layer PCB in which signal distribution is shown in table 8.

Number of Layers	Nature of Signal
Layer 1 (Top layer)	Power DC voltages
Layer 2	Ground plane
Layer 3	Small signals (V&I monitoring)
Layer 4 (Bottom layer)	Control signals (On/Off status)

Table8. Four-layer PCB proposed.

The second proposal was based on two-layer PCB. The signal distribution is shown in table 9. The reduction in the number of layers of PCB was possible thanks to the low amount of monitoring and control signal in the circuit.

Number of Layers	Nature of Signal
Layer 1 (Top layer)	Power DC voltages, monitoring, and control signals surrounded by a ground plane.
Layer 2 (Bottom layer)	Ground plane

Table9. Two-layer PCB proposed.

Additionally, the table 10 shows the number of monitoring, control and power signals involved in each LVPS module.

LVPS module	Type of Signal	Signal	Quantity	Magnitude
LVPS1-DP	Control	HL_CMD	6 x 2	12V
		CC	3 x 2	Open or shorted
	Monitoring	Voltage	3 x 2	0V to 5V
		Current	3 x 2	
	DC Voltage	PWR	4 x 2	$28V_{BAT}$, $5V_{CCB}$, $5V_{CLKB}$ & $5V_{GPSR}$
LVPS2-DP	Control	HL_CMD	4 x 2	12V
		CC	2 x 2	Open or shorted
	Monitoring	Voltage	2 x 2	0V to 5V
		Current	2 x 2	
	DC Voltage	PWR	2 x 2	$28V_{BAT}$, $12V_{CPU}$ & $5V_{DST}$
LVPS-PDM	Control	HL_CMD	4 x 2	12V
		CC	2 x 2	Open or shorted
	Monitoring	Voltage	2 x 2	0V to 5V
		Current	2 x 2	
	DC Voltage	PWR	2 x 2	$28V_{BAT}$, $5V_{EC}$ & $5V_{FPGA}$
LVPS-HK	Control	HL_CMD	2 x 2	12V
		CC	0	-----
	Monitoring	Voltage	2 x 2	0V to 5V
		Current	2 x 2	
	DC Voltage	PWR	2 x 2	$28V_{BAT}$, $\pm 12V_{MCU}$ & $3.3V_{LVDS}$

Table10. Control, monitoring and DC voltage signals considering returns at each LVPS module.

Therefore, considering an available PCB area of 100mmX220mm coming from the definition of 3U euro-card and the number of signals involved at each module (overall circuit complexity), as well as the cost and procurement time of flight model PCB production, it was decided to implement two-layer PCB resulting in a less expensive option and faster in its production and low procurement timescale.

The figure 59 shows, as example, the top-layer of LVPS1-DP PCB without components. The figure 59 also shows ground planes distribution of different subsection on PCB. There are four ground planes on figure 59; each one is related to specific subsystem in the instrument. As can be seen in the figure 59, the upper plane corresponds to battery subsystem and is the primary side of low-voltage power distribution. Meanwhile the lower three ground planes correspond to subsystem clients of LVPS1-DP: CCB, CLKB and GPSR; and comprise the secondary side of low-voltage power distribution.

The ground architecture used at the EUSO-Balloon instrument is based on a single point grounding topology. The star connection ties all subsystem together in a ground reference point (GRP) throughout the LVPS modules up to the negative

borne of the battery, which is called mechanical ground (GND_M). However, a drawback of this topology is that requires a considerable number of conductors, which is generally not practical in large distributed subsystems owing several nodes and voltage drop [64]. But in other hand, this architecture accomplishes the functions of signal return, while helping to control common-impedance interference coupled between subsystems. As was stated above, the separation of ground planes subsystems was in order to avoid closed-loop paths for noise current contamination between subsystems. These ground planes have 1mm clearance between them which is 50% more than specified in IPC2221 [65].

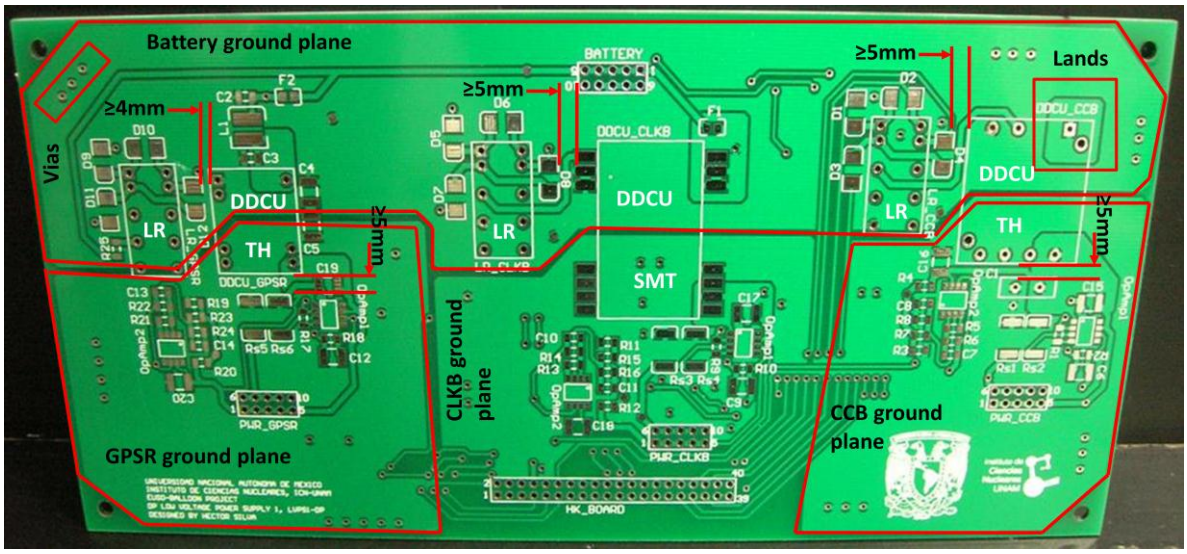


Figure59. PCB design consideration on LVPS1-DP.

The figure 60 shows the EUSO-Balloon grounding architecture implemented at entire instrument. The four LVPS modules serve as path returns to GRP at battery pack. These ground planes are denoted with small squares of different colors per each winding output transformer. On other hand, DDCU's were selected (most of them) with a metal enclosed in order to decrease radiated interference, as well as, be less susceptible to EMI. Cables were implemented as a twisted pair and connectors provided with back-shielding in order to minimize EMI radiation.

Additionally, slit apertures were avoided on ground planes in order to provide lower impedance. Also, in figure 59 is shown floating lands conductor areas which were avoided in order to reduce stray capacitances; instead floating, the areas were connected either to ground plane or used as thermal dissipation by the use of vias. Furthermore, it was procured that bottom layer was devoted (as much as possible) to different ground planes, and the most of signals were routed on the top-layer. The last concept brings the advantage of increasing mechanical strength of the board, it lower the impedance connections which reduced undesirable conducted noise, and it acts as shield to radiated noise coming from underneath the board [66].

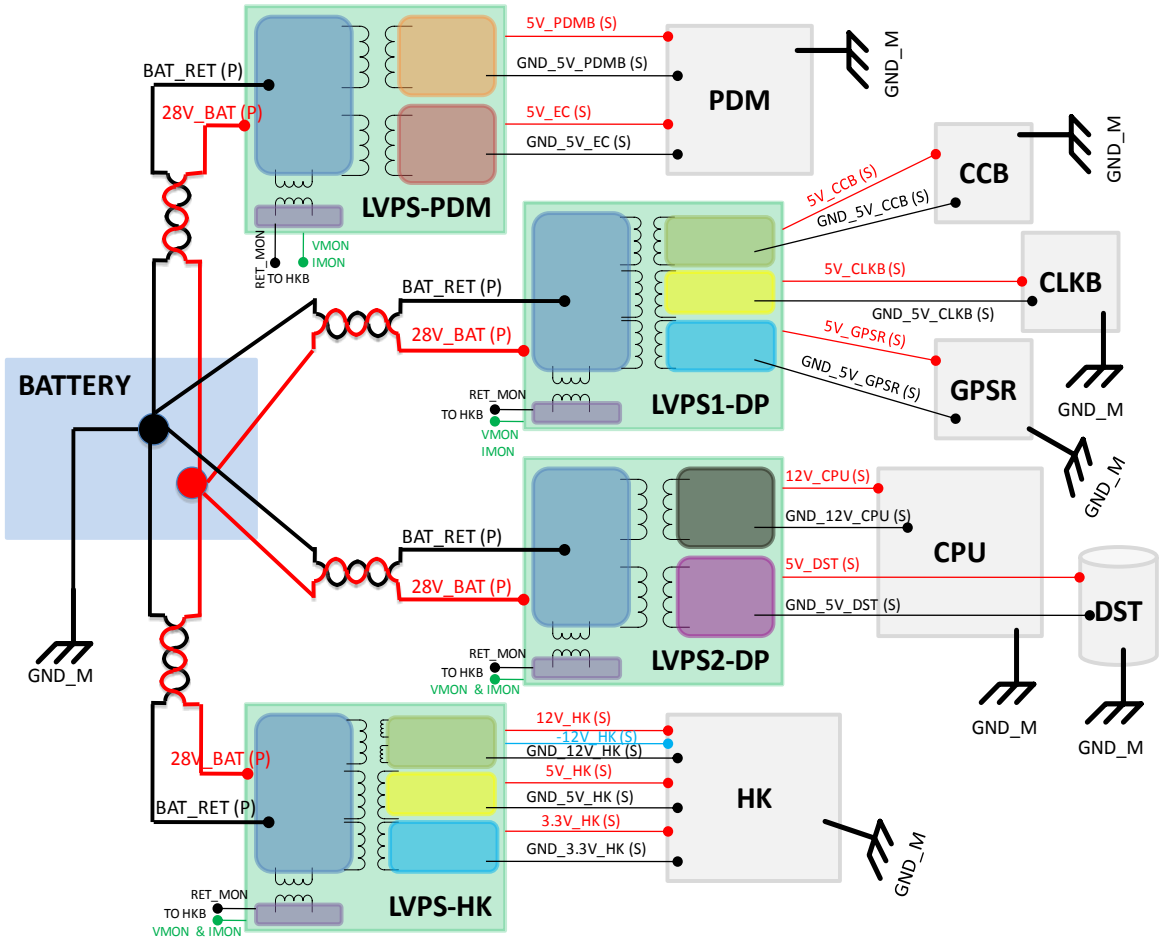


Figure60. EUSO-Balloon grounding architecture.

Another important aspect considered during design is the accommodation of different component technology, TH and SMD. As can be seen in figure 59, DDCUs and LRs are the most bulky components. Regarding DDCUs, signal traces and components were not routed and located underneath the modules to avoid noise coupling. Instead of that, ground plane was placed under the modules. Furthermore, for repairing and removal DDCU modules a 4mm clearance was practiced around the module outline. This clearance provides spacing and isolates adjacent components from exposure to heat during performance or removal process [66]. On the other hand, in single in-line package (SIP) modules as is the case of one DDCU OF LVPS-HK, similar guidelines were followed having the input ground plane extended below the module, and in the output side the output ground plane. In both sides were placed input and output capacitors (C_{out}) as close as possible to input and output pins in order to minimize trace impedance. These pins are connected to land planes as is stated in [66]. The figure 61a) shows this guideline implemented.

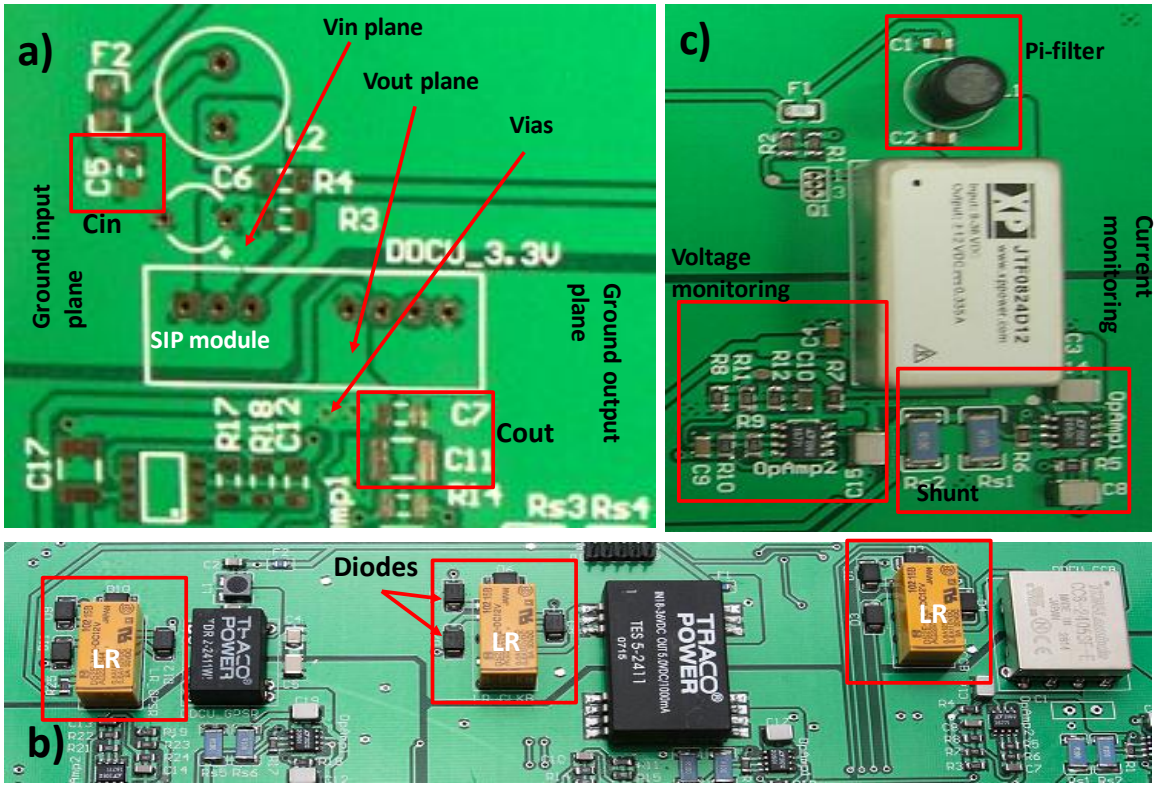


Figure61. PCB design guidelines regarding: a) Input/Output DC power and ground plane, b) Latching relay and diodes, and c) Input filter and V&I circuits monitor.

The figure 61b shows On/Off components. These components are represented by DPDT-LRs which receive commands provided by HK and SIREN subsystems. The commands are generated by CPU subsystem, and interpreted and executed by HK; which sends two HL_CMD's to LR's located next to DDCUs on the LVPS module. The HL_CMD is represented by a 9V to 15V amplitude of 10ms pulse width. These commands are used in order to bias the internal coils of the LR's, and diodes were included in design for feedback current protection.

On other hand, as was stated in section IV.8.2 the manufacturer recommends the implementation of LC and pi-filters at input of several DDCUs. The figure 61c shows the pi-filter implemented at input of the DDCU of LVPS-HK. This filter stage helps to reduce the input filter current flowing in the path from and back to the battery or DC supply. It is important to note that all information about each part as type of package, size of components and pin function were entered into a set of libraries in order to perform the PCB design.

Finally, figure 61c also shows voltage and current monitoring circuits. The current monitoring circuit is based on a differential amplifier. The output of this circuit is referenced to the lower Kelvin contact by using shunt resistors which are grounded due to single supply application.

The current monitoring circuit was designed based on the statement of that the maximum current consumption subsystem should be approximately 4A. Therefore, the selected resistors settled a relationship of 1:1 between the Op-Amp output voltage level and differential voltage sensed at shunt resistors. Therefore, the current levels obtained as telemetry information are presented in next chapter. Meanwhile, the figure 62 shows schematic circuit as well as its simulation.

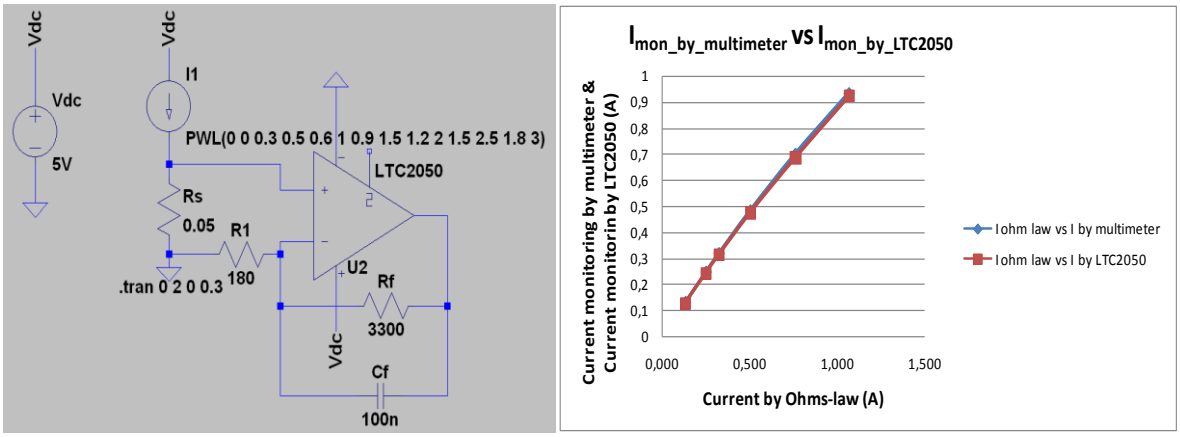


Figure62. Current monitoring circuit at the left, and simulation circuit at the right.

On the other hand, the voltage monitoring circuit is based on a non-inverter amplifier, with a constant gain factor of 0.326. In that way, a 3.3V level correspond to 1.07V, 5V level correspond to 1.63V, meanwhile 12V level correspond 3.9V output voltage. The figure 63 shows schematic circuit as well as its simulation.

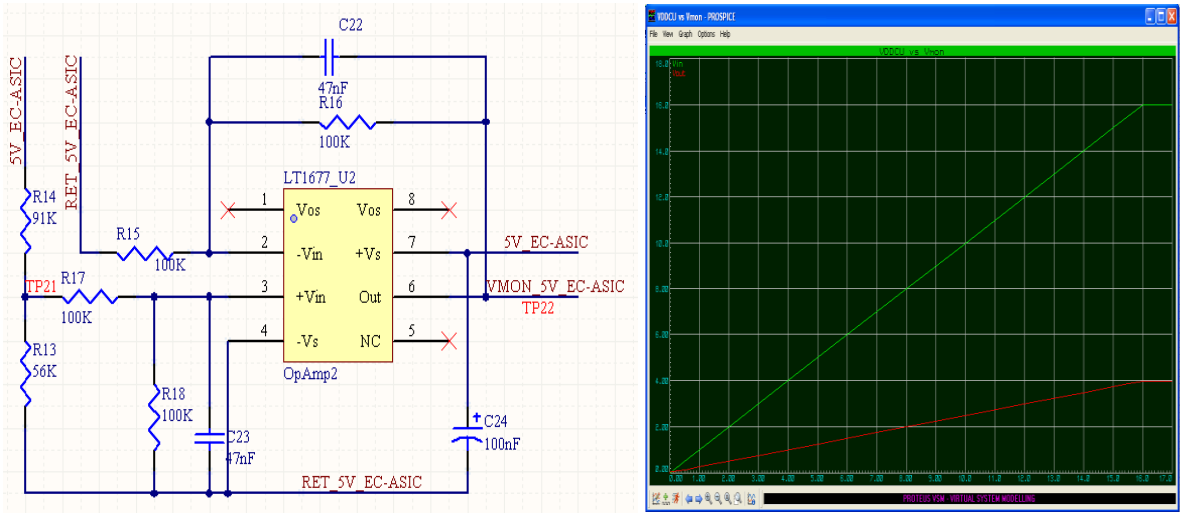


Figure63. Voltage monitoring circuit.

Regarding the current capability of traces on the LVPS PCB modules, the traces width were calculated according to power consumption for each subsystem. The latter implies that width traces are adequate to current and temperature rise expected for each subsystem specification requirements. Actually, there are many plots derived from experiments conducted more than half a century ago which help to determine PCB traces width regarding temperature rise. These plots are part of IPC2221A standard and can be described by the equation 19 [67].

$$I(A) = K * \Delta T^{0.44} * A_C^{0.725} \tag{19}$$

Where, "*I*" correspond to trace current capability in amperes, the ΔT is the temperature rise in ºC, A_C is the conductor cross-sectional area (WxT) in square mils and *K* constant takes the values of 0.048 or 0.024 depending whether outer layers or inner layers, respectively. However, the new standard IPC-2152, which is based on the latest studies is much more involved. It provides more than 100 different figures and lets you take into account many additional factors, such as thickness of PCB and conductors, distance to a copper plane, etc. In this standard the first parameter that you have to obtain is *Ac* by the equation 20 [67]. Once is determined *Ac*, is possible to find the required trace width for a given copper weight (1oz) by equation 21 [67].

$$A_C(sq.mil) = (117.555 \times \Delta T^{-0.913} + 1.15) * I^{(0.84 \times \Delta T^{-0.108} + 1.159)} \tag{20}$$

$$Trace\ width(mil) = \frac{A_C}{t} \tag{21}$$

Summarizing the above stated, the table 11 shows the minimum trace width and voltage drop of main power traces for several current rates demanded by each subsystem. The PCB traces width calculations are based on internal IPC2221 shown in [67], under the next conditions: 40ºC rise temperature, 1oz copper thickness, and 25mm to 50mm length trace. This analysis was applied for, the definition of each and every tracks of the PCBs, taking into account its local environment and operational conditions expected under maximum load.

Subsystem	Max. current carrying trace (A)	Trace width (mm)	Voltage drop (mV)
CCB	1.2	0.46	76.2
CLKB	1	0.36	61
GPSR	0.4	0.10	113.2
PDM-FPGA	3	1.61	54.7
EC-ASIC	3	1.61	54.7
CPU	1.3	0.51	111
DST	4	2.38	74
HK-MCU	0.5	0.14	15.7
HK-LVDS	0.335	0.08	150

Table11. Trace width and characteristic impedances of main power traces.

Finally, in the figure 64 are shown the output power traces width of CPU and DST subsystem.

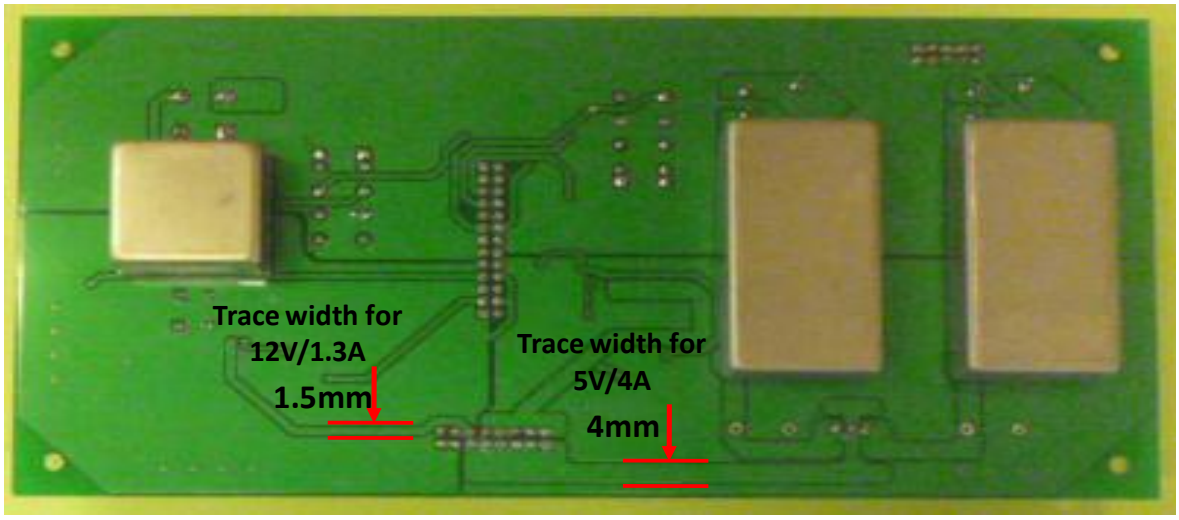


Figure64. Traces width according to CPU and DST current consumptions.

In the next section, this research will focus in describe the solutions proposed during LVPS module development process, in order to provide an efficient thermal performance of LVPS subsystem.

IV.8.4 Thermal management

Another important factor to consider in this kind of projects is the thermal performance of circuits. Due to the lack of natural convection (because of the altitude of balloon) heat dissipation becomes a critical issue, and some specific techniques must be implemented to conduct to the external structure the heat dissipated by DDCU's on different subsystems.

The LVPS modules contain semiconductor devices, capacitors and other components that are vulnerable to thermal stress. In this particular case, power devices inside of the DDCU's modules represent the major heat sources. Therefore, an adequate thermal architecture becomes vital to limit the DDCU temperature to a lower value for extremely high reliability performance. As an example, Figure 65 shows a general description of the thermal parameters involved on a DDCU mounted in two layers PCB. Parameters denoted with θ are described as thermal impedance of some heat power dissipation path. In that way, θ_{JA} represent thermal impedance from the junction, internally of DDCU under test, to the ambient environment and can be expressed as equation 22 shows [68].

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{22}$$

There are two primary heat paths for the DDCU in Figure 62, represented by their associated thermal resistance. The first path travels from the junction of DDCU to the plastic molding at the top of the case, θ_{JC}, and then to the ambient air, θ_{CA}. The second path is from the junction of the DDCU to an exposed pad, θ_{JEP}, when it exists. Therefore, the exposed pad is connected to the PCB, where the heat travels through the surface and finally to the ambient air [68].

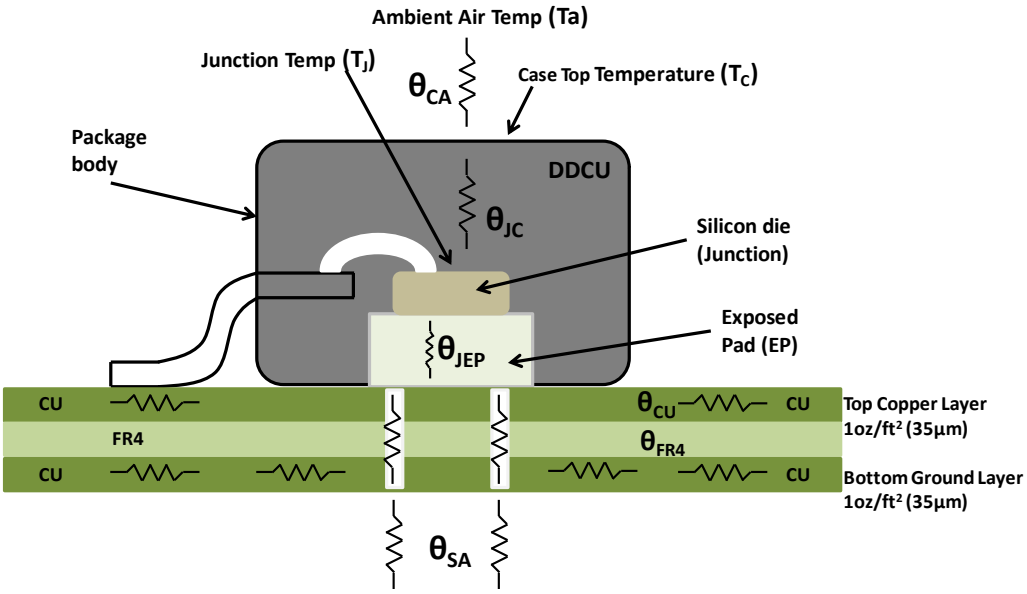


Figure65. Thermal resistance model of a DDCU for a two-layers PCB.

Following the same path, θ_{Cu} represent the thermal resistance of our board's cooper to lateral heat transfer. Meanwhile, θ_{FR4} is the thermal resistance between the cooper planes provided by the vertical resistance of FR4 laminate, and θ_{SA}, represent the thermal resistance from the surface of the PCB to the ambient air [68].

It is important to mention, that in near-space at 3mbar conditions, the losses are performed mainly by radiation, through good thermal coefficient materials, and by the "air". The latter, although not enough existing for natural convection performing, but still helping for conducting heat in a very reduced way. Furthermore and not less important, this reduced amount of "air" could serve as interface for arcing event occurrence.

In our case, the most critical module because of its high power dissipation and transient response conditions is the LVPS2-DP module which contains two DDCU's in parallel arrangement for powering the DST section. For this arrangement the heat transfer path is through the case to ambient.

On the other hand, special attention is paid in order not to exceed 105ºC case temperature for a reliable operation. Taking into account this issue, a preliminary setup was proposed in order to assess whether or not and how long it takes reach this critical temperature on the DDCU's. The set-up comprised by the DDCU's of the LVPS2-DP PCB and a fixed load of a 1Ω rheostat. The latter was selected in order to reach 5A which is next to the maximum current capability of the DDCUs parallel arrangement. A set of thermistors were added to metallic cases of the DDCU's as is showed in the figure 66 in order to get temperature increase. At a first run, in just 20min already ~85ºC were reached. Since this condition it will be even more critical at 3mbar, it is necessary to implement heat dissipation architecture to maintain the temperature bellow critical level. Furthermore, it is important to note that the previous set-up was fixed at ambient temperature; thus, the result represents a lower limit in temperature which makes strictly necessary the implementation of a strategy to heat dissipation.

The proposed architecture is based on conduction using a heatsink as material interface, which is to be attached to the DDCU's and the rack of DP structure. Regarding the thermal background above described, it is important to note that θ_{JA} is actually made up of at least two separate thermal resistances in series. One is the thermal resistance inside the device package, θ_{JC}, and the other one is the resistance between the case and the ambient, θ_{CA}. The last term can be splitted into θ_{CS} and θ_{SA}, thermal resistance from case to heatsink and thermal resistance from heatsink to ambient respectively, resulting in the equation 23 [69].

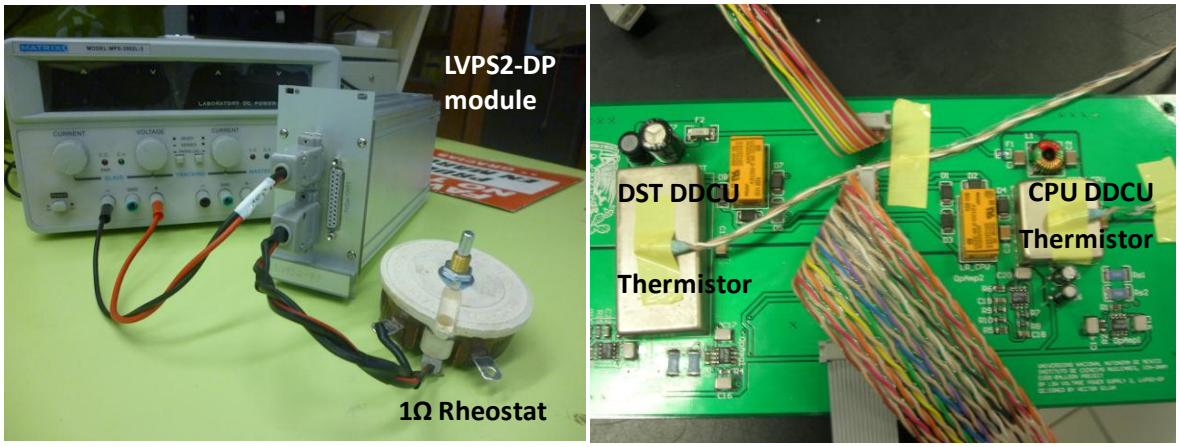


Figure66. Preliminary set-up (at the left) and thermistors on DDCU's (at the right).

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{23}$$

However, in order to select a heatsink, the term θ_{SA} has to be calculated. Therefore, is necessary to assume the next safety conditions and specification from the DDCU datasheet: T_{Jmax}=100ºC; Ta_{max}=50ºC; Tc_{max}=90ºC and P_D=7W.

And using equations 22, 24 & 25, the θ_{SA} term can be obtained by resolving equation 26.

$$\theta_{JC} = \frac{T_{Jmax} - T_{Cmax}}{P_D} \tag{24}$$

$$\theta_{CS} = \frac{t}{k * A_C} \tag{25}$$

Where "*t*" refers to thickness material ($9.6x10^{-3}m^2$), "*k*" is the thermal conductivity of aluminum 3003-'O' (190W/m*ºC), and "*Ac*" is the contact area between DDCU and HS ($1.3x10^{-3}m^2$).

$$\theta_{SA} = \theta_{JA} - \left(\theta_{JC} + \theta_{CS}\right) \tag{26}$$

Consequently, a θ_{SA}=5.68ºC/W was obtained which implies a selection of heatsink rated at 5.68ºC/W, or less. Therefore, and regarding the mechanical dimensions of plug-in unit box shown in figure 57, the heatsink proposed and its components were arranged as is shown in the figure 67.

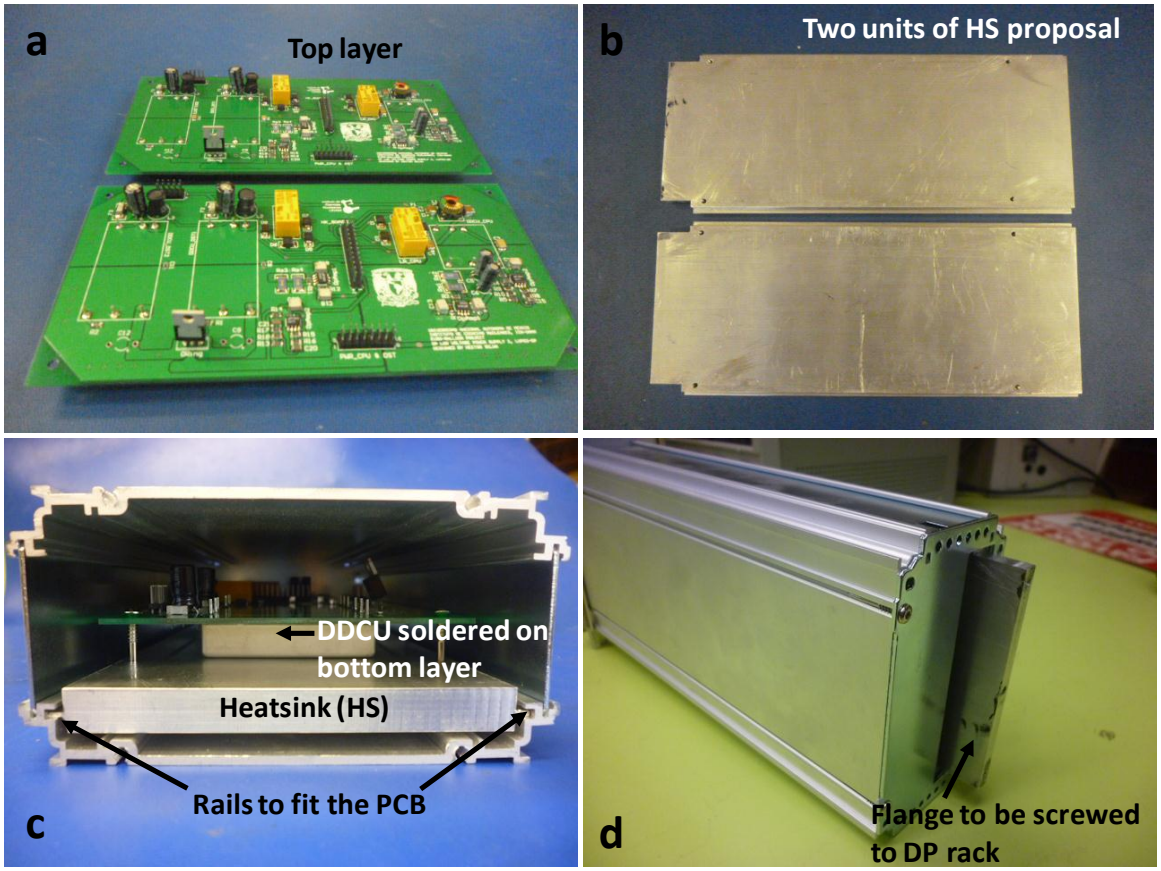


Figure67. (a) Two PCB's of LVPS2-DP, (b) Two HS proposed, (c) PCB, HS and unit box assembly, and (d) HS rear side to be assembly with cooling plate of DP rack.

As can be seen in figure 67a, most of the elements are in the top layer while the converters are in the bottom layer (see the figure 67c), unlike the PCB of the other rest power modules, in which all the components are in the top layer. Also, in this configuration it is the heatsink (see the figure 67b) who fits on the rails instead of the PCB. However, and due to necessity to screw heatsink flange to DP rack cooling plate, accommodation of elements were twisted as is showed in figure 67c. Consequently, the converters make direct contact with HS surface conducting the heat to edge coming out across the rear side panel of plug-in box, as can be seen in figure 67d. Finally, the heatsink edge (rear side) has holes in order to be screwed to cooling metal backplane, of DP rack, which is connected to heat metal conductive bars and then connected to external structure of balloon gondola improving in that way the thermal management of all instrument.

In the next chapter the proposed tests will be described, and also the results obtained from all the LVPS modules which were manufactured and assembled for the final integration phase of EUSO-Balloon project are also discussed.

V.1 Tests

In order to perform the LVPS subsystem evaluation under the relevant environmental conditions, two types of tests were done. The first one was devoted to evaluate the electrical performance of the LVPS modules under different load ranges (10% to 100% of full load) considering worst case scenario. The second one was focused in evaluating the critical electrical performance levels (at full load), and conducted at pressure conditions of ~3mBar with thermal cycling going form -20ºC to 55ºC.

V.2 Electrical Performance

The aim of this test was to characterize the four LVPS modules according to each subsystem specifications. A dc electronic load (dcEL) simulator, specifically developed at our group for this purpose, was used in order to automate the test process. The main idea of the dcEL is to operate in current regulation mode, for that purpose uses a simple feedback loop to allow a transistor works either as current drain, or as voltage source in voltage regulation mode [70]. At this particular case, current regulation mode is used for characterizing voltage sources, in which the power source must deliver a specific current level setting by serial software interface to dcEL hardware. The figure 68 shows the electrical performance setup used to perform the test.

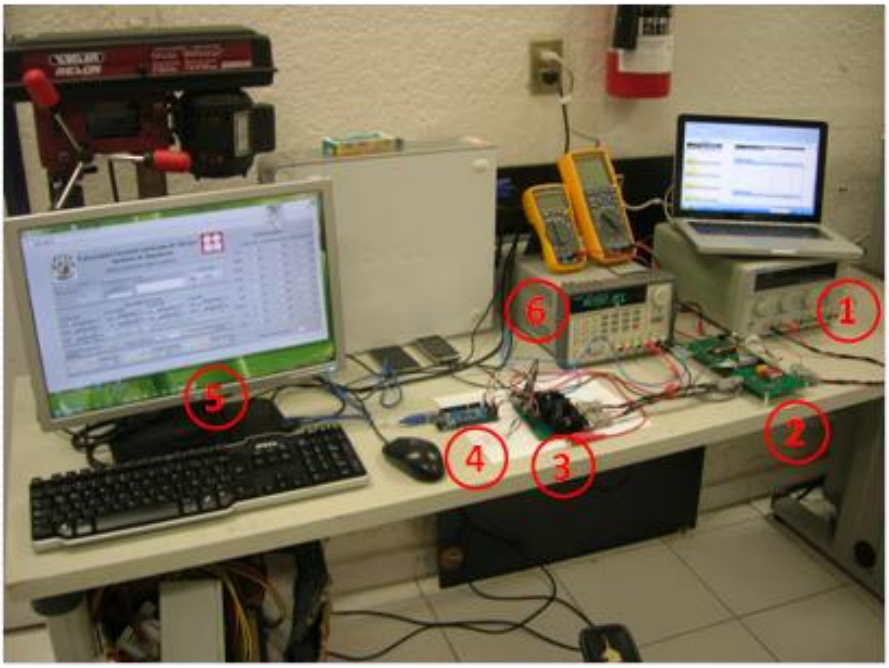


Figure68. Set-up of electrical performance test.

Basically, the setup shown in the figure 68 consists of a main laboratory power supply (labeled with number “1”), which provides the 28V primary power bus voltage to the LVPS module at number “2”. On the LVPS module, the DDCUs isolate and transform the main bus to a secondary power bus voltage which level depends on each subsystem. On the other hand, the dcEL (labeled with number “3”) receives commands from the HK subsystem (at number “4”), powered with an auxiliary power source (at number “6”). The HK maintains communication with a PC through a software interface application (at number “5”) via serial port. The software settled the current level that should provided the LVPS module to the dcEL. At the same time, the LVPS module provides V&I levels about the status consumption of DDCUs, as telemetry information, and the LVPS on/off status to the HK subsystem.

Based on the setup described in the figure 68, parameters like load and line regulation (& LnReg) were obtained at each LVPS module in the output connector using equations 27 and 28. The table 12 shows the results about the LdReg for each subsystem on LVPS modules. The performance curves related to efficiency versus output current and input voltage also were also obtained.

$$\%Load_{Reg} = \left(\frac{Vout_{full\ load} - Vout_{10\%\ load}}{Vout_{50\%\ load}}\right) \times 100 \quad (27)$$

$$\%Line_{Reg} = \left(\frac{Vout_{high\_Vin} - Vout_{low\_Vin}}{Vout_{nom\_Vin}}\right) \times 10 \quad (28)$$

Module	DDCU Subsystem	Secondary bus voltage (V)	%LdReg at Vin_{nom}	%LdReg at Vin_{low}
LVPS1-DP	CCB	5	1.4	1
	CLKB	5	1.2	1
	GPSR	5	2.8	2.6
LVPS2-DP	CPU	12	0.17	0.25
	DST	5	0.74	0.96
LVPS-PDM	FPGA	5.5	1.36	1.31
	EC-ASIC	5.5	1.35	1.32
LVPS-HK	MCU	±12	7.3	7.4
	LVDS	3.3	10	7.69

Table12. Load regulation of different subsystems on LVPS modules.

The percentage of LdReg indicates the variation in the output voltage in response to a change in load current, and is a reference to the LVPS modules for complying with the output voltage tolerances specified by the subsystems. The load regulation percentage measurements were obtained varying the load from 10% to full load, under both conditions, at nominal input voltage (28V) and the lowest input voltage (18V) allowed which represent the worst case condition level.

On other the hand, the LnReg plots according to secondary bus voltage level of subsystems powered with 5V, 5.5V, 12V and 3.3V are shown in the figures from 69 to 72 respectively. Those curves show fluctuations less than 10% on the output voltage at 90% of full load. The later complies with the subsystem specification requirements given in table 2. The behavior of the curves is almost constant, a slightly increment (less than 10mV) at the end of curves (when Vin>28V) is due to the temperature increase on resistor loads which cause mismatch on resistors tolerance specifications, and consequently variation in current level demand, which is compensated by increasing the output voltage in order to keep a constant output power.

Since the LnReg term represents the change in the output voltage in response to a change in the input voltage; this test was planned considering the possible voltage range excursion of battery which goes from 18V (which is the lowest level) to 30V. It is also important to note that the input voltage range of the DDCU's selected perfectly compensates the output excursion from battery.

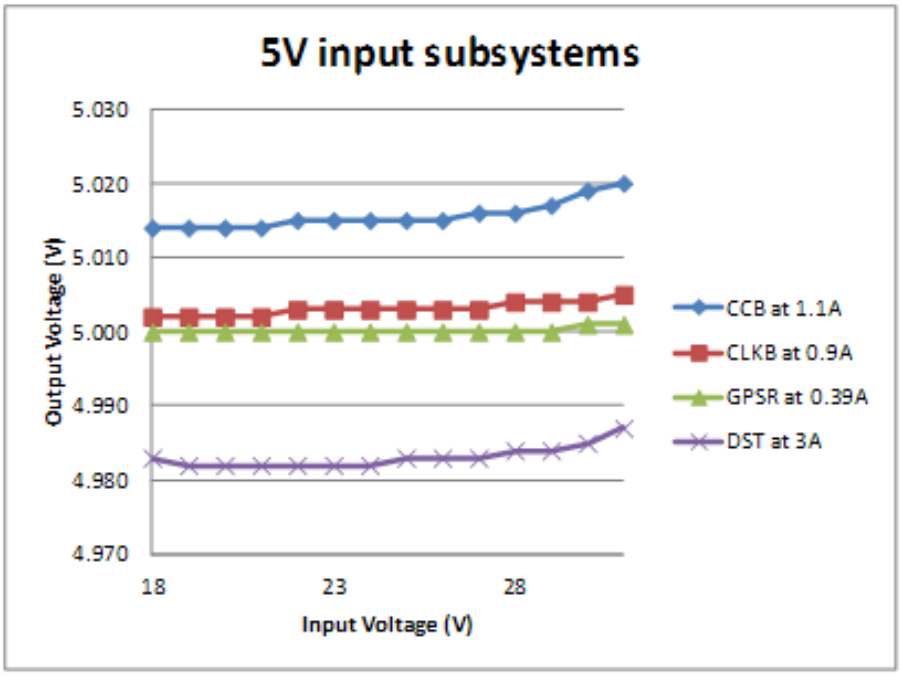


Figure69. Line regulation plot of the subsystems powered with 5V.

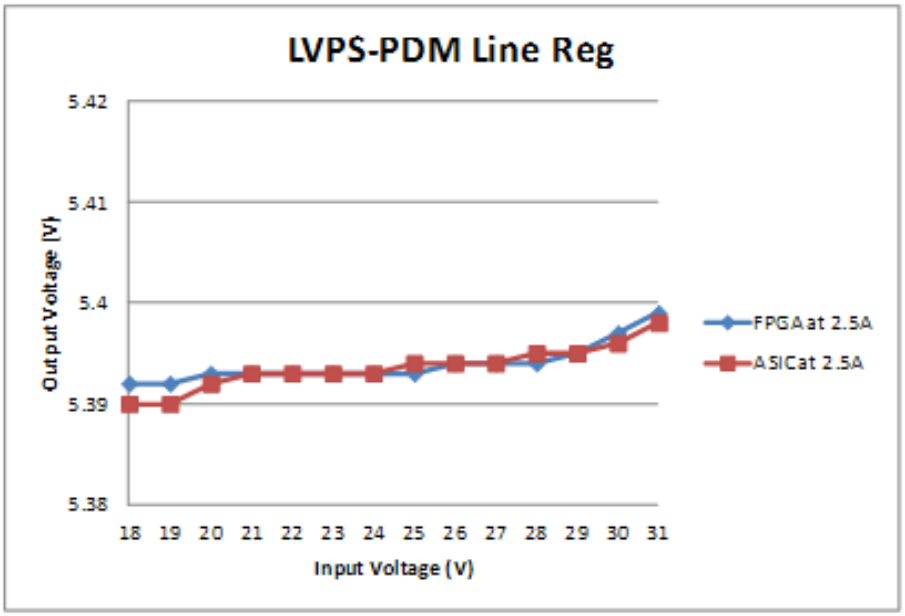


Figure70. Line regulation plot of the PDM subsystems powered with 5.5V.

On the other hand, a voltage drop in the HK curve can be observed in the figure 71, which exceeds the tolerance of 10% at upper level specified in the table 2. The disturbance is due to the bad LdReg on DDCU obtained in table 12. However, this abnormality is acceptable and absorbed by the linear regulator on the HK board, which withstands variations from 7V to 15V at its input.

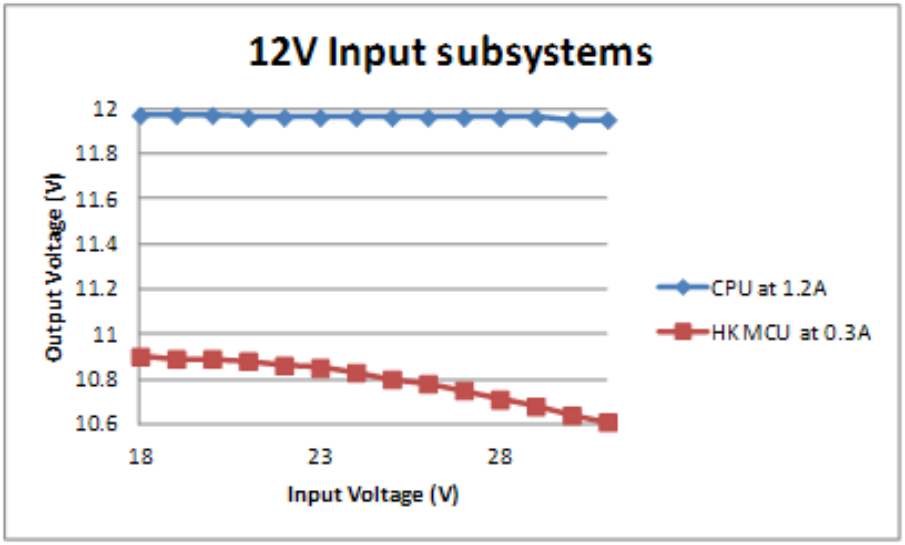


Figure71. Line regulation plot of the subsystems powered with 12V.

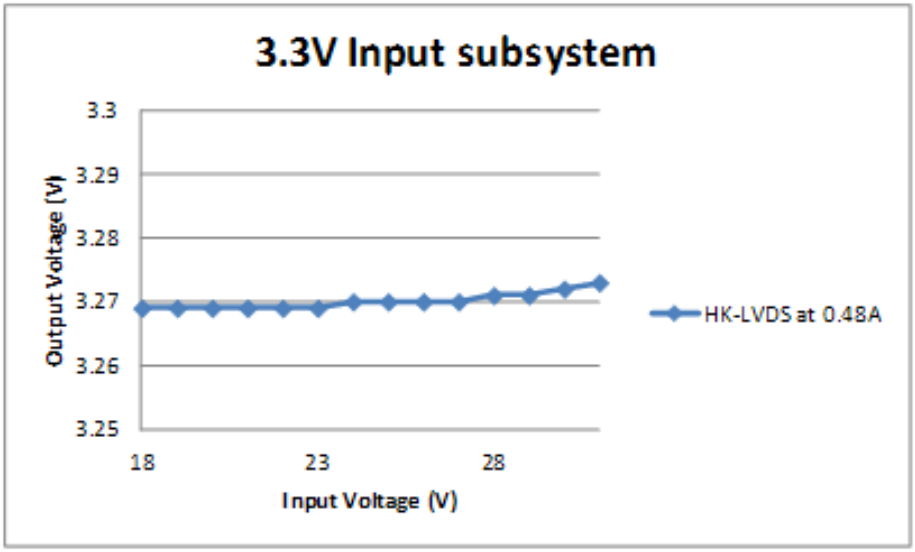


Figure72. Line regulation plot of HK-LVDS section powered with 3.3V.

Voltage drop due to the cables resistance represents a critical issue in any power distribution system. The table 13 shows the resistance of the recommended cables for this particular case with a length of 0.5m. Additionally, voltage drop is showed under test current conditions.

Subsystem	Test current (A)	Cable resistance (mΩ) per meter	Voltage drop (mV)
CCB	1.1	33.23	36.55
CLKB	0.9	42	37.8
GPSR	0.4	84.2	33.68
DST	3	6.57	19.71
FPGA	2.5	13.17	33
EC_ASIC	2.5	13.17	33
CPU	1.2	33.3	40
HK-MCU	0.3	53	16
HK-LVDS	0.48	53	12.72

Table13. Different cables resistance of recommended cables.

Efficiency curves of each LVPS module according to each subsystem were also obtained. The tests were performed varying the output current form 10% to full load demanded with increment steps of 10%. The later was done under the worst case condition (Vin=18V) in order to observe the behavior of the subsystem on each LVPS module at maximum current levels. For simplicity, plots are presented according to the current consumption level of each subsystem. Therefore, the efficiency curves of subsystems with maximum current consumption of 3A are shown in the figure 73. While those that current consumption are next to 1.2A are shown in the figure 74. The figure 75, on the other hand, shows the efficiency for those subsystems whose demand is less than 0.5A.

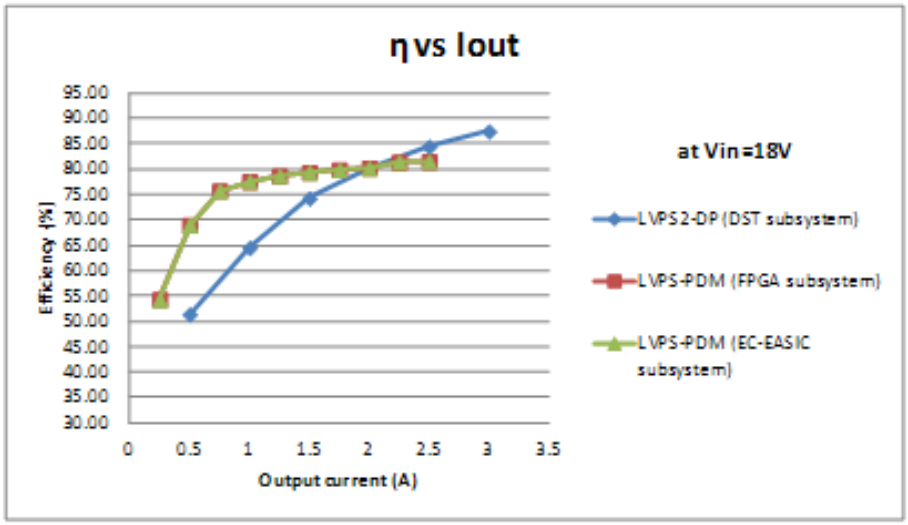


Figure73. Efficiency curves of 3A current consumption subsystems.

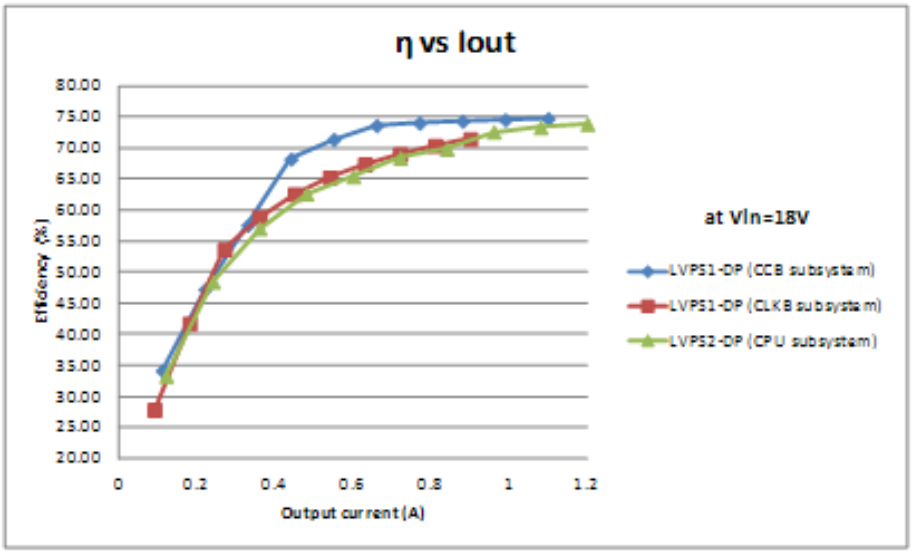


Figure74. Efficiency curves of ~1.2A current consumption subsystems.

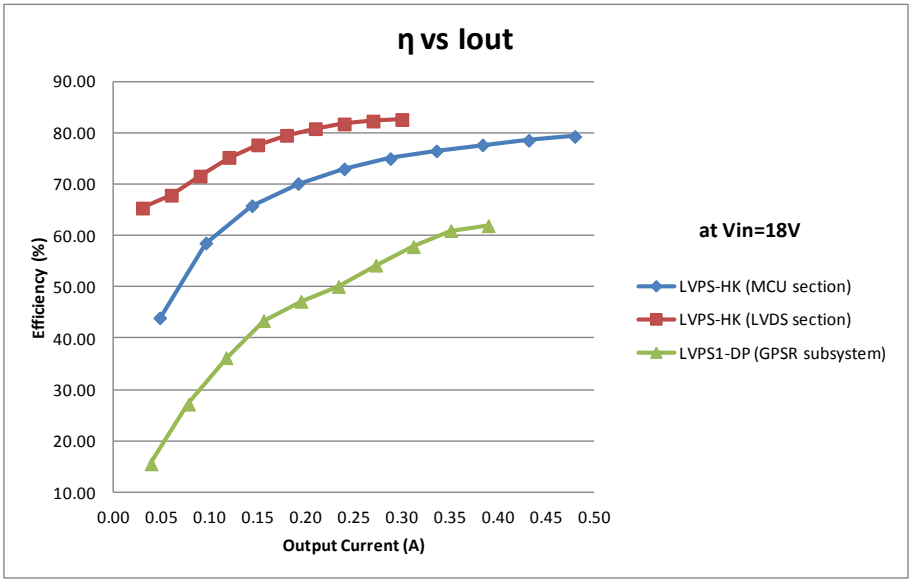


Figure75. Efficiency curves of 0.5A current consumption subsystems.

The curves above describe show how efficiency progressively improves as full load consumption is reached. However, it is important to note that the maximum efficiencies obtained experimentally (from 60% to 87%) do not reproduce the specifications provided by the datasheet converters, at full load, which are higher. The later is because the datasheet parameters are measured directly at the pin package of DDCU under test, with no influence of stray impedance traces, planes, components, connectors, etc. The efficiencies obtained are related to the dissipated power following equation 29.

$$P_D = P_{OUT}\left(\frac{1}{\eta} - 1\right) \tag{29}$$

Once the regulation and efficiency of the LVPS modules were obtained, it is important to verify other not less important issues about LVPS electrical performance as turn on/off and monitoring tasks.

V.2.1 Monitoring and activation of power modules

In order to test the reliability of each module of the power distribution system, and at the same time the interaction with one of the main subsystem, HK (also designed and provided by our group); the setup shown in the figure 76a was implemented. The figure 76b shows HK interfacing LVPS modules by HL_cmds board, and also auxiliary power supply for the HK subsystem. On the other hand, the figure 76c shows the power resistor housed in aluminum cases as fixed load; meanwhile the figure 76d shows the two main laboratory power supplies used as battery.

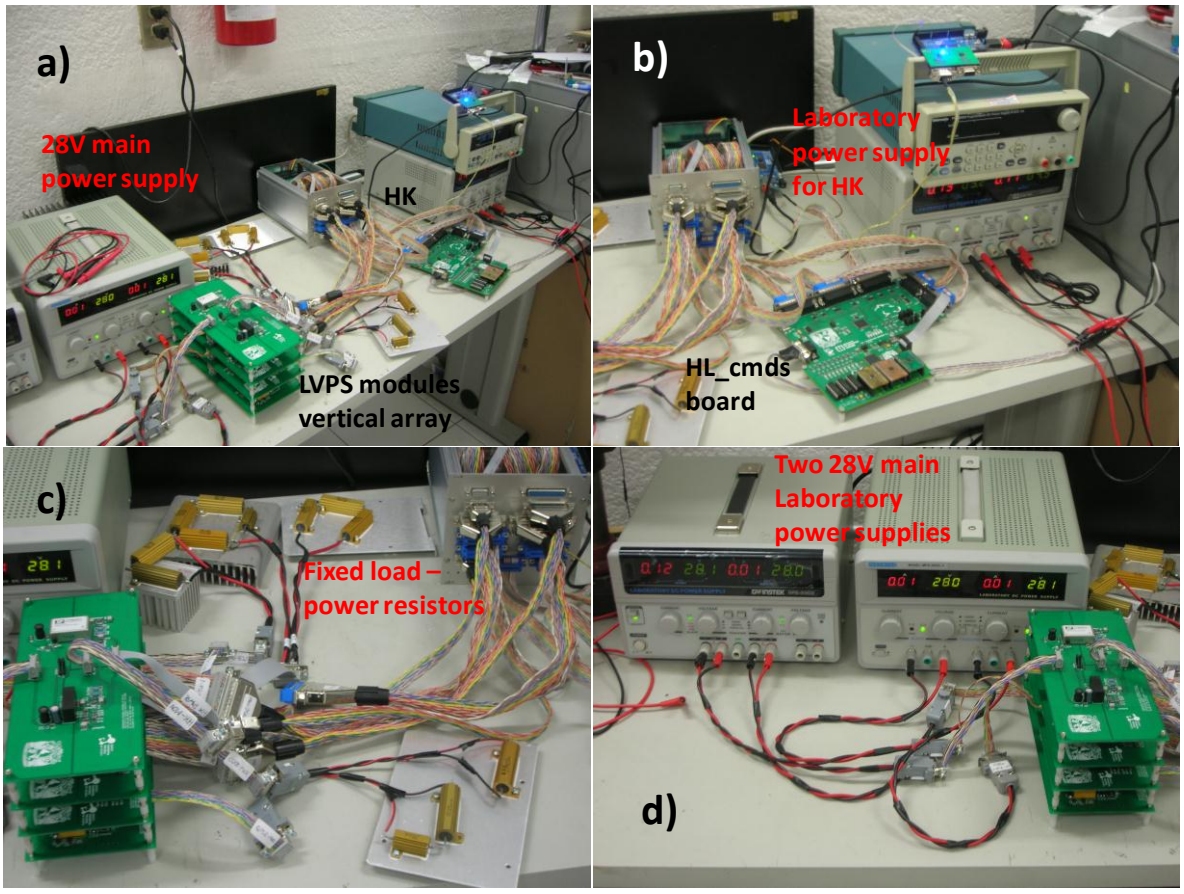


Figure76. Set-up for monitoring and activation of LVPS modules.

The commands provided by a software application on PC (simulating CPU subsystem) were sent to the HK subsystem. The commands were interpreted and executed by the HK; the latter, sends two HL_CMDs per LR's implemented on-board the LVPS modules. The HL_CMDs are represented by a 9V to 15V amplitude pulse of 10ms width. These commands are used in order to bias the internal coils of the LR's, besides diodes were included on the design for feedback current protection.

In order to minimize the required space on the test; the LVPS modules were arranged in a vertical assembly configuration, as can be observed in the figure 76a. Finally two dual laboratory power sources were added to the setup in order to provide the 28V primary bus voltage. This setup was used to verify the power consumption, at the moment of turning-on and no-load conditions, of the four LVPS modules. Also, telemetry information of current consumption levels from current monitoring circuits were also obtained using fixed resistive load.

Table 14 shows, the result of turning On/Off activation process (denoted with the green verification mark) for each subsystem after applying HL-CMDs several times under different circumstances and sequences. The second white column shows the power consumption levels of the LVPS modules (without load) after successful turning on/off process. Also voltage levels, obtained from voltage monitoring circuit as telemetry information, were measured and captured in the third white column. As was stated before, the monitored level on the LVPS module has to be multiplied by a gain factor of 0.326. In that way, a 3.3V level correspond to 1.07V, 5V level correspond to 1.63V, meanwhile 12V level correspond 3.9V output voltage.

Subsystem	Turning On/Off process	Current consumption (A) w/o load & once activated)	Monitored Voltage level (V)	Experimental fixed resistive load (Ω)	Monitored Current level (A) with experimental load
CCB	✔	0.03	1.613	5	0.982
CLKB	✔	0.005	1.688	6.3	0.971
GPSR	✔	0.02	1.678	14	0.347
PDM-FPGA	✔	0.025	1.716	2.5	1.95
PDM EC-ASIC	✔	0.025	1.707	2.5	1.97
CPU	✔	0.07	3.677	12	0.988
DST	✔	0.1	1.6	1.6	2.89
HK-MCU	✔	0.015	3.735	N.A.	0.107
HK-LVDS	✔	0.01	0.914	N.A.	0.183

Table14. LVPS modules activation and monitoring tests.

In relation with the current monitoring, a shunt resistor was implemented on the PCB as input of the Op-Amp circuit. The output voltage level corresponds directly with current consumption subsystem (1:1 relationship). Therefore, the table 14 shows the experimental load value used for demanding a range from 70% to 90%

load of each subsystem. The full-load was not reached in order to protect the DDCU under test. The last white column shows the current levels that were obtained and sent to the HK subsystem.

V.2.2 Mechanical assembly

In order to perform thermo-vacuum tests, the mechanical assembly of the LVPS modules and the HK subsystem into a similar DP rack structure has to be done. The latter is mandatory in order to achieve a thermally significant test. As was mentioned in the EMC section, plug-in unit boxes were used in order to minimize radiated EMI and enclose each LVPS module. The figure 77 shows, the LVPS-HK board housed into its plug-in box (left) including cables, and Figure 77 shows the final mechanical assembly of the four LVPS modules (right).

Figure77. LVPS-HK mechanical assembly (at left), and LVPS modules structures (at right).

The LVPS modules were housed together with the HK subsystem in order to interconnect them in easier way and perform the thermo-vacuum tests. The final mechanical assembly is showed in the figure 78.

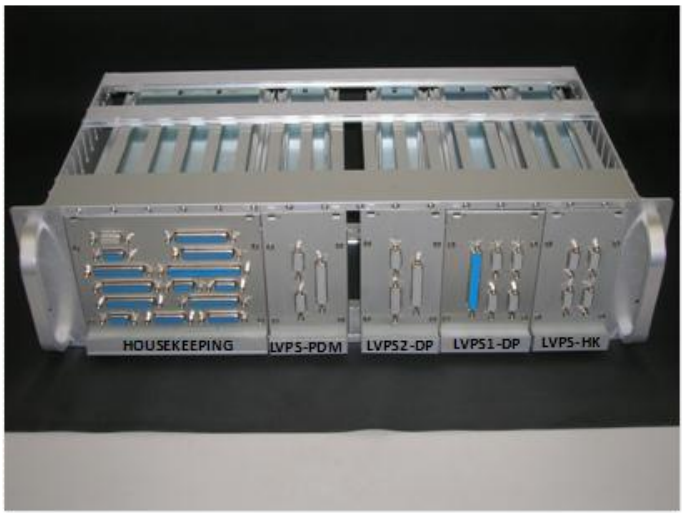


Figure78. LVPS and HK subsystems fitted in euro rack structure.

V.2.3 Subsystems weight

Once the modules were mechanically assembled, their weight was verified in order to check compliance with the requirements and specifications. The table 15 shows the weight of each LVPS module, as well as the total weight including rack structure.

Modules	Weight (kg)
LVPS1-DP	0.9
LVPS2-DP	1
LVPS-PDM	0.9
LVPS-HK	0.9
Sub-total	**3.7**
Rack	1.3
Total	**5**

Table15. Weight of the LVPS modules.

V.2.4 Heat dissipation

The suborbital environmental conditions limit heat dissipation to conduction and radiation. The problem of the very localized injection of heat at the electronic boards makes the heat dissipation a critical issue. In particular, the case of the LVPS2-DP, the heat generated by the DDCU's must be piped to the external mechanical structure of the gondola. The LVPS2-DP PCB, in particular, represents a hazardous case due to the power demand of its clients which, during integration phases, its current consumption levels were above of 4A for DST and 1.25A for CPU. Besides this consumption, due to different CPU operation modes and to several hard disks accessing processes (read/write), many transient events were generated. These transients cause not only high peaks of current, but also demand a faster response from the DDCU. Such transients are difficult to characterize and, after several tests during one of the integration phases of the DP at INFN-Naples, Italy, a PCB design based on two DDCUs in parallel was proposed to deal with the issue. The figure 79 shows the top and bottom layer of the flight model PCB LVPS2-DP module.

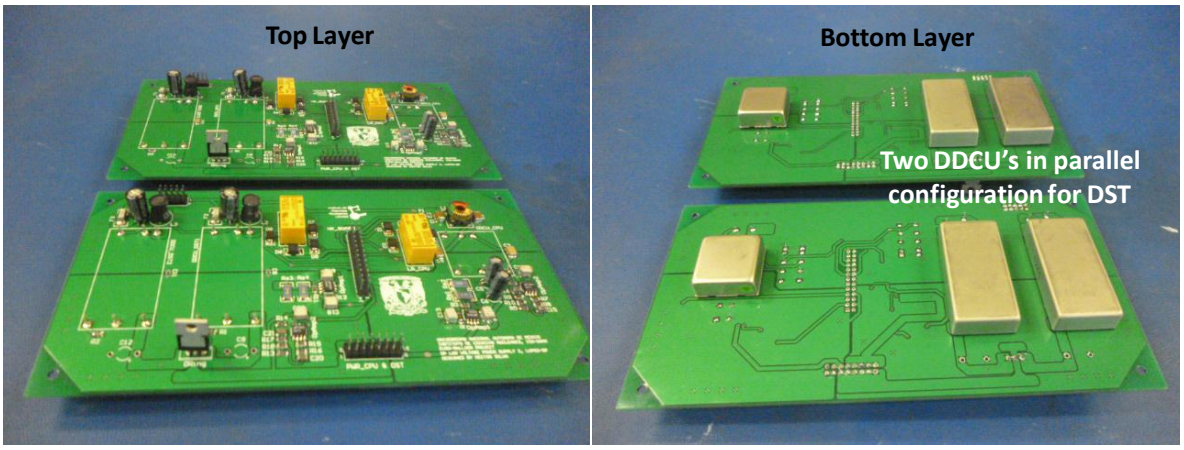


Figure79. LVPS2-DP FM PCB version.

Therefore, as was stated in chapter four, in order to manage the increase heat produced on the latter design, a heatsink was designed in order to improve the dissipation from three DDCU's on the LVPS2-DP. The figure 80 shows the mechanical assembly between heat sink and the LVPS2-DP PCB inside of the module.

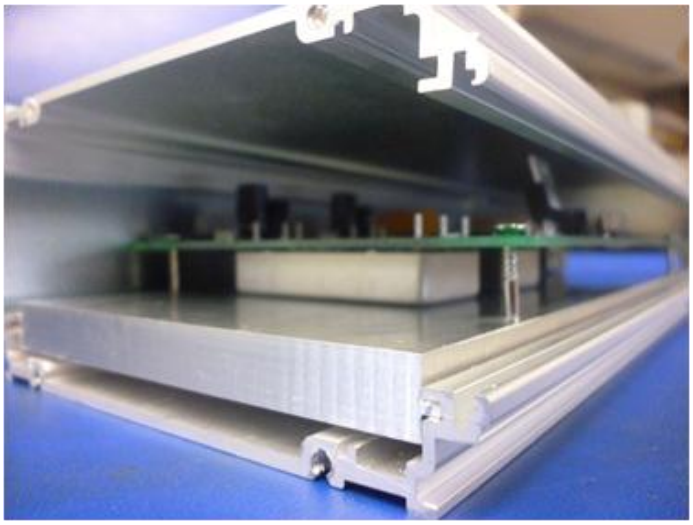


Figure80. Mechanical assembly of LVPS2-DP PCB and HS inside module.

V.3 Thermo-vacuum

An important goal of the present work was, to propose the use of industrial isolated DDCUs instead of military grade component in order to keep costs as low as possible. However, the DDCUs of TDK lambda were tested (by manufacturer) according to conditions showed in the table 16. This table shows two types of tests; in the first one, the DDCUs were tested successfully in operating mode at 0ºC and 40ºC at an altitude of 12km. Meanwhile, in the second test the DDCUs were tested in non-operating mode at -40ºC and 70ºC at an altitude of 15km. The tests were performed during 2 and 6 hours, respectively and were based on MIL-STD-810F.

Test condition	Operating combined test Temperature / Altitude		Non-operating combined test Temperature / Altitude	
Temperature (ºC)	0	40	-40	70
Altitude (km)	12.2	12.2	15.2	15.2
Test duration (hr)	2	2	6	6

Table16. Altitude tests performed to DDCUs by TDK lambda.

Therefore, in order to ensure the physical integrity of the LVPS subsystem in sub-orbital flight conditions in the upper atmosphere, a series of thermo-vacuum tests were conducted in a custom-made vacuum chamber with thermal control.

The figure 81 shows the custom-made vacuum chamber used. The experimental instrument is equipped with a refrigerator, coupled to a heater, which allows the temperature to be adjusted from -37ºC to +80ºC at a heat exchanger in its base. The chamber can reach a minimum pressure of 10^{-6} Torr (0.13 mPa =1.33E-09 Bar).

Figure81. Custom-made vacuum chamber.

The objective of the tests is to guarantee the operation of the LVPS modules at lower pressure of 3mbar, for temperatures ranging from -20ºC to 50ºC validating the overall thermal requirements imposed to the EUSO balloon experiment. The baseline duration time of the first flight of the EUSO-balloon is approximately 12 hours.

At the moment, all the phases of the ascension of the balloon cannot be simulated with the current experimental, conditions of humidity and radiation exposure are not implemented. The experimental setup is constituted of a vacuum bell jar with a working volume of roughly 60Lts, inside which an aluminum plate (30cmx30cmx1cm) is resting on 4 stainless steel rods. The aluminum plate is connected to a refrigerator, which allows cooling down to -37ºC tops. A heater, made of NiCr, attached to the surface of the plate, is used to regulate the aluminum plate temperature in the range from -37ºC to +80ºC.

In addition to the mechanical pump, if required, a second turbo pump stage can be used to reach 10^{-6} Torr. However, the most demanding test for the system is at the higher pressure of 3mb, where thermal conduction in air is highly reduced (although not fully insignificant) and convection is negligible, but there is still enough air in the rarefied atmosphere to produce unhindered sparks, while providing a low dielectric constant.

A series of tests comprising module on/off activation, constant full load operation, V&I monitoring information, status relay and temperature monitoring were conducted over a period beyond 12 hours in vacuum conditions. The figures 82 and 83 show a setup for testing at constant full load (at ambient), as well as the vacuum chamber setup with all the wiring subsystem each other respectively.

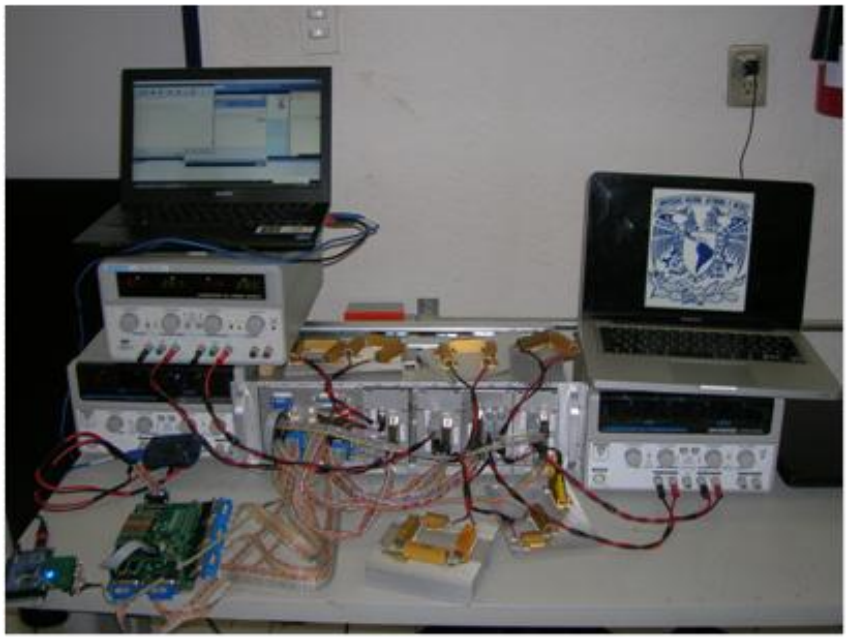


Figure82. LVPS modules at full load operation.

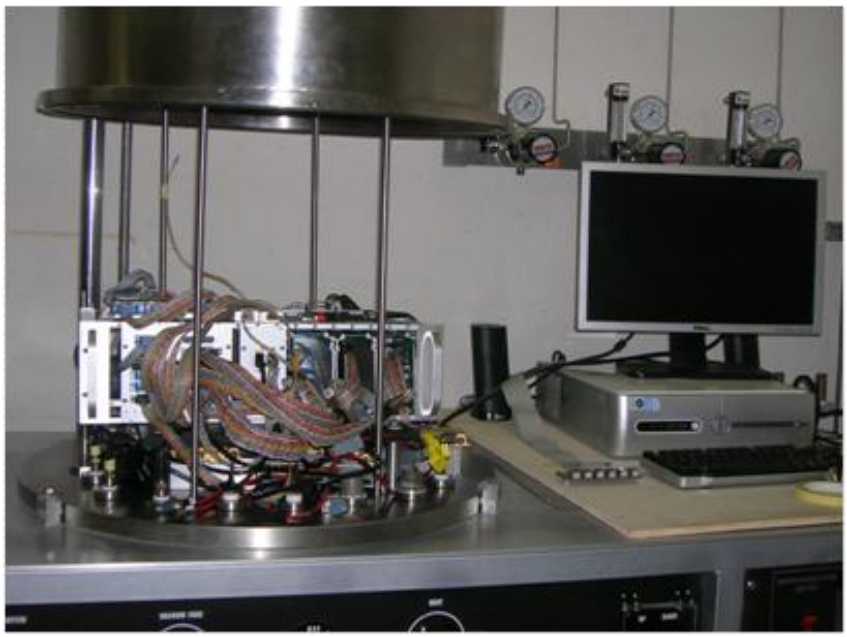


Figure83. Vacuum chamber test set-up.

The figure 83 shows an electronic setup with the four LVPS modules and the HK system housed in the same rack. Here the HK was used both through its regular interface with the LVPS subsystem, and as a probe inside vacuum for testing temperatures at several critical components of the LVPS modules. The power supply cables from two main laboratory power supplies were connected to the LVPS modules. Differential cables from monitoring LVPS connectors (color cables) come out to the HK unit. Twisted pair cables from 14AWG to 20AWG were connected, under the aluminum plate, to fixed value aluminum housed power resistors which were calculated in order to demand full load operation. Finally, three thermistors at the DDCU's on LVPS2-DP were located: one at CPU, and 2 at DST section. The figure 84 shows six twisted pair cables coming out of the rear side panel of the LVPS module; three pair cables from DDCU's and the remaining from heat sink side.

Figure84. Thermistors inside of the LVPS2-DP.

As mentioned in the thermal management section, a set-up was implemented at room temperature ~25ºC as a first test, which helps to know basically three aspects. The first one was got the measurements (at full load) from current monitoring circuits. The table 17 shows the measurements according to each subsystem.

Subsystem	Experimental current load (A)	Current monitoring (A)
CCB	1	0.982
CLKB	0.793	0.971
GPSR	0.357	0.347
PDM-FPGA	2	1.95
PDM-ECASIC	2	1.97
CPU	1	0.988
DST	3	2.89
HK-MCU	N.A.	0.107
HL-LVDS	N.A.	0.183

Table17. Monitored current measurements from DDCU's at full load.

The second one had the objective to ensure the same current consumption on both DDCU's of DST section implemented in parallel configuration. The later was achieved by verifying the temperature rise of both converters at same time. As it can be seen from figure 85, the temperature difference between converters DC/DC1 and DC/DC2, before 15min, was less than 2ºC which is acceptable. After that, the difference increases which probably indicate an unbalanced load operation. The later was solved adding ORing diodes in series with the output of each DDCU as is showed in figure 86.

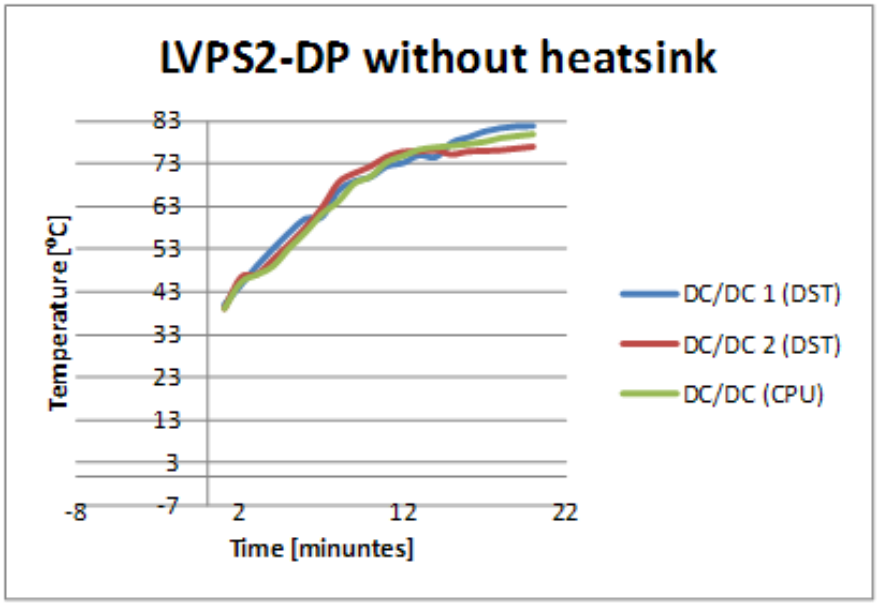


Figure85. Temperature mismatch on both DDCU's of the LVPS2-DP.

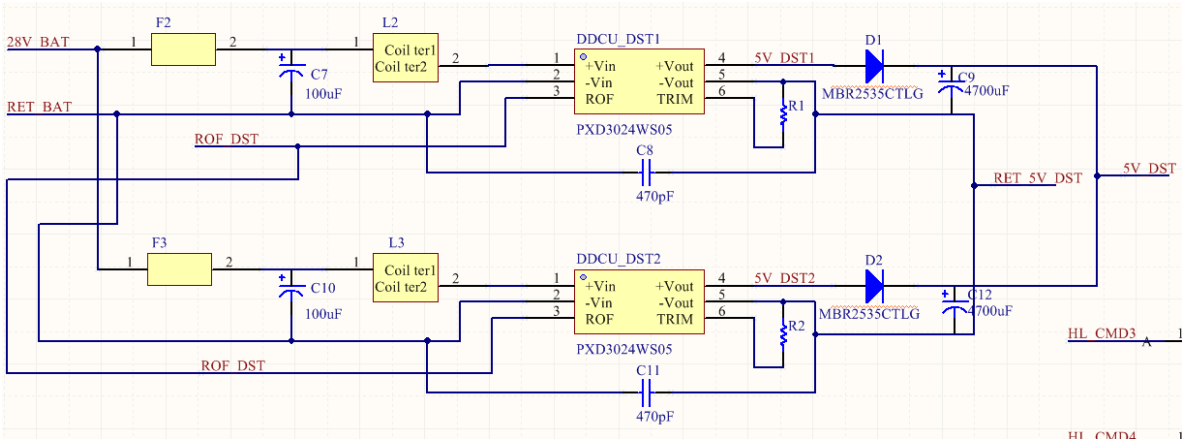


Figure86. The ORing diode array at the output of DDCUs of the DST section on LVPS2-DP.

The diode arrangement showed in the figure 86 above had the aim to balance loading on both power supplies. Consequently, both converters provided the same current level to the load.

The third reason was to figure out how long it takes to reach ~ 85ºC (maximum case temperature). Approximately, in 20min both the converters reach the temperature barrier. Therefore, in order to decrease the temperature on converters, the heat sink manufactured and implemented on LVPS2-DP module was used as a part of the setup shown in the figure 87. This setup comprise the HK subsystem, using through its regular interface with LVPS subsystem and as a probe for testing temperatures of LVPS components; and two LVPS modules: LVPS2-DP and LVPS-HK, the latter powers the HK subsystem. The LVPS2-DP module was fixed in vertical position, in that way, the rear side of heat sink (coming out from LVPS2-DP module) was in direct contact with aluminum plate of vacuum jar and the heat transfer between them was improved by using thermal grease, as is shown in figure 87 (at the right). A set of thermistors were implemented in similar way as was shown in the figure 84. Furthermore, two more thermistors were added, one on heat sink over the edge (het sink and aluminum plate boundary contact) and other on the aluminum plate. This test was conducted at room temperature inside of vacuum jar (the last not functioning) with the aim to compare the thermal performance over 20min.

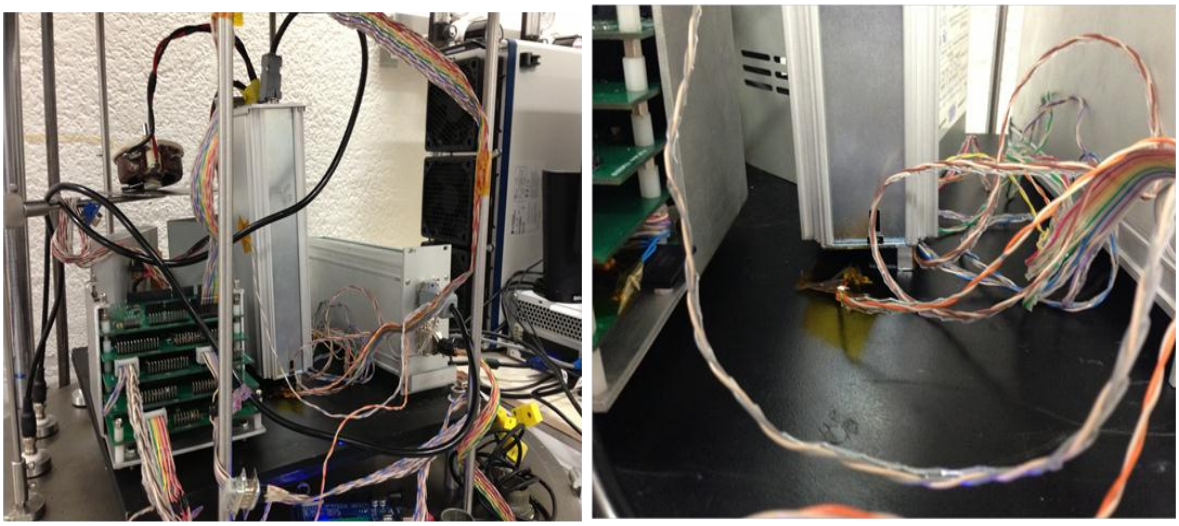


Figure87. Thermal performance test at room temperature of LVPS2-DP DDCU's.

The result was that temperature decreases until 35ºC at the 20min of test; nevertheless, temperature continues increasing as is showed in figure 88. Therefore, in order to continue the module test, the vacuum jar was closed and the environmental conditions and pressure were settled at 3mbar. The module continued working for 90min more, in which the temperature reached ~55ºC as can be observed in figure 89. The figure 89 also shows how the temperature continues increasing as a result of the LVPS module continuous operation at full load.

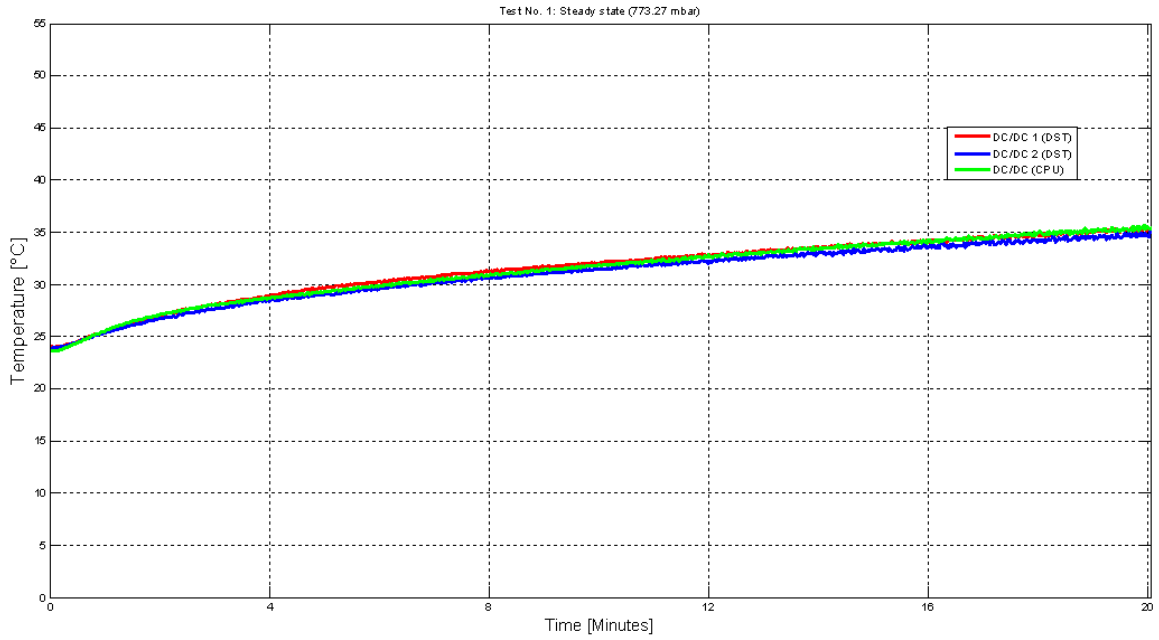


Figure88. Thermal test over 20min.

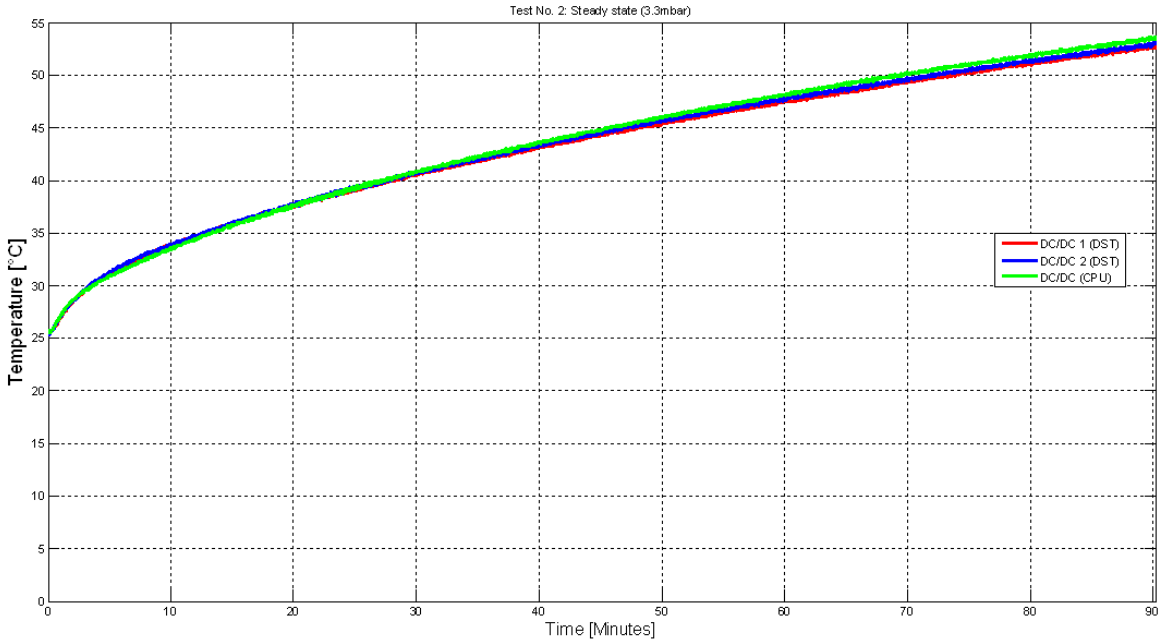


Figure89. Thermal test performance at 3mbar conditions of LVPS2-DP converters over 90min.

Finally and keeping same pressure and load conditions set-up, two thermal increments in the plate (blue line) were provided in extension to the DDCUs of the LVPS module, as can be observed in the figures from 90 to 92.

These two increments were done with the purpose to figure out the time in which converters reach the maximum case temperature. The red curve describes the two thermal increments steps by the heater attached to aluminum plate; meanwhile green line describes the temperature at the edge of heat sink and plate. The remaining two lines, light-green and purple, describe the rise temperature at heat sink (over DDCU) and lateral side case of DDCU package under test, respectively. The figures 90 to 92 describe, in separately way, the thermal performance of three DDCUs of the LVPS2-DP module.

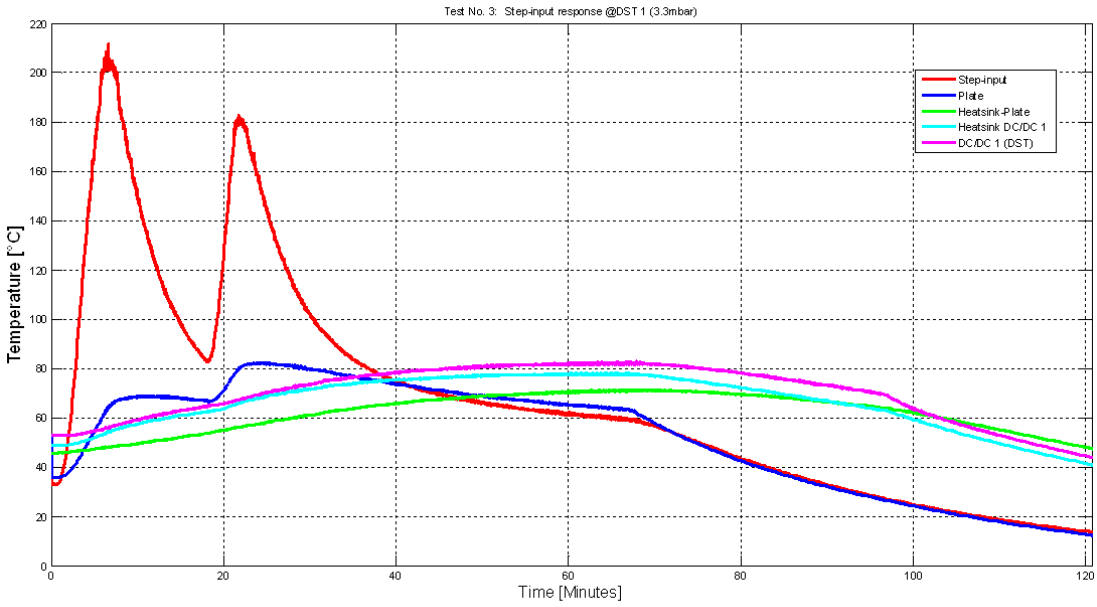


Figure90. Thermal performance of LVPS2-DP DDCU1 of DST section.

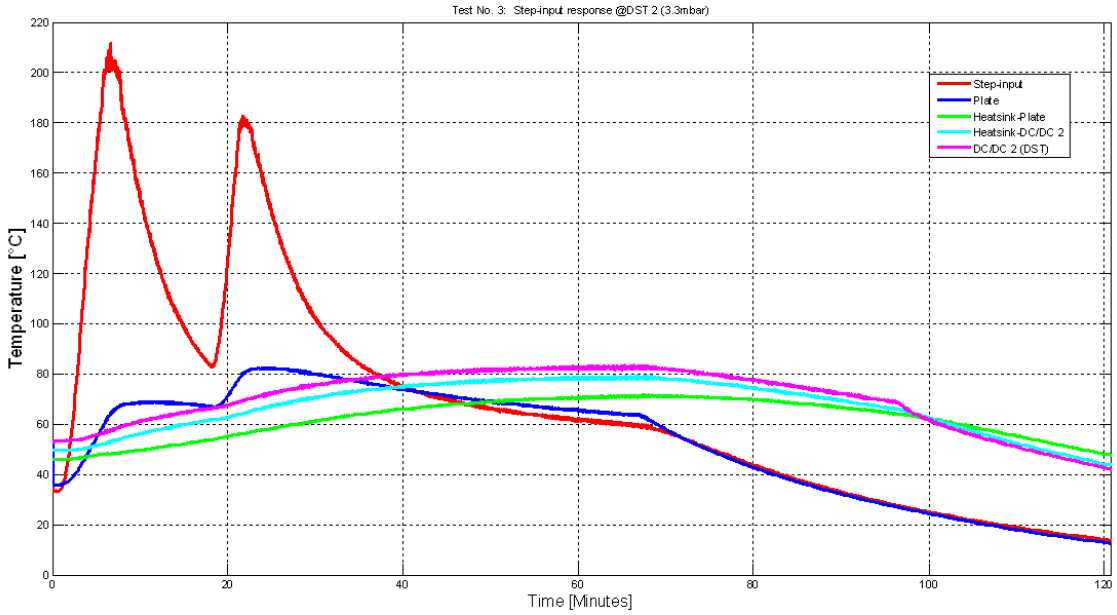


Figure91. Thermal performance of LVPS2-DP DDCU2 of DST section.

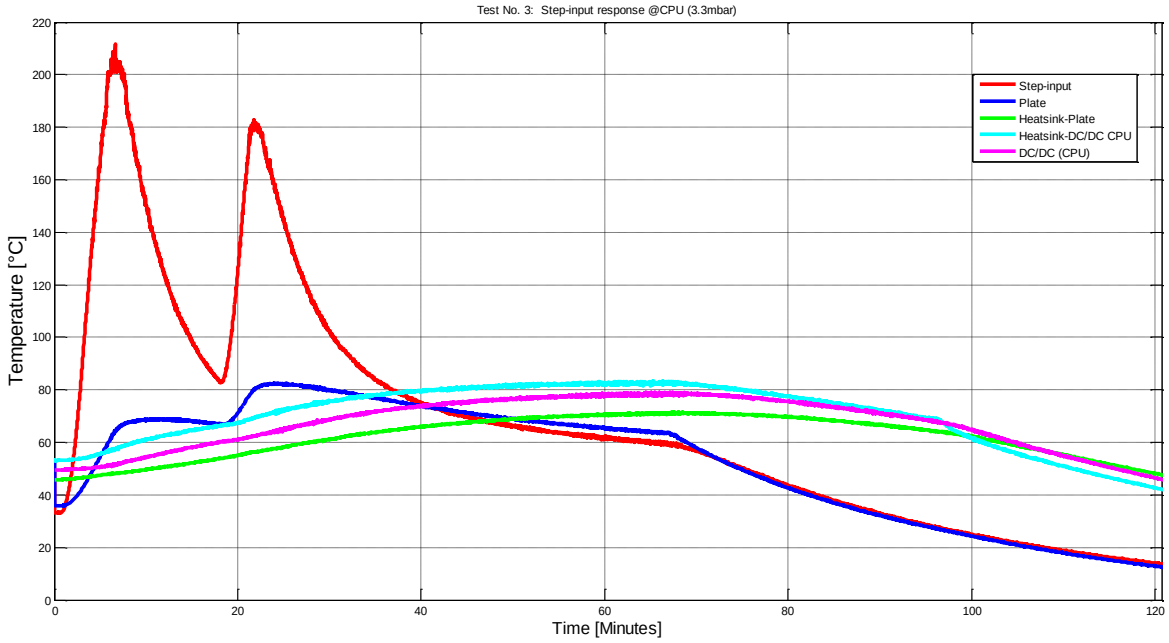


Figure92. Thermal performance of LVPS2-DP DDCU of CPU section.

Consequently, the figures above show the thermal performance of LVPS2-DP DDCU's under environmental conditions provided by aluminum plate of vacuum jar. The maximum case temperature was reached after 60 min of continuous performance at full load. It is important to state that the results showed in previous graphs are acceptable regarding two important points. The first one lies in the real operation modes. During normal operation, the LVPS modules are not intended to use at these current operations rates on EUSO-Balloon project. The second one lies on the final surface dissipation area. In the final assembly, the heat sink of the LVPS2-DP module will be attached to cooling plate located on the back of the DP rack. Furthermore, these tests also serve to verify the behavior of the protections of the LVPS subsystem under such conditions including the safety factor margins.

Finally, the figure 93 shows the resulting thermal performance plot from tests performed at final integration stage. The test conditions were settled at a pressure of 3mbar and under the real load conditions represented by the several operation modes of all subsystems on balloon. Furthermore, the LVPS performance at this test was in the real position into DP rack structure. In the figure 93 it can be seen how the temperature is stabilized, at 51ºC, after reach 10hrs of continues working.

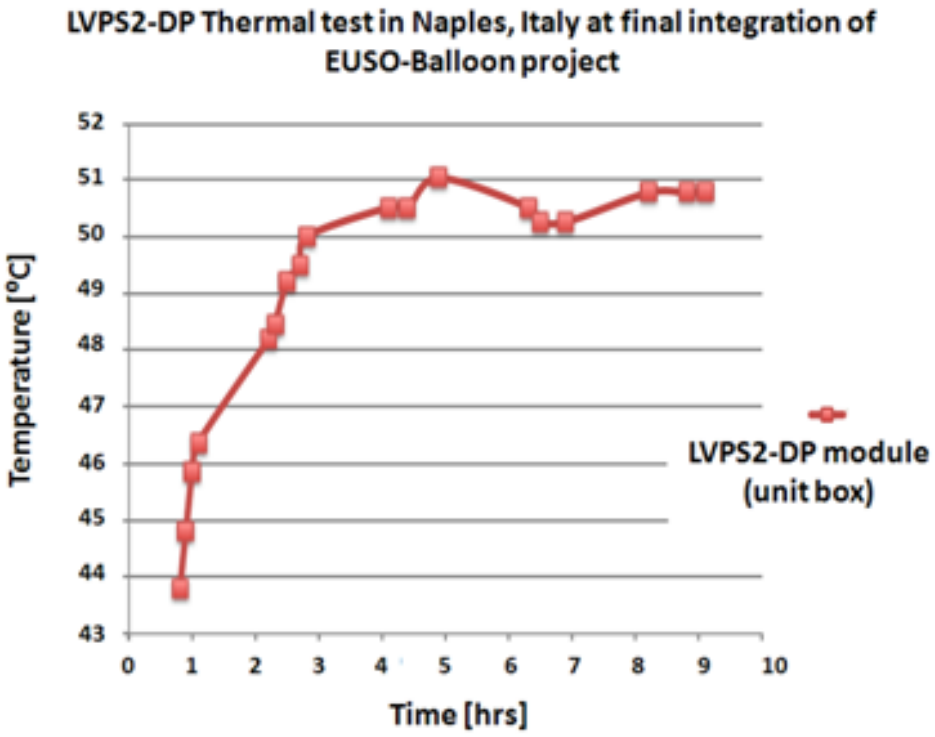


Figure93. The thermal performance of the LVPS2-DP at final integration test.

The present work shows the results of a research performed about the state-of-the-art in low-voltage power distribution architectures at space environment. The research performed focused on large scale instruments as the international Space Station and more complex satellites which carry on-board a large number of payloads. The constraints imposed by other sorts of applications, considering micro-satellites and medium scale satellites, were also described. Furthermore, this work states the necessity to develop the optimal low-voltage power distribution architecture in order to be implemented on large and complex space experiments, as the Extreme Universe Space Observatory on-board Japanese Experiment Module and the EUSO stratospheric Balloon projects.

As a result of this research, a fully operational low voltage power supply subsystem has been developed for a sub-orbital EUSO-Balloon instrument. The low voltage power distribution strategy proposed represents the basis for designing a low-voltage power supply subsystem for a unique and novel large scale instrument, JEM-EUSO. The low voltage power supply subsystem developed has the capability to operate under an environment of 3mbar pressure, within a temperature range from -20ºC to 50ºC, and load consumptions imposed by the several operation modes of the subsystem clients (payload). The subsystem developed is comprised by four power modules: LVPS-PDM, LVPS1-DP, LVPS2-DP and LVPS-HK. The power modules are able to provide 30W, 13W, 45W and 10W respectively. The reliability of the instrument performance is provided by prioritize the hierarchy of the payloads during the power distribution. On the other hand, the power modules can be remotely activated, in reliable way, through 12V HL_CMDs pulses provided by the external subsystems, Housekeeping and SIREN. The four low voltage power supply modules developed provide isolation between the 28V main power bus and the secondary power bus avoiding failure propagation. At the same time, the modules provide transformation (secondary bus) to low-voltage levels of ±12V, 5.5V, 5V and 3.3V, allowing to implement tight regulation stage equal or less than ±1% with efficiencies higher than 90% on-board subsystems by the use of linear regulators or non-isolated point-of-load converters.

The modules are able to withstand low input excursions voltage levels of battery, from 30V to 18V, and provide 10% of tolerance on output voltage levels of DC-DC converter units. On the other hand, due to the environmental conditions and importance level of some subsystems, the low voltage power supply modules provide different protection circuitry related to input/output short circuit by the use of fuse at input, over-temperature protection, and since the switching power supplies are the major EMI noise contributors on instrument, input/output EMI filters were implemented (according to manufacturer specifications) in order to minimize the instrument contamination by conducting interference from tracks, connectors, cables, etc. Furthermore, a complementary analysis was performed to ensure system stability due to the LC and pi-filter configurations proposed by manufacturer.

Additionally, PCB power modules were enclosed into individually unit boxes with the main purpose to minimize the radiated interference and, at the same time, be less susceptible to external EMI. The enclosure boxes comply with the Eurocard dimensions (55mmX100mmX220mm) imposed as requirement for its accommodation into main DP rack structure.

Another capability of the low voltage power supply subsystem consists of providing voltage and current levels of each module, within the range of 0V to 5V output as telemetry data to Housekeeping. Furthermore, the power modules allow to verify the activation status of latching relays in order to control in reliable way the subsystems powered by the power modules. The two-layer printed circuit boards of power modules also comply with the Eurocard size dimensions. Regarding mass constraints, the low voltage power supply modules comply with the requirement of not exceeding 5kg.

The thermal management was a complicated issue. A heat sink of θ_{SA}=5.68ºC/W was manufactured. The implementation of the heat sink helped to decrease the temperature on tests, although most of test revealed that temperature still increasing even heat sink used, this inconvenient was mainly because of the load regime imposed on tests. The results obtained were acceptable regarding two important points. The first one lies in the real operation modes. During normal operation, the low voltage power supply modules are not intended to use at these current operations rates on EUSO-Balloon project. The second one lies on the final surface dissipation area. In the final assembly, the heat sink of the LVPS2-DP module will be attached to cooling plate located on the back of the DP rack. Furthermore, these tests also served to verify the behavior of the protections of the power subsystem developed.

Finally, the low voltage power supply modules were tested under real load tests conditions imposed by its clients during the final integration phase. Furthermore, the thermal performance was improved attaching the designed heat sink to cooling plate of DP structure, located at rear side of the rack, this action increased the surface heat dissipation. The test done, at final integration stage shows how temperature is stabilized, at 51ºC, after reaching 10hrs of continues working.

WORK TO DO

As a future work, a deep analysis on the feasibility of redundant system implementation in the low voltage power distribution system for JEM-EUSO has to be performed. The impact of such modifications in the entire system have to evaluated together with others topics like new component selection and losses by harness length and mass.

[1] Ley, W. Wittmann, K. Hallmann, W. Handbook of Space Technology. Wiley, 2009. p16, p26, p33-34, p246.
[2] Fortescue, P. Stark, J. Swinerd, G. Spacecraft Systems Engineering. Wiley Third edition, 2003. P1, p326.
[3] Mukund, R. Spacecraft Power Systems. CRC Press editorial, 2005. p7-11.
[4] http://www.cap-ny153.org/satellites.htm
[5] Nagle, H. T., Santiago, P., Miller, T. K., McAllister, D. F. and Mehrotra, R. Fault Tolerance for single events. J. Rad. Effects Res. Eng., 6, 2. 1989.
[6] Third Van Allen Radiation Belt Around Earth Modeled and Explained [online]. University of California, Los Angeles (UCLA) available in: http://guardianlv.com/2013/09/third-van-allen-radiation-belt-around-earth-modeled-and-explained/
[7] Solar Storm Potential To Wreck Havoc On Grid Says, NASA [online]. Available in: http://www.ufo-blogger.com/2012/07/solar-storm-potential-to-wreck-havoc-on.html
[8] Ozkaya, H. Akkus, E. Karagoz, F.E. Next Generation Power Distribution Module Featuring UYGAR. Recent Advanced in Space Technologies (RAST), 2013 6th International Conference on, pp. 613-618.
[9] Zhifei, W. Zheng, Y. Salvignol, J. Tsinghua-1 Micro-Satellite Power System Architecture and Design. Published in Tsinghua Science and Tecnology, Oct. 2001. TUP publisher, Vol. 6, Issue 4, pp.289-293.
[10] Van Der Zel, V. Blewett, M.J. Clark, C.S. Hamill, D.C. Three Generations of DC Power Systems for Experimental Small Satellites. In Applied Power Electronics Conference and Exposition, San Jose CA, USA, March 1996. Vol. 2, pp. 664-670.
[11] Christopher, P. Winter and Vincent, L. Electrical Power System Trade Analyses for Space Surveillance Satellites. In Applied Power Electronics Conference and Exposition, San Jose CA, USA, March 1996. Vol. 2, pp. 664-670.
[12] Maskell A, C. Electrical Power on a 30kW Space Based Radar Satellites. Aerospace and Electronic Systems Magazine, IEEE 1992. Vol. 7, Issue 1, pp. 46-50.
[13] A. Capel, D. O'Sullivan, and J-C. Marpinard, "High-Power Conditioning for Space Applications". Proc. IEEE, Vol. 76, No. 4, April 1988.
[14] Denney, J. Keys, P.E. Earth Observing System (EOS) TERRA Spacecraft 120 Volts Power Subsystem. Requirements, Development, and Implementation. Energy Conversion Engineering Conference and Exhibit, 2000. (IECEC) 35th Intersociety. Volume 1, pages: 197-206.
[15] Dewald, D. B. Power Distribution and Conditioning for a Small Student Satellite: design of the NUTS backplane & EPS module. Master of Science in Engineering Cybernetics. Norwegian University of Science and Technology, Department of Engineering Cybernetics. June, 2011.
[16] D. Rusta. Battery interface design and sizing. Proceedings of Annual Battery Conference on Applications and Advances, California State University, Long Beach, Jan. 1986.
[17] P. Perol, Written communication, European Space Agency, to S. Krauthamer, Jet Propulsion Laboratory, California Institute of Technology, Pasadena.
[18] S. Peck, R. T. Callen, P. Pierce, and T. Wylie. STC-DBS electrical power subsystem. Proceedings at 19th IECEC. Vol. 1. 1984, pp. 428-441.
[19] Krauthamer, S. Gangal, M. Das, R. State of the Art of DC Components for Secondary Power Distribution of Space Station Freedom. Power Electronics, IEEE Transactions on, 1991. Vol. 6, Issue 3, pp.548-561.
[20] National Space Development Agency of Japan (NASDA), JEMS Power Systems Study, Space Station internal communication, Apr. 1988.
[21] SAE-AE7 Proceedings, Aeroelectronics 2000 Annual Meeting, Phoenix, AZ. April 20, 1988.
[22] Architectural Control Document, Electric Power System, Space Station Program Office Draft-SSP 30263, Rev. C3, Feb. 17. 1989.

[23] A. Capel and D. O'Sullivan. Influence on the Bus Regulation on Telecommunication Spacecraft Power System and Distribution. Presented at the IEEE Power Electronics Specialists Conference. Toulouse, France, June 24-28, 1985.
[24] E. Gholdston, ACD Star Architecture, Rocketdyne Doc. EG-890212, Feb. 14, 1989.
[25] Youhao, X. Jain, P.K. Distributed Point-of-Use Power Supply Architectures. The 4th International of Power Electronics and Motion Control Conference, 2004. Vol. 3, pp. 1149-1151.
[26] Tabisz, W.A. Jovanovic, M.M. Lee, F.C. Present and Future of Distributed Power Systems. Conference Proceedings of Applied Power Electronics Conference and Exposition, 1992. Seventh Annual, pp. 11-18.
[27] Marchetti, R. Power Systems Architectures What's in? What's out? Battery Power Products& Technology magazine. Vicor Corporation, 2003.
[28] Lindman, P. and Thorsell, L. Applying Distributed Power Modules in Telecom Systems. IEEE Transactions on Power Electronics, 1996. Vol. 11, Issue 2 pp. 365-373.
[29] Zhang, M.T. Jovanovich, M. M. Lee, F.C. Design Considerations for Low-voltage on-board dc/dc Modules for Next Generation Data Processing Circuits. Transactions on Power Electronics. IEEE. Vol. 11, Issue. 2, pp. 328-337.
[30] Xi, Y. Jain, P.K. Distributed OB Power Supply Architectures for Electronic Cards Employing High-speed LV Semiconductor Circuits. IEEE 35th Annual Power Electronic Specialists Conference, 2004. Vol. 6, pp. 4333-4339.
[31] Factorized Power Architecture (FPA) and V*I Chips. Vicorpower.com FPA White paper. May, 2007.
[32] Salato, M. Datacenter Power Architecture: IBA versus FPA. IEEE 33rd International Telecommunications Energy Conference (INTELEC), 2011. VICOR Company. Andover, MA-USA, pp. 1-4.
[33] Caballero, R. D'Olivo, J.C. Medina-Tanco, G. Nellen, L. Sánchez, F. Valdés-Galicia, J.: Instrument Overview of the JEM-EUSO mission. Proceedings of the 30th International Cosmic Ray Conference Mérida, Mexico 2008. Vol. 5(HE part 2), pages 1070-1080.
[34] JEM-ESUO Collaboration. "JEM-EUSO Report on Phase A study (purple book)". December 2010.
[35] JEM-EUSO Instrument Overview official website in: http://jemeuso.riken.jp/en/about10.html
[36] International Space Station image by the website Illustrate and credits by NASA available in: http://www.nasa.gov/mission_pages/station/main/onthestation/facts_and_figures.html#.U5nhLSjab-I
[37] ISS Utilization: JEM/kibo-EF. Available in: http://directory.eoportal.org/web/eoportal/satellite-missions/i/iss-jemef.
[38] The IMR ISS Reference Page. Available in: http://www.myspacemuseum.com/iss_ref1.htm
[39] Necessities for kibo Exposed Facility Utilization. http://iss.jaxa.jp/kibo/kibomefc/apbus_e.html
[40] Gietl, E. B. Gholdston, E. W. Cohen, F. Manners, B. A. Delventhal, R. A. The architecture of the Electrical Power System of the International Space Station and its Application as a Platform for Power Technology Development. 35th Intersociety Energy Conversion Engineering Conference and Exhibit, 2000. NASA Glen Research Center. Cleveland, OH. Vol. 2, pp. 855-864.
[41] From E.B. Gietl et al. NASA Report No. 210209, 2000.
[42] EUSO-Balloon collaboration. "EUSO-BALLOON Book". V1.0 LAL France 13/01/2012.
[43] Dagoret-Campagne, S. EUSO-Balloon project On the road toward CDR with CNES. JEM-EUSO Simulation and AMS meeting, ISDC Geneva. October 17th, 2012.
[44] Aera, J. Photo Detector Module Board Power. Version 3.1. November, 2013.
[45] Bayer, J. Status of the Cluster Control Board at 8th EUSO-Balloon Progress Meeting at Paris. Faculty of Science Institute for Astronomy & Astrophysics Kepler Center for Astro & Particle. October 12th, 2012.

[46] Osteria, G. Data Processor Status Hardware. EUSO- Balloon 8th progress meeting. INFN Sezione di Napoli. Paris, October 12. 2012.
[47] Kawasaki, K. Overview of JEM-EF on ISS. Space Environment Utilization Center. Tsukuba, Ibaraki, Japan.
[48] Parizot, E., Dagoret-Campagne, S., Von Ballmoos, P.: Organization Note of the EUSO-Balloon Instrument v1.0. EUSO-ON-INST-201-LAL (2012).
[49] Prieto, H. Dupieux, M. Roudil, G. Tsuno, K. Casolino, M. EUSO-Balloon Battery Power Pack. February, 2013.
[50] Auger Observatory: A new Astrophysics facility rises from the Pampa. Available in the website: http://www.auger.org/observatory/
[51] Rudolf, F. Modern Dictionary of Electronics. Seven edition. Newnes editorial, 1999, pp.831
[52] Brown, M. Power Supply Cookbook. Second edition. Newnes of Butterworth-Heinemann Editorial. 2001, pp. 14-45.
[53] Bussarakons, T. Thick film hybrid dc-dc converters are standard “bricks” for satellite power systems. Defense Electronics. June, 2006.
[54] Santos, M. Ribeiro, H. Martins, M. Guilherme, J. Switch Mode Power Supply Design Constraints for Space Applications. Proc. Conference on Telecommunications. Conf Tele, Peniche, Portugal. Vol. 1, pp. 157-160, Mayo, 2007.
[55] Masao, U. TDK EMC TECHNOLOGY: Basic Knowledge of EMC Standards. TDK Corporation Application Center, 2009-2010, pp. 15-16.
[56] Power Topics for Power Supply Users by TDK-Lambda. Guide to EMC Standards for Power Supplies. Monday, November 5, 2007. Available in http://power-topics.blogspot.mx/2007/11/guide-to-emc-standards-for-power.html
[57] Traco Power: Test Conditions of Environmental Tests. Created by Traco Electronic AG. Rev: 1.2. Date: April 16, 2010. Available in: www.tracopower.com/products/mil810.pdf
[58] SINPRO CO. LTD. “Introduction EMI – EMC” by SINPRO Electronics.
[59] Xiaogang, Jinjun, L. Lee, F. C. Impedance Specifications for Stable DC Distributed Power Systems. IEEE Transactions on Power Electronics, 2000. Vol. 17, Issue. 2, pp. 157-162.
[60] Schlecht, M. F. Input System Instability. Application Note PQ-00-05-1 Rev. 01-5/16/00.
[61] Kenneth L. Kaiser. Electromagnetic Compatibility Handbook. CRC PRESS. pp. 7-34, 2005.
[62] Henry W. Electromagnetic Compatibility Engineering. 2009 John Wiley & Sons Inc. Chapter 6.
[63] Montrose, M.EMC and the Printed Circuit Board. Design, Theory, and Layout Made Simple. IEEE Press Series on Electronics Technology. Chapter tree. 1999, New York.
[64] Joffe, B. Lock, K. Grounds for Grounding. IEEE press, John Wiley & Sons Inc. 2010.
[65] A Generic Standard on Printed Board Design Developed by IPC. Association Connecting Electronics Industries, IPC2221. Table 6-1. May, 2003.
[66] Carter, B. Circuit Board Layout Techniques by Texas Instruments. Excerpted from Op Amps for everyone, Chapter 17. Literature number SLOD006A, 2008.
[67] Calculation of PCB trace width based on IPC-2152 available in: http://www.smps.us/pcb-calculator.html
[68] Davis-Marsh, M. Thermal Design by Insight, Not Hindsight. Application Report AN-2020. April, 2010. Revised June 2011. Texas instruments.
[69] Seshasayee, N. Understanding Thermal Dissipation and Design of a Heatsink. Application Report SLVA462. May, 2011. Texas Instruments.
[70] Garrigós, A. Blanes, J.M. Power MOSFET is core of regulated-dc electronic load. University Miguel Hernández, Electronic Technology Division, Elche, Spain. Design Ideas edited by Brad Thompson.