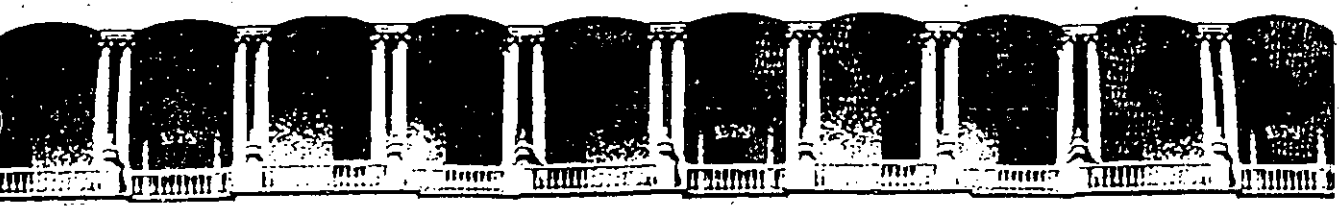

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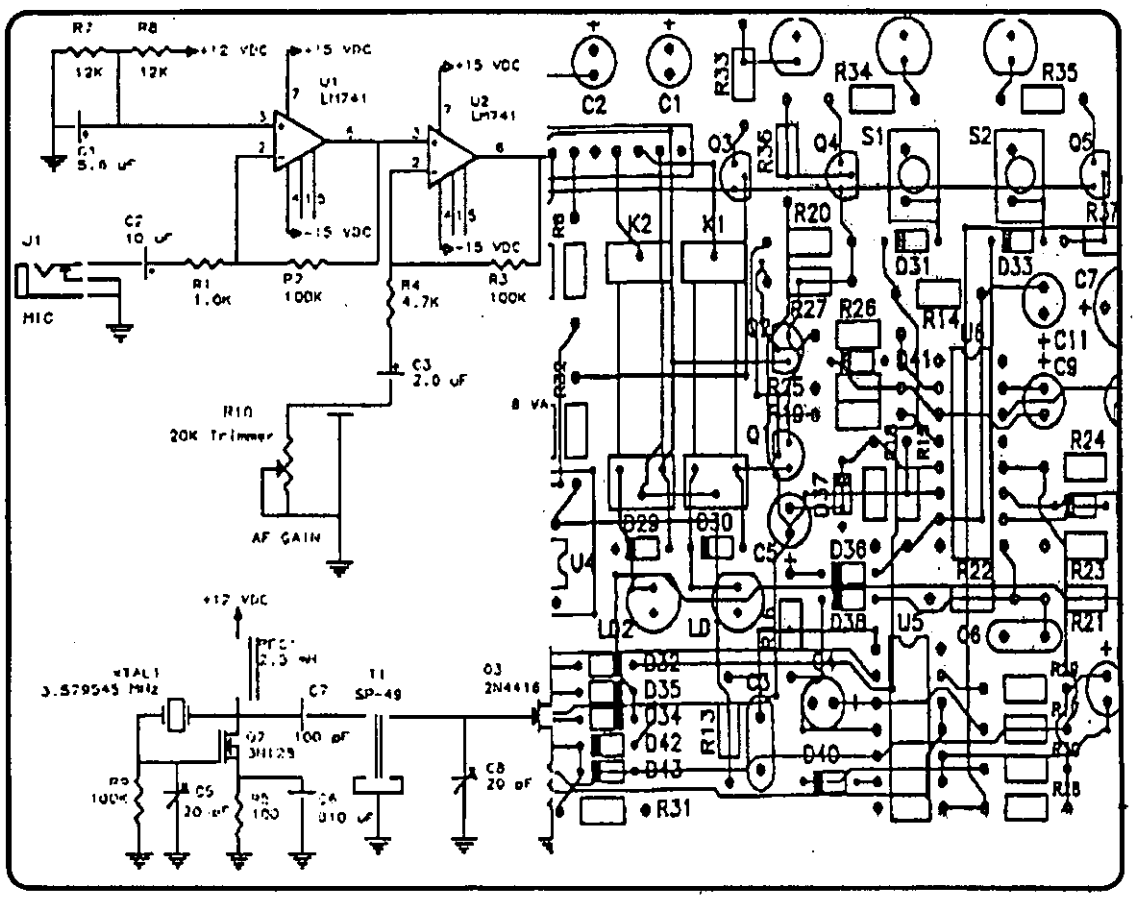
CAD



CIRCUITOS IMPRESOS

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OBJETIVOS

I) Proporcionar los elementos necesarios para diseñar un Circuito Impreso empleando como herramientas los sistemas **OrCAD** y **Tango-Plus.**

II) Proporcionar las bases para lograr la interfase entre Software para Dibujo **(AutoCAD),** y el procesador de texto **(Word 5.0)** a partir de la información proporcionada por **OrCAD** y **Tango-Plus.**

INTRODUCCION

Algunos de los sistemas de computación más avanzados que se emplean hoy en día, se diseñan contemplando la generación de despliegues gráficos, reconociéndose así el valor de una imagen como un medio eficaz de comunicación.

Prácticamente, no existe en la actualidad ningún área en la cual no se pueda utilizar la graficación con alguna ventaja; si, se encuentran gráficas en la mayoría de las aplicaciones en ciencia e ingeniería se basaron en equipos costosos y complicados, lo cual se ha superado debido a los adelantos registrados en computación permitiendo así acceder a la graficación como una herramienta útil y práctica a bajo costo.

Durante las fases de evolución del **CAD/CAM** podemos identificar a finales de la década de los 70's, la integración de la graficación por computadora al proceso de diseño, originando el crecimiento de la tecnología CAD -*Computer-Aided Design*- o *Diseño Asistido por Computadora*. Esta tecnología ofrece poderosas herramientas para el diseño en ingeniería, pemitiendo, entre otras cosas, agilizar el proceso de conceptualización, modelado, análisis y documentación de un producto con las etapas respectivas de retroalimentación, formando así, un ambiente de control de ciclo cerrado que contrasta con los mecanismos tradicionales de diseño.

La influencia de la tecnología CAD ha alcanzado las áreas de eléctrica y electrónica, con ejemplos como el diseño de circuitos electrónicos empleando sistemas interactivos basados en íconos gráficos para la representación de los diferentes componentes, con lo cual un diseñador puede construir un circuito, agregando compoentes en forma sucesiva extraidos de una Base de Dato. Además, el despliegue gráfico puede emplearse para comparar circuitos equivalentes con la finalidad de minimizar el número de componentes o bien, para llevar a cabo una mayor integración.

INTRODUCCION AL DISEÑO ASISTIDO POR COMPUTADORA

El Diseño Electrónico Asistido por Computadora (**DEAC** o su equivalente anglosajón de **CAE**) podemos considerarlo como una rama específica del **CAD/CAM** de tipo general.

Las principales aplicaciones del CAD/CAM se dan en dos campos de acción principalmente: **EL MECANICO Y EL ELECTRONICO**, dominando el primero con un 50% el mercado, mientras que el diseño electrónico alcanza tan solo el 19%, (según datos referidos al 1988).

El mercado de CAD electrónico, conocido como E.D.A. (Electronic Design Automation) ha experimentado, a lo largo de 1989, una serie de uniones, fusiones y alianzas entre empresas del sector que posibilitan la oferta de una serie de productos capaces de funcionar en entornos más amplios.

• EVOLUCION DE LAS COMPUTADORAS PERSONALES Y WORKSTATION

A principios de los 70's, surgen a partir de las necesidades de fabricantes de electrónica ó mécanicos, las **herramientas CAD**, las cuales han experimentado, evidentemente, grandes cambios de acuerdo con la tecnología.

Durante esta década se empleaban las minicomputadoras a las cuales se conectaban terminales que servian a programas funcionando en "Batch". En 1971, INTEL introduce el primer micro-procesador, el 4004 y en 1974 presentaba el 8080, por otra parte, MOTOROLA presentaba el X6800.

A principios de los 80's APOLLO crea la estación de trabajo (WorkStations, con el un concepto novedoso de potentes gráficos y red local produciéndose el cambio de **CAD** a **CAE** (Ingeniería Asistida por Computadora), donde el software desarrollado permitía al ingeniero Concebir, Diseñar, Simular, Modificar, Verificar y Documentar un circuito en una placa de circuito impreso, desde una potente máquina colocada en su mesa de trabajo.

Por otra parte, a finales de los 80's, surgen las tecnologías de integración **RISC Y CISC** poniendo a disposición del fabricante de software máquinas sin limitaciones tecnológicas, capaces de desarrollar aplicaciones más complejas, de tal manera que las actuales PC's equipadas con 80386 o 80486, se comparan tanto en prestaciones de la CPU como en precio con las actuales WoskStation, dicho término se encuentra ligado indisolublemente cada vez que se habla de **CAD/ CAM/CAE/CIM.**

TIPOS DE MAQUINAS	
NIVEL TECNOLOGICO **Características**	**NIVEL DE APLICACION** **Características**
* Los estándares que imperan en la PC son la compatibilidad, tanto en Hardware como en software, mientras que en las estaciones de trabajo se impone el UNIX en cuanto a Sistema Operativo, el MOTIF en cuanto a interfase de usuario, el OSI en comunicaciones y el PHIGS en gráficos. * En arquitectura, la PC comienza con 8 bits y crece hasta 32 bits, prevaleciendo en la actualidad los equipos con CPU de 16 bits, mientras que en las WorkStation, la mayoria son de 32 bits y algunas de 64 bits. * Las ventajas de un WorkStation suelen estar siempre por encima de las PC, aunque el auge experimentado por las máquinas con 386 y 486 ha igualado el nivel de prestaciones. Entre las ventajas que han mejorado las estaciones de trabajo respecto a las PC's son algunas de las siguientes: mayor definición a nivel de gráficos, lentitud de visualización, limitado margen de direccionamiento de la memoria, baja potencia de cálculo de la CPU y bajo nivel de conectividad.	* La PC se encuentra orientada fundamentalmente a manejar textos y números, mientras que una WorkStation está orientada a manejar gráficos. * La PC funciona "normalmente" en un entorno monousuario tratando de incrementar la productividad del individuo mientras que el entorno de trabajo de una WorkStation es por lo general, multiusuario.

EVOLUCION A MEDIANO PLAZO EN CUANTO A NIVEL TECNOLOGICO Y NIVEL DE APLICACION.

	ARQUITECTURA	GRAFICOS	SISTEMAS OPERATIVOS
PC	Tienden hacia el nuevo bus estándar EISA (MicroChanel de IBM) y CPU 80486.	Aparecen los primeros sistemas en 3D así como sistemas capaces de manejar más de 100000 vectores por seg. en 2D.	Se estandariza tantoUNIX como 0S/2 en los dos equipo mientras que en interfases de usuario, vemos como el MOTIF empieza a incorporarse al mundode las PC a través de UNIX.
WORKSTATION	Tienden a una mejora en los chips, así como la ejecución de multiples instrucciones por cada ciclo de reloj.	Incrementa sus ventajas en 3D en tiempo real con capacidades como fotorealismo.	

- **JUSTIFICACION Y NECESIDAD DEL CAE.**

En la actualidad los objetivos básicos de toda empresa en el entorno económico consisten en incrementar la **PRODUCTIVIDAD** y mejorar la **COMPETITIVIDAD**. Para ello, es necesario reducir los costos involucrados en la fase de desarrollo del producto, el tiempo empleado desde la especificación hasta la puesta en el mercado del producto; así como incrementar la **CALIDAD** del producto..

En este tipo de técnicas es donde el **CAD/CAM/CAE** ha puesto de relieve la importancia de automatizar informáticamente cualquier proceso industrial desde el diseño hasta la manufactura.

Dicha información incide de forma directa sobre dicho proceso de varias formas:

* Reducción de tiempos y sencillez en la etapa de diseño.

* Seguridad de un correcto funcionamiento ya que se ha simulado el prototipo sin necesidad de elaborarlo.

* Fácil integración sin problemas adicionales, dentro de un proceso en serie para su manufactura.

* Obtención de un producto económico, de óptima calidad y en el menor tiempo posible.

El proceso típico de fabricación de un determinado producto electrónico podemos sintetizarlo en las siguientes fases:

* Construcción del Prototipo
* Pruebas y Puestas a Punto del Prototipo
* Elaboración en Serie del Producto Final

• EVOLUCION DEL CAE.

Los primeros sistemas de diseño surgieron como réplica de los procesos tradicionales, con la ventaja de la facilidad de uso, edición y rápidez.

Conforme el hardware evoluciona y disminuyen los costos del equipo, los sistemas son más rápidos y las bases de datos de mayores dimensiones, fue apareciendo un fenómeno de insatisfacción en los usuarios: Un buen programa de dibujo, no bastaba; era necesario un sistema que diseñará el producto desde el principio (*Diagrama Esquemático*) hasta el final (*Placa de Circuito Impreso Terminado*) siguiendo **Reglas de Diseño.**

Como sonsecuencia de estas necesidades surguieron los paquetes de **CAE**, cuyas reglas de diseño referidas al CAE electrónico, se mencionan a continuación:

* **Captura de Diseños Esquemáticos**
* **Diseño de Circuitos Analógicos y Digitales**
* **Simulación Lógicas y Analógicas de Dichos Circuitos**
* **Análisis Térmico**
* **Diseño de la Placa de Circuito Impreso (PCB)**
* **Proceso de Electromecánica.**

• VENTAJAS EN EL USO DE PAQUETES CAE

* **Facilidad y Comodidad en el Diseño**
* **Rápidez, Exactitud y Uniformidad en la Fabricación**
* **Alto Porcentaje de Exito**
* **Eliminación de la Necesidad de Prototipos**
* **Aumento de la Productividad**
* **Productos más Competitivos**

• PRESENTE Y FUTURO DEL MERCADO CAE

Se considerá hoy en día que más del 30% de los diseños industriales se realizan con herramientas CAE. Empero, debido a la mayor complejidad y competitividad del mercado, se prevee que antes del año 2000 el grado de utilización se aproximará al 80%.

Los costos asociados a la detección de errores en el desarrollo pueden representar hasta 1000 veces más si se detectan en una fase final del producto que si se realiza en las especificaciones.

El factor tiempo también repercute de forma prioritaria en el desarrollo de prototipos. Los circuitos son cada vez más complejos, desarrollando mayor número de funciones, por lo tanto, deben diseñarse en un menor plazo de tiempo. La competencia es cada día mayor y el tiempo de lanzamiento de un producto es primordial al momento de conseguir mayores beneficios.

- **CARACTERISTICAS**

Las características de cualquier software de CAE partiendo de la base del CAD, podemos enfocarla bajo dos aspectos:

* **Común**
* **Específico**

y en cada uno de estos aspectos, dos niveles:

* **Hardware**
* **Software**

Características comunes a cualquier paquete de CAD

- **HARDWARE:**

* Necesidades de tarjetas gráficas y monitores que presenten una resolución y color adecuados respectivamente EGA, VGA, SuperVGA.

* Velocidad de ejecución y presentación de gráficos, lo que nos obliga a trabajar con equipos AT como mínimo (80286 12MHz), y para gráficos muy densos, utilizar coprocesador matématico.

* Periféricos de E/S adecuados. Ratones y Tabletas digitalizadoras a la entrada, por otro lado graficadores e impresoras láser a la salida.

* Memoria RAM suficiente (640K mínimo) y disco duro (20 Mb. mínima).

- **SOFTWARE:**

* Herramientas gráficas adecuadas (Menús tipo persiana con selección de opciones mediante ratón, menús de íconos, procurando dejar el máximo espacio libre de pantalla).

* Niveles adecuados, tanto en lo referente a escalas como en lo referente a zoom

* Edición adecuada, tanto de texto (tamaño, tipo de letra, posición, etc.) como de gráficos (buena resolución, acorde con el hardware)

* Facilidad en la colocación, copia, borrado, y desplazamiento de objetos.

* Menús de Ayuda (On-Line) y de configuración lo más flexible posible (driver's de todo tipo) de forma que no exista restrinciones en el uso del equipos

* Libreria de objetos, lo más extensa posible.

* Creación de archivos que pueden ser exportados o importados por otros paquetes.

• CARACTERISTICAS ESPECIFICAS DE UN SISTEMA CAE

* Amplia biblioteca de componentes, lo más actualizada posible y con posibilidad de edición de componentes

* Recomposición automática de líneas de conexión

* Numeración automática de componentes

* Incorporación de uno o más verificadores de normas y reglas eléctricas

* Conversión de esquemas de versiones anteriores

* Simulación de los circuitos diseñados

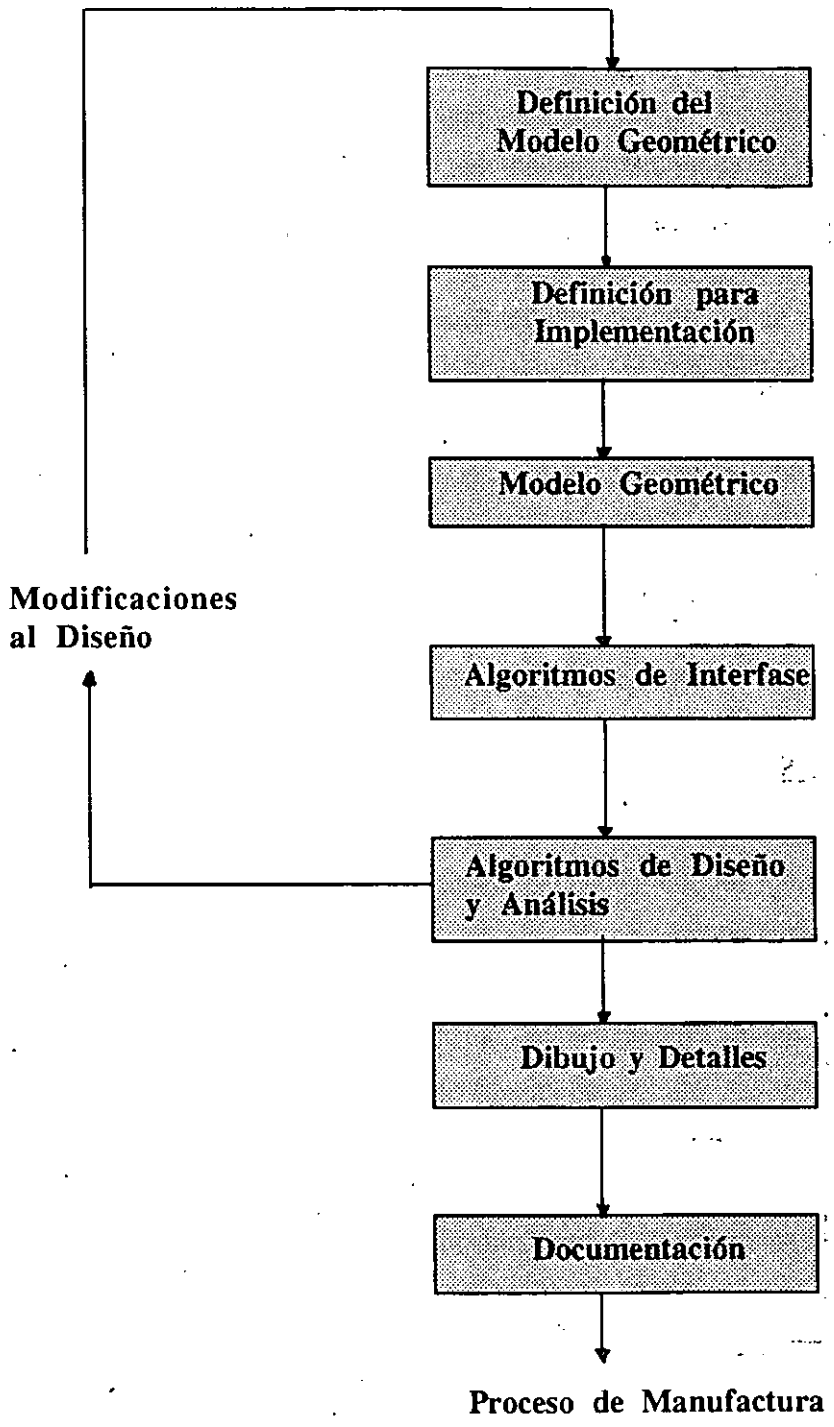
* Obtención del circuito impreso a partir del diagrama esquemático, mediante trazado manual o automático.

* Análisis térmico

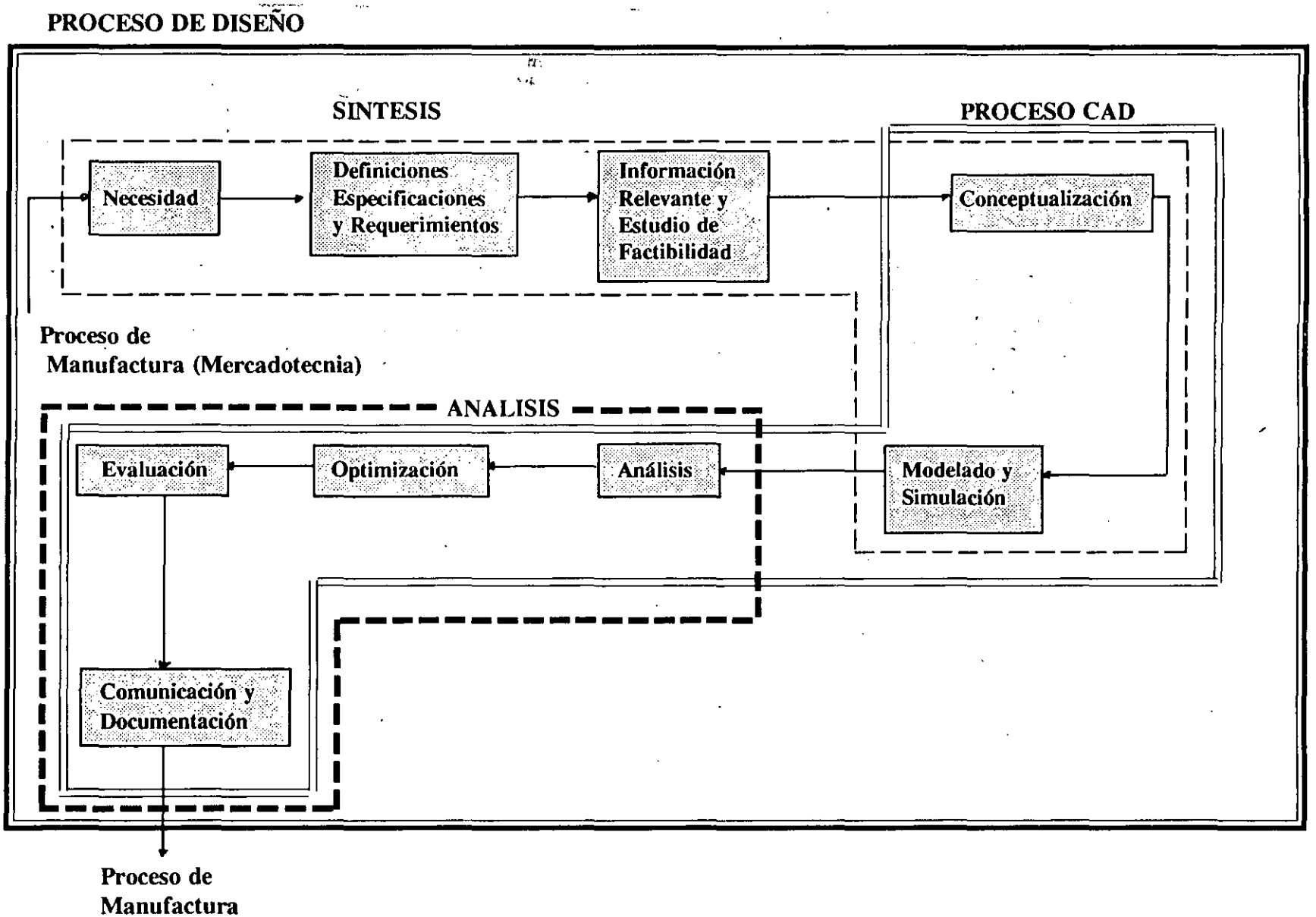
* Interfase para control numérico.

HERRAMIENTAS CAD REQUERIDAS POR EL PROCESO DE DISEÑO	
Fase de Diseño	**Herramientas CAD**
Conceptualización	*Técnicas de Modelado Geomeérico: Asistencia gráfica, Manipulaciones, Visualización.*
Modelado y Simulación	*Algunos como: Animación, Ensamblado, Paquetes Especiales para Modelado FEM.*
Análisis	*Software para análisis; Paquetes de Acuerdo a la Necesidad, Paquetes Comerciales*
Optimización	*Optimización Estructural*
Evaluación	*Dimensionamiento: Tolerancias, Especificaciones del Material, Control Numérico.*
Comunicación y Documentación	*Dibujo y Detalles; Ensamble de Piezas*

IMPLEMENTACION DE UN TIPICO PROCESO CAD DENTRO DE UN SISTEMA CAD/CAM



CICLO DE PRODUCCION TIPICO



DISEÑO ESQUEMATICO

(OrCAD v. 3.21)

OrCAD

Es una herramienta para diseño esquemático. Su Fácil uso de menús permite la creación, edición, manipulación, almacenamiento e impresión de esquemas electrónicos.

DRAFT: Es un editor esquemas de OrCAD, que permite crear, editar y salvar hojas esquemáticas. Además carga los manejadores de los dispositivos periféricos necesarios como: impresora, video, graficador; así como las librerias necesarias.

NOTA: **DRAFT/C** se emplea para configurar el sistema.

Dentro de las características de DRAFT se incluye:

- Acceso a más de 6000 elementos en las librerias
- Partes equivalentes a D'Morgan
- Crear líneas, buses, conectores, etiquetas, etc.
- Rotación y espejo de elementos
- Movimiento, copias y borrado de objetos o bloques de objetos
- Disponibilidad de una malla visible de puntos
- Paneo automático de la hoja de trabajo
- 5 niveles de acercamiento
- Niveles ilimitado de jerarquía
- Directorio de librerias
- Busqueda de cadenas
- Opción de orientación textos (verticales y horizontales)
- Soporta cinco tamaños de hojas de trabajo
- Etc.

LIBRERIAS

Incluye librerias muy extensas de las más comunes en la industria, tales como:

- TTL
- CMOS
- MEMORY
- ECL
- DISCRETAS
- ANALOGICAS
- MICROPROCESADORES
- DISPOSITIVOS PERIFERICOS
- ALTERA
- ETC.

UTILERIAS

TREELIST: Rastrea la organización jerárquica de las hojas y despliega su estructura, nombre de la hoja raíz así como las asociadas a ésta.

ANNOTATE: Actualiza automáticamente cualquier componente dentro de un diseño esquemático , numerándolo de forma correlativa, si éste se ha incluido al diseño esquemático. Actualizando en número de pines asociados a dicho componente.

PRINTALL: Imprime una hoja esquemática o grupo de hojas esquemáticas utilizando una impresora.

PLOTALL: Imprime una hoja esquemática o grupo de hojas esquemáticas utilizando un graficador.

PARTLIST: Reporta todas los elementos utilizados en el diseño esquemático o grupo de hojas esquemáticas (diseño jerárquico).

ERC: Lleva a cabo una verificación de reglas eléctricas comunes, para advertir si existe algún error como, p. ej. entradas sin señal, pines desconectados, etc.

NETLIST: Genera un archivo (NETLIST) adecuado para ser capturado por un programa de colocación de componentes (PCB), en diferentes formatos, empleados por programas de PCB de los más usuales.

BACKANNO: Actualiza las referencias correspondientes a componentes que han sido agregados o modificados dentro de un diseño esquemático después de la ejecución de **Annotate**

CROSSREF: Muestrea cualquier diseño esquemático, recopilando información sobre los componentes empleados, y crea un archivo de referencia que contiene la localización de cada componente.

CLEANUP: Verifica las conexiones, buses, uniones, etiquetas y cualquier objeto, mostrando mensajes oportunos cuando detecta algún elemento gráfico duplicado, borrandolo.

EXTRACT: Crea archivos fuente, para ser utilizados por el módulo de PLD´S a partir de archivos creados con SDT.

FLDATTRB: Modifica los atributos, (referencia, valor y campos) de los componentes que integran un diagrama esquemático, ya sea de bloques, jerárquico o simple, haciendo que estos sean visibles o invisibles.

FLDSTUFF: Modifica los atributos (*referencia y campos*) de aquellos componentes que han sido definidos a través de un archivo tipo texto y que previamente han sido combinados mediante **KEY FIELD.**

LIBARCH: Permite crear una librería fuente a partir de sólo los componentes empleados en un diseño esquemático..

SIMPLE: Convierte diseños jerárquicos complejos en jerarquías simples.

XFEROVL: Transfiere información de configuración desde una versión a otra del archivo ORCADSDT.OVL. Esto sólo es posible con versiones de OrCAD/SDT III superiores a la 3.12.

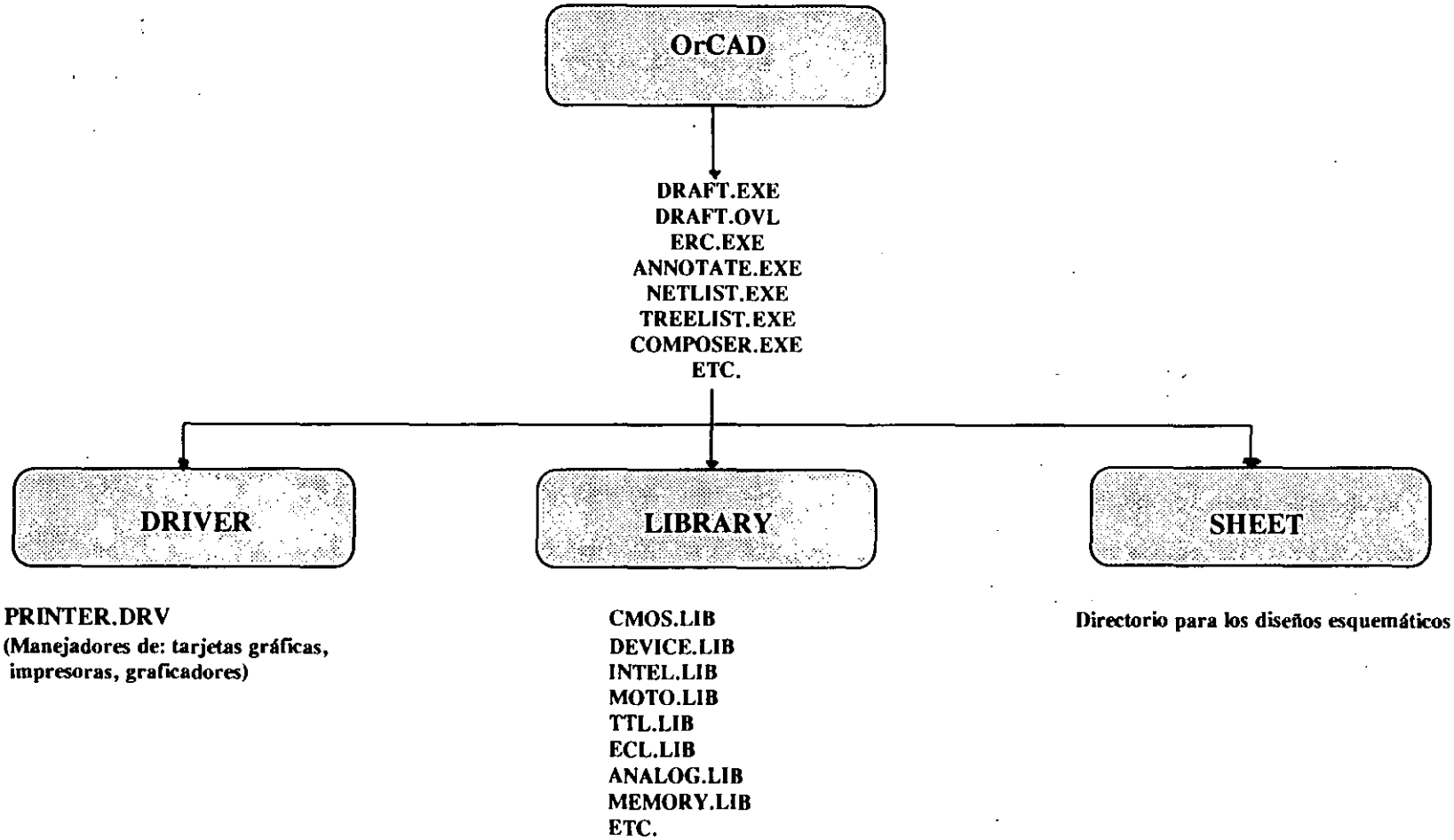
DECOMP: Esta utileria, es un decompilador de librerias de OrCAD, (archivos con extensión .LIB) a librerias en archivos fuentes. Los archivos fuente se pueden editar usando un editor de textos. De esta manera se pueden agregar o modificar elementos de las librerias.

COMPOSER: Es un compilador de libreria; se emplea para convertir la libreria de archivo fuente (formato ASCII) en libreria de archivo objeto para ser utilizada por DRAFT.

REQUERIMIENTOS DE HARDWARE

A continuación se detalla un configuración mínima para que el sistema funcione con un rendimiento adecuado:

* Una computadora PC/XT o AT ó compatibles.
* Coprocesador matemático opcional.
* 640 Kbytes de RAM.
* Sistema Operativo MS-DOS mayor a ver. 2.0.
* Disco duro de 20 Mbytes mínimo de capacidad.
* Tarjeta gráfica recomendable: EGA color.
* Uno o dos puertos serie (para ratón y plotter).
* Un puerto paralelo.
* Ratón.
* Graficador HP o compatibles.



CONFIGURACION RECOMENDADA PARA DISCO DURO.

6.9 PLOTALL

Purpose:

Plots a group of schematic sheets which may be a hierarchy, flat file, one sheet file structure, or an annotation file. As an option, grid references may be specified.

Format: PLOTALL *source* [*destination*] [/A][/C][/E][/F][/G][/O][/Q]

Remarks:

The *source* may be either the root sheet name of a hierarchical file structure, the name of a text file in a flat file structure, or the file name of a one sheet file structure.

If the *source* is the name of a text file in a flat file structure, the /F switch must be included. If the *source* is the file name of a one sheet file structure, the /O switch must be included. If the source is the annotation file created by the ANNOTATE program, then the /A switch must be included on the invocation line.

The *destination* is any valid DOS path name and is where the output of the program is to be placed. If a *destination* is not specified, the output of the PLOTALLprogram is directed to the serial channel specified in the plotter configuration (refer to Section 2 for configuration information).

The /A switch causes the PLOTALL program to read the source path as an annotation file.

The /C switch causes the configuration menu to be invoked. This allows the OrCAD/SDT environment to be modified.

The /E switch causes the utility program to display the message "Type Any Key To Continue", enabling the system to pause for you to remove the DRIVER/LIBRARY disk in drive B and insert the

SHEET disk. This switch is used only on systems with two floppy disk drives.

The /F switch causes the PLOTALL program to read the source as a text file, for flat file structure applications.

The /G switch causes GRID REFERENCES to be included in the sheet when plotting.

The /O switch causes the file name of the source to be read as a one sheet file structure.

The /Q switch causes the PLOTALL program to run "quietly". This means that only the invocation messages and error messages if any, are displayed. If this switch is not specified, the program will display intermediate tracking activity.

6.9.1 Invocation Examples Using Hierarchical Structured Files

1. To plot sheets in a hierarchical schematic:

   PLOTALL *root.sch*

   Where *root.sch* is the path and name of the root sheet in the hierarchy.

2. To plot a sub-sheet in a hierarchical schematic:

   PLOTALL *subsheet.sch* /O

Where *subsheet.sch* is the path and name of the sub-sheet in the hierarchy, /O signifies that the *subsheet.sch* file name is a single sheet.

6.9.2 Invocation Examples Using Flat File Structures

1. To plot a flat file structure containing multiple sheets:

PLOTALL *flatfile.txt* /F

Where *flatfile.txt* is a text file containing a list of schematic file names to be plotted; /F is used to signify that *flatfile.txt* is a text file.

2. To plot one sheet in a flat file structure:

   PLOTALL *sheetname.sch* /O

   Where *sheetname.sch* is the name of the single sheet in the flat file structure, /O is used to signify that *sheetname.sch* is a single sheet schematic.

6.9.3 Invocation Examples Using A One Sheet File Structure

1. To plot a single sheet schematic:

   PLOTALL *sheetname.sch* /O

   Where *sheetname.sch* is the name of the single sheet schematic, /O is used to signify that *sheetname.sch* is a single sheet schematic.

6.9.4 Invocation Example - Directing The Output To A File

1. To direct the output of the PLOTALL program to a file:

   PLOTALL *sheetname.sch whatfile* /O

   Where *sheetname.sch* is the name of the single sheet schematic, *whatfile* is the path and file name to place the PLOTALL information, and /O is used to signify that *sheetname.sch* is a single sheet schematic.

NOTE

The file *whatfile* may be sent to a plotter using the DOS MODE and COPY commands. For example, if your plotter is connected to serial channel 1, enter the following at the DOS prompt:

COPY *whatfile* COM1:

For additional information on the MODE and COPY commands, refer to your DOS Users Manual.

6.9.5 Plotting Schematics Based on Annotation Files

1. To plot schematics based on the annotation file information:

   PLOTALL *annotation.out* /A

   Where *annotation.out* is the output from the ANNOTATE program, /A causes the PLOTALL program to read *annotation.out* as an annotation file.

6.9.6 Setting Up The Plotter Configuration

To setup the plotter configuration, go to the DRAFT configuration menu by entering the following from the DOS command line:

PLOTALL /C

Press the <P> and <L> keys to configure the plotter drivers, serial channel, baud rates, parity and word length.

To configure OrCAD/SDT for the plotter driver, select the letter that corresponds to the plotter driver that you are using at the "Enter Letter to Select the Plotter to be used->" prompt. If your plotter name does not appear, press <S> for Special.

When selected, the plotter driver name only appears on the "CONFIGURATION OF OrCAD/SDT" menu.

To modify the serial channel, baud rate, parity, or word length configuration, press the colon <:> key at the "Enter Letter to Select the Plotter to be used->" prompt.

Enter a "1" for serial channel 1, or a "2" for serial channel 2 at the "Channel 1 or 2 ->" prompt.

After you select the serial channel, you may select the baud rate, parity, and word length that is required.

To modify the baud rate, enter the letter that corresponds to the baud rate you require at the "Baud Rate ->" prompt.

To modify the parity, enter the number that corresponds to the parity you require at the "Parity ->" prompt.

To modify the word length, enter the number that corresponds to the word length you require at the "Word Length ->" prompt.

When you return to the "CONFIGURATION OF OrCAD/SDT" menu, be sure to update the information by pressing the letter <U>.

Typical configuration for HP and HI plotters is as follows:

Baud Rate : 2400 or 9600
Parity : No Parity
Word Length: 8 bits

6.9.7 Plotter Cable Wiring Diagrams

The PLOTALL utility program uses BIOS to communicate to the serial port. It does not talk to the hardware directly. This is to insure compatibility to all PC's and compatibles.

For this reason, additional wires other than TXD and RXD must be connected to implement hardware handshake.

Figure 6-20 shows a wiring diagram that is required for connecting a PC/XT (25 pin connector) to a plotter. Figure 6-21 shows a wiring diagram that is required for connecting a PC AT (9 pin connector) to a plotter.

Since this cable connects the TXD and RXD lines, it also works with software that communicates to the hardware directly.

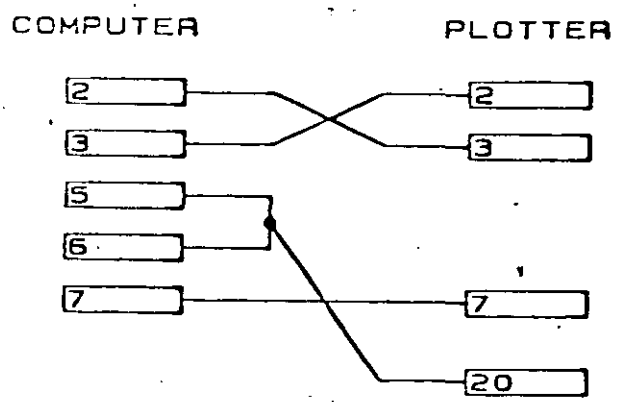


Figure 6-20. PC/XT 25-Pin Cable Wiring Diagram

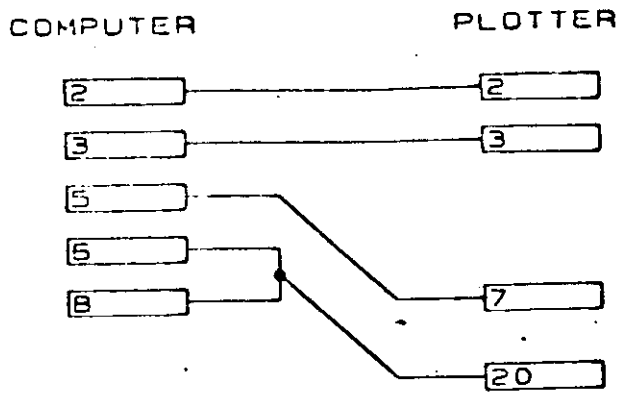


Figure 6-21. PC AT 9-Pin Cable Wiring Diagram

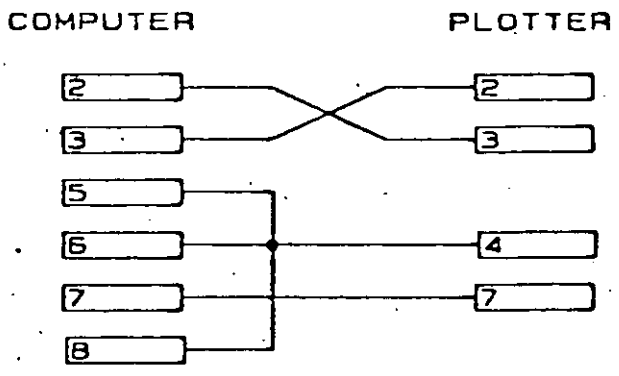


Figure 6-22. PC/XT 25-Pin Cable to IOline Plotter

6.9.8 Plotter Problems

Most plotter problems are typically a result of incorrectly wired plotter cables. If you have difficulty with your plotter, check the following items before procceding or calling OrCAD:

1. Wire the cable as shown in Figures 6-20, 6-21, and 6-22 above. If your plotter works with another software package, and does not work with OrCAD, the first item to check is the wiring of your cable. Chances are, the other CAD packages only require the TXD and RXD signal lines. OrCAD requires additional connections.

   The cable must be wired correctly as recommended!

2. Check for an open in the cable by performing a continuity check.

3. Read your plotter manual to be sure you understand how the plotter operates. Know how it is programmed for baud rate,parity, word length, and find out what these settings are.

4. Check to make sure that the plotter baud rate, parity, and word length settings correspond to the plotter configuration information.

   For HI plotters, if data and parity do not match, the message: "<<<error>>> Unable to read back from plotter"appears on the screen.

5. Use DOS to send a plot file to the plotter. This will be useful for isolating whether the problem is in the serial port hardware or the plotter hardware. To do this, first send the worksheet to a plot file as outlined below:

   PLOTALL *sheetname.sch whatfile* /O

   Where *sheetname.sch* is the name of the single sheet schematic, *whatfile* is the path and file name to place the PLOTALL information, and /O is used to signify that *sheetname.sch* is a single sheet schematic.

   Then, use the DOS MODE command to configure the serial channel as follows:

   MODE COM1:2400,N,8,1,P <ENTER>

This assumes that you are using serial channel 1 (COM1) and have your plotter set for 2400 baud. For more information on the MODE command, refer to your DOS users guide for Asynchronous Communications.

After the serial channel has been configured, send the plot file to the plotter using the DOS COPY command as follows:

COPY *whatfile* COM1: <ENTER>

Where *whatfile* is the name of the plot file.

If the plotter works, this indicates the problem may be in the plotter cable (incorrectly wired), or the hardware handshaking is incorrectly set (check PLOTALL configuration).

If the plotter does not work, this indicates that there is a hardware problem. Check the the following: serial card, incorrect serial channel configuration, plotter hardware, or a cable problem.

6. If yours is an IOline plotter, be sure you have PROM version 114 or greater.

6.9.9 Output Scaling

OrCAD does not control the scale of the plotter output. Output scaling is controlled entirely by your plotter. Plotter scaling is typically controlled by the size of the paper used, P1 and P2 point settings (HP plotters), rotation settings, and the default settings on the plotter.

If you change the size of the worksheets you are plotting, (plotting a C size, then a B size worksheet for example) always RESET the plotter when changing worksheet size. If you have further scaling questions, refer to your specific plotter manual.

6.9.10 Plotter Hints

When making a plot, use the proper pens and paper designed for the plotter. Plotter paper has a "memory" to it. If it hangs on the plotter bed for a period of time, it will stretch. This effects the registration of the plot. Plotter paper is also temperature sensitive. Be sure that the paper is at room temperature before plotting. The longer the drawing takes to plot, the more care must be exercised with the paper.

The configuration of the plotter includes the ability to change the velocity of the pens. When the pen can not draw at the speed the plotter is capable of moving, reduce the velocity. You will need to consult your plotter manual for the range to set the velocity. The velocity can be set only in whole number values.

When you make a plot with different pens, the plotter has a registration inaccuracy that must be considered. If you wish to have the highest quality plot, always use only one pen.

When you make a plot on a paper size that does not match the worksheet size, the plotter drivers will scale the drawing to fit the paper selected. We do not recommend making a plot more than one size off of the worksheet size since the width of the pen is fixed. For example, you can plot a C size worksheet on B, C, or D and it will work fine. If you plot an E worksheet on A paper, you will not be able to read the writing. If you plot an A worksheet on E size paper, the bit mapped devices will be "grainy".

When you are directed by the program to change paper or pens, always wait until the plotter has finished the present plotting activity. Before sending a plot directly to the plotter, be sure that the plotter is on line, the pen(s) are properly set up, and the paper size is correct. When you have a pen that must be manually changed, the PLOTALL program will pause and inform you of the objects to be plotted with the new pen.

6.9.11 HP Plotters

The HP plotter family has a facility to set the corner points of the plot and automatically scale the plot to be within these points. These points are called P1 and P2.

When you change the paper size, or at power up, these points are set to default values which depend on the size of the paper and the plotter's margin requirements. You may reset P1 and P2 to the outer most boundary of the paper and the plot will be slightly larger.

If you plot on paper that is not the same size as the worksheet, you will have to manually adjust the locations of P1 and P2 to correct for the aspect ratio.

6.9.12 HI Plotters

The HI plotter family does not automatically scale the drawing. If you direct the output of the PLOTALL program to a file you will be prompted, for each plot, for the paper size to use for the plot. The aspect ratio is corrected for both direct-to-plotter and re-directed-to-file plots.

The HI 40 Series defaults to 2400 baud, and the 50 Series defaults to 9600.

Always check to make sure that the plotter baud rate, and data bit settings correspond to the plotter configuration (refer to "Setting Up The Plotter Configuration" above).

If data and parity do not match, the message: "<<<error>>> Unable to read back from plotter" appears on the screen.

Be sure that the plotter is on-line before beginning a plot. The HI plotters do not have a means to set the velocity to the power-up default. If you change any of the velocity settings of the pens in the configuration, you will need to set them all. The velocity ranges can be found in the plotter operation manual for your specific plotter.

6.9.13 Suppressing the Title Block and Border

To suppress the title block and border of the worksheet, invoke the Configuration Menu by entering "DRAFT /C" from the DOS command line.

Press <C> <T> to obtain the "Color Table / Plotter Pen Table". At the "Command ->" prompt, press the <P> <M> keys. Then, press <9> <9> followed by the <ENTER> key. The plotter pen is now IGNORED for drawing the worksheet title block and border.

6.10 PRINTALL

Purpose:

Prints a group of schematic sheets which may be a hierarchy, flat file, one sheet file structure, or an annotation file. As options, grid references, scaled output, and wide paper can be specified.

Format:

PRINTALL *source* [*destination*] [/A][/C][/E][/F][/G][/O][/Q][/S][/W]

Remarks:

The *source* may be either the root sheet name of a hierarchical file structure, the name of a text file in a flat file structure, or the file name of a one sheet file structure.

If the *source* is the name of a text file in a flat file structure, the /F switch must be included. If the *source* is the file name of a one sheet file structure, the /O switch must be included. If the *source* is the annotation file created by the ANNOTATE program, then the /A switch must be included on the invocation line.

The *destination* is any valid DOS path name and is where the output of the program is to be placed. If a *destination* is not specified, the output of the PRINTALL program is directed to the printer PRN.

The /A switch causes the PRINTALL program to read the *source* path as an annotation file.

The /C switch causes the configuration menu to be invoked. This allows the OrCAD/SDT environment to be modified.

The /E switch causes the utility program to display the message "Type Any Key To Continue", enabling the system to pause for you to remove the DRIVER/LIBRARY disk in drive B and insert the

SHEET disk. This switch is used only on systems with two floppy disk drives.

The /F switch causes the PRINTALL program to read the *source* as a text file, for flat file structure applications.

The /G switch causes GRID REFERENCES to be included in the sheet printout.

The /O switch causes the file name of the *source* to be read as a one sheet file structure.

The /Q switch causes the PRINTALL program to run "quietly". This means that only the invocation messages and error messages if any, are displayed. If this switch is not specified, the program will display intermediate tracking activity.

The /S switch causes the PRINTALL program to generate scaled output. If this switch is not specified, then the printer will print the worksheet in compressed mode.

The /W switch causes the printing to formatted for wide paper. With this switch, the printing will be setup for 13" wide paper based on the parameters of the printer driver. If the /W switch is not present, then the printing will be formatted for 8" paper.

NOTE

Epson MX printers cannot print in compressed mode. Therefore, printer output will always be in scale mode even if you attempt to print compressed.

6.10.1 Invocation Examples Using Hierarchical Structured Files

1. To print sheets in a hierarchical schematic:

   PRINTALL *root.sch /S*

Where *root.sch* is the path and name of the root sheet in the hierarchy.

2. To print a sub-sheet in a hierarchical schematic:

   PRINTALL *subsheet.sch* /O /S

   Where *subsheet.sch* is the path and name of the sub-sheet in the hierarchy, /O signifies that the *subsheet.sch* file name is a single sheet.

6.10.2 Invocation Examples Using Flat File Structures

1. To print a flat file structure containing multiple sheets:

   PRINTALL *flatfile.txt* /F

   Where *flatfile.txt* is a text file containing a list of schematic file names to be printed, /F is used to signify that *flatfile.txt* is a text file.

2. To print one sheet in a flat file structure:

   PRINTALL *sheetname.sch* /O

   Where *sheetname.sch* is the name of the single sheet in the flat file structure, /O is used to signify that *sheetname.sch* is a single sheet schematic.

6.10.3 Invocation Examples Using A One Sheet File Structure

1. To print a single sheet schematic:

   PRINTALL *sheetname.sch* /O /S

Where *sheetname.sch* is the name of the single sheet schematic, /O is used to signify that *sheetname.sch* is a single sheet schematic.

2. To direct the output of the PRINTALL program to a file:

   PRINTALL *sheetname.sch whatfile* /O

   Where *sheetname.sch* is the name of the single sheet schematic, *whatfile* is the path and file name to place the PRINTALL information, and /O is used to signify that *sheetname.sch* is a single sheet schematic.

NOTE

Since *whatfile* is a binary print file, it will consume an extensive amount of disk space.

The file *whatfile* may be sent to a printer using the DOS COPY Command. For example, enter the following at the DOS prompt:

COPY *whatfile prn*: /b

For additional information on the COPY Command, refer to your DOS Users Manual.

6.10.4 Printing Schematics Based on Annotation Files

1. To print schematics based on the annotation file information:

   PRINTALL *annotation.out* /A /S

   Where *annotation.out* is the output from the ANNOTATE program, /A causes the PRINTALL program to read *annotation.out* as an annotation file.

7. LIBRARIES

This section explains how to create your own "custom" part libraries for use with OrCAD/SDT. Section 7 describes the COMPOSER and DECOMP utilities. Then, it describes the steps you would go through to create a custom library and provides numerous examples. The section then presents a formal description of OrCAD's Symbol Description Language and concludes with examples of complete library source files.

7.1 An Overview of the Library Development Process

To create a custom library, you need a text editor and the COMPOSER utility. COMPOSER takes a library source file, which you created with the text editor, and produces a library data file, readable by DRAFT. You may also find the DECOMP utility useful. DECOMP takes a library data file and produces a library source file. You can think of DECOMP as the inverse of COMPOSER. Creating a custom library consists of the following three steps, as illustrated in Figure 7-1.

1. Create a library, text, or source file. The convention is to give the file a .SRC extension. The source file is an ASCII text file that contains instructions in OrCAD's Symbol Description Language.

   You can use any text editor. The only requirement is that it produce an ASCII file without any hidden formatting characters. For example, Wordstar in the non-document mode produces such an ASCII file.

2. Compose the source file using the COMPOSER utility. This is similar to a compilation; it produces another file, a data file readable by DRAFT. The convention is to give this data file a .LIB extension.

3. Reconfigure DRAFT to add the new library to the list of library files.

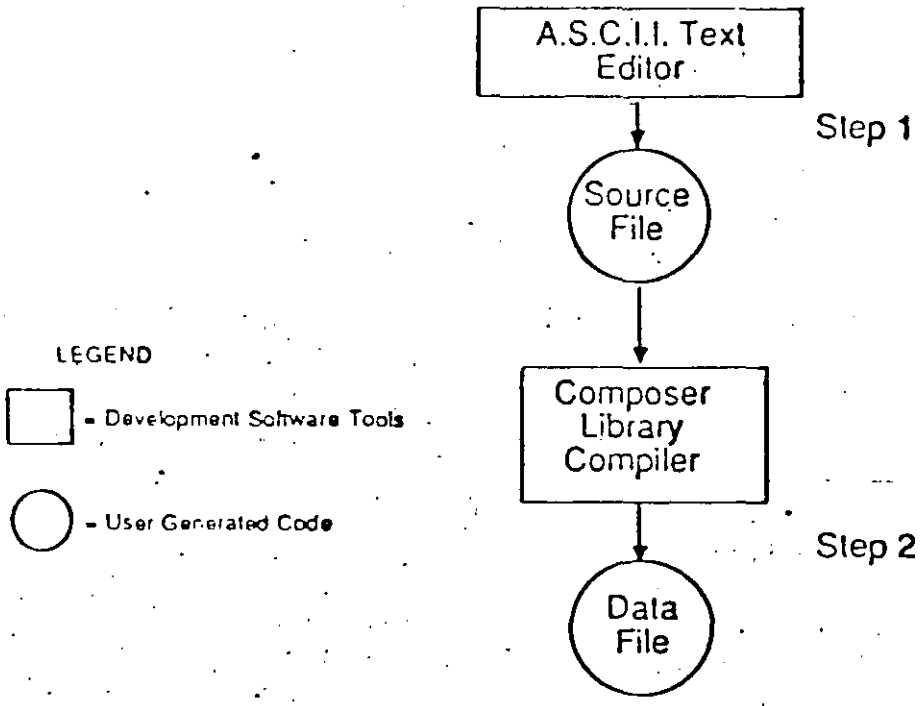


Figure 7-1: The Library Development Process

OrCAD Systems supplies a number of part libraries for use with DRAFT. Part of configuring DRAFT means choosing what libraries it will have access to. The libraries you choose at configuration time

are loaded into RAM when you invoke DRAFT. This eliminates disk searching and provides for quick part retrieval.

You can choose from OrCAD-supplied libraries as well as your own custom libraries to load into DRAFT. The custom libraries that you create will behave just like the OrCAD-supplied libraries.

OrCAD-supplied libraries are shipped as library data files. This is for your convenience (data files are ready to use) and also to save disk space. A library source file takes up much more disk space than its corresponding library data file. A source file can be four or five times as large as its data file.

By applying DECOMP to an OrCAD-supplied library, you can construct a source version of that library. This feature is useful if the library you want to create has parts similar, but not identical, to those in the OrCAD-supplied library. With a text editor, you can extract the similar parts and edit them. The supplied libraries also serve as an extensive list of examples. If, while creating your own library, you get stuck, you can always look inside a source version of a supplied library "to see how OrCAD did it."

Creating custom libraries is preferable to modifying OrCAD-supplied libraries. If you modify an existing library, you run the risk of future OrCAD updates negating your changes. It is not good practice to run DECOMP on an OrCAD-supplied library, edit the resulting source file, and then run COMPOSER and replace the original library.

You may have parts with the same name in different libraries. If you do and those libraries are selected, DRAFT searches through the libraries in the order you specify at configuration time.

7.2 The COMPOSER and DECOMP Utilities

The COMPOSER utility is called COMPOSER.EXE and the DECOMP utility is called DECOMP.EXE. Both files are found on the LIBRARY disk. To execute either utility, you must be at the DOS command level in the directory that contains the utility you want to execute.

7.2.1 Invoking COMPOSER

COMPOSER *source library* <ENTER>

where: *source* is the name of the ASCII text file that describes your custom parts using OrCAD's Symbol Description Language. The .SRC extension is a convention, not a requirement. *library* is the name of the resulting library file. If you give the name of an existing file, COMPOSER asks if you want to overwrite the existing file. You cannot append to an existing file. <ENTER> represents the ENTER key on your computer. DOS commands are executed when you type the ENTER.

Both *source* and *library* may be complete pathnames -- that is, if either is in a directory other than your current directory, you must specify the complete path. Here are two examples.

COMPOSER *custom.src custom.lib* <ENTER>

The files COMPOSER.EXE and *custom.src* are in the same directory, and this directory is your working directory. This example creates the file *custom.lib* in your working directory.

COMPOSER \orcad\library*custom.src* \orcad\library*custom.lib* <ENTER>

The file COMPOSER.EXE is in your working directory, which is not necessarily \orcad\library. This example creates the file *custom.lib* in the directory \orcad\library.

7.2.2 Invoking DECOMP

DECOMP *library source* <ENTER>

where: *library* is the name of an existing library file. The .LIB extension is a convention, not a requirement. *source* is the name of the resulting ASCII text file that describes the parts

in the specified library. Comments are included in the file for clarity. If you give the name of an existing file, DECOMP asks if you want to overwrite the existing file. You cannot append to an existing file. <ENTER> represents the ENTER key on your computer. DOS commands are executed when you type the ENTER.

As with COMPOSER, both *source* and *library* may be complete pathnames -- that is, if either is in a directory other than your current directory, you must specify the complete path.

Here are two examples.

DECOMP *custom.lib custom.src* <ENTER>

The files DECOMP.EXE and *custom.src* are in the same directory, and this directory is your working directory. This example creates the file *custom.src* in your working directory.

DECOMP \orcad\library*custom.lib* \orcad\library*custom.src* <ENTER>

The file DECOMP.EXE is in your working directory, which is not necessarily \orcad\library. This example creates the file *custom.src* in the directory \orcad\library.

Note that DECOMP does not return your source; it makes its own. For example, the comments in your original source are not reproduced. DECOMP adds its own comments. Also, DECOMP may rearrange the order of the part definitions. DECOMP lists parts in numeric order followed by parts in alphabetical order. For example, assume that you define two parts, one called resistor and one called 7400. You place resistor in your source file before 7400, run COMPOSER, then DECOMP to produce a new source file. Unlike your original source file, the new source file has 7400 listed before resistor.

7.3 Creating a Source File

A source file consists of a prefix definition followed by a series of part definitions. You can have only one prefix definition per library, and it occurs at the beginning of the library. There are two types of part definitions: block symbol definitions and bitmap symbol definitions. Comments are delimited with braces ({}).

Block symbol definitions represent parts that are either square or rectangular. These parts are typically memory chips, microprocessors, peripheral controllers, and many TTL and CMOS devices. Bitmap symbol definitions represent parts that are complicated to define graphically. Instead, you draw them on a bitmap. They include such parts as resistors, diodes, transistors, MOSFETs, relays, and many others.

Note that lines in a source file end with a <RETURN>. The source examples in this section do not show the <RETURN>.

7.3.1 The Prefix Definition

The prefix definition is delimited by the keywords, PREFIX and END. The initial delimiter is the keyword PREFIX all alone on a line. Subsequent lines contain the definition itself. The terminating delimiter is the keyword END all alone on a line.

All source files must begin with a prefix definition. If you decide your custom library doesn't need a prefix definition, you must still supply a null prefix. A null prefix consists only of the delimiting keywords. Here is how a null prefix definition looks.

```
PREFIX
END
```

On the other hand, you may find a prefix definition very useful. OrCAD specifically designed the prefix definition to handle the various TTL logic families. For example, the 74LS00, the 74S00, and the 74ALS00 have different prefixes (74LS, 74S, and 74ALS), but the same suffix (00). When you use a prefix definition, you reduce the

memory required to store multiple families of parts that have different prefixes, but the same suffix.

Here is an example of a prefix definition. The example comes from OrCAD System's TTL source library, TTL.LIB.

```
PREFIX
'74LS'    =  'LS'
'74S'     =  'S'
'74ALS'   =  'ALS'
'74AS'    =  'AS'
'74HCT'   =  'HCT'
'74HC'    =  'HC'
'74ACT'   =  'ACT'
'74AC'    =  'AC'
'74F'     =  'F'
'74'
END
```

DRAFT uses the prefix definition when you obtain a part with the Get command. Instead of entering the entire name of the part, you can enter just the suffix. DRAFT displays a pop-up menu that lists all the valid part names constructed by appending the suffix you provided with the prefixes in the prefix definition. For example, if TTL.LIB is one of your libraries and you enter the suffix 04, the pop-up menu lists the following parts.

```
74LS04
74S04
74ASL04
74AS04
74HCT04
74HC04
74F04
7404
```

A prefix definition is constructed as follows. First, enter the PREFIX keyword followed by a <RETURN>. Then, begin the first prefix string by entering a single quote ('). Type the prefix string. It consists of a string of printable ASCII characters no more than seven

characters long. DRAFT does not distinguish between upper- and lower-case. Close a prefix string with another single quote.

Then, enter a <SPACE> followed by an equal sign (=) followed by another <SPACE>. To improve readability, you can delimit the equal sign with any number of <SPACE>s or <TAB>s. Now enter the shorthand string. This is the part of the prefix string that varies. The shorthand string also consists of no more than seven printable ASCII characters. Then, enter a <RETURN> and type the next line. You can define a maximum of sixteen prefix strings.

The shorthand string enables you to bypass the pop-up prefix menu and still enter an abbreviated part name. For example, you can obtain the part 74HC04, by supplying the GET command with the abbreviated name HC04. This is possible because HC is a shorthand string for 74HC.

7.3.2 The Part Definition

The part definition defines the part's name, its size (in unit lengths on the screen and in tenths of an inch on the printed worksheet), the number of parts per package and the pin functions (input, output, open collector, etc.). There are two types of part definitions: block symbol definitions and bitmap definitions.

You do not have to group your block definitions and bitmap definitions together. For example, your source file may contain a block definition, followed by a bitmap definition, followed by another block definition.

Block and bitmap definitions follow much the same syntax. A bitmap definition looks like a block definition followed by a bitmap. When COMPOSER sees a bitmap, it uses that bitmap to represent the part, rather than defaulting to a square or rectangle.

A symbol definition has the following fields.

- One or more part name strings. A name is a printable ASCII string enclosed in single quotes. If you have more than one part name

string, delimit them with a <SPACE> or put them on separate lines. When obtaining a part, you can use any of your supplied names.

- An optional reference designator. The ANNOTATE utility automatically updates reference designators.

- The symbol size. Each unit represents a unit length on the screen and 0.1 inch on the printed worksheet. You give the X size first and then the Y size. On the same line you list the number of parts per package. If the part is a pin grid array, specify the keyword GRIDARRAY instead of the number of parts per package.

- The pin definition. Each pin is defined on a separate line. A pin definition consists of the following fields:

  - The pin position

  - The pin number or GRIDARRAY pin name

  - The optional DOT keyword (which places the inversion bubble at the pin position)

  - The optional CLK keyword (which places the clock symbol at the pin position)

  - The optional keyword SHORT (which places 0.1-inch leads at the pin position instead of the standard 0.3-inch leads). SHORT cannot be used with DOT or CLK

  - The pin function (IN, OUT, I/O, OC, PWR, PAS, HIZ)

  - The pin name string

- An optional bitmap. Use this if the symbol you want is not a square or rectangle.

- An optional conversion. This only has meaning if you've defined a bitmap. The most common use for converted bitmaps is to specify the DeMorgan equivalent of the defined part.

7.3.3 Block Symbol Definition

Illustrated below is an example of a block symbol definition. The example does not represent a real part, although it is similar to a JK flipflop. Figure 7-2 shows the symbol produced by this block definition.

```
'74EXAMP'
REFERENCE        'LATCH'
6      10   2
L1     3    11    SHORT  IN     'J'
L5     1    13    DOT CLK  IN   'CLK'
L9     2    12    SHORT  IN     'K'
B3     15   14    DOT  IN       'CL'
T3     4    10    DOT  IN       'P'
R1     6    7     OUT           'Q'
R9     5    9     OUT           'Q\'
T0     16   16    PWR           'VCC'
B0     8    8     PWR           'GND'
```

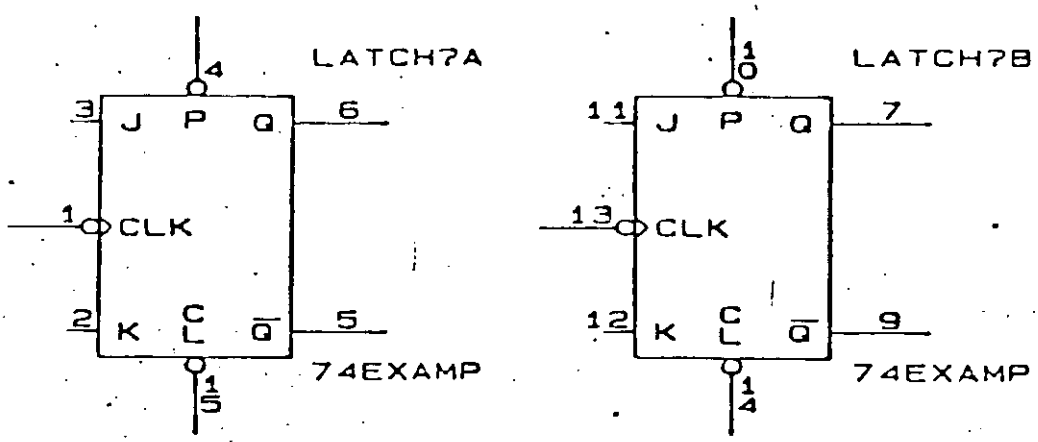


Figure 7-2: The Block Symbol for 74EXAMP

Part name string. The example has only one part name string, '74EXAMP'.

Reference designator. After the part name string comes the optional reference designator.

For this example, the reference designator would appear on the screen as LATCH?A. Note the question mark. When you run the ANNOTATE utility the question mark will be replaced with a number. For example, if the reference designator for a resistor were R? and there are 16 resistors in your design, ANNOTATE would change the designators to R1, R2, ... R16.

This example has more than one part per package, so the reference designator appears with an A after the question mark. ANNOTATE then sequences the letters. ANNOTATE would convert the A of the second part into a B. For example, after running ANNOTATE, the first two occurrences of the 74EXAMP would appear as LATCH1A and LATCH1B, the next two as LATCH2A and LATCH2B, etc. If you omit the REFERENCE line, the default designator U?A appears.

Figure 7-3 illustrates the relationship between the number of parts per package and the reference designator that appears on the part. You must specify a part name, that is what lets you extract the device from the library. However, the REFERENCE keyword is an option. If the REFERENCE keyword has not been specified, it defaults to a designator of "U".

	NUMBER OF PARTS PER PACKAGE	
SOURCE FILE ...	0	1 OR MORE
DOES NOT USE "REFERENCE" KEYWORD	NOTHING IS DISPLAYED	"U" IS DEFAULT REFERENCE DESIGNATOR
USES "REFERENCE" KEYWORD	USES REFERENCE KEYWORD YOU ENTER IN SOURCE LIBRARY	USES REFERENCE KEYWORD YOU ENTER IN SOURCE LIBRARY

Figure 7-3. Controlling Display of Reference Designators

What appears when you call up a part is determined as follows.

1. If the device has 0 parts per package and you do not specify a REFERENCE key word, none appears. Nor does the part name appear.

2. If the device has 0 parts per package and you specify a REFERENCE key word, it appears. It consists of the string you specified followed by a question mark. ANNOTATE replaces the ? with a sequential number. The part name also appears.

3. If the device has one or more parts per package, and you do not specify a REFERENCE key word, a default reference designator (U?A) appears. ANNOTATE replaces the ? with a sequential number that identifies the occurrence of the device and replaces the A with a letter that cycles through the parts of a device. The part name also appears.

4. If the device has one or more parts per package, and you specify a REFERENCE key word, it appears. It consists of the string you specified followed by ?A. The part name also appears.

XY size and parts/package. The next line has the three numbers 6 10 2. The first two represent the size. The size of the part is 6X by 10Y, where each unit represents one screen unit or 0.1 inch on the printed worksheet. The 2 indicates that there are two parts per package. If the part were a pin-grid array, you would supply the keyword GRIDARRAY in place of the number of parts per package.

Pin definitions. The rest of the example consists of the pin definitions. Consider the second pin position. The first field L5 locates the pin on the left side of the part in the fifth position counting from the top down. The Y dimension specified 11 possible positions, 0 through 10. The first possible position is L0 and the last is L10. The specified pin position (L5) is 0.5 inches from the top of the part, when seen on the printed worksheet.

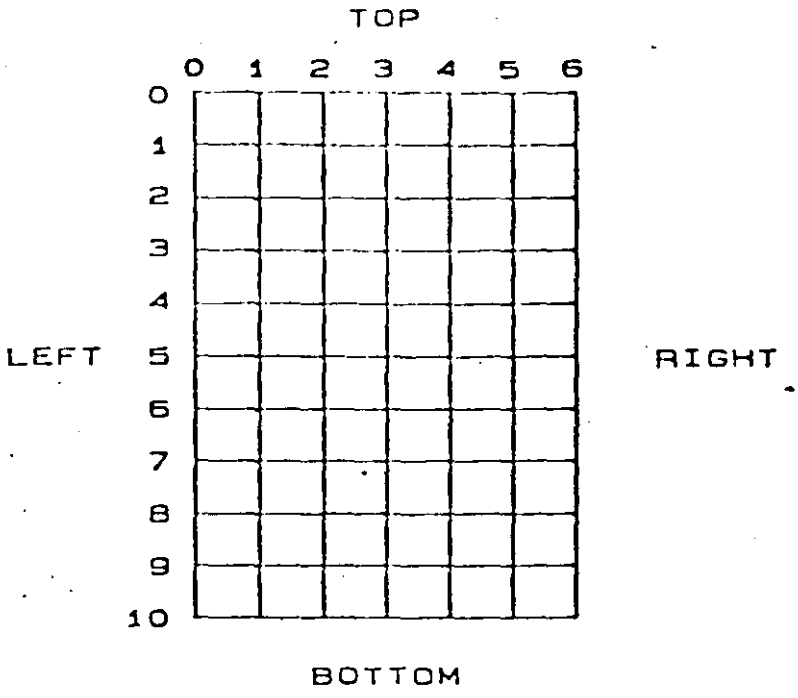


Figure 7-4. The Grid of a 6X by 10Y Block Symbol

The next two pin position fields identify the pin numbers, 1 for the first part of the package and 13 for the second part of the package. The pin at L5 specifies DOT to obtain the inversion bubble and CLK to get the clock symbol. In this case, DOT and CLK are modifiers of the pin function, IN.

R9 puts a pin on the right side in the ninth position, and B3 puts a pin on the bottom in the third position counting right. The two power supply connections are at the top and bottom in the zero position.

Figure 7-4 shows a grid that represents the possible pin positions for the 74EXAMP library part.

Note the SHORT keyword in the first pin position. Pins with the SHORT keyword have 0.1-inch leads rather than the default 0.3 inches. The SHORT keyword, however, cannot be used with with DOT or CLK keywords. Finally, the 'CLK' gives the pin a name Power pins. One possible pin function is PWR for power. Note that power pins do not appear on the screen. The NETLIST utility,

however, does categorize all power pins that are connected to library parts.

If you want to make power pins visible, change the pin function from PWR to IN or PAS. If you do this, you may notice that the power pin overlaps other pin names on the symbol. To avoid this overlap, you must reposition the power pin in the corresponding library source file.

Parts per Package. If the device has more than one part per package, you can selectively display the pins. For example, assume you wanted to display the power pins VCC and GND, but only on the second part of the device, not on the first. You could do that by coding the last two lines of the block symbol as follows.

```
T0  0   16  PAS 'VCC'
B0  0   8   PAS 'GND'
```

When you place this symbol on the screen, the power pins do not display because the first column of pin locations contains a 0. When you place another symbol on the screen, it looks identical to the first. Both are called LATCH?A, and neither shows the power pins. However, if you exit DRAFT and run the ANNOTATE utility with the /M option (this causes the annotation information to be merged into the sheet directly) and then look at the sheet again with DRAFT, you'll see the two parts labeled LATCH1A and LATCH1B. The power pins appear only on the second part of the device, LATCH1B.

This technique also works for non-power pins. By specifying a pin number of 0, you can cause a pin not to appear for the part of a package.

However, if your device has one part per package, specifying a pin number of 0 does not prevent the pin from appearing. The pin appears with a pin number of 0. If your device has 0 parts per package, you cannot specify pin numbers, and consequently, none appear. Figures 7-5A and 7-5B illustrate how the number of parts per package, the pin number, and the ANNOTATE utility affect the screen symbol.

The device 74ONE is identical to 74EXAMP, except that it has one part per package. Note that the ANNOTATE utility affects both the

pinout and reference designator for 74EXAMP, but only the reference designator for 74ONE. Also note that in Figure 7-5A and 7-5B, the locations of the power pins were moved from T0 and B0 to R3 and R7, so that they would not overlap existing pins.

Before ANNOTATE

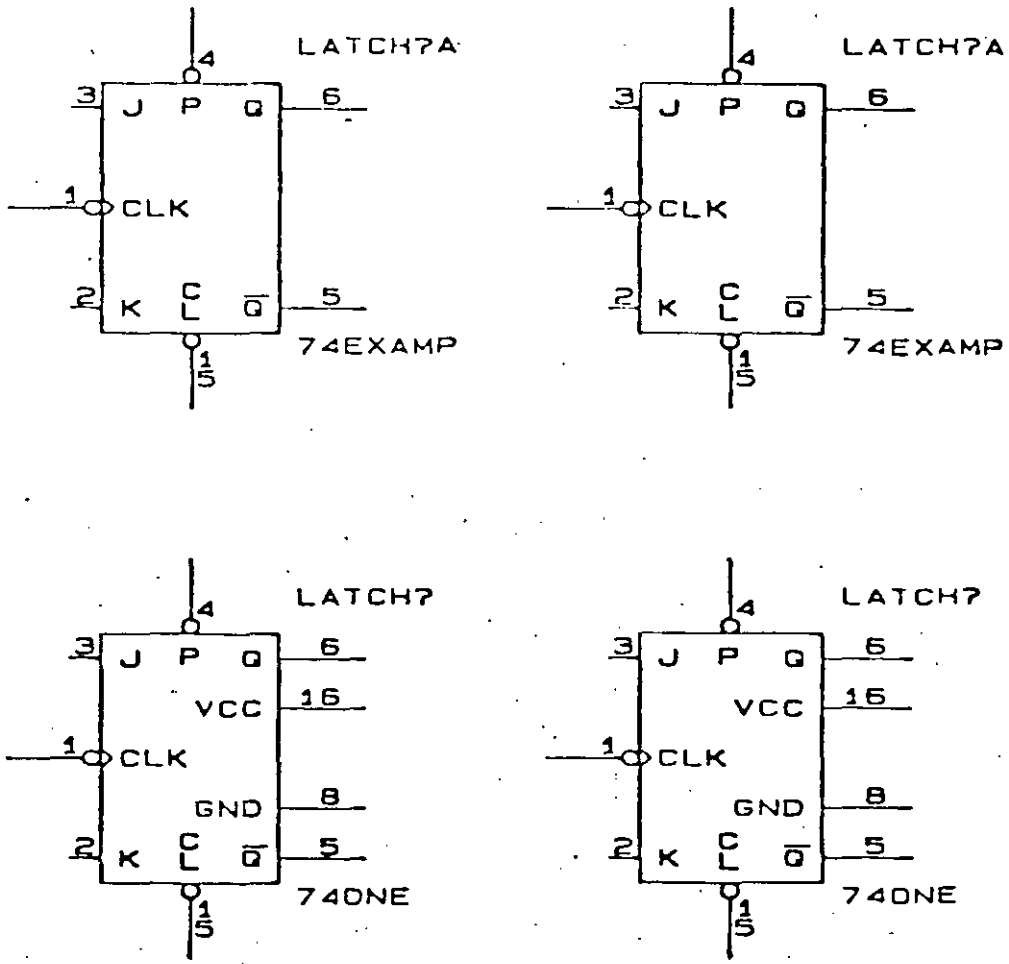


Figure 7-5A. Before Annotation

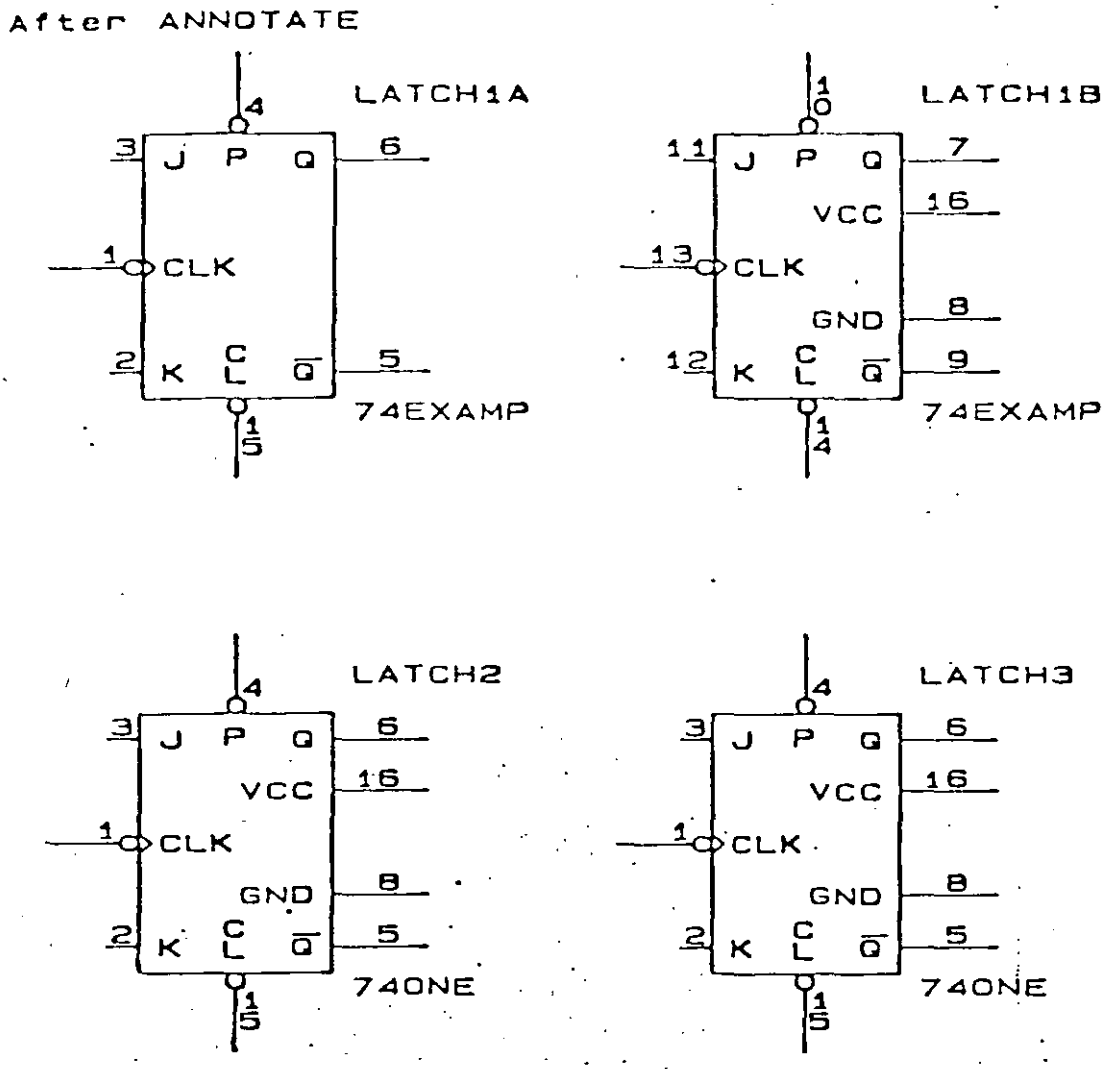


Figure 7-5B. After Annotation

If a device has more than one part per package, you may want power pins on some parts present and the power pins on other parts not to be present.

Pin-grid array. If the part were a pin-grid array, you would supply the gridarray pin name instead of the pin number. A gridarray name consists of a capital letter followed by a number. The letter is in the

range A through S, and the number is in the range 1 through 16. There can be no space between the letter and the number.

Here is an example of a pin-grid array part definition. The example is the 68020 from the Motorola library, MOTO.LIB. The definition is quite long so only the first few lines are shown.

Figure 7-6 shows the resulting screen figure.

```
'68020'
15    66    GRIDARRAY
L1    C2    CLK IN  'CLK IN'
L3    J12   IN      'I\P\L\0\' (the \ bars the pin name)
L4    J13   IN      'I\P\L\1\'
L5    H12   IN      'I\P\L\2\'
                .
                .
                .
```

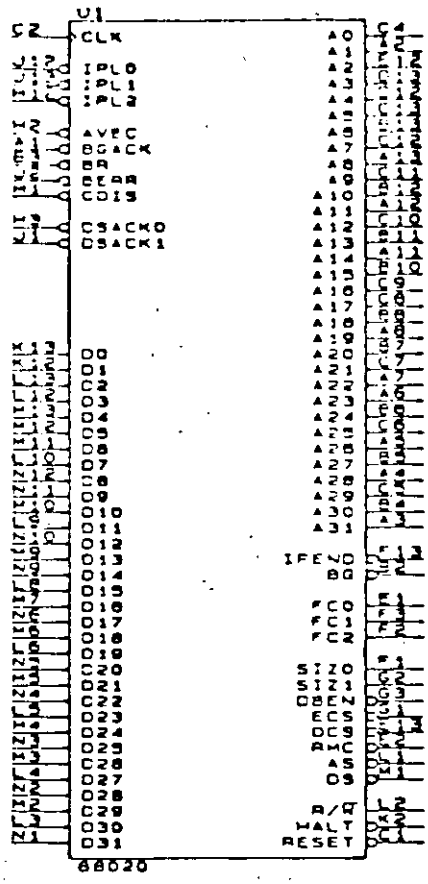


Fig. 7-6. The Block Symbol for 68020

Pin string. The pin string is delimited by single quotes. If you want a single quote as part of the pin string, you must use two single quotes. For example, 'CLK"s' defines the string CLK's. Also, a backslash after the pin string name puts a bar over the name. 'Q\' results in Q with a bar over it. If you have a multi-letter pin name, you must put a \ after each letter. For example, the 68020 shows IPL0, and the corresponding pin string entry in the part definition is 'I\P\L\0\'.

Note that the power pins do not appear on the screen. The NETLIST utility, however, does categorize all power supply pins that are connected to library parts.

7.3.4 Bitmap Symbol Definition

Creating a bitmap is an easy way to represent non-square or non-rectangular parts such as resistors, diodes, transistors, MOSFETs, relays, and many others. DRAFT draws complex parts on the screen by selectively turning on pixel bits that represent the library part. Activating the correct pixel bit is controlled by a bitmap in the library source file you created. You create the bitmap in the library source file.

To define a part with a bitmap, you define the part just as you would if it were a block symbol, but you include a bitmap after the last pin definition. You can either draw out the bitmap with periods (.) and pound signs (#), or you can reference a previously drawn-out bitmap. Previously drawn-out means the bitmap was defined previously in the library source file.

You would reference a previously drawn-out bitmap if two parts had different pinouts, but the same symbol. For example, the 7439 and the 7400 have the same symbol, but different pinouts. Assume that you've defined the 7400 and you're now defining the 7439. Instead of drawing another bitmap for the 7439, you can use the 7400's bitmap by including the line

```
BITMAP '7400'
```

There are four points you should keep in mind when creating bitmaps, as opposed to block symbols.

1. You have to pay more attention to pin placement. The pin definition line and the bitmap have different scales, and you need to take the conversion into account when you draw the symbol.

2. Although you can put a pin name in the pin definition, the pin name will not appear on the screen. The pin name will, however, be recognized by the NETLIST utility.

3. A bitmap symbol gives you the opportunity to define a converted symbol. Bitmap devices always have a normal form. You have the

option of also defining a converted form. Block symbols cannot have a converted form. When you use the GET command and extract a part from a library, it appears in normal form. The resulting menu enables you to choose its converted form instead. You define what the converted form is when you create the library source file. Typically, users define the converted form as the DeMorgan equivalent of the normal form.

4. The maximum number of bits allowed in a bitmap is 16,384. The bitmap begins after the last pin definition. A pound sign (#) indicates that the pixel bit is turned on, and a period (.) indicates that the pixel bit is turned off.

Each . or # represents a screen pixel spacing of 0.01 inch in the X direction. Each line of the bitmap represents 0.01 inch in the Y direction. Remember, the X and Y sizes in the part definition are given in units of 0.1 inch. For example, if you specify X an Y to be 3 and 2, your bitmap actually is 31 characters in the X direction and 21 lines in the Y direction. The extra 1 results because the bitmap starts counting at zero.

An example should make this clearer. Here is a part definition for a resistor.

```
      {Part definition for a resistor}
      'resistor'
      REFERENCE         'R'
      3  2  0
      L1     PAS         ''
      R1     PAS         ''

            {Top side}
{00}.............................
{01}.............................
{02}.............................
{03}.............................
{04}.............................
{05}.............................
{06}.............................
{07}...#.........#.........#...
{08}..#.#.......#.#.......#.#..
{09}.#...#.....#...#.....#...#. {Right side}
{10}#.....#.....#.....#.....#.....#
{11}.....#...#.....#...#.....
{12}.....#.#.......#.#.....
{13}.....#.........#.....
{14}.............................
{15}.............................
{16}.............................
{17}.............................
{18}.............................
{19}.............................
{20}.............................

            {Bottom side}
```

Note that the number of parts per package is given as 0. Hence, there are no columns for pin numbers. The pin types are PAS for passive, and there are no pin names (however, they may be specified).

The X size is specified as 3, so the bitmap has lines that are 31 characters long. The Y size is specified as 2, so the bitmap has 21 lines. The part definition specifies two pins, one on the left in the first position (L1) and another on the right in the first position (R1). The pin positions are always spaced 0.1 inch apart. As far as the bitmap is concerned, pin positions are at lines 0, 10, 20, 30, etc.

The line numbers are enclosed in comment delimiters. It isn't necessary to number the bitmap lines this way, but doing so makes the bitmap more readable.

You can reduce the size of bitmaps used in your library by observing the following rules.

1. An empty row (one that has only dots) can be represented by a dot in the zeroth column. If that is the only character on the row, then the row is held as cleared.

2. Empty rows below the actual symbol need not appear in the bitmap.

3. Periods are not required after the last # in a row.

Here is an example of the same resistor definition that follows the reduction rules just described. Figure 7-7 shows the symbol that results from this part definition.

```
{Part Definition for a resistor.}

'RESISTOR'
REFERENCE 'R'
3 2 0
L1    PAS  ''
R1    PAS  ''

                        {Top side}
{00}.
{01}.
{02}.
{03}.
{04}.
{05}.
{06}.
{07}...#...........#...........#
{08}..#.#.........#.#.........#.#
{09}.#...#.......#...#.......#...#        {Right side}
{10}#.....#.....#.....#.....#.....#
{11}.......#...#.......#...#
{12}.........#.#.........#.#
{13}..........#...........#

                        {Bottom side}
```

Figure 7-7. The Symbol for a Resistor

After defining a bitmap, you have the option of defining a conversion bitmap. As stated previously, the typical use of a conversion bitmap is to supply a DeMorgan equivalent symbol, but more generally a conversion specifies another bitmap that is displayed on the screen whenever you choose the Convert option of the GET command. You can return to the original bitmap by selecting the Normal subcommand option.

You begin the specification of a conversion bitmap with the keyword CONVERT. The conversion bitmap consists of pin definitions followed by a bitmap. If the conversion has been previously defined, you can reference it by including the name of the part that has the conversion in single quotes.

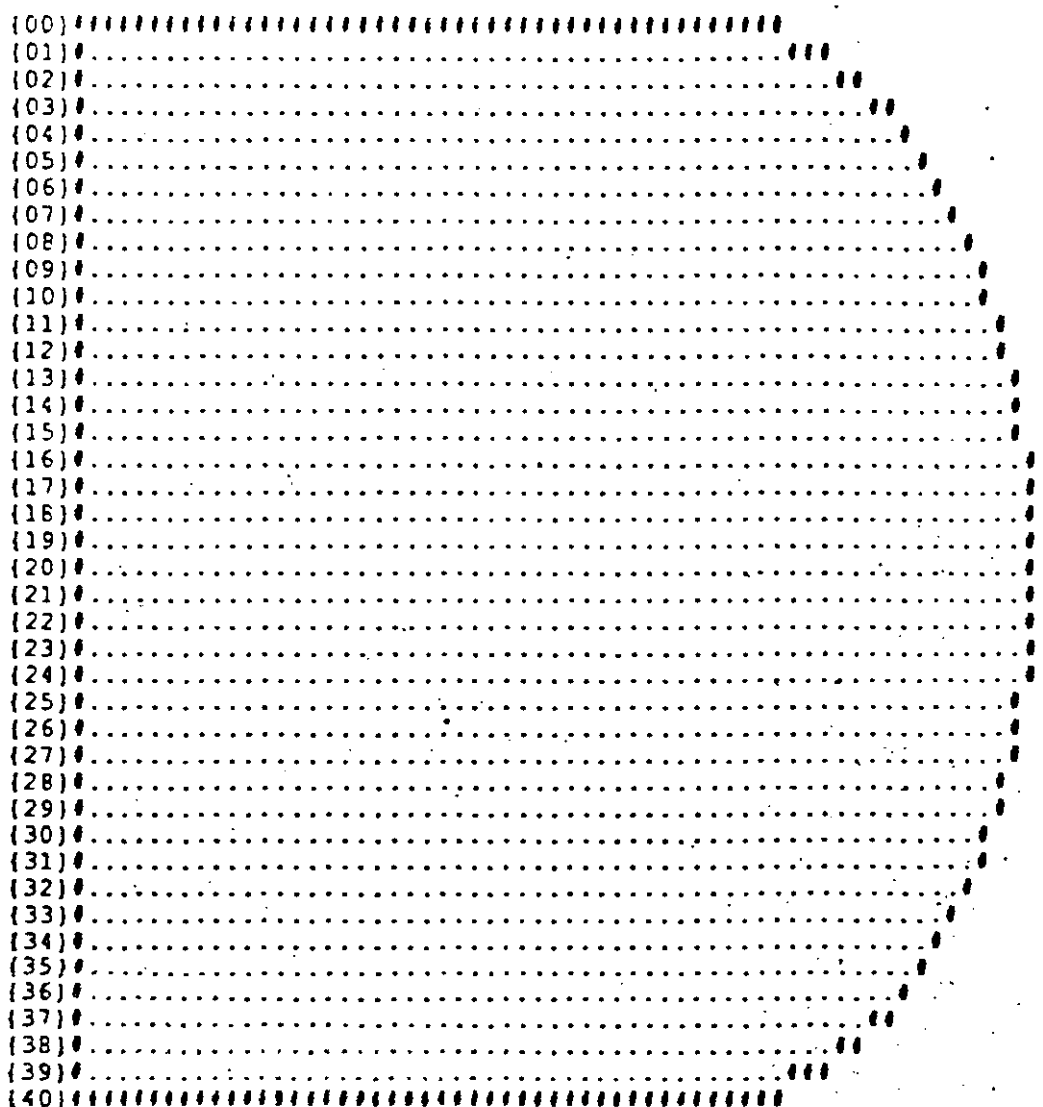
The next example should clarify the use of conversion bitmaps. First, is the definition of the 7400. Then, comes the conversion bitmap -- it's the DeMorgan equivalent of the 7400. Figure 7-8 shows the normal and converted symbols that result from this part definition.

The 7400 has five pins, two of which are power pins that do not appear in the symbol. The screen size is 6 X-units and 4 Y-units. It has four parts per package.

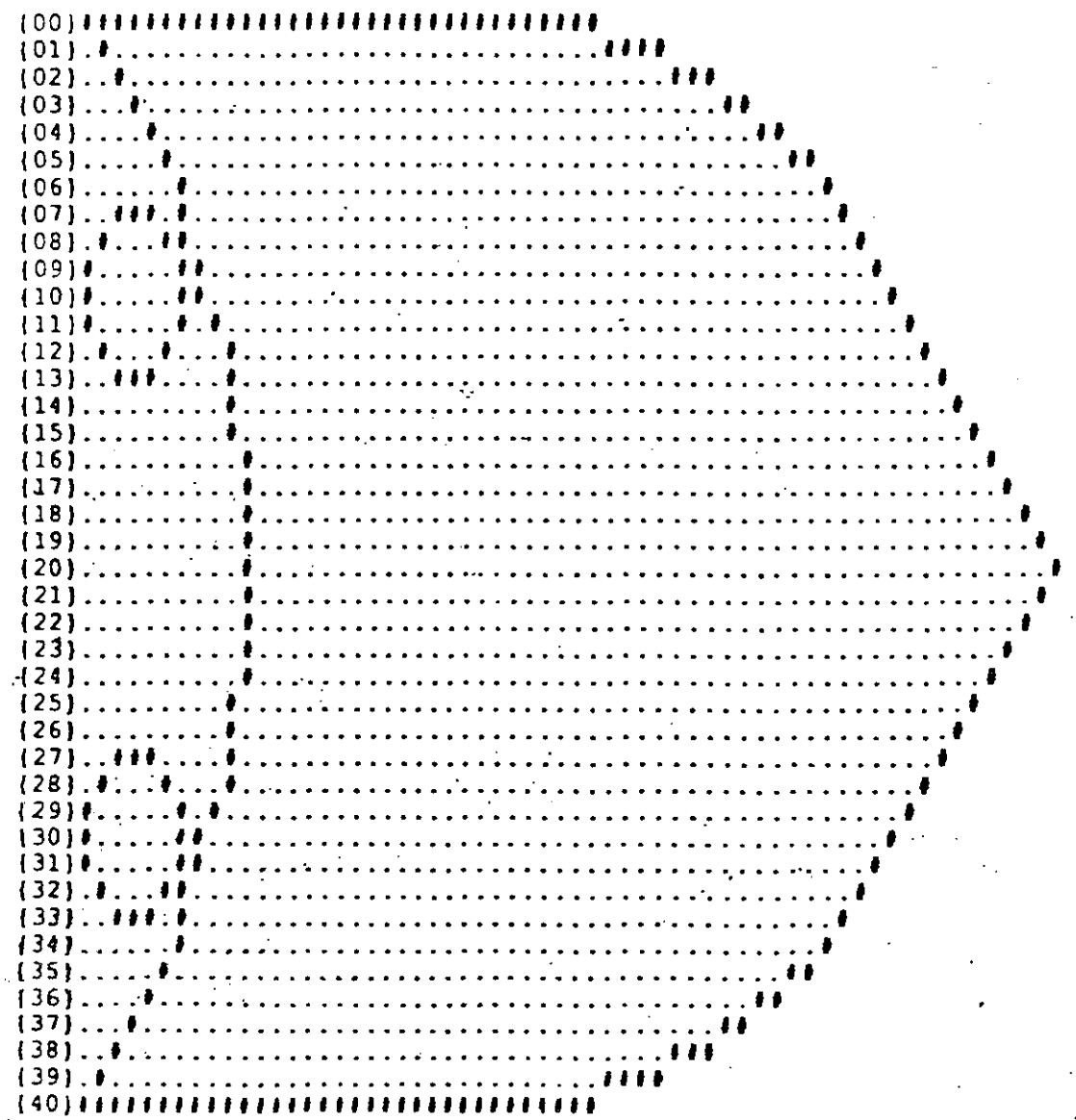
The conversion bitmap uses the same XY size and parts per package as the normal bitmap. You must, however, redefine the pins. Note the DOT keyword missing from the redefinition of the pin at R2.

Note that the conversion bitmap has the same number of parts per package as the normal bitmap. The number of parts per package determines how many columns of pin numbers appear in the definition. The converted definition must have the same number of columns as the normal definition.

```
'7400'
6     4     4
L1    1     4     9     12    IN      'I0'
L3    2     5     10    13    IN      'I1'
R2    3     6     8     11    DOT     OUT       'O'
T0    14    14    14    14            PWR       'VCC'
B0    7     7     7     7             PWR       'GND'
```



```
CONVERT
L1    1     4     9     12          IN        'I0'
L3    2     5     10    13          IN        'I1'
R2    3     6     8     11          OUT       'O'
T0    14    14    14    14          PWR       'VCC'
B0    7     7     7     7           PWR       'GND'
```



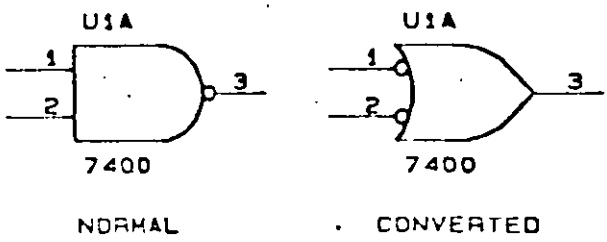


Figure 7-8. The 7400 Symbol and its Conversion

7.4 SDL Reference

This section is a complete description of how to define a part in a custom library. It presents OrCAD's Symbol Description Language (SDL) in the form of syntax diagrams. A syntax diagram consists of identifiers (enclosed in ovals) and tokens (enclosed in rectangles). The syntax diagram is also followed by a textual representation.

7.4.1 Syntax Diagram

Figure 7-9 is an example of a syntax diagram. It represents the complete syntax for a library source file.

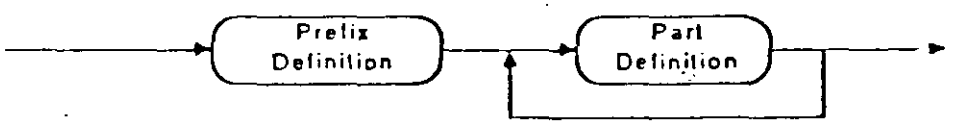


Figure 7-9. Syntax Diagram for a Library Source File

To read a syntax diagram, observe the following rules.

1. Read a syntax diagram from left to right.

2. Every path that you follow in the direction of the arrows represents a correct syntax form.

3. Junctions represent a connection point where you have the choice of selecting another path. For example, the syntax diagram for the library source file shown in Figure 7-9 has a junction after a part definition. You can choose to complete the diagram or to make another part definition.

4. You cannot continue along a path that goes against the arrows. For example, in Figure.7-9 after making a part definition you cannot choose to return to the prefix definition.

5. Text enclosed in ovals represents an identifier. Text enclosed in squares represents a token.

What are identifiers? Identifiers serve as placeholders for a more detailed level of syntax structure. They do not represent command syntax or tokens. Rather, they provide the ability to give a overview of the syntax. When you create the part, you must work down through all the nested identifiers. For example the syntax diagram for a library source file shown in Figure 7-9 has two identifiers and no tokens. This section will now expand each of those identifiers and present all the possible tokens.

What are tokens? They are the building blocks of a library source file. Just as a sentence is made up of words, a library source file is made up of tokens. A token belongs to one of the following categories.

- Numeric constants. A numeric constant consists of one or more whole-number digits.

  Examples: 15
  2
  127

- Character strings. A character string consists of one or more alphanumeric ASCII characters.

  Examples: 74ALS04
  ZENER
  LS
  CLOCK

- Keywords. A keyword is one of the following:

  BITMAP — Takes an argument (an ASCII string representing a part name) and represents the bitmap of the identified part.

CLK	Represents the clock symbol in a pin definition.
CONVERT	Introduces a converted bitmap. With an argument, it refers to the converted bitmap of a bitmap symbol.
DOT	Represents the inversion bubble in a pin definition
END	Delimits the close of a prefix definition.
GRIDARRAY	Specifies that the device is a pin-grid array. Used in place of the number of parts per package.
HIZ	Identifies the pin as a high impedance (3-state) output.
IN	Identifies the pin as an input.
I/O	Identifies the pin as input/output.
OC	Identifies the pin as open collector.
OUT	Identifies the pin as an output.
PAS	Identifies the pin as passive.
PREFIX	Delimits the beginning of a prefix definition.
PWR	Identifies the pin as a power pin. The PWR keyword prevents a pin from being displayed.
REFERENCE	Takes an argument (an ASCII string representing a reference value). Overrides the default reference value.
SHORT	Specifies that the pin lead lengths be 0.1 inch instead of the normal 0.3 inch.

7.4.2 Textual Representation of Syntax

In addition to the syntax diagram, syntax is represented in text. The symbols are defined as follows.

	Text enclosed in *italics* represents either a character string or a numeric constant.
[]	Text enclosed in square brackets is optional. You choose whether to type it in or not. Do not type the square brackets.
{}	Text enclosed in braces is required. You must enter what's represented within the braces.
,	If items within square brackets or braces are separated by commas, you must choose one of them only. Do not type the comma.
...	Three periods mean you can repeat the last item. How many times you can repeat the item depends on the context. Do not type the periods.

Here is an example of syntax represented in text.

pos [*pin#...,grid...*]

First, you must enter a representation of *pos*. An accompanying description explains what you can put in for *pos*. The square brackets around the next item indicate that you don't have to enter it at all. If you do, you must choose between *pin#* or *grid*; and you can choose a repeated number of each.

7.4.3 PREFIX Definition

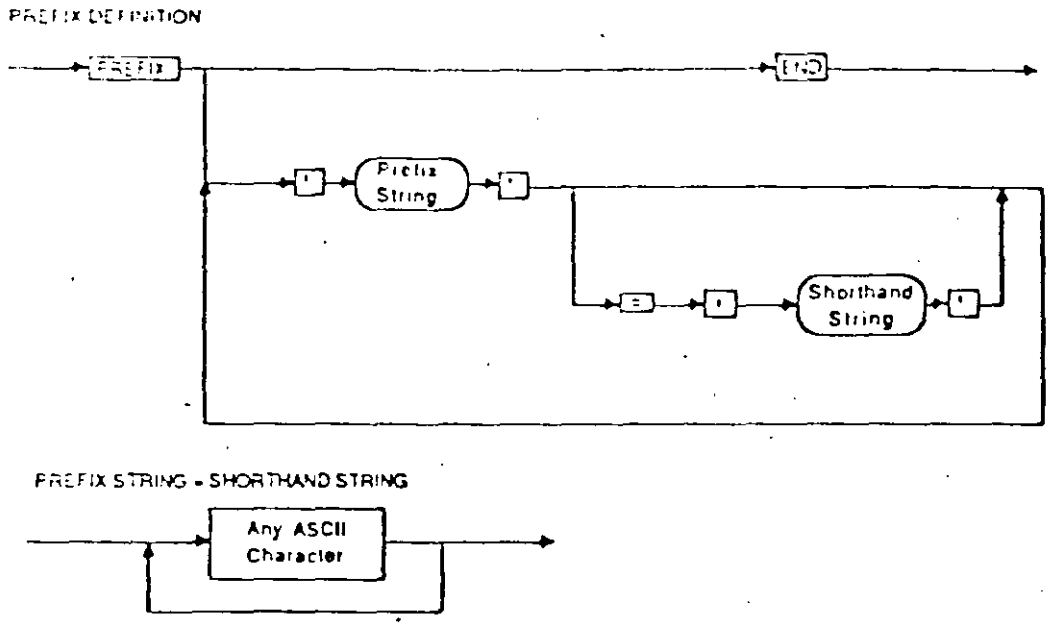


Figure 7-10. Syntax Diagram For a Prefix Definition

```
PREFIX
[ 'prefix string' [= 'shorthand string' ]]
.
.
.
END
```

where:

prefix string	A character string of up to seven printable ASCII characters. You can have a maximum of 16 prefix strings.
shorthand string	A character string of up to seven printable ASCII characters.

NOTES

The equal sign must be separated by one or more <SPACE>s or <TAB>s.

EXAMPLES

Example:

```
PREFIX
'74LS'     = 'LS'
'74S'      = 'S'
'74ALS'    = 'ALS'
'74AS'     = 'AS'
'74HCT'    = 'HCT'
'74HC'     = 'HC'
'74ACT'    = 'ACT'
'74AC'     = 'AC'
'74F'      = 'F'
'74'
END
```

Example:

```
PREFIX
END
```

7.5.4. Part Definition

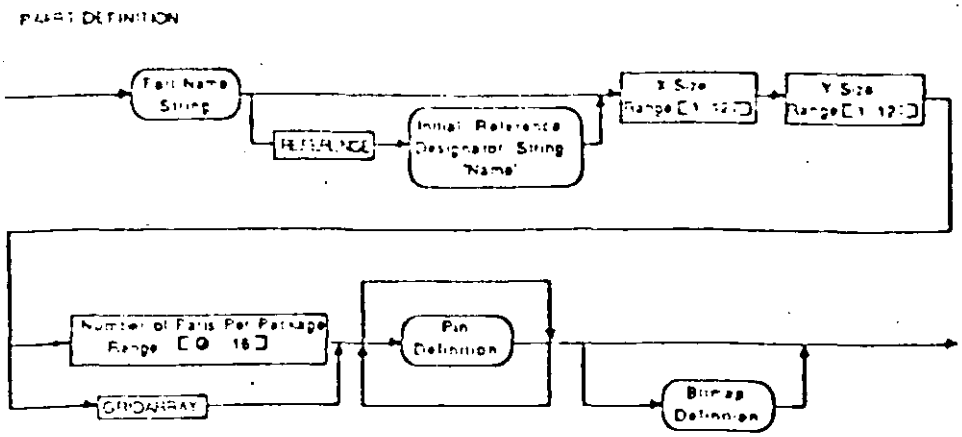


Figure 7-11. Syntax Diagram for a Part Definition

'part name string'...
[REFERENCE *'ref string'*]
X size Y size {*parts/pckg* , GRIDARRAY}
pin definition
.
.
.
[*bitmap definition*]
[*conversion bitmap*]

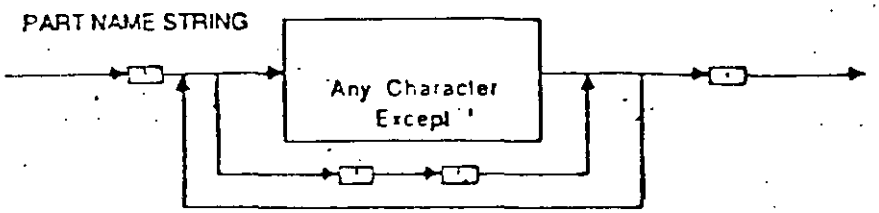


Figure 7-12. The Part Name String

where:

part name string	A character string of up to seven printable ASCII characters that identifies the part. This is the string that can be used as an argument for the Get command.
ref string	A character string of printable ASCII characters. If present, the reference designator replaces the default reference designator.
X size	A numeric constant in the range 1 to 127. The horizontal size of the part as it appears on a printed worksheet. Each entry corresponds to one unit length on the screen or 0.1 inch on a printed worksheet.
Y size	A numeric constant in the range 1 to 127. The vertical size of the part as it appears on a printed worksheet. Each entry corresponds to one unit length on the screen or 0.1 inch on a printed worksheet.
parts/pckg	A numeric constant in the range 0 to 16. If you specify a 0, the pins are not numbered on the symbol.
pin definition	These are identifiers for a more detailed *bitmap definition* level of syntax. See the corresponding *conversion bitmap* entry.

NOTES

To improve readability, you can include comments within a part definition. You can also place blank lines within a source file. Typically blank lines are placed between different part definitions.

EXAMPLES

Example 1:

```
'2114'    '214B'
  6     14      1

 pin definition
    .
    .
    .
```

(Two part name strings. These may be on the same or separate lines.)

Example 2:

```
'7474'    '74ALS74'  '74LS74'   '74S74'
'74HC74'  '74AC74'
6     6       2
pin definition
      .
      .
      .
```

7.4.5 Pin Definition

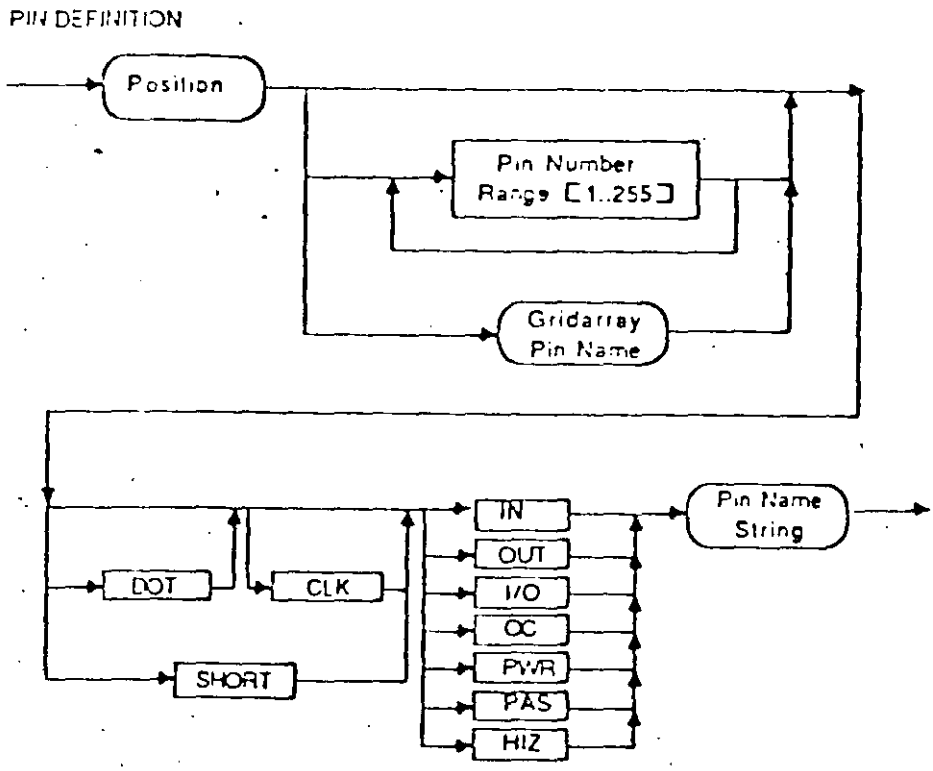


Figure 7-13. Syntax Diagram for a Pin Definition>

pos [*pin#, grid* .] [DOT] [CLK] [SHORT] [IN] [OUT] [I/O] [OC] [PWR] [PAS] [HIZ] *pin name*

where:

pxx

A letter followed by a number. The letter is one of the following: T, L, R, B where

T indicates the top of the symbol.
L indicates the left side of the symbol.
R indicates the right side of the symbol.
B indicates the bottom of the symbol.

The number represents the distance along the indicated side. The distance is measured in unit lengths on the screen and in 0.1 inches on the printed worksheet. For example, if the block symbol were 6X by 10Y the grid used for placing pins is as follows. The figure below shows the location of L3.

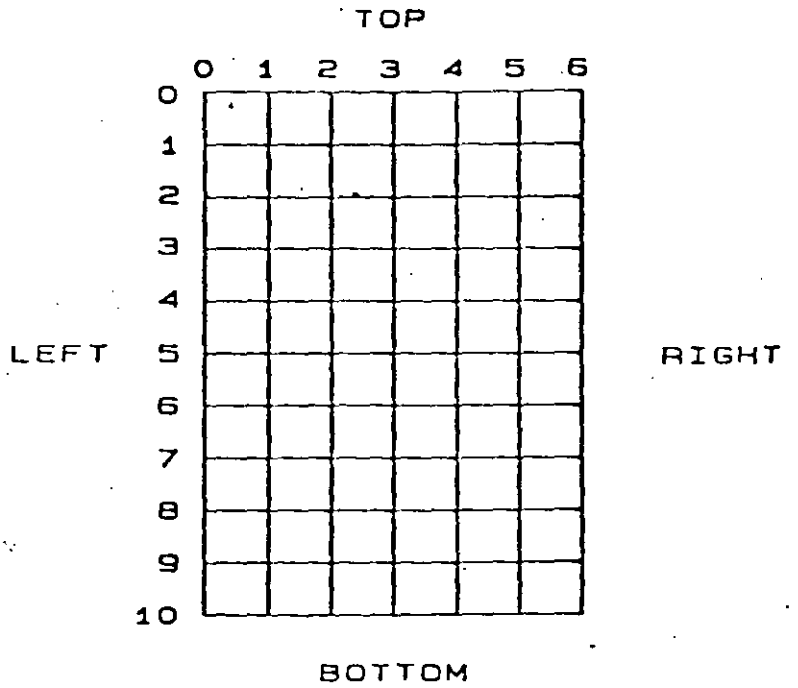


Figure 7-14. The Grid of a 6X by 10Y Block Symbol

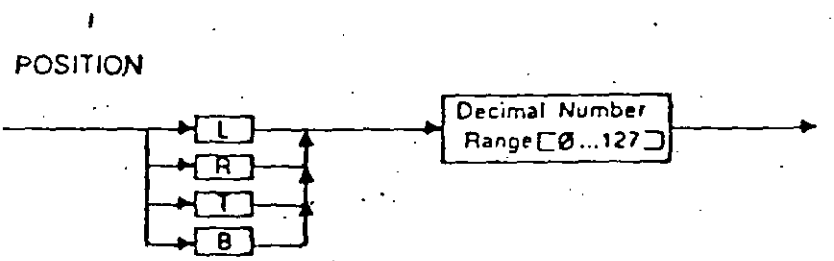


Figure 7-15. The Position Syntax Diagram

pin# A numeric constant representing the pin number. This is the pin number that appears in the screen symbol.

grid A letter followed by a number. *grid* represents the pin-grid array pin number. You can only choose a pin-grid array pin number if, in place of *parts/pckg*, you chose the keyword GRIDARRAY. The letter must be in the range A through S; the number must be in the range 1 through 15.

Figure 7-16. Gridarray Pin Name Syntax Diagram

SHORT A keyword that places a short lead length at the specified pin. The normal lead length is 3 screen units or 0.3 inches on the printed worksheet. When the SHORT keyword is present, the lead length is 1 screen unit or 0.1 inch on the printed worksheet. The SHORT keyword cannot describe a pin that also has either the CLK or DOT keywords.

DOT A keyword that places the inversion symbol (the bubble) at the specified pin location. The DOT keyword cannot describe a pin that also has the SHORT keyword. The primary use of the bubble is to identify pins that have logic negation, either at an input or an at an output. The figure below shows the inversion symbol.

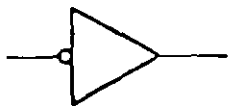


Figure 7-17. The Inversion DOT Symbol

CLK — A keyword that places the clock symbol at the specified pin location. The CLK keyword cannot describe a pin that also has the SHORT keyword. The figure below shows the CLK symbol.

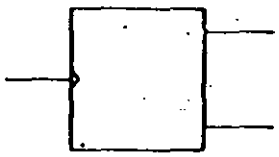


Figure 7-18A. The CLK Symbol

You can use the CLK keyword in conjunction with the DOT keyword to produce a DOT CLK symbol. The figure below shows the DOT CLK symbol.

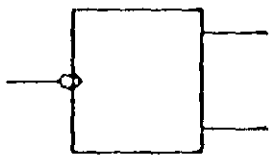


Figure 7-18B. The DOT CLK Symbol

IN	A keyword that identifies the pin as an input.
OUT	A keyword that identifies the pin as a standard totem-pole output.
I/O	A keyword that identifies the pin as a dual function input/output pin.
OC	A keyword that identifies the pin as an open collector or open drain.
PWR	A keyword that identifies a power pin, such as Vcc, Gnd, Vss, Vdd, and others. Power pins are not displayed on library parts when they appear on the screen or printed worksheet. However, the NETLIST utility connects all power supply pins that are defined in library source files.
PAS	A keyword that identifies a pin as passive. Passive pins are typically pins on passive devices such as resistors, transistors, inductors, and others.
HIZ	A keyword that identifies a pin as a high-impedance (3-state) output.
pin name	A character string that represents a name for the specified pin. For block symbols, this name

appears on the screen or the printed worksheet. Pin names do not appear on the screen or the printed worksheet when they are are part of pin definitions for a a bitmap symbol. However, you may still choose to use pin names in bitmap symbols. The NETLIST utility still recognizes them, and you may find them useful as personal references.

You can enter pin names either in upper- or in lower-case, but they always appear in upper-case.

The backslash (\) and single quote (') are special characters. A backslash (\) after a character indicates that the character should have a bar over it. If you want to bar multiple characters, you must place a backslash after each character. The single quote delimits the part name string. If you want a single quote as part of the pin string, you must escape it with another single quote.

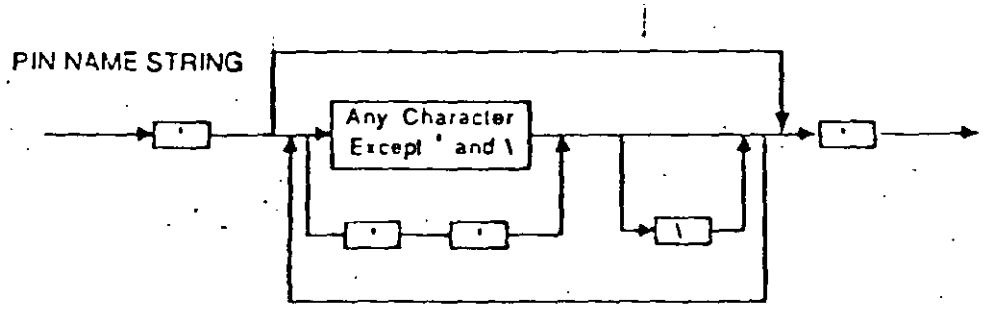


Figure 7-19. Pin Name String Syntax Diagram

EXAMPLES

Example:

```
'2114'  '2148'
6       14      1
L1      5       IN      'A0'
L2      6       IN      'A1'
L3      7       IN      'A2'
L4      4       IN      'A3'
L5      3       IN      'A4'
L6      2       IN      'A5'
L7      1       IN      'A6'
L8      17      IN      'A7'
L9      16      IN      'A8'
L10     15      IN      'A9'
L12     8       IN      'C\S\'
L13     10      IN      'W\E\'
R1      14      HIZ     'D0'
R2      13      HIZ     'D1'
R3      12      HIZ     'D2'
R4      11      HIZ     'D3'
T0      18      PWR     'VCC'
B0      9       PWR     'GND'
```

Example:

```
'68020'  (This device is in a pin-grid array package.)
15      66      GRIDARRAY
L1      C2      CLK IN      'CLK'
```

Example:

```
'7474'      '74ALS74'   '74AS74'   '74LS74'   '74S74'
'74HC74'    '74AC74'
6       6       2
L2      2       12      IN          'D'
L4      3       11      CLK IN      'CK'
B3      1       13      DOT IN      'CL'
```

7.4.6 Bitmap Definition

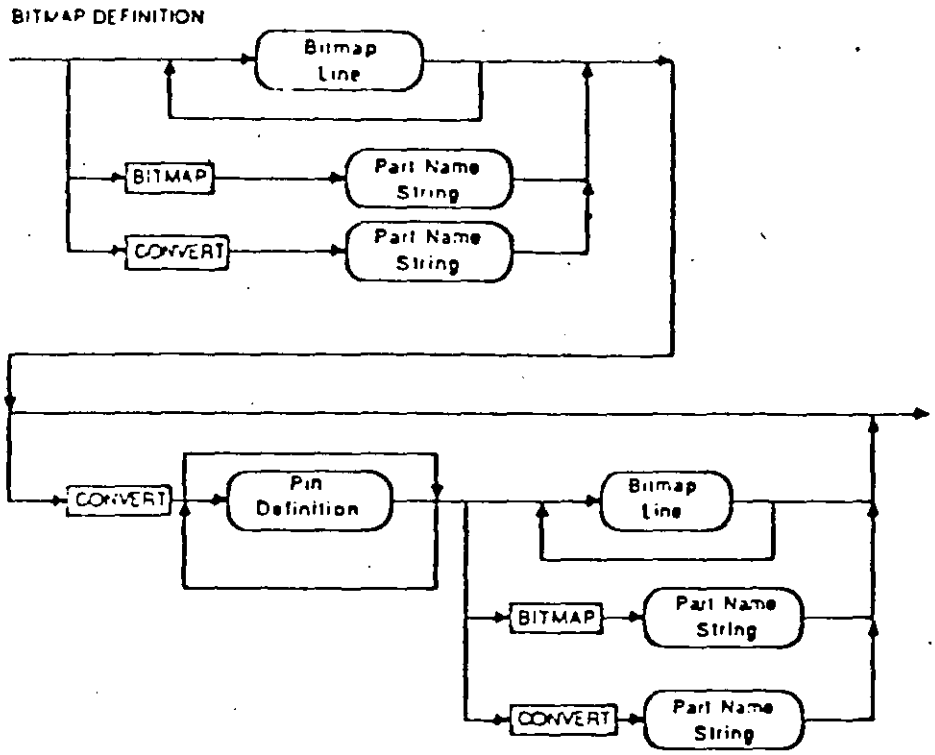


Figure 7-20. The Bitmap Syntax Diagram

```
[[.,#]...,BITMAP 'part name'  ,CONVERT'part name'  ]
    .
    .
    .
```

where:

. A . represents cleared pixel bit that is not displayed on the screen.

A # represents a set pixel bit.

- If you use the BITMAP option, be sure that the part name you refer to is previously defined. Be aware that DECOMP may reorder part definitions. DECOMP order parts numerically and then alphabetically.

EXAMPLES

```
Example 1:

'CAPACITOR'
2       3       0
T1      PAS     ''
B1      PAS     ''
{    01234567890123455678901234567890}
{   0           1           2           3}
{00}..........#
{01}..........#
{02}..........#
{03}..........#
{04}..........#
{05}..........#
{06}..........#
{07}..........#
{08}..........#
{09}..........#
{10}..........#
{11}..........#
{12}..........#
{13}####################
{14}.
{15}.
{16}.
{17}.
{18}.....###########
{19}...###....#....###
{20}.##.......#......##
{21}#.........#........#
{22}..........#
{23}..........#
{24}..........#
{25}..........#
{26}..........#
{27}..........#
{28}..........#
{29}..........#
{30}..........#
```

Example 2: BITMAP '7400'

{This takes the bitmap defined for the device 7400.}

Example 3: CONVERT '7400'

{This takes the conversion bitmap defined for the device 7400. This part must have a conversion bitmap if the library source file is to COMPOSE without errors.}

7.4.7 Conversion Bitmap

```
CONVERT
pin definitions
    .
    .
    .
bitmap definition
```

where:

pin definition	A previously described identifier. Note that the pin definition for a converted bitmap must have the same value for parts/pckg and the normal bitmap.
bitmap definition	A previously described identifier.
part name	A previously defined part name that has a converted bitmap.

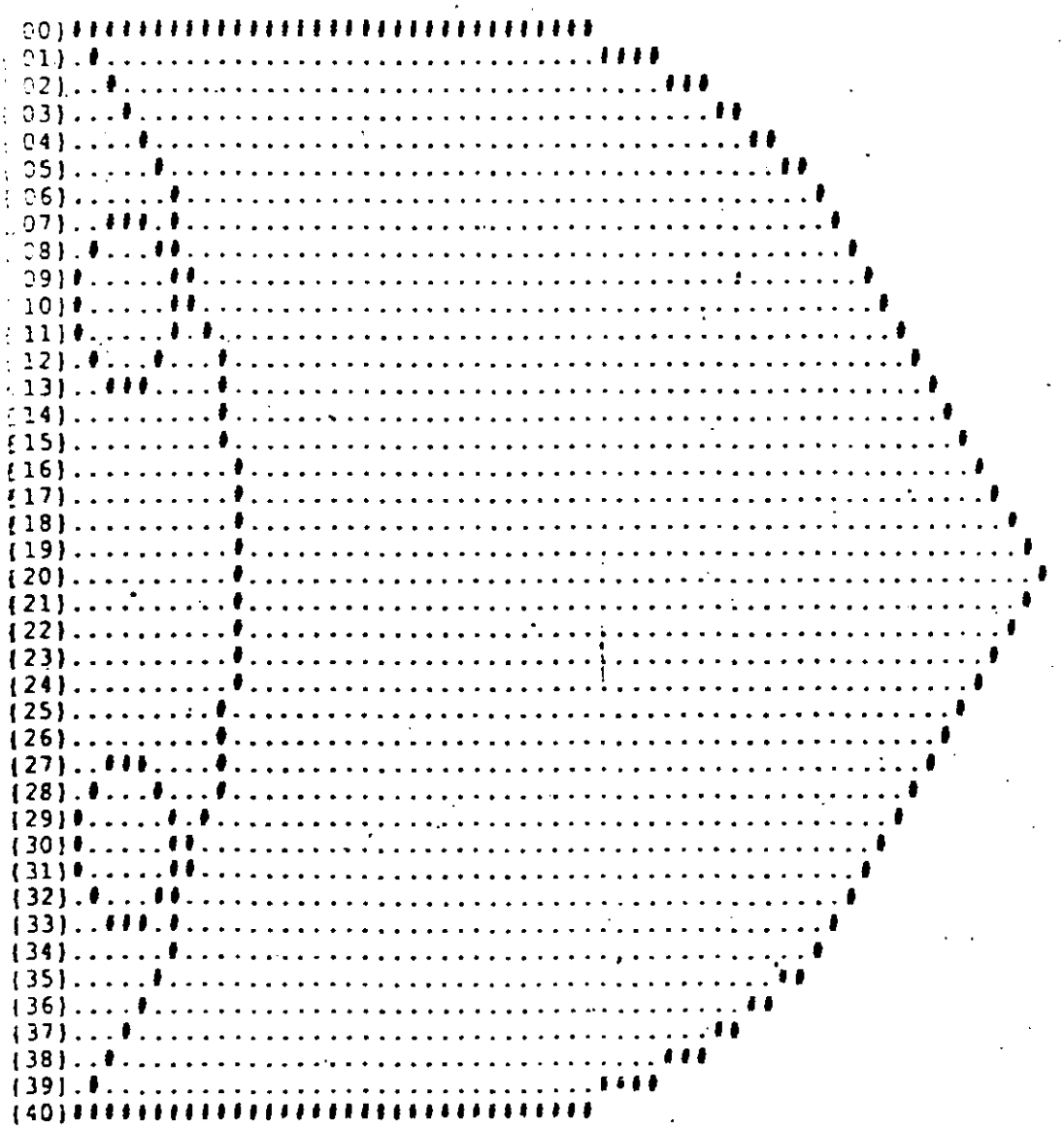
NOTES

If you use the CONVERT '*part name*' option, be sure that the part name you refer to is previously defined. Be aware that DECOMP may reorder part definitions. DECOMP orders parts numerically and then alphabetically.

EXAMPLES

Example 1: CONVERT

```
        L1    1     4     9     12    IN    'I0'
        L3    2     5     10    13    IN    'I1'
        R2    3     6     8     11    OUT   'O'
        T0    14    14    14    14    PWR   'VCC'
        B0    7     7     7     7     PWR   'GND'
```



Example 2: CONVERT '7400'

7.5 A Final Example: Making a Connector

A typical custom part is a connector. You could use module ports to make a connector, but OrCAD doesn't recommend it. If you use module ports to represent a connector, the NETLIST utility has no way of knowing what the pin numbers are.

Instead, use module ports to represent hierarchical and flat file signals that go from one sheet to another. Connectors, however, such as the DB25 or the IBM 62-pin edge connector, are best represented as library parts. In that way, you treat connectors as physical devices with pin names, which is what they are.

Here is a partial example of a part definition for an IBM 62-pin edge connector.

```
'CONNECTOR IBM'
10      32      0
L1      IN      'B1'
L2      IN      'B2'
L3      IN      'B3'
L4      IN      'B4'
L5      IN      'B5'
L6      IN      'B6'
        .
        .
        .
L30     IN      'B30'
L31     IN      'B31'
R1      IN      'A1'
R2      IN      'A2'
R3      IN      'A3'
R4      IN      'A4'
R5      IN      'A5'
R6      IN      'A6'
        .
        .
        .
R30     IN      'A30'
R31     IN      'A31'
```

7.6 Examples of Source Libraries

Using the techniques discussed just described, we can now examine some examples of library source files. Remember, comments are enclosed within braces {...}. We present three sample source libraries.

SAMPLE_1.SRC	This file contains some typical block symbol definitions. It has some memory devices and two microprocessors, the 8086MAX (the 8086 in maximum mode) and the 68020 (a pin-grid array).
SAMPLE_2.SRC	This file contains some standard TTL devices. Note the use of a prefix definition.
SAMPLE_3.SRC	This file contains some typical bitmap definitions. It has an AND gate with its DeMorgan equivalent, and antenna, a capacitor, a triode, and other non-square or non-rectangular symbols.

Although these examples separate the kinds of definitions (block from bitmap) into different libraries, that is not a requirement. You can intersperse block and bitmap definitions in the same file.

To use these sample files, construct a pure ASCII file (no formatting characters) and execute the COMPOSER utility. Then reconfigure DRAFT to recognize the new library. For example, to COMPOSE the sample files, enter the following commands on the DOS command line. The file COMPOSER.EXE and the sample files must be in the same directory.

```
COMPOSER SAMPLE_1.SRC SAMPLE_1.LIB   <RETURN>
COMPOSER SAMPLE_2.SRC SAMPLE_2.LIB   <RETURN>
COMPOSER SAMPLE_3.SRC SAMPLE_3.LIB   <RETURN>
```

Then, reconfigure DRAFT, as outlined in Section 2. You can add one or more of the resulting library files. DRAFT expects the library files

to have a pathname constructed by placing the library prefix (set with the LP command) before the library file (set with the LF command).

7.6.1 SAMPLE_1.SRC: A Block Symbol Library Source File

```
(Beginning of source file, SAMPLE_1.SRC)

PREFIX
END
(The following are memory devices)

(1K x 4 static RAM)
'2114'  '2148'  '2149'  '5513'  '5514'  '9114'  '9124'
6       14      1
L1      5       IN      'A0'
L2      6       IN      'A1'
L3      7       IN      'A3'
L4      4       IN      'A4'
L5      3       IN      'A5'
L6      2       IN      'A6'
L7      1       IN      'A7'
L8      17      IN      'A7'
L9      16      IN      'A8'
L10     15      IN      'A9'
L12     8       IN      'C\S\'
L13     10      IN      'W\E\'
R1      14      HIZ     'D0'
R2      13      HIZ     'D1'
R3      12      HIZ     'D2'
R4      11      HIZ     'D3'
T0      18      PWR     'VCC'
B0      9       PWR     'GND'
```

{All of the above memory devices have the same block symbol. The part's size is 6X by 14Y, and it has one part per package.}

```
(256K x 1 dynamic RAM)
'21256'  '51C256' '50256'  '50257'  '81256'  '81257'  '6256'
'6257'   '4256'   '4257'   '41256'  '37256'
6        14       1
L1       5        IN       'A0'
L2       7        IN       'A1'
L3       6        IN       'A2'
L4       12       IN       'A3'
L5       11       IN       'A4'
L6       10       IN       'A5'
L7       13       IN       'A6'
L8       9        IN       'A7'
L9       1        IN       'A8'
L11      4        IN       'R\A\S'
L12      15       IN       'C\A\S\'
L13      3        IN       'W\E\'
R1       14       HIZ      'D0'
```

```
R3        2         IN        'D1'
T0        8         PWR       'VCC'
B0        16        PWR       'VSS'

(4K x 8 EPROM)
'2732'
7         16        1
L1        8         IN        'A0'
L2        7         IN        'A1'
L3        6         IN        'A2'
L4        5         IN        'A3'
L5        4         IN        'A4'
L6        3         IN        'A5'
L7        2         IN        'A6'
L8        1         IN        'A7'
L9        23        IN        'A8'
L10       22        IN        'A9'
L11       19        IN        'A10'
L12       21        IN        'A11'
L14       18        IN        'C\E\'
L15       20        IN        'O\E\/VPP'
R1        9         HIZ       'O0'
R2        10        HIZ       'O1'
R3        11        HIZ       'O2'
R4        13        HIZ       'O3'
R5        14        HIZ       'O4'
R6        15        HIZ       'O5'
R7        16        HIZ       'O6'
R8        17        HIZ       'O7'
T0        24        PWR       'VCC'
B0        12        PWR       'GND'
```

{The following are microprocessor devices}

```
'8086MAX'
13        32        1
R1        16        I/O       'AD0'
R2        15        I/O       'AD1'
R3        14        I/O       'AD2'
R4        13        I/O       'AD3'
R5        12        I/O       'AD4'
R6        11        I/O       'AD5'
R7        10        I/O       'AD6'
R8        9         I/O       'AD7'
R9        8         I/O       'AD8'
R10       7         I/O       'AD9'
R11       6         I/O       'AD10'
R12       5         I/O       'AD11'
R13       4         I/O       'AD12'
R14       3         I/O       'AD13'
R15       2         I/O       'AD14'
R16       39        I/O       'AD15'
R17       38        OUT       'A16/S3'
```

```
R18       37          OUT       'A17/S4'
R19       36          OUT       'A16/S5'
R20       35          OUT       'A19/S6'
R22       34          OUT       'B\H\E\/S7'
R24       26 DOT      OUT       'S0'
R25       27 DOT      OUT       'S1'
R26       28 DOT      OUT       'S2'
R28       32          OUT       'R\D\'
R29       29 DOT      OUT       'LOCK'
R30       25          OUT       'QS0'
R31       24          OUT       'QS1'
L3        22          IN        'READY'
L4        19          CLK IN    'CLK'
L5        21          IN        'RESET'
L7        18          IN        'INTR'
L27       31 DOT      I/O       'RQ/GT0'
L28       30 DOT      I/O       'RQ/GT1'
L29       17          IN        'NMI'
L30       23 DOT      IN        'TEST'
L31       33          IN        'M\X\'
T0        40          PWR       'VCC'
B0        20          PWR       'GND'
B5        1           PWR       'GND'
```

(This device is in a pin-grid array package. Notice the keyword GRIDARRAY in place of parts per package)

```
'68020'
16        53          GRIDARRAY
L1        C2                    CLK IN    'CLK'
L3        J12 DOT               IN        'IPL0'
L4        J13 DOT               IN        'IPL1'
L5        H12 DOT               IN        'IPL2'
L7        H2  DOT               IN        'AVEC'
L8        A1  DOT               IN        'BGACK'
L9        B3  DOT               IN        'BR'
L10       J2  DOT               IN        'BERR'
L11       H1  DOT               IN        'CDIS'
L13       H3  DOT               IN        'DSACK0'
L14       J1  DOT               IN        'DSACK1'
L21       K13                   I/O       'D0'
L22       K12                   I/O       'D1'
L23       L13                   I/O       'D2'
L24       L12                   I/O       'D3'
L25       M13                   I/O       'D4'
L26       M12                   I/O       'D5'
L27       M11                   I/O       'D6'
L28       L10                   I/O       'D7'
L29       N12                   I/O       'D8'
L30       N11                   I/O       'D9'
L31       M10                   I/O       'D10'
L32       L9                    I/O       'D11'
L33       N10                   I/O       'D12'
```

L34	M5	I/O	'D13'
L35	N4	I/O	'D14'
L36	L4	I/O	'D15'
L37	M4	I/O	'D16'
L38	N6	I/O	'D17'
L39	M6	I/O	'D18'
L40	L6	I/O	'D19'
L41	N5	I/O	'D20'
L42	M5	I/O	'D21'
L43	N4	I/O	'D22'
L44	L5	I/O	'D23'
L45	M4	I/O	'D24'
L46	N3	I/O	'D25'
L47	M3	I/O	'D26'
L48	L4	I/O	'D27'
L49	N2	I/O	'D28'
L50	M2	I/O	'D29'
L51	L3	I/O	'D30'
L52	N1	I/O	'D31'
R1	C4	OUT	'A0'
R2	A2	OUT	'A1'
R3	E12	OUT	'A2'
R4	D13	OUT	'A3'
R5	D12	OUT	'A4'
R6	C13	OUT	'A5'
R7	B13	OUT	'A6'
R8	C12	OUT	'A7'
R9	A13	OUT	'A8'
R10	C11	OUT	'A9'
R11	B12	OUT	'A10'
R12	A12	OUT	'A11'
R13	C10	OUT	'A12'
R14	B11	OUT	'A13'
R15	A11	OUT	'A14'
R16	B10	OUT	'A15'
R17	C9	OUT	'A16'
R18	C8	OUT	'A17'
R19	B8	OUT	'A18'
R20	A8	OUT	'A19'
R21	B7	OUT	'A20'
R22	C7	OUT	'A21'
R23	A7	OUT	'A22'
R24	A6	OUT	'A23'
R25	B6	OUT	'A24'
R26	C6	OUT	'A25'
R27	A5	OUT	'A26'
R28	B5	OUT	'A27'
R29	A4	OUT	'A28'
R30	C5	OUT	'A29'
R31	B4	OUT	'A30'
R32	A3	OUT	'A31'
R34	F13 DOT	OUT	'IPEND'
R35	B2 DOT	OUT	'BG'
R37	E1	OUT	'FC0'

```
R38     F3              OUT     'FC1'
R39     F2              OUT     'FC2'
R41     F1              OUT     'SIZ0'
R42     G2              OUT     'SIZ1'
R43     G3   DOT        OUT     'DBEN'
R44     G1   DOT        OUT     'ECS'
R45     E13  DOT        OUT     'OCS'
R46     E2   DOT        OUT     'RMC'
R47     L1   DOT        OUT     'AS'
R48     M1   DOT        OUT     'DS'
R50     L2              OUT     'R/W\'
R51     K2   DOT        I/O     'HALT'
R52     C1   DOT        I/O     'RESET'
T0      A9              PWR     'VCC'
T1      D1              PWR     'VCC'
T3      D2              PWR     'VCC'
T6      E3              PWR     'VCC'
T9      G11             PWR     'VCC'
T12     G13             PWR     'VCC'
T15     M8              PWR     'VCC'
T16     N8              PWR     'VCC'
B0      A10             PWR     'GND'
B1      G12             PWR     'GND'
B3      H13             PWR     'GND'
B6      J3              PWR     'GND'
B9      K1              PWR     'GND'
B12     L7              PWR     'GND'
B15     N7              PWR     'GND'
B16     B9              PWR     'GND'

(End of source file, SAMPLE_1.SRC)
```

7.6.2 SAMPLE_2.SRC: A TTL Block Symbol Library Source File

```
(Beginning of the source file, SAMPLE_2.SRC)

PREFIX
'74LS'      =     'LS'
'74S'       =     'S'
'74ALS'     =     'ALS'
'74AS'      =     'AS'
'74HCT'     =     'HCT'
'74HC'      =     'HC'
'74ACT'     =     'ACT'
'74AC'      =     'AC'
'74F'       =     'F'
'74'
END


'7442' '74LS42' '74HC42' '7443' '7444'
S       11          1
L4      1           IN          'A'
L5      15          IN          'B'
L6      13          IN          'C'
L7      12          IN          'D'
R10     11          DOT OUT     '9'
R9      10          DOT OUT     '8'
R8      9           DOT OUT     '7'
R7      7           DOT OUT     '6'
R6      6           DOT OUT     '5'
R5      5           DOT OUT     '4'
R4      4           DOT OUT     '3'
R3      3           DOT OUT     '2'
R2      2           DOT OUT     '1'
R1      1           DOT OUT     '0'
T0      16          PWR         'VCC'
B0      8           PWR         'GND'


'7446' '7447' '74LS47'
S       8           1
L1      4           IN          'R\B\0\'
L2      5           IN          'R\B\1\'
L3      3           IN          'L\T\'
L4      7           IN          '1'
L5      1           IN          '2'
L6      2           IN          '4'
L7      6           IN          '8'
R7      14          DOT OC      'G'
R6      15          DOT OC      'F'
R5      9           DOT OC      'E'
R4      10          DOT OC      'D'
R3      11          DOT OC      'C'
```

```
R2          12          DOT OC      'B'
R1          13          DOT OC      'A'
T0          16          PWR         'VCC'
B0          8           PWR         'GND'


'74?4'   '74ALS74' '74AS74' '74LS74' '74S74'
'74HC74' '74AC74'
6           6           2
L2          2           12          IN          'D'
L4          3           11          CLK IN      'CK'
B3          1           13          DOT IN      'CL'
T3          4           10          DOT IN      'P'
R4          6           8           OUT         'Q\'
R2          5           9           OUT         'Q'
T0          14          14          PWR         'VCC'
B0          7           7           PWR         'GND'
```

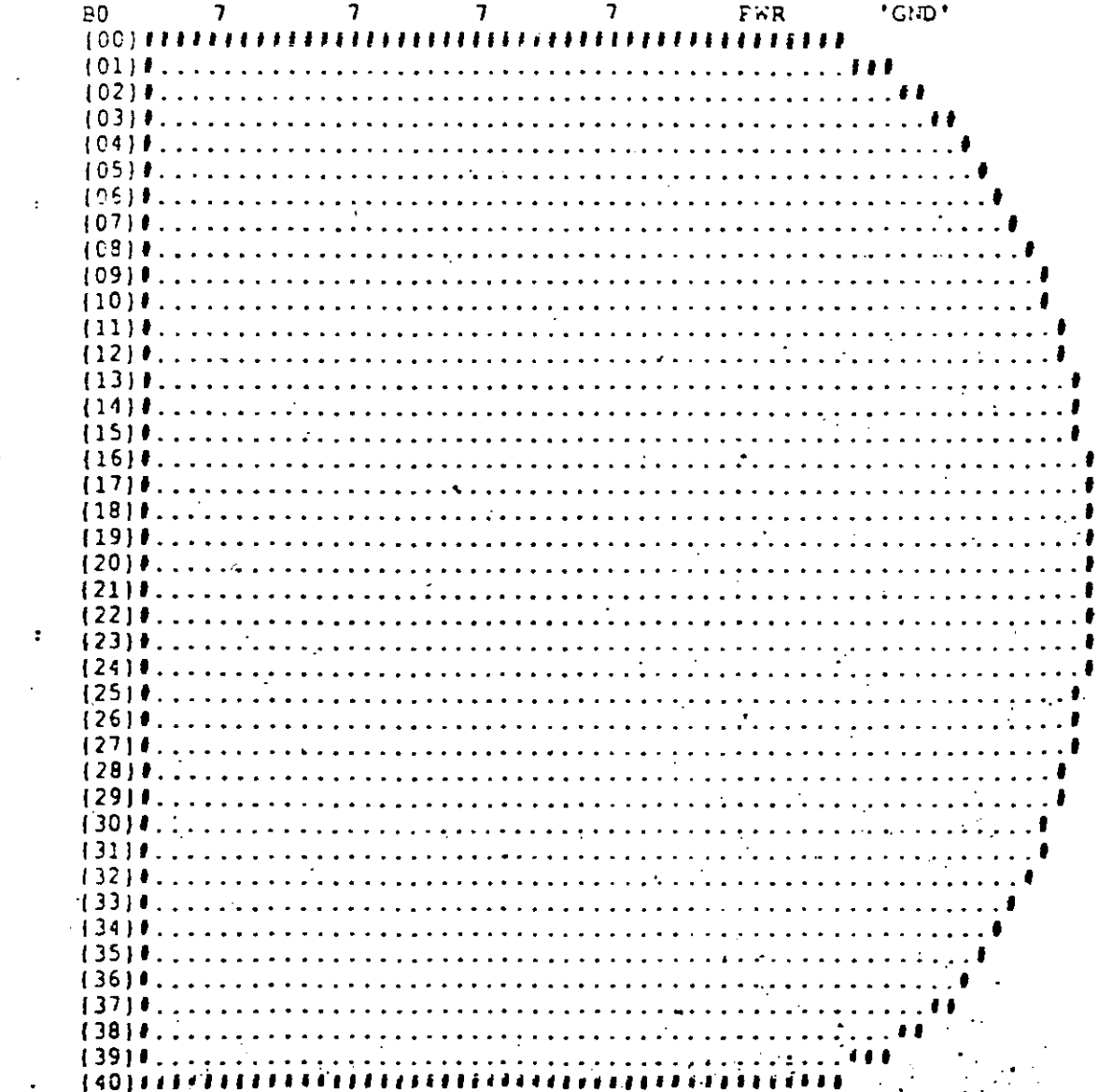
{This part has two parts per package. The far left column represents the pin position. The second column contains the pin numbers of the first D flip-flop in the package. The third column contains the pin number of the second D flip-flop in the package. Note the power pins on 14 and 7. They are required for both devices.}

```
'74ALS160' '74AS160' '74LS160' '74HC160'
'74ALS161' '74AS161' '74LS161' '74HC161'
'74ALS162' '74AS162' '74LS162' '74S162' '74HC162'
'74ALS163' '74AS163' '74LS163' '74S163' '74HC163'
8           10          1
B4          1           DOT IN      'CL'
L1          9           DOT IN      'LD'
L2          10          IN          'ENT'
L3          7           IN          'ENP'
L4          2           CLK IN      'CLK'
L6          3           IN          'A'
L7          4           IN          'B'
L8          5           IN          'C'
L9          6           IN          'D'
R9          11          OUT         'QD'
R8          12          OUT         'QC'
R7          13          OUT         'QB'
R6          14          OUT         'QA'
R4          15          OUT         'CO'
T0          16          PWR         'VCC'
B0          8           PWR         'GND'
```

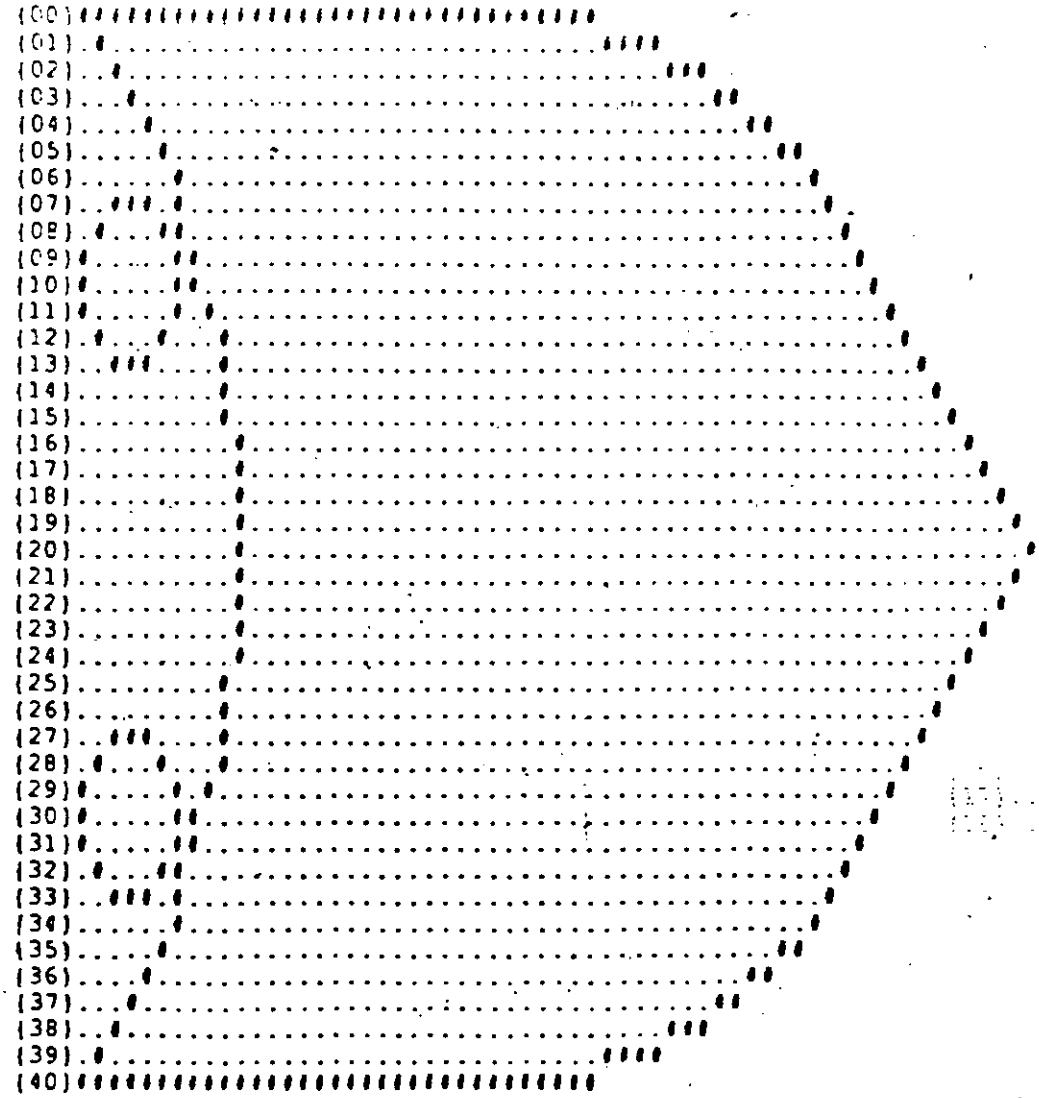
{End of the source file, SAMPLE_2.SRC}

7.6.3 SAMPLE_3.SRC: A Bitmap Symbol Library Source File

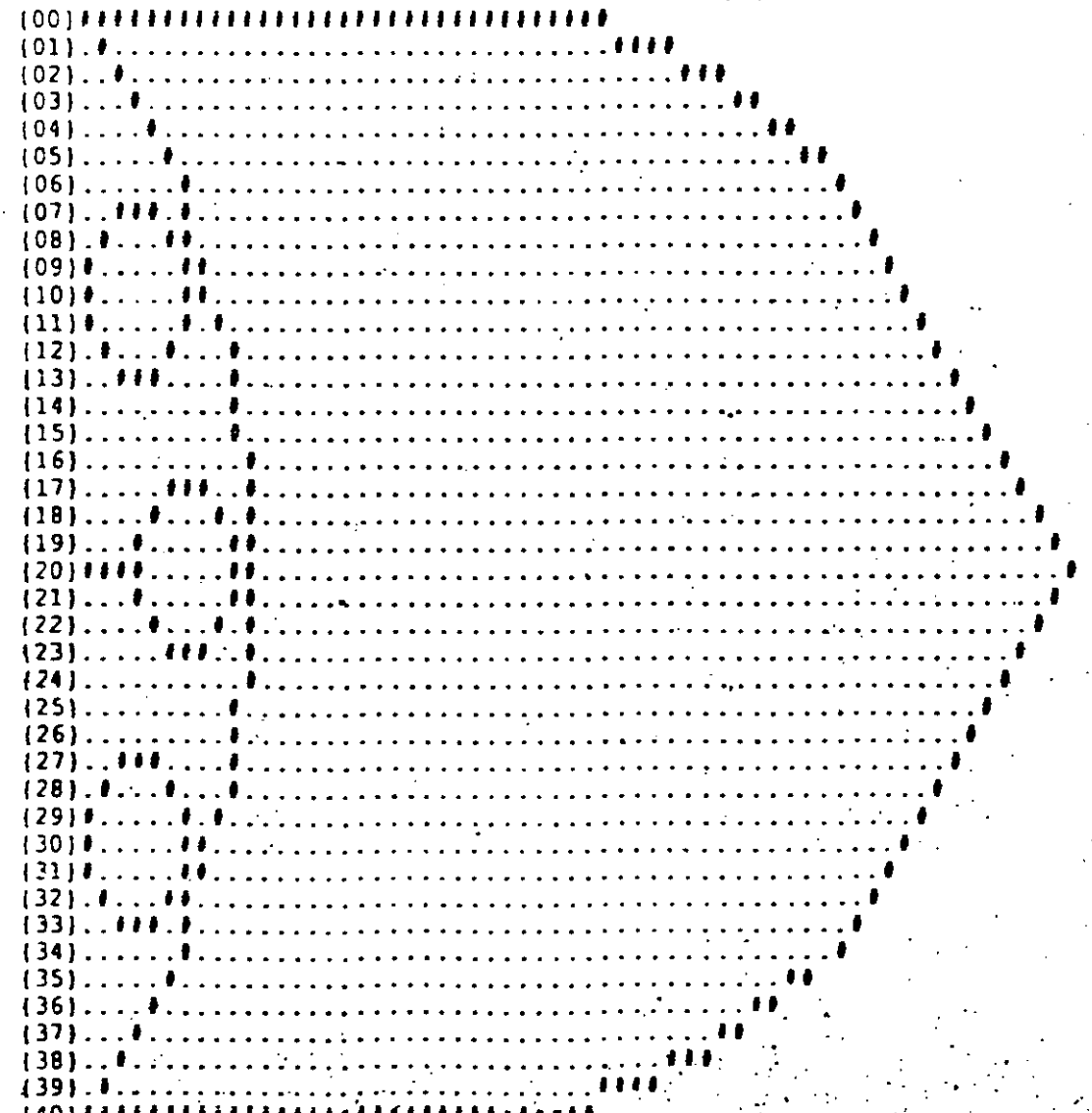
```
{Beginning of the source file, SAMPLE_3.SRC}

PREFIX
END

'7400'
6       4       4
L1      1       4       9       12      IN      'I0'
L3      2       5       10      13      IN      'I1'
R2      3       6       8       11 DOT  OUT     'O'
T0      14      14      14      14      PWR     'VCC'
B0      7       7       7       7       PWR     'GND'
```



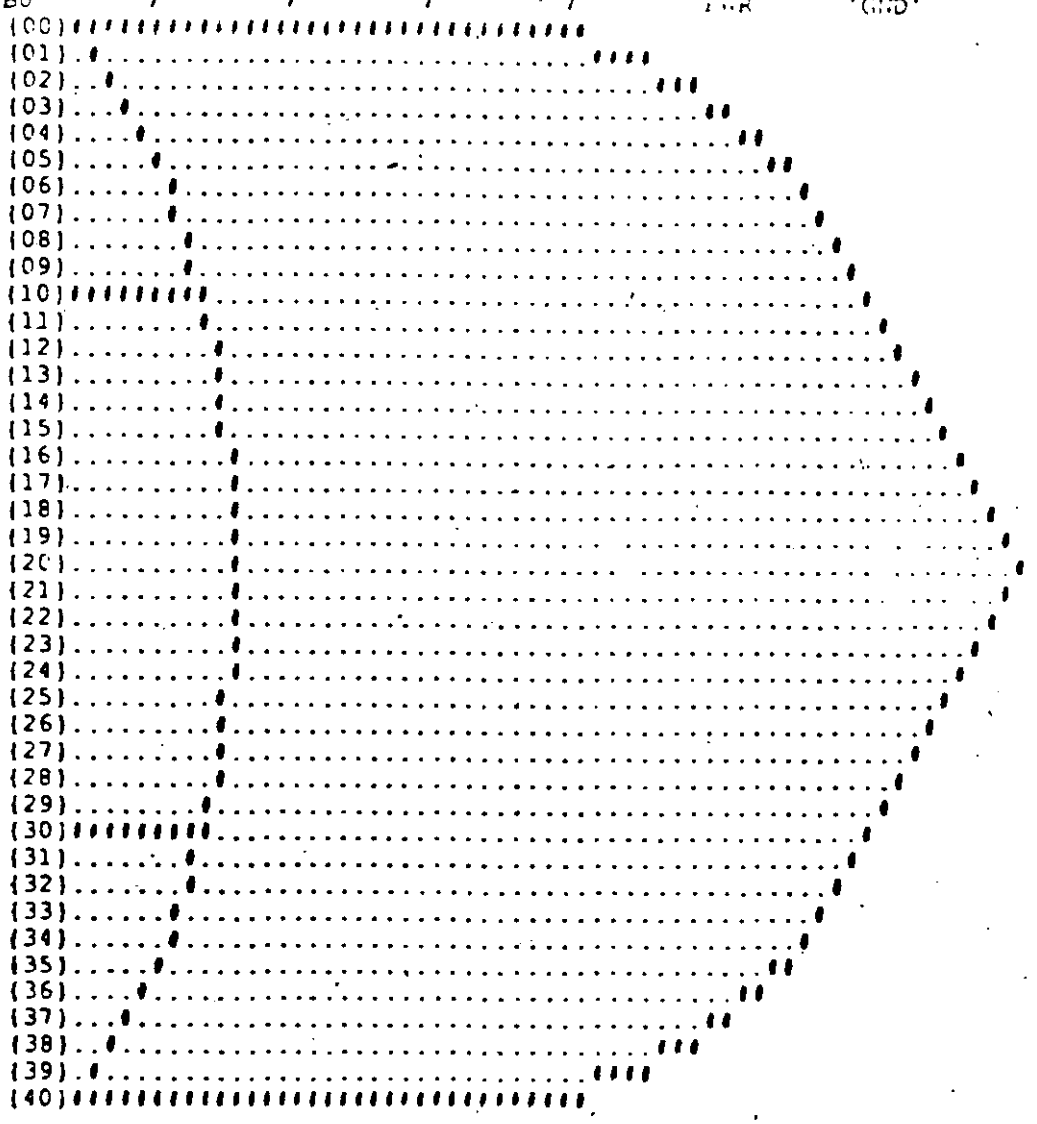
```
CONVERT
L1        1         4         9         12        IN        'I0'
L3        2         5         10        13        IN        'I1'
R2        3         6         8         11        OUT       'O'
T0        14        14        14        14        PWR       'VCC'
B0        7         7         7         7         PWR       'GND'
```



```
'74ALS10'
6          4          3
L1         1          3          9          IN         'I0'
L2         2          4          10         IN         'I1'
L3         13         5          11         IN         'I2'
R2         12         6          8  DOT     OUT        'O'
T0         14         14         14         PWR        'VCC'
B0         7          7          7          PWR        'GND'
BITMAP '7400'
CONVERT
L1         1          3          9          IN         'I0'
L2         2          4          10         IN         'I1'
L3         13         5          11         IN         'I2'
R2         12         6          8          OUT        'O'
T0         14         14         14         PWR        'VCC'
B0         7          7          7          PWR        'GND'
```



```
'7402'
6          4          4
L1         2          5          8          11         IN         '10'
L3         3          6          9          12         IN         '11'
R2         1          4          10         13 DOT     OUT        'O'
T0         14         14         14         14         PWR        'VCC'
B0         7          7          7          7          PWR        'GND'
```



```
CONVERT
L1        2         5         8         11        DOT       IN'I0'
L3        3         6         9         12        DOT       IN'I1'
R2        1         4         10        13                  OUT'O'
T0        14        14        14        14        PWR'VCC'
B0        7         7         7         7         PWR'GND'
BITMAP '7400'

'7433' '74LS33' '74ALS33'
6.        4         4
L1        2         5         8         11                  IN'I0'
L3        3         6         9         12                  IN'I1'
R2        1         4         10        13        DOT       OUT'O'
T0        14        14        14        14        PWRVCC'
B0        7         7         7         7         PWR'GND'
BITMAP '7402'
CONVERT
L1        2         5         8         11        DOT       IN'I0'
L3        3         6         9         12        DOT       IN'I1'
R2        1         4         10        13                  OUT'O'
T0        14        14        14        14        PWR'VCC'
B0        7         7         7         7         PWR'GND'
BITMAP '7400'
```

(The following are electrical and electronic parts)

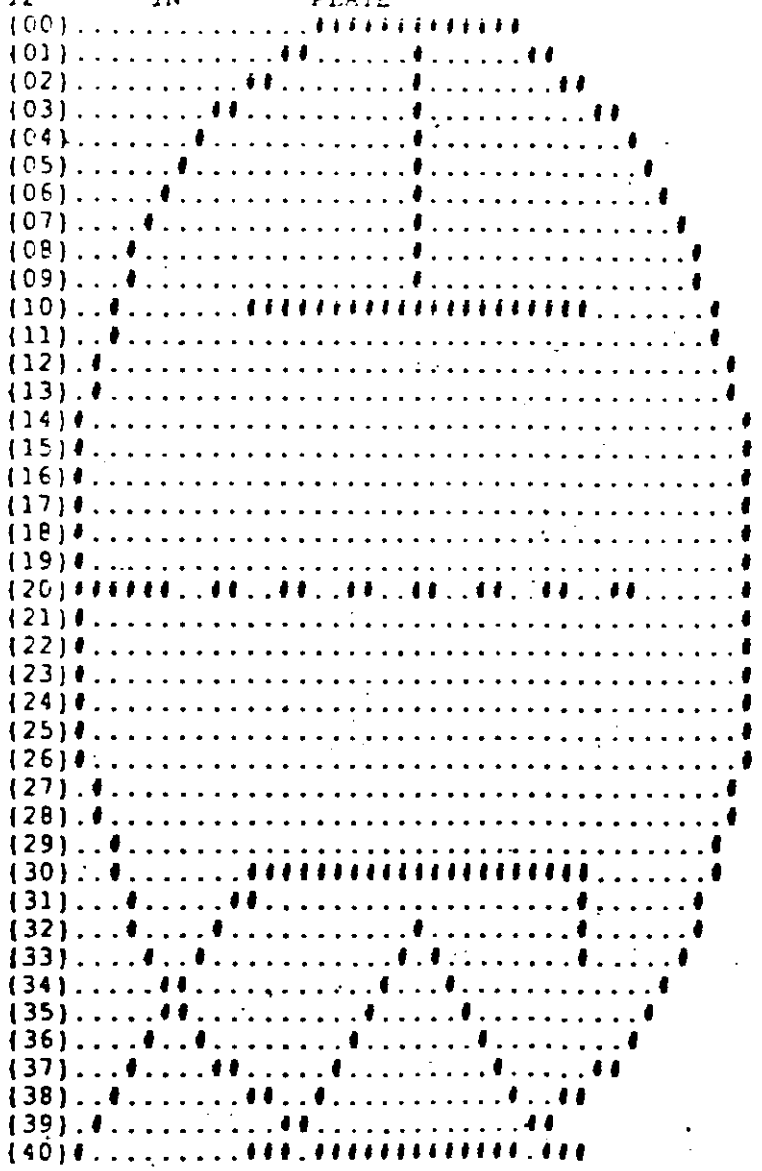
```
'ANTENNA'
2                   1         0
B1                  OUT       'ANT'
(  0)####################
(  1).#.......#.......#.
(  2)..#.....#.....#..
(  3)...#...#...#...
(  4)....#.#.#....
(  5).....#.#.....
(  6)....#...#....
(  7)...#.....#...
(  8)..#.......#..
(  9).#.........#.
( 10)#...........#
```

```
'CAP'
'CAPACITOR'
REFERENCE  'C'
(X Size =) 2       (Y Size =) 1       (Parts per Package =)) 0
T1        SHORT    PAS       '1'
B1        SHORT    PAS       '2'
(  0).....#.....
(  1).....#.....
(  2).####################.
(  3).....#.....
(  4).....#.....
(  5).....#.....
(  6).....#.....
(  7).....#.....
(  8)...###.....#.....###...
(  9).##.....#.....##.
( 10).....#.....
```

```
'GND POWER'
(X Size =)  2      (Y Size =)  1      (Parts per Package =)  0
T1                 PWR       'GND'
(  0)#####################
(  1).....#.....
(  2).....#.....
(  3)...#################...
(  4).....#.....
(  5).....#.....
(  6).....#.....
(  7).....#.....
(  8).....#.....
(  9).....###.....
( 10).....#.....
```

```
'MOSFET N'
REFERENCE  'Q'
3          2          0
L2         SHORT      IN         'GATE'
T2         SHORT      IN         'DRAIN',
B2         SHORT      IN         'SOURCE'
(  0).........#...........#...........
(  1).........#...........#...........
(  2)....#....############............
(  3)....#....#.......................
(  4)....#....#.......................
(  5)....#....#.....#.................
(  6)....#....#....##.................
(  7)....#....#...###.................
(  8)....#....#..####.................
(  9)....#....#.#####.................
( 10)....#....############............
( 11)....#....#.#####.....#...........
( 12)....#....#..####.....#...........
( 13)....#....#...###.....#...........
( 14)....#....#....##.....#...........
( 15)....#....#.....#.....#...........
( 16)....#....#...........#...........
( 17)....#....#...........#...........
( 18)....#....############............
( 19)....#....#...........#...........
( 20)#####....#...........#...........
```

```
'TRIODE'
4          4          0
L2         IN         'GRID'
B0         IN         'CATHODE'
B1         IN         'FILAMENT_1'
B3         IN         'FILAMENT_2'
T2         IN         'PLATE'
```



APPENDIX A

SUMMARY OF LIBRARY COMPONENTS

Directory of ANALOG.LIB

1458	1558	7621	ADC0801
ADC0802	ADC0803	ADC0804	ADC0805
ADC0808	ADC0809	DAC0800	DAC0801
DAC0802	DAC0806	DAC0807	DAC0808
DAC0808	LF13741H	LF13741N	LF147D
LF147N	LF155H	LF156H	LF157H
LF255H	LF256H	LF257H	LF347D
LF347N	LF351H	LF351N	LF353H
LF353N	LF355H	LF355N	LF356H
LF356N	LF357H	LF357N	LF411H
LF411N	LF412H	LF412N	LF441M
LF441N	LF442H	LF442N	LF444D
LF444N	LH0002N	LH0003H	LH0004H
LM101H	LM101J	LM101J14	LM102H
LM107H	LM107J	LM107J14	LM108H
LM108J	LM108J8	LM10H	LM10N
LM11D	LM11H	LM11N	LM124
LM13080N	LM13080P	LM1458H	LM1458J
LM1458N	LM146J	LM148J	LM149
LM1558H	LM1558J	LM158H	LM159J
LM192H	LM192J	LM201H	LM201J
LM201J14	LM202H	LM207H	LM207J
LM207J14	LM208H	LM208J	LM208J8
LM216H	LM224	LM246J	LM246N
LM248	LM248J	LM258H	LM2900J
LM2900N	LM2904N	LM2924J	LM2924M
LM292H	LM292J	LM301H	LM301J
LM301J14	LM301N	LM302H	LM307H
LM307J	LM307J14	LM307N	LM308H
LM308J	LM308J8	LM316H	LM324
LM3301N	LM339	LM3401N	LM346J
LM346N	LM348	LM348J	LM348M
LM349N	LM358H	LM358M	LM358J
LM359N	LM3900N	LM392H	LM392J
LM392N	LM4250M	LM4250J	LM555
LM709H	LM709N	LM709N8	LM725H

LM725H LM741L LM741M LM741J/8
LM741N LM741N/8 LM747 LM747H
LM747J LM748H LM748J LM748N
LM7805 LM7806 LM7808 LM7810
LM7812 LM7815 LM7818 LM7824
LM788S MC1455 MC1555 MC1741
NE555 OPAMP TL072 TL082
TL092 UA741 VOLTAGE REGULATOR

Directory of ASSEMBLY.LIB

08 PIN 14 PIN 16 PIN 24 PIN
28 PIN 40 PIN SOCKET 40 PIN TOP CAP 2X7
EDGE CONNECTOR RESISTOR 0X2 RESISTOR 1X3 RESISTOR 1X5
RESISTOR PACK TO 220 TO 39 TO 92
XTAL

Directory of CMOS.LIB

4000	4001	4002	4006	4007	4008	4009	4010	4011
4012	4013	4014	4015	4016	4017	4018	4019	4020
4021	4022	4023	4024	4025	4026	4027	4028	4029
4030	4031	4032	4033	4034	4035	4037	4038	4040
4041	4042	4043	4044	4045	4046	4047	4048	4049
4050	4051	4052	4053	4054	4055	4056	4057	4059
4060	4063	4066	4068	4069	4070	4071	4072	4073
4075	4076	4077	4078	4081	4082	4085	4086	4089
4093	4094	4095	4096	4098	4099	4501	4502	4503
4504	4505	4506	4508	4510	4511	4512	4513	4514
4515	4516	4517	4518	4519	4520	4521	4522	4524
4526	4527	4528	4529	4530	4531	4532	4534	4536
4537	4538	4539	4541	4543	4544	4547	4549	4551
4552	4553	4554	4555	4556	4557	4558	4559	4560
4561	4562	4566	4568	4569	4572	4573	4574	4575
4580	4581	4582	4583	4584	4585	4597	4598	4599
5101	14000	14001	14002	14006	14007	14008	14011	14012
14013	14014	14015	14016	14017	14018	14020	14021	14022
14023	14024	14025	14027	14028	14029	14032	14034	14035
14038	14040	14042	14043	14044	14046	14051	14052	14053
14066	14068	14069	14070	14071	14072	14073	14075	14076
14077	14078	14081	14082	14093	14094	14099	14160	14161
14162	14163	14174	14175	14194	14501	14502	14503	14504
14505	14506	14508	14510	14511	14512	14513	14514	14515
14516	14517	14518	14519	14520	14521	14522	14526	14526
14527	14528	14529	14530	14531	14532	14534	14536	14537
14538	14539	14541	14543	14546	14547	14548	14551	14552
14553	14554	14555	14556	14557	14558	14559	14560	14561
14562	14566	14568	14569	14572	14573	14574	14575	14580
14581	14582	14583	14584	14585	14587	14595	14598	40109

40101 40102 40103 40104 40105 40106 40115 40116 40160
40161 40162 40163 40174 40175 40182 40192 40193 40194
42100 45100 45101 45104 45106 45107 45109 45112 145104
145106 145107 145109 145112

Directory of DEVICE.LIB

12 HEADER
1RSW10
1RSW12
1RSW3
1RSW6
2RSW12
2RSW3
2RSW5
4 HEADER
ANTENNA
BATTERY
BNC
BRIDGE
BUZZER
CAP
CAPACITOR
CAPACITOR FEED
CAPACITOR POL
CAPACITOR VAR
CIRCUIT BREAKER
COAX
CONNECTOR COAX
CONNECTOR COAX-F
CONNECTOR COAX-M
CONNECTOR DB15
CONNECTOR DB25
CONNECTOR DB9
CRYSTAL
DIODE
DIODE BREAKDOWN
DIODE SCHOTTKY
DIODE TUNNEL
DIODE VARACTOR
DIODE ZENER
DIODE ZENER1
FUSE
GND EARTH
GND FIELD SIGNAL
GND POWER
GND SIGNAL
GTO
INDUCTOR
INDUCTOR IRON
INDUCTOR IRON1
INDUCTOR ISOLATED
INDUCTOR VAR
INDUCTOR VARIABLE IRON
JFET N
JFET P
JUMPER
LAMP
LAMP NEON
LED
METER AMP
METER MA
METER MV
METER UA
METER UV
METER VOLT
METER VU
MICROPHONE
MOSFET DUAL G/N
MOSFET DUAL G/P
MOSFET N
MOSFET P
MOTOR SERVO
MOTOR STEPPER
NPN
NPN DAR
NPN DIAC
OPTO ISOLATOR
OPTO ISOLATOR-A
PHONEJACK
PHONEJACK STEREO
PHONEJACK STEREO.SW
PHONEPLUG
PHOTO NPN
PHOTODIODE
PLUG AC FEMALE
PLUG AC MALE
PNP
PNP DAR
PNP DIAC
POT
R
R-PACK
RCA JACK
RELAY DPST
RELAY SPDT
RELAY SPST
RESISTOR
RESISTOR 8PACK
RESISTOR BRIDGE
RESISTOR TAPPED
RESISTOR VAR
RESISTOR VAR 2
SCR
SIGNAL AC
SOURCE CURRENT
SOURCE VOLTAGE
SPARK GAP
SPARK GAP CAP
SPEAKER
SW DIP-4
SW DIP-8
SW POSHBUTTON
SW SPDT
SW SPST
THERMAL FUSE
THERMISTOR
TRANSFORMER
TRANSFORMER AIR CORE
TRANSFORMER CT
TRANSFORMER ISOLATED
TRANSFORMER STEPUP
TRANSFORMER VAR
TRANSCORE
TRIAC
TRIAC DRIVER
TRIGGERED SPARK GAP
TRIODE
TUBE PHOTO MULTIPLIER
UJT N
UJT P
VARISTOR

Directory of ECLLIB:

MC10100	MC10101	MC10102	MC10103	MC10104	MC10105	MC10106
MC10107	MC10109	MC10110	MC10111	MC10113	MC10114	MC10115
MC10116	MC10117	MC10118	MC10119	MC10122	MC10123	MC10124
MC10125	MC10128	MC10129	MC10130	MC10131	MC10132	MC10133
MC10134	MC10135	MC10136	MC10137	MC10138	MC10139	MC10141
F10145A	MC10153	MC10154	MC10158	MC10159	MC10160	MC10161
MC10162	MC10163	MC10164	MC10165	MC10166	MC10168	MC10170
MC10171	MC10172	MC10173	MC10174	MC10175	MC10176	MC10177
MC10178	MC10179	MC10180	MC10181	MC10182	MC10186	MC10188
MC10189	MC10190	MC10191	MC10193	MC10195	MC10197	MC10210
MC10211	MC10212	MC10216	MC10231	F10402	F10414	F10415
F10416	F10422	F10470	F10474	MC10500	MC10501	MC10502
MC10503	MC10504	MC10505	MC10506	MC10508	MC10514	MC10515
MC10516	MC10517	MC10518	MC10519	MC10527	MC10530	MC10531
MC10532	MC10534	MC10535	MC10536	MC10537	MC10538	MC10539
MC10541	MC10558	MC10559	MC10560	MC10561	MC10562	MC10563
MC10564	MC10565	MC10566	MC10568	MC10570	MC10571	MC10572
MC10574	MC10575	MC10576	MC10578	MC10579	MC10580	MC10581
MC10582	MC10586	MC10588	MC10590	MC10591	MC10593	MC10595
MC10597	MC10610	MC10611	MC10612	MC10616	MC10631	F100101
F100102	F100107	F100112	F100113	F100114	F100117	F100118
F10012	F100123	F100124	F100125	F100126	F100130	F100131
F100136	F100141	F100142	F100145	F100150	F100151	F100155
F100156	F100158	F100160	F100163	F100164	F100165	F100166
F100171	F100179	F100180	F100181	F100182	F100183	F100184
F100472	F100216	F100425	F100426	F100427	F100470	F100478

F100170/4
F100170/8

Directory of INTEL_LIB

280	280PIO	8031	80C31	8032	8035	80C35
8039	80C39	8040	8041	8042	8044	8048
80C48	8049	80C49	8050	8051	80C51	8052
8085	8086MAX	8086MIN	8087	8088MAX	8088MIN	8089
8096	8097	8155	8156	8185	8203	8205
8206	8207	8208	8212	8216	8226	8231
8237	8237A	8243	8251	8251A	8253	8254
82C54	8255	82C55	8256	8257	8259A	8272
8272A	8273	8274	8275	8276	8279	8282
8283	8284	8286	8287	8288	8289	8291
8292	8294	8294A	8295	8344	8396	8397
8641	8741	8742	8744	8748	8749	8751
8755	80186	80188	80286	80287	80386	8206-2
82062	82064	82188	82284	82288	82289	82364
82501	82530	82586MA	82586MI	82596EI	82EEHM	82720
82731						

Directory of MEMORY.LIB

10H8	10L8	12H6	12L6	14H4	14L4	14L8	16C1
16H2	16L2	16A4	16R4	16RP4	16X4	16L6	16PR6
16R6	16H8	16HD8	16L8	16LD8	16P8	16R8	16RP8
16V8	16Z8	18L4	18P8	20C1	20L2	20R4	20X4
20R6	20L8	20R8	20V8	20X8	315	406	426
12L10	1400	1420	1421	1430	1600	1601	18S42
18S46	18SA46	20L10	20X10	2015	2016	2018	2019
2063	2064	2068	2069	2114	2115	2125	2130
2141	2147	2148	2149	2164	2167	2168	2186
2187	22V10	24S10	24SA10	24S41	24SA41	24S81	2600
2620	2630	27S12	27S1E	27S18	27S19	27S20	27S21
27S29	27S30	27S31	27S32	27S32	27S33	27S40	27S41
27S43	2764	27C64	2816	2817	2864	28S86	3628
3636	3764	39V18	4015	4044	4104	4161	4164
4256	4257	4264	4416	4564	4864	48C64	5063
5133	5143	51C64	51C65	51C66	51C67	51C68	51C69
52B13	52B23	52B33	5301	5305	5306	5330	5331
5340	5341	5349	5352	5353	538I	5513	5514
5516	5517	5564	5565	5600	5604	5605	5610
5623	5624	5625	6116	6147	6164	6167	6256
6257	6264	6267	6287	6301	6305	6306	6330
6331	6340	6341	6349	6352	6353	6380	6381
6665	7051	7052	7053	7056	7057	7058	7121E
7122E	712BE	7131	7132	7134	7137	7138	7142E
7602	7603	7610	7611	7620	7621	7640	7641
7642	7643	7649	7680	7681	7685	8128	8167
8168	82S23	8264	8266	8281	8416	8417	841R
8464	87C64	9044	9064	9114	9124	9126	9244
9864	99C68	18S030	18SA030	21256	25044	25045	25085

25088 25089 25168 25169 27010 27011 27128 27512B
27512L 27512S 27513D 27513L 27520D 27210 27256 27C256
27S25D 27S27L 27S29D 27S29L 27S12 27S13 27916 28S11B
28S166 29611 29621 29625 29630 29631 29651 29661
29680 29681 37256 41256 48416 50256 50257 51C256
51C259 57256 74S188 74S287 74S288 74S387 74S472 74S474
74S475 74S570 74S571 74S572 74S573 76160 76161 76168
76165 76321 76641 81256 81257 81416 82S123 82S126
82S129 82S130 82S131 82S136 82S137 82S147 82S180 82S181
82S185 82S190 82S191 82S321 87S180 87S181 87S185 87S190
87S191 87S280 87S281 87S290 87S291 93415 93417 93425
93427 93436 93438 93446 93448 93L450 93L451 93452
93453 93S10 93S11 93S12 93S41 63S168L

Directory of MOTOLIB:

6800 6800 6850 6801 6801EM 6801RM 6802
6802NS 6803 6803EM 6808 6809 6809E 68HC09E
6810 6821 6822 6829 68HC34 6835 6839
6840 6844 6845 6846 6847 6847T 6850
6852 6854 6875 6875A 68000CC 68000D 68000GA
68000P 68000Q 68010CC 68010D 68010GA 6801U4 6801U4EM
6801U4NM 68020 6803U4 6803U4EM 6804J2 6804P2 68HC04P2
68HC04P3 6805K2 6805P2 6805R2 6805T2 6805U2 6805K3
6805R3 6805U3 6805P4 6805P6 68120EM 68120NM 68120SC
68121EM 68121NM 68121SC 68440 6845I 6868I 68901
6836S16 6836A16 6870SR3 6870SU3 6870S25 6870S05 146805E2
146805E4

Directory of RF.LIB:

AIR INDUCTOR AIR INDUCTOR VARIABLE AIR INDUCTOR WIPER
AIR T INDUCTOR ANTENNA DIPOLE ANTENNA MONOPOLE
ANTENNA-1 ANTENNA-2 ARROW
BOX CAPACITOR FEED CIRCLE
COAX PLUG COAX RECEPTACLE CONNECTOR COAX
CONNECTOR COAX-F CONNECTOR COAX-M CRT
ENVELOPE FLYBACK GROUNDED CAP
HOTLINE JACK PENTODE PHASE SHIFTER
PHASE SHIFTER VERT PHASE SHIFTER THICK PSE
PST RF DPDT RF SPDT
STDA115 STDA116 STEPUP
SWITCH NETWORK TETRODE TRANSMISSION LINE
TRANSMISSION SHIELD TRIODE TWICE VCAP

Directory of TTL.LIB

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
00	••	••	••	••	••	••	••	••	••	••
01	••	••	••	..	..	..	..	..	..	••
02	••	••	••	••	••	••	••	••	••	••
03	••	••	••	..	••	••	..	..	..	••
04	••	••	••	••	••	••	••	••	••	••
05	••	••	••	..	••	••	..	..	..	••
06	..	..	..	..	..	..	..	..	..	••
07	..	..	..	..	..	..	..	..	..	••
08	••	••	••	••	••	••	..	..	••	••
09	••	••	••	..	..	••	..	..	..	••
10	••	••	••	••	••	••	..	..	••	••
11	••	••	••	••	••	••	..	..	••	••
12	••	..	••	..	..	..	..	..	..	••
13	••	..	..	..	..	..	..	..	••	••
14	••	..	..	..	••	••	..	••	••	••
15	••	••	••	..	..	..	..	..	..	..
16	..	..	..	..	..	..	..	..	..	••
17	..	..	..	..	..	..	..	..	..	••
18	••	..	..	..	..	..	..	..	..	..
19	••	..	..	..	..	..	..	..	..	..
20	••	••	••	••	••	••	..	..	••	••
21	••	..	••	••	••	••	..	..	..	••
22	••	••	••	..	..	..	..	..	..	••
24	••	..	..	..	..	..	..	..	..	..
25	..	..	..	..	..	..	..	..	..	••
26	••	..	..	..	..	..	..	..	..	••
27	••	..	••	••	••	••	..	..	..	••
28	••	..	••	..	..	..	..	..	••	••
30	••	••	••	••	••	••	..	..	••	••
32	••	••	••	••	••	••	••	••	••	••
33	••	..	••	..	..	..	..	..	..	••
34	..	..	••	••	••	..	..	..	..	..
35	..	..	••	..	..	..	..	..	..	..
36	..	..	..	..	..	••	..	..	..	..
37	••	••	••	..	..	..	..	..	••	••
38	••	••	••	..	..	..	..	..	••	••
39	..	..	..	..	..	..	..	..	..	••

Directory of TTL.LIB Continued

	74LS	74S	74ALS	74LS	74HC	74HC	74AC	74AC	74F	74
40	••	••	••	••	••	••	••	••	••	••
42	••	••	••	••	••	••	••	••	••	••
43	••	••	••	••	••	••	••	••	••	••
44	••	••	••	••	••	••	••	••	••	••
45	••	••	••	••	••	••	••	••	••	••
46	••	••	••	••	••	••	••	••	••	••
47	••	••	••	••	••	••	••	••	••	••
48	••	••	••	••	••	••	••	••	••	••
49	••	••	••	••	••	••	••	••	••	••
50	••	••	••	••	••	••	••	••	••	••
51	••	••	••	••	••	••	••	••	••	••
54	••	••	••	••	••	••	••	••	••	••
55	••	••	••	••	••	••	••	••	••	••
56	••	••	••	••	••	••	••	••	••	••
57	••	••	••	••	••	••	••	••	••	••
60	••	••	••	••	••	••	••	••	••	••
63	••	••	••	••	••	••	••	••	••	••
64	••	••	••	••	••	••	••	••	••	••
65	••	••	••	••	••	••	••	••	••	••
68	••	••	••	••	••	••	••	••	••	••
69	••	••	••	••	••	••	••	••	••	••
70	••	••	••	••	••	••	••	••	••	••
72	••	••	••	••	••	••	••	••	••	••
73	••	••	••	••	••	••	••	••	••	••
74	••	••	••	••	••	••	••	••	••	••
75	••	••	••	••	••	••	••	••	••	••
76	••	••	••	••	••	••	••	••	••	••
77	••	••	••	••	••	••	••	••	••	••
78	••	••	••	••	••	••	••	••	••	••
30	••	••	••	••	••	••	••	••	••	••
82	••	••	••	••	••	••	••	••	••	••
83	••	••	••	••	••	••	••	••	••	••
85	••	••	••	••	••	••	••	••	••	••
86	••	••	••	••	••	••	••	••	••	••
90	••	••	••	••	••	••	••	••	••	••
91	••	••	••	••	••	••	••	••	••	••
92	••	••	••	••	••	••	••	••	••	••
93	••	••	••	••	••	••	••	••	••	••
94	••	••	••	••	••	••	••	••	••	••
95	••	••	••	••	••	••	••	••	••	••
96	••	••	••	••	••	••	••	••	••	••

Directory of TTL.LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74BCT	74ACT	74AC	74F	74
97	..	..	..	..	..	..	..	..	..	..
100	..	..	..	..	..	..	..	..	..	..
104	..	..	..	..	..	..	..	..	..	..
105	..	..	..	..	..	..	..	..	..	..
107	..	..	..	..	..	..	..	..	..	..
109	..	..	..	..	..	..	..	..	..	..
110	..	..	..	..	..	..	..	..	..	..
111	..	..	..	..	..	..	..	..	..	..
112	..	..	..	..	..	..	..	..	..	..
113	..	..	..	..	..	..	..	..	..	..
114	..	..	..	..	..	..	..	..	..	..
116	..	..	..	..	..	..	..	..	..	..
120	..	..	..	..	..	..	..	..	..	..
121	..	..	..	..	..	..	..	..	..	..
122	..	..	..	..	..	..	..	..	..	..
123	..	..	..	..	..	..	..	..	..	..
124	..	..	..	..	..	..	..	..	..	..
125	..	..	..	..	..	..	..	..	..	..
126	..	..	..	..	..	..	..	..	..	..
128	..	..	..	..	..	..	..	..	..	..
131	..	..	..	..	..	..	..	..	..	..
132	..	..	..	..	..	..	..	..	..	..
133	..	..	..	..	..	..	..	..	..	..
134	..	..	..	..	..	..	..	..	..	..
135	..	..	..	..	..	..	..	..	..	..
136	..	..	..	..	..	..	..	..	..	..
137	..	..	..	..	..	..	..	..	..	..
138	..	..	..	..	..	..	..	..	..	..
139	..	..	..	..	..	..	..	..	..	..
140	..	..	..	..	..	..	..	..	..	..
141	..	..	..	..	..	..	..	..	..	..
142	..	..	..	..	..	..	..	..	..	..
143	..	..	..	..	..	..	..	..	..	..
144	..	..	..	..	..	..	..	..	..	..
145	..	..	..	..	..	..	..	..	..	..
147	..	..	..	..	..	..	..	..	..	..
148	..	..	..	..	..	..	..	..	..	..
150	..	..	..	..	..	..	..	..	..	..
151	..	..	..	..	..	..	..	..	..	..
152	..	..	..	..	..	..	..	..	..	..

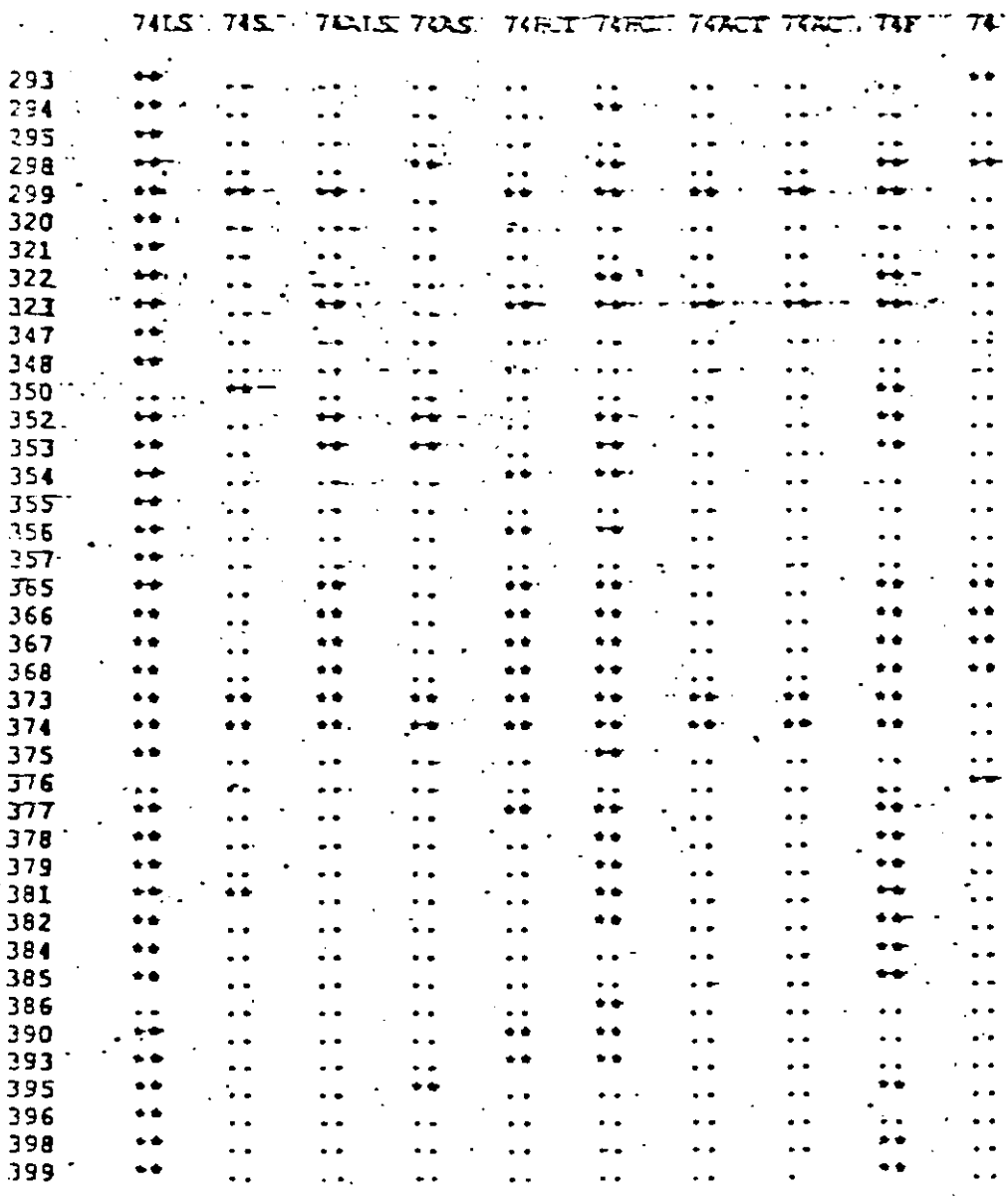
Directory of TTL.LIB Continued

	74LS	74S	74ALS	74AS	74BCT	74HC	74ACT	74AC	74F	74
153	••	••	••	••	••	••	••	••	••	••
154	••	..	..	..	••	••	..	..	..	••
155	••	..	..	..	••	••	..	..	..	••
156	••	..	..	..	..	..	..	..	..	••
157	••	••	••	••	••	••	••	••	••	••
158	••	••	••	••	••	••	••	••	••	..
159	..	..	..	..	..	..	..	..	..	••
160	••	..	••	••	••	••	..	..	••	..
161	••	..	••	••	••	••	••	••	••	..
162	••	••	••	••	••	••	..	..	••	..
163	••	••	••	••	••	••	••	••	••	..
164	••	..	••	..	••	••	..	..	••	••
165	••	..	••	..	••	••	..	..	..	••
166	••	..	••	..	••	••	..	..	••	••
167	..	..	..	..	..	..	..	..	..	••
168	••	••	••	••	..	..	..	..	••	..
169	••	••	••	••	••	••	..	..	••	..
170	••	..	..	..	..	..	..	..	..	••
171	••	..	..	..	..	..	..	..	..	..
172	..	..	..	..	..	..	..	..	..	••
173	••	..	..	..	••	••	..	..	..	••
174	••	••	••	••	••	••	..	..	••	••
175	••	••	••	••	••	••	..	..	••	••
176	..	..	..	..	..	..	..	..	..	••
177	..	..	..	..	..	..	..	..	..	••
178	..	..	..	..	..	..	..	..	..	••
179	..	..	..	..	..	..	..	..	..	••
180	..	..	..	..	..	••	..	..	..	••
181	••	••	..	••	••	••	..	..	••	••
182	..	••	..	..	••	••	..	..	••	••
183	••	..	..	..	..	..	..	..	..	..
184	..	..	..	..	..	..	..	..	..	••
185	..	..	..	..	..	..	..	..	..	••
190	••	..	••	..	••	••	..	..	••	••
191	••	..	••	..	••	••	••	••	••	••
192	••	..	••	..	••	••	..	..	••	••
193	••	..	••	..	••	••	••	••	••	••
194	••	••	..	..	••	••	..	..	••	••
195	••	••	..	..	••	••	..	..	••	••
196	••	••	..	..	..	..	..	..	..	••

Directory of TTL_LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
197	••	••	..	..	..	..	..	..	..	••
198	..	..	..	..	..	..	..	..	••	••
199	..	..	..	..	..	..	..	..	..	..
221	••	..	..	..	••	••	..	..	..	••
226	..	••	..	..	..	..	..	..	..	..
237	..	..	..	..	••	••	..	..	..	..
240	••	••	••	••	••	••	••	••	••	..
241	••	••	••	••	••	••	••	••	••	..
242	••	..	••	••	••	••	..	..	••	..
243	••	..	••	••	••	••	..	..	••	..
244	••	••	••	••	••	••	••	••	••	..
245	••	..	••	..	••	••	••	••	••	..
246	..	..	..	..	..	..	..	..	..	••
247	••	..	..	..	..	..	..	..	..	••
248	••	..	..	..	..	..	..	..	..	••
249	••	..	..	..	..	..	..	..	..	••
250	..	..	..	••	..	..	..	..	..	..
251	••	••	••	••	••	••	••	••	••	••
253	••	..	••	••	••	••	••	••	••	..
257	••	••	••	••	••	••	••	••	••	..
258	••	••	••	••	••	••	••	••	••	..
259	••	..	••	..	••	••	..	..	••	••
260	..	••	..	..	..	..	..	..	••	..
261	••	..	..	..	..	..	..	..	..	..
266	••	..	..	..	..	••	..	..	..	..
268	..	••	..	..	..	..	..	..	..	..
273	••	..	••	..	••	••	..	..	••	••
274	..	••	..	..	..	..	..	..	..	..
275	••	••	..	..	..	..	..	..	..	..
276	..	..	..	..	..	..	..	..	..	••
278	..	..	..	..	..	..	..	..	..	••
279	••	..	..	..	..	..	..	..	..	••
280	••	••	..	..	••	••	••	••	••	..
282	..	..	..	••	..	..	..	..	..	..
283	••	••	..	..	••	..	••	••	••	••
284	..	..	..	..	..	..	..	..	..	••
285	..	..	..	..	..	..	..	..	..	••
286	..	..	..	••	..	..	..	..	..	..
290	••	..	..	—	..	..	..	..	..	••
292	••	..	..	..	..	••	..	..	..	..

Directory of TTL.LIB Continued:



Directory of TTL_LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
412	..	••	..	..	..	..	..	..	••	..
422	••	..	..	..	..	..	..	..	..	..
423	••	..	..	..	••	••	..	..	.	..
425	..	..	..	..	..	..	..	..	..	••
426	..	..	..	..	..	..	..	..	..	••
428	..	••	..	..	..	..	..	..	..	..
432	..	..	..	..	..	..	..	..	••	..
436	..	••	..	..	..	..	..	..	..	..
437	..	••	..	..	..	..	..	..	..	..
440	••	..	..	..	..	..	..	..	..	..
441	••	..	..	..	..	..	..	..	..	..
442	••	..	..	..	..	..	..	..	..	..
443	••	..	..	..	..	..	..	..	..	..
444	••	..	..	..	..	..	..	..	..	..
445	••	..	..	..	..	..	..	..	..	..
446	••	..	..	..	..	..	..	..	..	..
447	••	..	..	..	..	..	..	..	..	..
448	••	..	..	..	..	..	..	..	..	..
449	••	..	..	..	..	..	..	..	..	..
465	••	..	••	..	..	..	••	..	..	..
466	••	..	••	..	..	..	••	..	..	..
467	••	..	••	..	..	..	••	..	..	..
468	••	..	••	..	..	..	••	..	..	..
484	..	••	..	..	..	..	..	..	..	..
485	..	••	..	..	..	..	..	..	..	..
490	••	..	..	..	..	••	..	..	..	••
518	..	..	••	..	..	..	..	..	..	..
519	..	..	••	..	..	..	..	..	..	..
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539	..	..	••	..	..	..	..	..	••	..
540	••	..	••	..	••	••	••	••	••	..
541	••	..	••	..	••	••	••	••	••	..

Directory of TTL.LIB Continued...

	74LS	74S	74ALS	74AS	74HC	74HC	74HCT	74AC	74F	74
560	••	••	••	••	••	••	••	••	••	••
561	••	••	••	••	••	••	••	••	••	••
563	••	••	••	••	••	••	••	••	••	••
564	••	••	••	••	••	••	••	••	••	••
568	••	••	••	••	••	••	••	••	••	••
569	••	••	••	••	••	••	••	••	••	••
573	••	••	••	••	••	••	••	••	••	••
574	••	••	••	••	••	••	••	••	••	••
575	••	••	••	••	••	••	••	••	••	••
576	••	••	••	••	••	••	••	••	••	••
577	••	••	••	••	••	••	••	••	••	••
580	••	••	••	••	••	••	••	••	••	••
588	••	••	••	••	••	••	••	••	••	••
589	••	••	••	••	••	••	••	••	••	••
590	••	••	••	••	••	••	••	••	••	••
591	••	••	••	••	••	••	••	••	••	••
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594	••	••	••	••	••	••	••	••	••	••
595	••	••	••	••	••	••	••	••	••	••
596	••	••	••	••	••	••	••	••	••	••
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598	••	••	••	••	••	••	••	••	••	••
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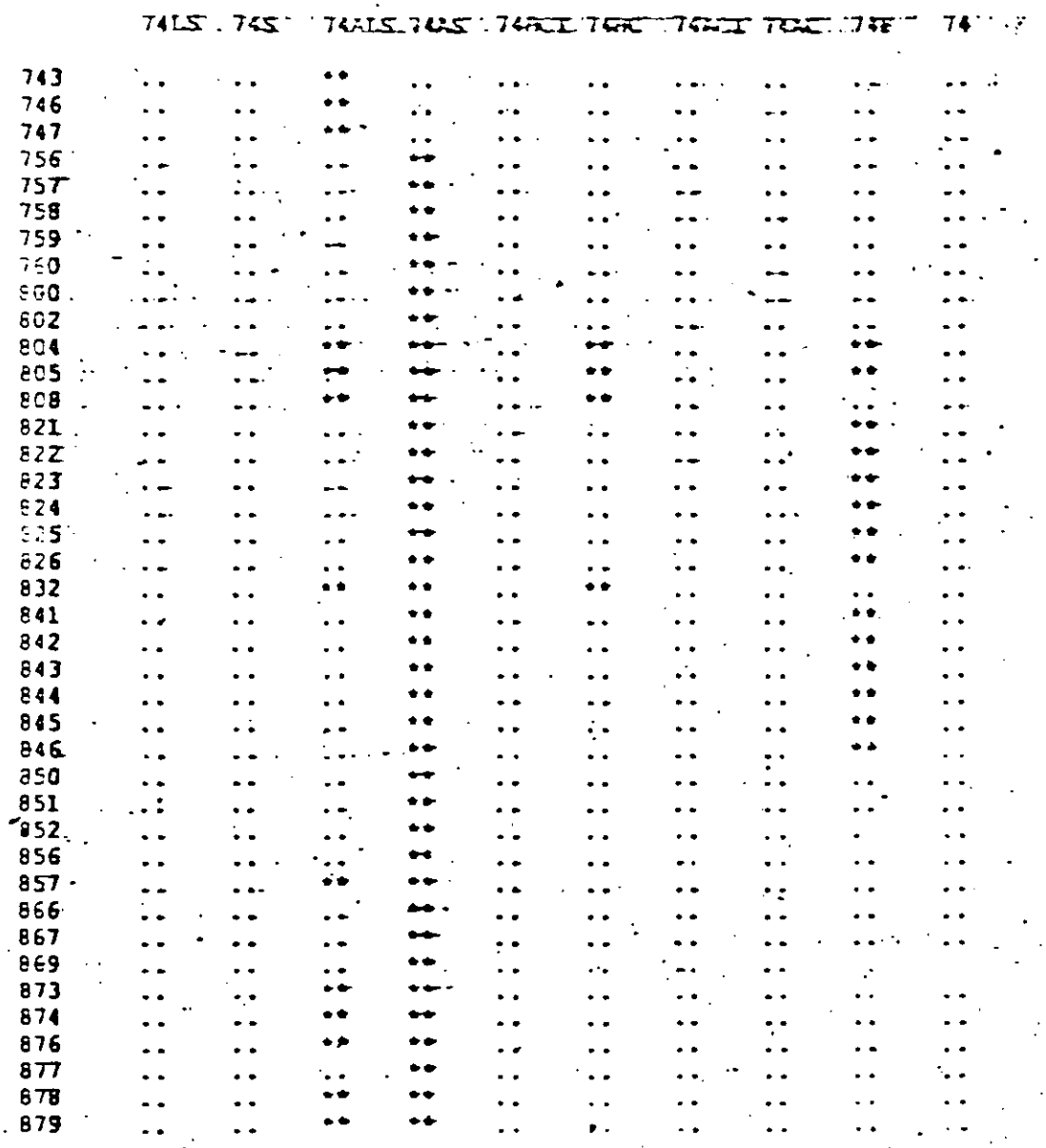
604	••	••	••	••	••	••	••	••	••	••
605	••	••	••	••	••	••	••	••	••	••
606	••	••	••	••	••	••	••	••	••	••
607	••	••	••	••	••	••	••	••	••	••
608	••	••	••	••	••	••	••	••	••	••
618	••	••	••	••	••	••	••	••	••	••
619	••	••	••	••	••	••	••	••	••	••
620	••	••	••	••	••	••	••	••	••	••
621	••	••	••	••	••	••	••	••	••	••
622	••	••	••	••	••	••	••	••	••	••
623	••	••	••	••	••	••	••	••	••	••
638	••	••	••	••	••	••	••	••	••	••
639	••	••	••	••	••	••	••	••	••	••
640	••	••	••	••	••	••	••	••	••	••
641	••	••	••	••	••	••	••	••	••	••
642	••	••	••	••	••	••	••	••	••	••

Directory of TTL.LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
643	••	..	••	••	••	••	••	..	..	..
644	••	..	••	••	..	..	..	..	..	..
645	••	..	••	••	..	••	..	..	..	..
646	••	..	••	••	••	••	••	••	••	..
647	••	..	••	••	..	..	..	..	••	..
648	••	..	••	••	••	••	••	••	••	..
649	••	..	••	••	..	..	..	..	••	..
651	••	..	••	••	••	••	..	..	••	..
652	••	..	••	••	••	••	..	..	••	..
653	••	..	••	••	..	..	..	..	••	..
654	••	..	••	••	..	..	..	..	••	..
668	••	..	..	..	..	..	..	..	..	..
669	••	..	..	..	..	..	..	..	..	..
670	••	..	..	..	••	••	..	..	..	..
671	••	..	..	..	..	..	..	..	..	..
672	••	..	..	..	..	..	..	..	..	..
673	••	..	..	..	..	••	..	..	••	..
674	••	..	..	..	..	••	..	..	••	..
677	..	..	••	..	..	••	..	..	..	..
678	..	..	••	..	..	••	..	..	..	..
679	..	..	••	..	..	••	..	..	..	..
680	..	..	••	..	..	••	..	..	..	..
681	••	..	..	..	..	..	..	..	..	..
682	••	..	..	..	..	••	..	..	..	..
683	••	..	..	..	..	..	..	..	..	..
684	••	..	..	..	..	••	..	..	..	..
685	••	..	..	..	..	..	—	..	..	..
686	••	..	..	..	..	••	..	..	..	..
687	••	..	..	..	..	..	..	..	..	..
688	••	..	••	..	••	••	..	..	..	..
689	••	..	••	..	..	..	..	..	..	..
690	••	..	..	..	..	••	..	..	..	..
691	••	..	..	..	..	••	..	..	..	..
692	••	..	..	..	..	••	..	..	..	..
693	••	..	..	..	..	••	..	..	..	..
696	••	..	..	..	..	••	..	..	..	..
697	••	..	..	..	..	••	..	..	..	..
698	••	..	..	..	..	••	..	..	..	..
699	••	..	..	..	..	••	..	..	..	..
742	..	..	••	..	..	..	..	..	..	..

Directory of TTL.LIB Continued



Directory of TTL.LIB Continued

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881	..	..	..	**	..	**	..	..	**	..
882	..	..	..	**	..	**	..	..	**	..
885	..	..	..	**	..	..	..	..	..	..
888	..	..	..	**	..	..	..	..	..	..
888G	..	..	..	**	..	..	..	..	..	..
890	..	..	..	**	..	..	..	..	..	..
890G	..	..	..	**	..	..	..	..	..	..
1000	..	..	**	**	..	..	..	..	..	..
1002	..	..	**	..	..	..	..	..	..	..
1003	..	..	**	..	..	..	..	..	..	..
1004	..	..	**	**	..	..	..	..	..	..
1005	..	..	**	..	..	..	..	..	..	..
1008	..	..	**	**	..	..	..	..	..	..
1010	..	..	**	..	..	..	..	..	..	..
1011	..	..	**	..	..	..	..	..	..	..
1020	..	..	**	..	..	..	..	..	..	..
1032	..	..	**	**	..	..	..	..	..	..
1034	..	..	**	**	..	..	..	..	..	..
1035	..	..	**	..	..	..	..	..	..	..
1036	..	..	**	..	..	..	..	..	..	..
1240	..	..	**	..	..	..	..	..	..	..
1241	..	..	..	..	..	..	..	..	**	..
1242	..	..	**	..	..	..	..	..	**	..
1243	..	..	**	..	..	..	..	..	**	..
1244	..	..	**	..	..	..	..	..	**	..
1245	..	..	**	..	..	..	..	..	**	..
1620	..	..	**	..	..	..	..	..	..	..
1621	..	..	**	..	..	..	..	..	..	..
1622	..	..	**	..	..	..	..	..	..	..
1623	..	..	**	..	..	..	..	..	..	..
1638	..	..	**	..	..	..	..	..	..	..
1639	..	..	**	..	..	..	..	..	..	..
1640	..	..	**	..	..	..	..	..	..	..
1641	..	..	**	..	..	..	..	..	..	..
1642	..	..	**	..	..	..	..	..	..	..
1643	..	..	**	..	..	..	..	..	..	..
1644	..	..	**	..	..	..	..	..	..	..
1645	..	..	**	..	..	..	..	..	..	..
2620	..	..	..	**	..	..	..	..	..	..

Directory of TTL.LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
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2640	--	--	--	**	--	--	--	--	--	--
2645	--	--	--	**	--	--	--	--	--	--
8003	--	--	**	--	--	--	--	--	--	--
11000	--	--	--	--	--	--	**	**	--	--
11002	--	--	--	--	--	--	**	**	--	--
11004	--	--	--	--	--	--	**	**	--	--
11008	--	--	--	--	--	--	**	**	--	--
11010	--	--	--	--	--	--	**	**	--	--
11011	--	--	--	--	--	--	**	**	--	--
11015	--	--	--	--	--	--	**	**	--	--
11014	--	--	--	--	--	--	**	**	--	--
11020	--	--	--	--	--	--	**	**	--	--
11021	--	--	--	--	--	--	**	**	--	--
11027	--	--	--	--	--	--	**	**	--	--
11030	--	--	--	--	--	--	**	**	--	--
11032	--	--	--	--	--	--	**	**	--	--
11034	--	--	--	--	--	--	**	**	--	--
11074	--	--	--	--	--	--	**	**	--	--
11109	--	--	--	--	--	--	**	**	--	--
11112	--	--	--	--	--	--	**	**	--	--
11132	--	--	--	--	--	--	**	**	--	--
11138	--	--	--	--	--	--	**	**	--	--
11139	--	--	--	--	--	--	**	**	--	--
11151	--	--	--	--	--	--	**	**	--	--
11153	--	--	--	--	--	--	**	**	--	--
11157	--	--	--	--	--	--	**	**	--	--
11158	--	--	--	--	--	--	**	**	--	--
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11162	--	--	--	--	--	--	**	**	--	--
11163	--	--	--	--	--	--	**	**	--	--
11168	--	--	--	--	--	--	**	**	--	--
11169	--	--	--	--	--	--	**	**	--	--
11174	--	--	--	--	--	--	**	**	--	--
11175	--	--	--	--	--	--	**	**	--	--
11181	--	--	--	--	--	--	**	**	--	--
11190	--	--	--	--	--	--	**	**	--	--
11191	--	--	--	--	--	--	**	**	--	--
11192	--	--	--	--	--	--	**	**	--	--

Directory of TTL.LIB Continued

	74LS	74S	74ALS	74AS	74HCT	74HC	74ACT	74AC	74F	74
11193	..	..	..	..	..	..	**	**	..	..
11194	..	..	..	..	..	..	**	**	..	..
11240	..	..	..	..	..	..	**	**	..	..
11241	..	..	..	..	..	..	**	**	..	..
11244	..	..	..	..	..	..	**	**	..	..
11245	..	..	..	..	..	..	**	**	..	..
11251	..	..	..	..	..	..	**	**	..	..
11253	..	..	..	..	..	..	**	**	..	..
11257	..	..	..	..	..	..	**	**	..	..
11258	..	..	..	..	..	..	**	**	..	..
11280	..	..	..	..	..	..	**	**	..	..
11286	..	..	..	..	..	..	**	**	..	..
11299	..	..	..	..	..	..	**	**	..	..
11323	..	..	..	..	..	..	**	**	..	..
11352	..	..	..	..	..	..	**	**	..	..
11353	..	..	..	..	..	..	**	**	..	..
11373	..	..	..	..	..	..	**	**	..	..
11374	..	..	..	..	..	..	**	**	..	..
11640	..	..	..	..	..	..	**	**	..	..
11643	..	..	..	..	..	..	**	**	..	..
11881	..	..	..	..	..	..	**	**	..	..
1488										
1489										
75188										
75189										

CIRCUITO IMPRESO

(TANGO-PLUS)

4 Learning Tango-PCB PLUS

4.1 Introduction

Learning Tango-PCB PLUS is a hands-on tutorial that helps you become familiar with many of the program's features. The purpose of the tutorial is to give you the confidence to begin using Tango-PCB PLUS to create your own board designs.

We know that you're anxious to get started. It is a basic human urge to run a new software package without thoroughly reading the manual. We've done it ourselves once or twice. But we highly recommend that you follow the complete tutorial. It is designed to be a quick and somewhat painless way to get acquainted with Tango-PCB PLUS. The rest of the manual contains reference information that you can read as you need it.

This tutorial is intended to help you get acquainted with the artwork options, editing features, and "look-and-feel" of Tango-PCB PLUS. We'll show you how to run the program and point out a dozen or so operations that are typical of a short design session.

If an error message is displayed during the tutorial, see Appendix E: Error Messages for a description of the problem and a possible solution.

4.2 Before Starting The Tutorial

Before starting the tutorial, follow the installation instructions in Chapter 3: Getting Started. We assume that you have first:

- Installed the Tango-PCB PLUS security device.

- Made backup copies of the Tango-PCB PLUS diskettes.
- If you are using a mouse, installed and invoked your system's mouse hardware and mouse software driver.
- If you are using EMS (expanded memory), installed and invoked EMS hardware and software driver.
- Made sure that your CONFIG.SYS file is correctly configured for running Tango-PCB PLUS.
- Installed the Tango-PCB PLUS software in a directory on the hard disk.
- Configured Tango-PCB PLUS for your system's graphics card.

4.3 Running Tango-PCB PLUS

To run the Tango-PCB PLUS program, type:

```
pcb <Enter>
```

After a few seconds, the Tango-PCB PLUS screen is displayed. Now we can put the program through its paces.

4.4 The ACCEL Productivity Interfaces

The screen before you is the result of extensive research into the ergonomics of electronic design. To build a more productive interface, ACCEL studied engineers' work habits and design flow, on-screen user interfaces from dozens of different software programs, and hundreds of user comments and suggestions. The resulting ACCEL Productivity Interface (API) allows for flexibility in user options and a wide variety of editing commands. It will serve as a consistent front end for all of ACCEL's electronic design software programs.

Let's take a tour around the screen to familiarize you with the API's features.

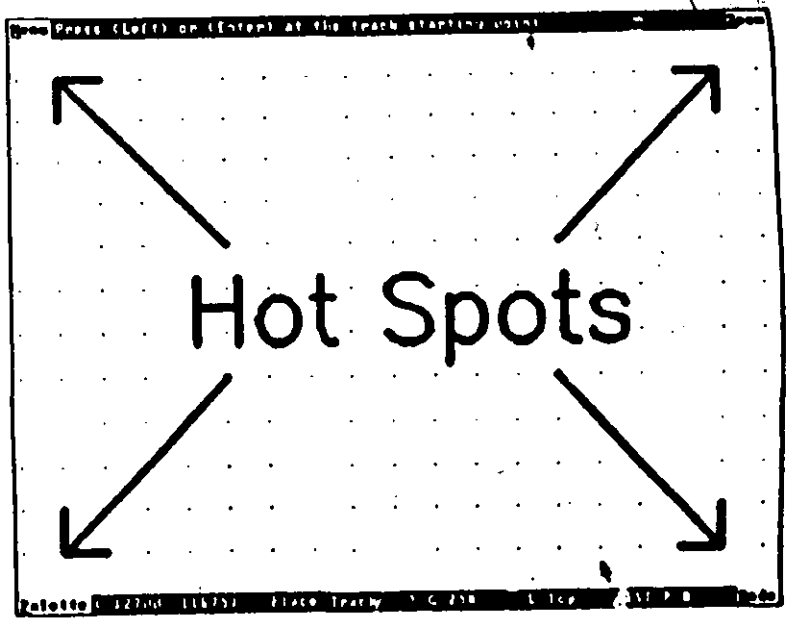


Figure 4-1. The hot spots provide one-click access to the Menu, Zoom, Undo, and Speed Palette functions.

In the four corners are buttons we call *hot spots* (Figure 4-1). One click of the <LeftMouse> button over the hot spots will: a) pop-up the Main Menu, b) enable the Zoom Window command, c) undo the last command, or d) pop-up the Speed Palette. We'll try all these functions in a moment and you'll see why the hot spots make these oft-repeated operations a breeze.

Across the top of the screen is a single line of text called the *prompt line* (Figure 4-2). As the program first loads, it displays the usual copyright information. But as you toggle through command options on Tango's menus, the prompt line does what its name implies: provides a brief help message on whatever command is active at the time.

On the bottom of the screen you'll find the *status line*. From left to right, the status line indicates the cursor location, the command mode, a ? (question mark) for accessing the on-line help utility, the grid selection field, the current layer and its color, and the currently loaded PCB file.

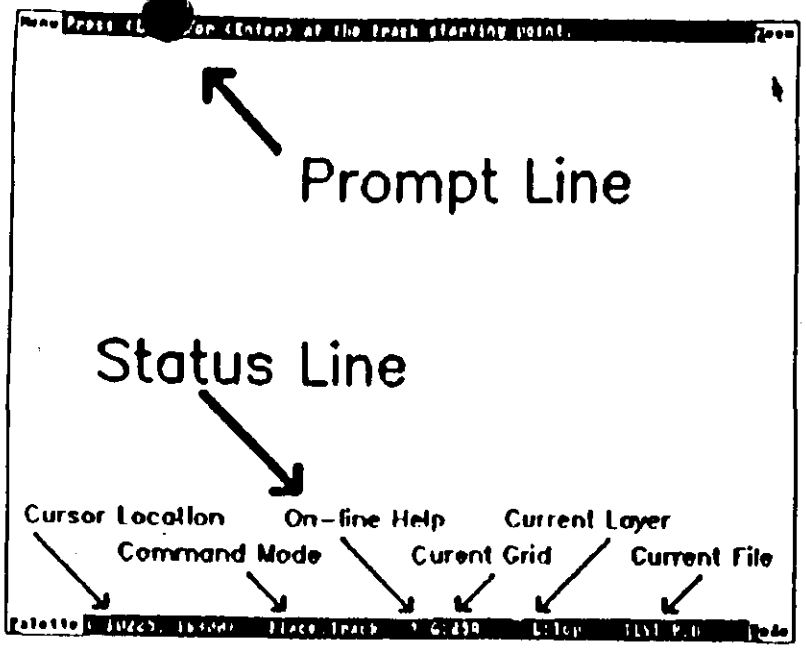


Figure 4-2. Tango-PCB PLUS' prompt line and status line keep you informed.

If you need assistance at any time during your design session, you can click over the ? on the status line or type ? on your keyboard. One or more screens of information will appear which describe the command current at the time you ask for help (Figure 4-3).

Use the Help facility's Up and Down buttons to view additional pages of help on the current topic. Next and Previous display help on the next and previous topics, and Index produces an index of all available topics.

With over 100 screens of on-line help, your Reference Manual may just gather dust on the shelf. (Our printing department is getting nervous).

One final note on our screen design before we move on. All on-screen information is displayed in as little space as possible to provide the maximum screen area available for editing. This trait carries through to our pop-up menus and dialog boxes, which are designed to cover as little of the workspace as possible. Compare this approach to many other systems with permanent, on-screen menus that take up as much as 25% of the available work area.

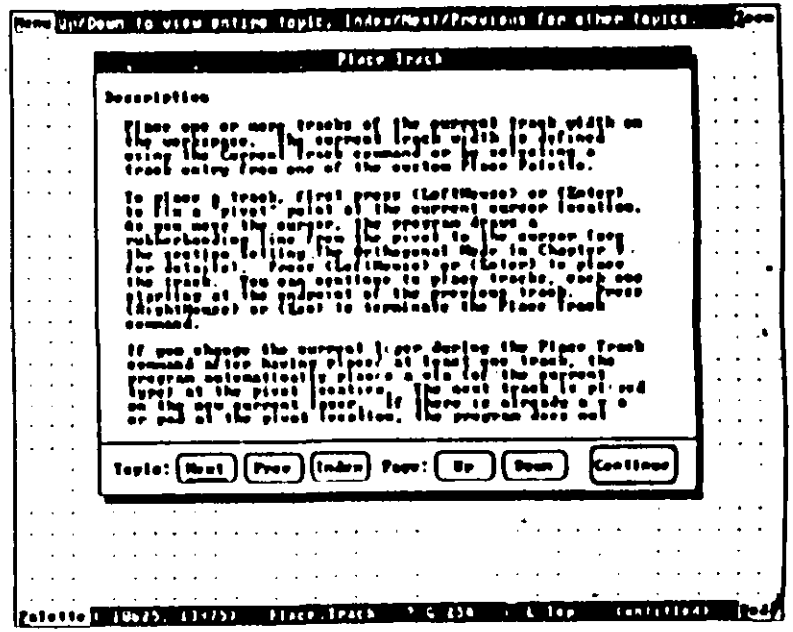


Figure 4-3. Tango-PCB PLUS features context-sensitive on-line help.

4.5 Loading Files

To load files, select the File Load command from Tango's pop-up menus. There are three convenient ways to pop-up the Main Menu:

- Move the cursor over the Menu hot spot and click the <LeftMouse> button.
- With the cursor in any location, click both the <RightMouse> and <LeftMouse> buttons at the same time.
- With the cursor in any location, press the <Spacebar> or type M on your keyboard.

Pressing <RightMouse> or <Esc> removes the menu. Pop-up the Main Menu now using your choice of any of the three methods.

With Tango's menus displayed, use the mouse or arrow keys to move the highlighting bar up or down the display of menu items. You can select highlighted menu items by pressing <LeftMouse> or <Enter>. You can also run a command, whether it's highlighted or not, by typing the first letter of the command name.

Highlight the Main Menu's File command. Notice that the prompt line indicates the commands immediately available beneath the Main Menu item File. All of Tango-PCB PLUS' 75+ commands are available from the Main Menu, or at most, one menu level down. You can view *every menu option* on the prompt line by sliding the highlight bar up and down the Main Menu. Tango's two-level architecture was designed to eliminate the navigational problems of deep hierarchical menu structures. No more swinging from one branch of a complex menu tree to another. Tango-PCB PLUS lets you move quickly between operations without monkeying around.

Now press <Enter> or click <LeftMouse> to select the File menu. You are presented with the five File commands: File Clear, File DOS (allows you to exit to DOS from within Tango), File Load, File Quit, and File Save. Select the File Load command.

Up pops a dialog box where you make your selection of which file to load (Figure 4-4). You have asked Tango to load a file. Now the program is asking you whether to load a PCB, block, or photoplot file, and which specific file to load. In essence, you are having a dialog with the program, hence the name *dialog box*.

There are three types of files you can load with Tango-PCB PLUS: PCB files, block files, and photoplot files. PCB files are the basic printed-circuit-board drawings. Blocks are portions of boards, like memory arrays or microprocessors and their glue logic, which you define and save away for future repeated use. Photoplot files are Gerber-format files created with Tango which are used to generate final artwork on photoplotters.

We want to load a PCB file now. Select PCB as the file type and click on List. Select the file IBMCARD.PCB in the list box and select OK. Click on OK again to load the file.

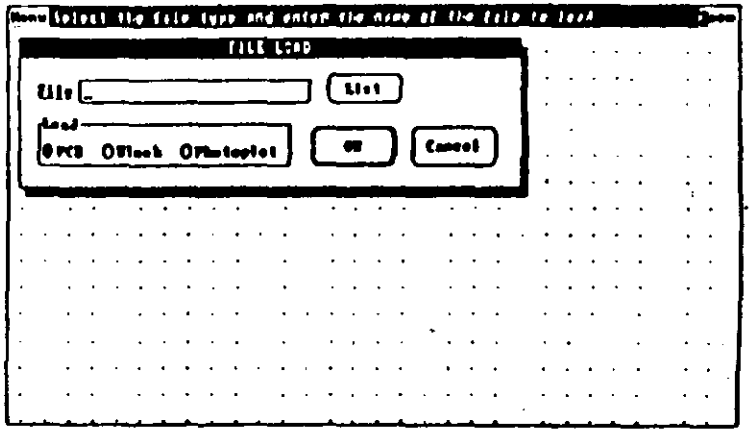


Figure 4-4. Tango-PCB PLUS' dialog boxes provide a consistent, logical way to interact with the program.

When the file IBMCARD.PCB is loaded into memory, Tango-PCB PLUS immediately displays the PCB, automatically zoomed to display the entire board on the workspace. You are looking at the board outline and edge connectors of an IBM-compatible PC plug-in card. Common board configurations, such as PC, VME, or MultiBus cards, can be easily saved as templates for future designs.

Besides PCB and block files, Tango will automatically create definition and initialization files which save information on how you've customized Tango for your own particular use.

With Tango-PCB PLUS, you have tremendous flexibility in selecting pad shapes and sizes, track widths, via sizes, and Gerber apertures. However, most designers work with a fairly standard set of artwork primitives. Therefore, Tango allows you to define a set of standard primitives. The program automatically saves these primitives in a definition file, PCB.DFN, which is loaded when you run the program.

Likewise, any options which you select in the setup commands described below will be saved automatically in an initialization file, PCB.INI, which is loaded upon program startup. For added convenience and consistency, both Tango-PCB and Tango-Route operate using the same initialization file.

4.6 Setting Up Your System

Besides flexibility in artwork specifications, Tango-PCB PLUS also lets you tailor the program's operation to suit your own needs and taste. The Setup commands allow you to enable layers, choose colors, set grids, and so on:

Setup Communications	Set up the COM1 and COM2 ports for use with plotters or printers.
Setup Display	Enable/disable layers, pads, vias, grids; select cursor type (arrow, small cross, large cross); select colors for menus, background, status/prompt lines, layers, pads, vias, grids, etc.
Setup Grids	Set the Absolute, Relative and Visible grids in increments of one mil or greater.
Setup Options	Enable/disable the orthogonal track modes and drag tracks options.
Setup Palette	Customize the Place Speed Palette with your own selection of pads, vias, text sizes, and trace widths for quick placement.

To start, we've set all of these options for you. But feel free to scan the Setup menus and change Tango to suit yourself. When you quit, Tango-PCB PLUS saves the current setup in the initialization file (PCB.INI) so everything looks the same the next time you run the program.

4.7 Placing Components

We'll begin our design by placing a few components and then routing connections between them. Tango-PCB PLUS ships complete with extensive libraries of through-hole and surface mount (SMT) patterns, and provides powerful facilities for graphically browsing, listing, merging, and renaming library components. Adding new components is

simple: just create the part graphically in Tango-PCB PLUS and add it to a library, even in the middle of a board design session.

In the Tango-PCB PLUS package, we've provided the sample library file EVAL.LIB. This library includes a group of through-hole, connector, and surface-mount patterns, all of which are available in the three standard Tango-PCB PLUS libraries: PCBMAIN.LIB, PCBCONN.LIB, and PCBSMT.LIB.

The Library Browse command provides an easy method to scan a list of the patterns in a library and to visually inspect their shape. Run the Library Browse command now. In the dialog box, click on List to display a list of the available libraries. Select EVAL.LIB and click on OK. The dialog box now lists the patterns in EVAL.LIB. To browse each of the patterns we're about to place, first click on DIP16, and after viewing the displayed pattern, click on PLCC28A (Figure 4-5).

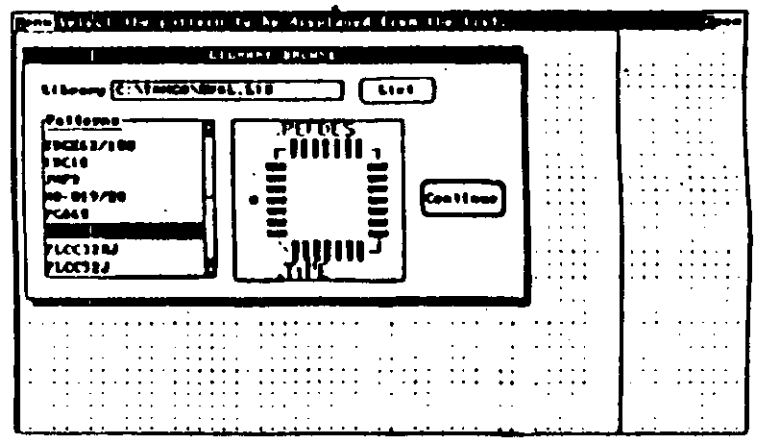


Figure 4-5. List and view component patterns with Library Browse.

The .REFDES and .TYPE fields displayed with the pattern in the browse window will be replaced with the reference designator and component type when the part is placed. Let's click on Continue to start placing.

Throughout Tango-PCB PLUS, there are two methods of operation: using the two-level menus described above or accessing many of the

same commands with the Speed Palette. We'll demonstrate both methods as we place components and text on our sample board.

Using the first method, we place a component pattern by popping up the menus and selecting the Place Component command. Press <LeftMouse> or <Enter> to display a dialog box which lets us select libraries and library components. The current library should be EVAL.LIB.

Using the component list box (Figure 4-6), select the DIP16 pattern from the library, and give it a reference designator U1. This satisfies the dual function of naming the first component to be placed and of setting the template for a series of reference designators. Tango-PCB PLUS will automatically increment reference designators for each successive component placed. You can ignore Type and Value if you wish, or add information which would eventually find its way into a Bill of Materials report.

Click on OK. An outline of the DIP16 appears on the current layer (Top), ready to be placed. (If the current layer, as shown on the status line, is not Top, press L to cycle through the enabled layers until Top appears.) Move your cursor to location 5000,5000 and press <LeftMouse> or <Enter>.

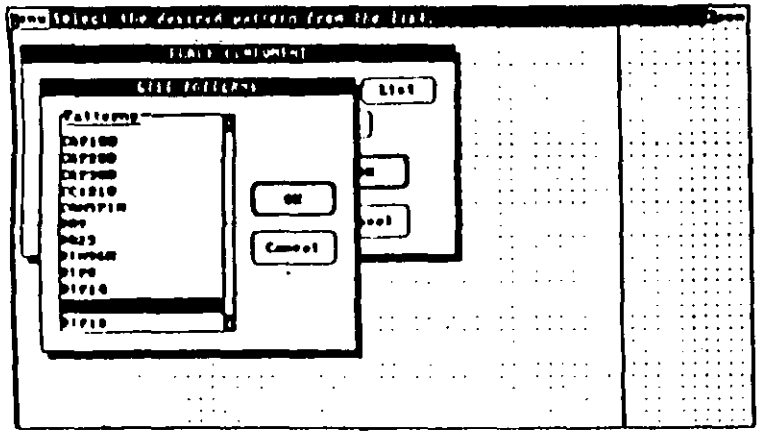


Figure 4-6. List boxes aid library component selection.

You're still in Place Component mode, as indicated by the command mode field on the status line. If you wanted to place an identical component (a DIP16) with the reference designator incremented by one, all you have to do is click the <LeftMouse> or press <Enter>.

We want to place a new pattern, however, so first click <RightMouse> or <Esc> to exit Place Component mode and then <LeftMouse> or <Enter> to re-display the Place Component dialog box. Use the component list box again to select the pattern PLCC2RA. The reference designator will default to U2, so click on OK and the part's outline appears.

The pattern PLCC2RA is a surface-mount part and we want to place it on the other side of the board. Notice that our options are indicated on the prompt line: Press R to rotate, F to flip, <LeftMouse> or <Enter> to place. Press F on your keyboard to flip the pattern to the Bottom layer. Now move your cursor to location 6200,4700 and click <LeftMouse> or <Enter> to place the part (Figure 4-7).

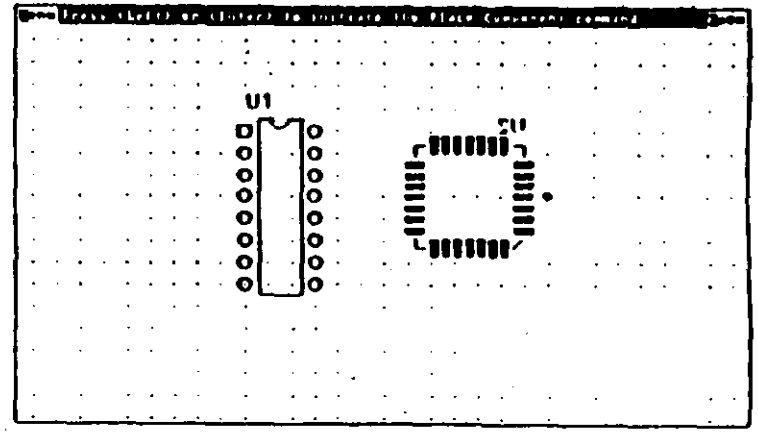


Figure 4-7. One keystroke flips a surface-mount device to the board's Bottom layer.

4.8 Using The Speed Palettes

Tango's second operating method, using the Speed Palette, makes placing components, text strings, tracks, pads, and vias even quicker. To display the Speed Palette, click over the Palette hot spot or press P.

There are actually five Speed Palettes available in Tango-PCB PLUS: Place, Delete, Edit, Move, and Nets. To select a different palette, toggle through the Menu name options in the status line's Command Mode field (to the left of the colon), and you'll see the various palettes appear. You can also click on the palette name on the left side of the Speed Palette. Press <LeftMouse> to move forward through the available palettes; press <RightMouse> to move backward through the list.

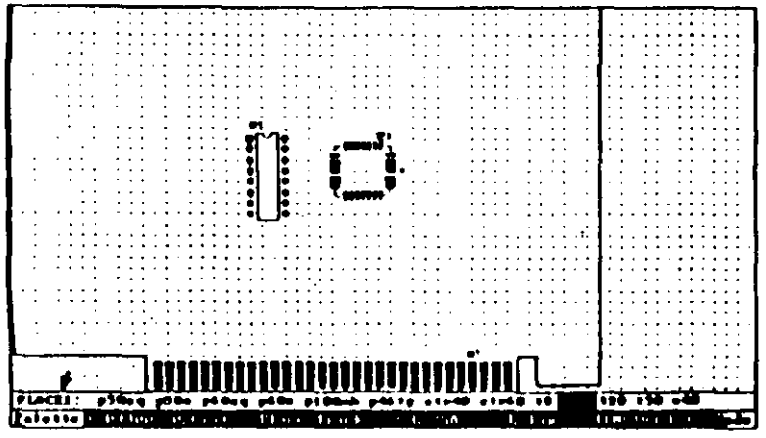


Figure 4-8. A place of your own: the customized PLACE1 Speed Palette.

NOTE

A mouse is require[illegible] use the Speed Palettes.

You'll also notice a sixth Speed Palette, PLACE1, which contains a collection of pads, trace widths, text string sizes, and vias for placement (Figure 4-8). Using the Setup Palette command, you can customize one or more Place Speed Palettes with your own selection of design primitives.

Toggle back to the Place Speed Palette and click over the word String. This changes the current mode to Place String. Now press <LeftMouse> or <Enter> to display the Place String dialog box. You may key in any text string you wish, up to 60 alphanumeric characters. Click on OK. An outline of the string appears on the board, ready for placement. (You can set the string's height, line width, and orientation with the Current String command before running Place String, or modify the string after placing it using the Edit String command.) Center your text below the two component we've placed and press <LeftMouse> or <Enter> (Figure 4-9).

You have just learned two methods to rapidly place components and text in Tango-PCB PLUS. But here's some *great* news. You have also mastered the same two ways Tango lets you place pads, vias, tracks, area fills, arcs, and block copies. Because all items placed on a Tango board are done so in the *same manner* -- with consistency and speed in mind. Beginners may need the added prompts of the menus and dialog boxes, but as your familiarity with the program grows, Tango keeps pace with productivity boosters like the Speed Palette.

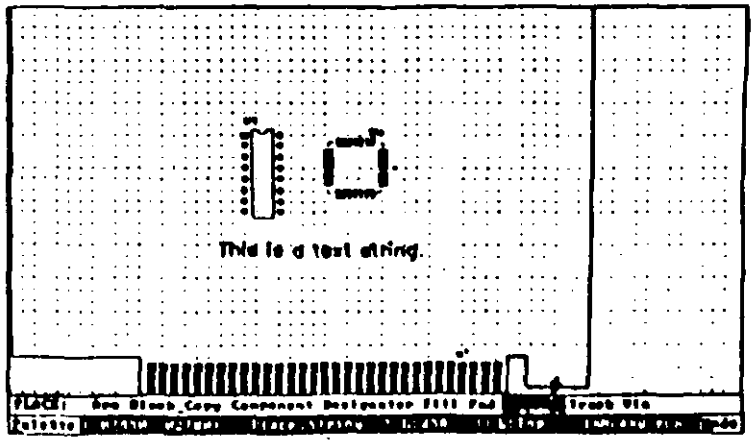


Figure 4-9. Tango pros can place, move, edit, or delete tracks, pads, and text without popping up menus or remembering keystrokes!

9 The Right Connections

ow let's draw some connections between the components on the oard. First, we want to zoom in for a better view of the workspace. ango-PCB PLUS includes several zoom and pan options on its Zoom enu, including Zoom All, Board, Center, In, Out, Redraw, and Window. You can also re-center the screen around the current cursor sation by simply pressing C on your keyboard. Like all zoom and pan ptions in Tango, this *pan-on-demand* may be used at any time: in the iddle of laying tracks, placing components, or just looking around.

nother handy feature for focusing on your design, the Zoom Window ommand can be accessed from the menus, or more quickly by clicking n the Zoom hot spot located in the top right corner of the screen, or by ust pressing Z on your keyboard.

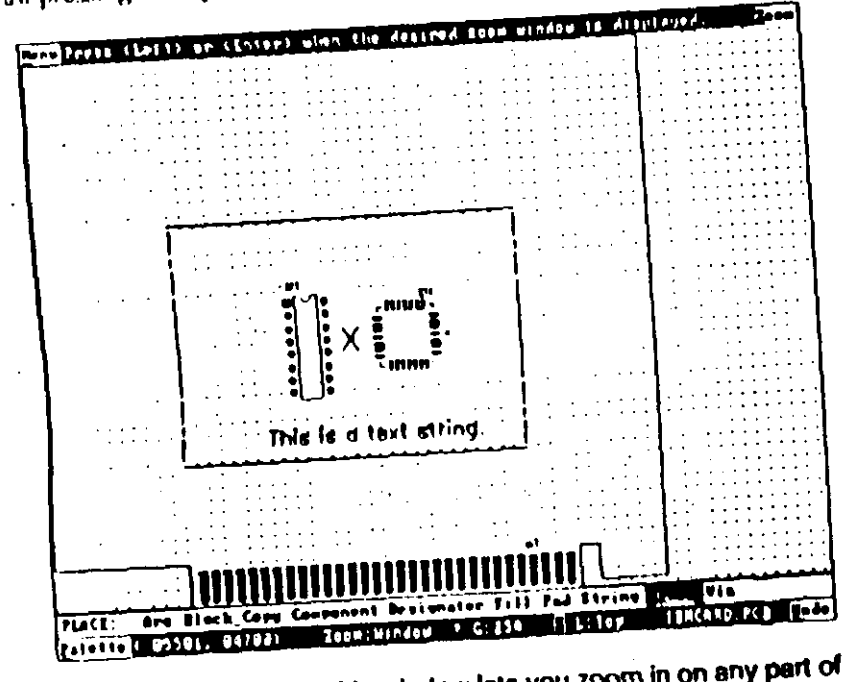


Figure 4-10. An adjustable window lets you zoom in on any part of the board.

Do so now and move the cursor right between U1 and U2 (around the point 5500,4700). Click <LeftMouse> again and then move the mouse

in any direction. Stretch the Zoom window (Figure 4-10) until it covers both U1 and U2 and click <LeftMouse> again. Tango redraws the screen at the new, user-defined zoom level.

4.10 The Three Grids

We're going to draw a trace from Pin 1 of U1 (top left corner) to Pin 1 of U2 (center, right side -- remember, U2 has been flipped over to the other side of the board). To make it interesting, let's run our trace between the pads on both parts. You'll note from the visible grid (currently set at 100 mils), that the pads on the through-hole part are set on 100-mil centers, and the SMD pads are on 50-mil centers. If we route on a grid of 25 mil, we can place an eight-mil trace with adequate clearance between pads on both components.

The current Absolute Grid as noted on the status line is 25 mil. Tango's Setup Grids command allows you to reset the Absolute, Relative and Visible grids to a variety of popular grids, or to any integer between one and 1000 mils (Figure 4-11). The Relative Grid allows you to specify an independent grid beginning from a new origin, perfect for creating and placing edge connectors and metrically spaced parts.

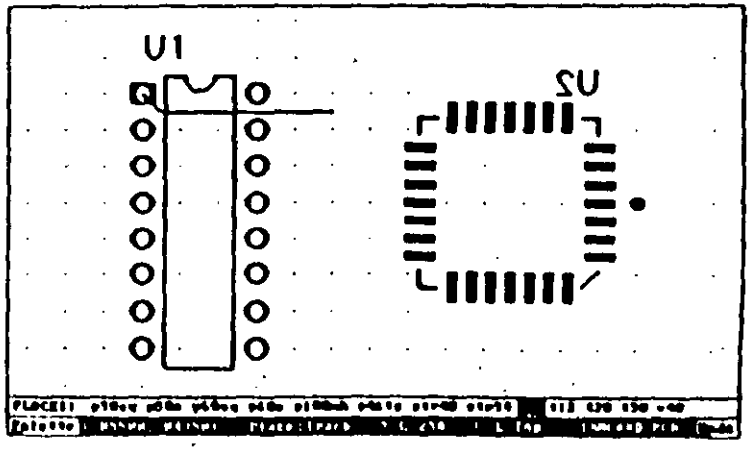


Figure 4-11. With Tango's variable grid, running one or more tracks between DIP parts is easy.

With the grid set to 25 mils, we'll begin laying tracks. Clicking over t8 (the alias for an eight-mil track) on the PLACE! Speed Palette puts you in Place Track mode and changes the current track to eight mils in width. Move your cursor to Pin 1 on U1 and press <LeftMouse>. Begin drawing the trace to the right, (under the component). Press <LeftMouse> each time you wish to finish a track *segment*. Move downward to the right on a 45-degree angle, and then to the right again, heading out between any two pins.

Continue your trace to the half-way point between the two components and end the track segment by pressing <LeftMouse>. Now pop up the Main Menu by pressing M, <Spacebar>, or clicking both mouse buttons at once. Run the Current Layer command and select **Bottom** to change the layer to the other side of the board. When you click on **OK**, program automatically inserts a via, allowing you to continue your trace on the bottom of the board.

A Tango Tip: Since you're almost a Tango pro, here's a short-cut for changing layers. Just click over the Current Layer field on the status line or press L.

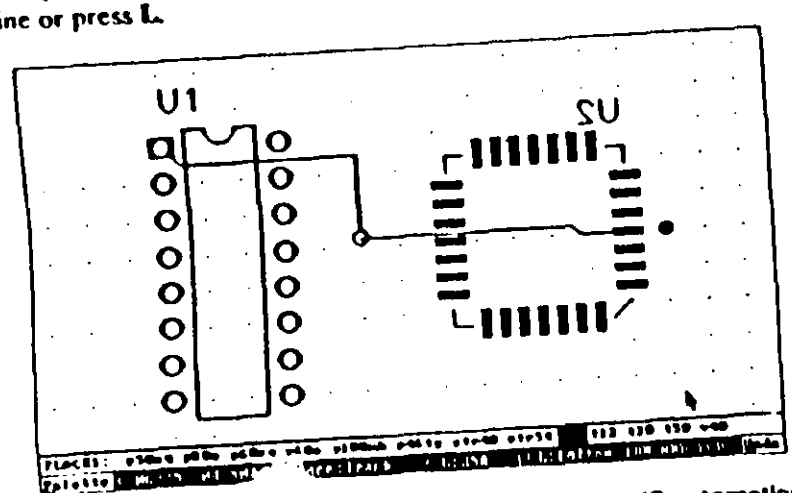


Figure 4-12. When placing tracks, Tango-PCB PLUS automatically inserts a via when you change layers.

Continue drawing your track between the pads on U2 until you reach Pin 1. Press <LeftMouse> again to end the final segment and then quit the track drawing mode by pressing <RightMouse> or <Esc>

(Figure 4-12). Go ahead and practice drawing a few more tracks on both sides of the board.

You can see how simple it is to place components, and to draw connections in Tango-PCB PLUS. While the program includes powerful net list features, which we'll describe a bit later, you can also draw *free hand*, creating nets, breaking them, and re-creating them. All without the cumbersome chore of maintaining the sanctity of a net list throughout the entire design process.

4.11 A Board's-Eye View

You've done great work so far! Not bad for such a short time on the system. To put your editing in perspective, let's zoom out to a full view of the board.

First, pop-up the Main Menu and click on **Zoom**. Now run the **Zoom Board** command from the Zoom Menu. Tango quickly redraws the entire board with all enabled layers displayed. Tango-PCB PLUS' vector graphics make its redraw speed among the fastest in the industry. Redraw time is strictly a function of your computer's microprocessor speed and the amount of board information being displayed. You can improve redraw by disabling layers not currently being edited and/or operating the program on faster machines. Our mostly integer-based graphics routines do not require nor take advantage of a math co-processor.

Now let's assume an ECO has just come through eliminating component U2. To delete the part, use the menus or the Delete Speed Palette to run the Delete Component command. You are now in Delete Component mode. Move the cursor over U2, press <LeftMouse> or <Enter>, and the component disappears.

On second thought, we decide to restore U2. No problem. Just click over the Undo hot spot and your deletion is un-deleted. The Undo command -- accessible from the Main Menu, the Undo hot spot, or by pressing U -- *undoes* the previous editing command. Besides deletions, you can also undo Place, Move, and Edit operations, and *unwind* tracks placed or rerouted. This is one hot spot that will keep you out of hot water. Undo will even let you undo your previous undo.

4.12 Net List Operations

Whether you've drawn your electronic circuit in a sophisticated schematic capture system or on the back of an envelope, generating a net list will help with your PCB design. The benefits include faster layout, because Tango-PCB PLUS displays nets and their nodes for easy routing, and higher quality, and because Tango's Nets Verify command and integrated design rule checker conduct electrical connectivity as well as clearance gap checks to ensure the integrity of the design.

For the uninitiated, a net list is simply a list of all components and connections in the circuit. Tango-PCB PLUS supports a simple, ASCII net list format which may be generated by hand with a text editor or by popular schematic capture systems including Tango-Schematic, OrCAD/SDT, and Schema. We're adding support for additional programs, so call us if you wish to check on another.

As noted above, an important distinction between Tango and other net-list-based PCB design software is that while Tango-PCB PLUS *supports* net lists, it does not *require* them. This means you can load a net list and take advantage of several productivity enhancing features in the program, while you are still free to make or break any connection at any time without updating the net list information.

Besides speeding up board design in Tango-PCB PLUS, the net list also feeds component and connection information to our powerful autorouter, Tango-Route PLUS. If you don't have a net list, you can still use the powerful *what-you-see-is-what-you-get* editing capability of Tango-PCB PLUS to lay out your circuit by hand.

In the next few pages, we'll load a net list, display a *rat's nest* and *force vectors*, then display, route, and verify individual nets.

The net list is loaded after all components have been placed on the board. Since we know your time is valuable, we have supplied a PCB file with 100+ components already placed. Pop-up the menus to run the File Load command. Key in, or select from the list box, DEMO1.PCB and click on OK. Tango prompts you to save the changes to our current board. Let's leave IBMCARD.PCB as-is. Click on No Save.

4.13 Loading A Net List

Next, pop-up the menus again and run the Nets Load command. The Tango-PCB PLUS package includes an associated net list called DEMO1.NET. In the Nets Load dialog box, either key in the name DEMO1.NET or select it from the list box. Click on OK to load the net list. After a few moments, Tango will prompt you for the names of the nets to be assigned to power and ground planes, if so desired. Key in, or select from the list box, VCC for the Power Plane Net and GND for the Ground Plane Net. For the Plane Connection, select Thermal and click on OK.

Tango-PCB PLUS redraws the screen with all point-to-point connections in the net list displayed on a special Connections layer. This representation is appropriately called the *rat's nest* (Figure 4-13). The rat's nest, along with force vectors to be discussed below, provide a visual cue as to the quality of our parts placement.

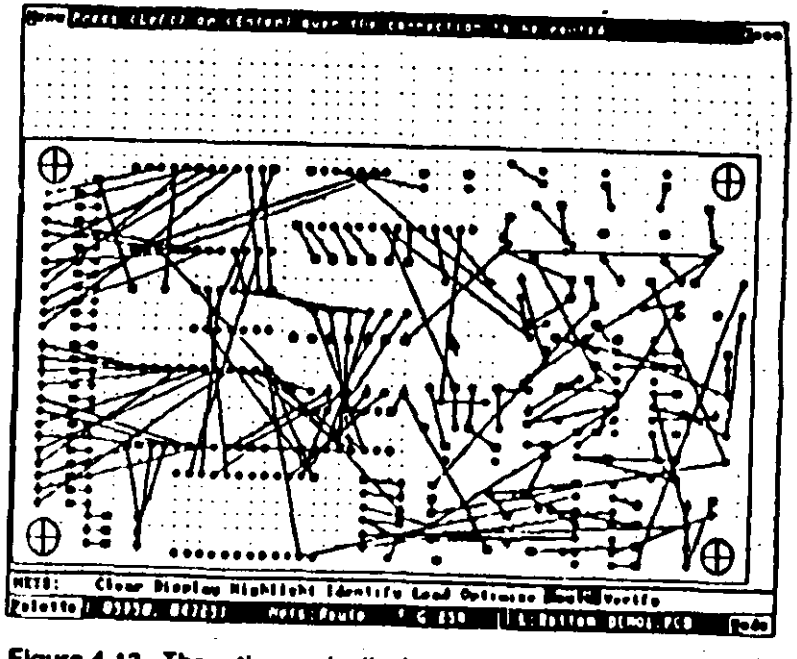


Figure 4-13. The rat's nest is displayed on a special Connections layer.

4.14 Optimizing Nets

Whether you intend to manually route the design or use Tango-Route to autoroute the board, optimal component placement is crucial to your success. Tango-PCB PLUS include three powerful features to aid in component optimization: the Nets Optimize and Move Component commands, and force vectors.

When you first loaded the net list, Tango-PCB PLUS connected all the nodes in the order they were connected in the schematic, which may not make any sense on the PCB. Therefore, it almost always pays to first run the Nets Optimize command, which re-connects the nets using a shortest distance, X-bias, or Y-bias strategy. Run the command now, either selecting it from the menus or from the Nets Speed Palette. Choose the Minimize Total Length option and click on OK.

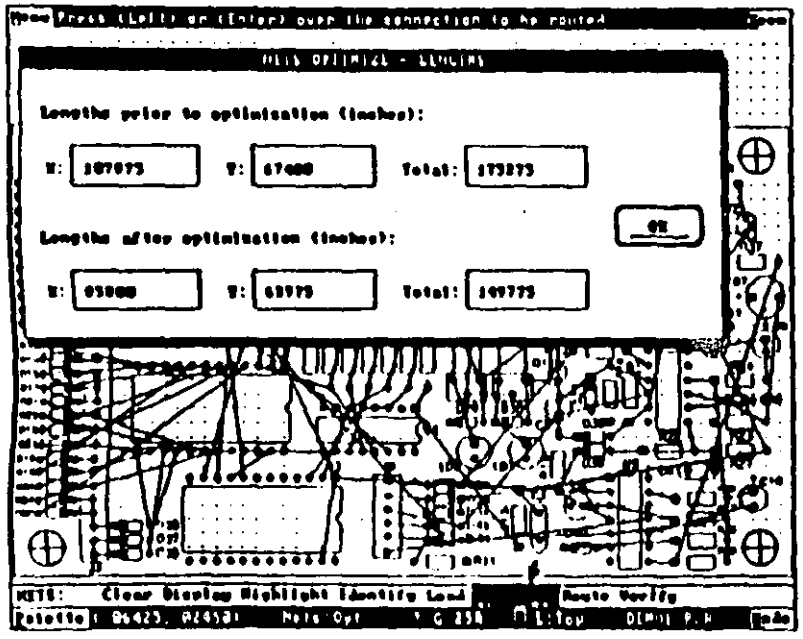


Figure 4-14. Use the Nets Optimize command to help clean up the rat's nest.

Tango-PCB PLUS takes a few moments to recalculate all connections and, prior to redrawing the new rat's nest, displays the reduction in connection inches. In this case, the length prior to optimization is 175.275 inches and the length after optimization is 149.775 inches (Figure 4-14). Click on OK to view the rat's nest.

With the nets now optimized, you get a visual cue to the effectiveness of your initial component placement. Parts which might be better placed are identified by long connections flung to disparate locations on the board. The Move Component command provides an effective tool for highlighting and moving components and their connections.

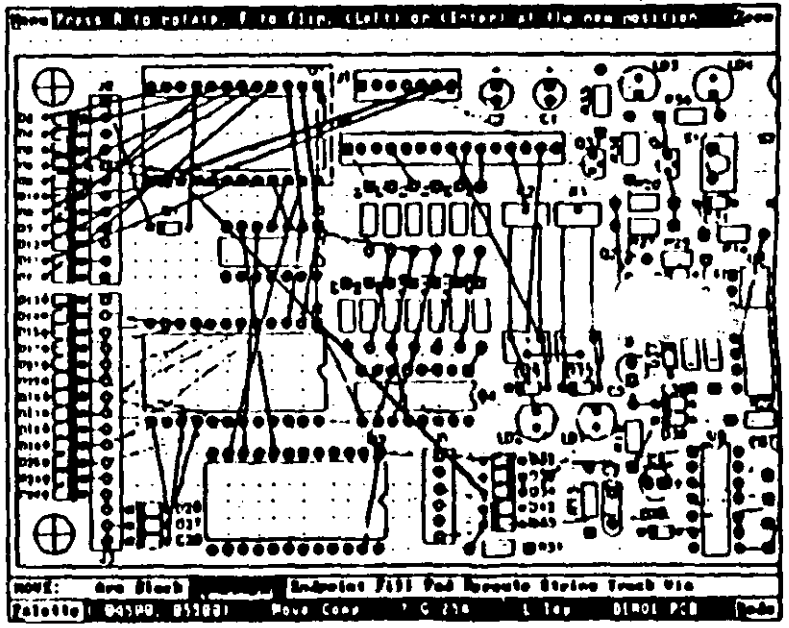


Figure 4-15. When you run the Move Components command, Tango-PCB PLUS highlights and dynamically rubberbands connections to the component.

Change to Move Component mode now by selecting the command from the menus or the Move Speed Palette. Place the cursor over an IC, U1, (located at 4500,5500 in the top left portion of the board), and press <LeftMouse> or <Enter>. The component and its connections are highlighted for easy viewing. Move the part in any direction, flip or rotate it, and its connections are dynamically rubberbanded (Figure 4-15). As it turns out, this component is fairly well placed, so press

<RightMouse> or <Esc> to cancel the operation and return the part to its original position.

Now place the cursor over the diode D1, (located at 3400,4600, just below U1), and press <LeftMouse> or <Enter>. Both connections to this component lead to the top of the board, indicating it should be moved up. Practice rubberbanding other components with Move Component.

While the rat's nest and Move Component operations help you visually see the density of connections on the board, they can become overwhelming on boards of average or greater complexity. A cleaner, easier way to see what's going on is to use Tango's force vector display. Force vectors are arrows emanating from each component which represent the weighted average of all connections to that component. They give an indication of where the component should be moved to reduce the connection length to that component.

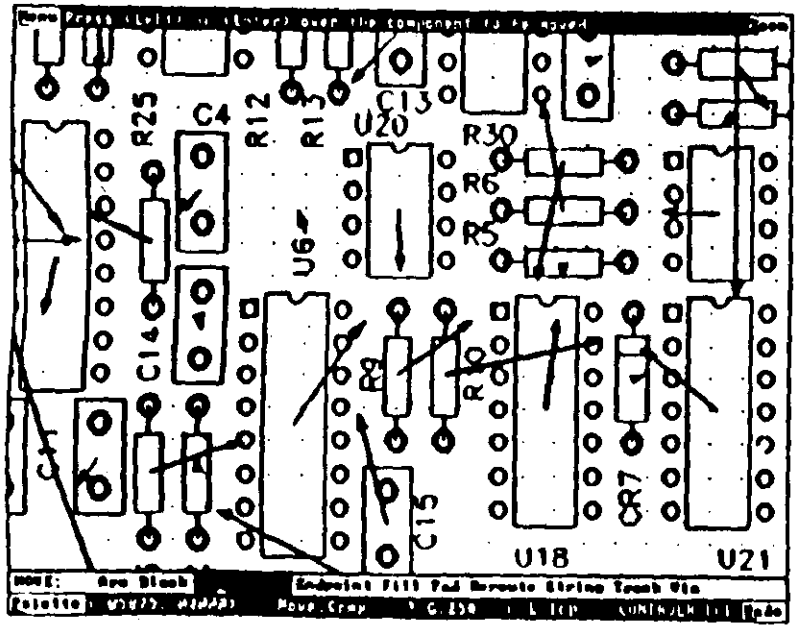


Figure 4-16. Force vectors aid component placement.

To display force vectors, enable their display in the Nets Display dialog box. Generally, you will want to hide all connections (the rat's nest) during the display of force vectors.

If you move a component, its force vector is updated as it is moved; once you place the component, the force vectors for all components connected to the component just moved are also updated.

Another handy feature for getting a feel for the overall effect of each component move is to toggle Undo several times (just press U or click on the Undo hot spot), before accepting the move or trying again.

Good component placement is still more of an art than a science, but Tango's placement tools augment your own judgment and experience to make the job go faster.

4.15 Routing Nets

Assume now that the component placement is optimal. The next step is to begin routing actual traces on the board. If you were a Tango-Route owner, at this point you would simply save the design to a PCB file and load the board and its net list into Tango-Route for autorouting. Should Tango-Route not complete 100% of the connections, you would come back to Tango-PCB PLUS for manual routing of the remaining connections, which are displayed in rat's nest fashion on the Connections layer.

Without the aid of Tango-Route, you are faced with the task of manually routing traces in Tango-PCB PLUS. But keep your chin up, because Tango's powerful editing tools again come through to make this task easier. With the net list loaded, you can use the Nets Display command to display individual connections for easy manual routing.

Selecting a connection to work on can be a difficult task with the entire rat's nest displayed, even on smaller boards. Average designs can easily contain hundreds of nets, making the ability to selectively display a subset of them an important feature.

To selectively display individual nets, we'll use the Nets Display command. Since you are going to use several of the Nets commands in

the component pins of all nodes in a particular net (the Nets Highlight command).

4.16 Verifying Nets

Since you're free to make or break any connection in any net, you should verify that all connections have been made properly. You can wait and perform a board-wide check at the end of the design with Tango-PCB PLUS' integrated design rule checker. Or better yet, verify on a net-by-net basis during the layout process, *and* run Tango's DRC at the end for a final measure of confidence.

To verify the net we just completed (RESET), run the Nets Verify command. This command performs an electrical design rule check on all nets currently displayed using the Nets Display command. Since RESET, and only RESET, is displayed, its connections as shown on the screen will be checked against the net list. Any incorrectly connected or missing pins will be flagged with an error message which is displayed on the screen. You have the option of continuing the verification process or stopping to fix the problem.

If there were other nets on the board displayed with Nets Display, they too would undergo the net list verification. Late in the design, you may find it necessary to break connections, which were previously completed and verified, to make room for a subsequent trace. Even though you diligently re-connected the broken nets, a final and complete DRC can greatly enhance your peace of mind.

4.17 Checking the Entire Design

The Nets Verify command is designed to be used interactively during layout and manual routing. Its verification is limited to making sure the connectivity of a routed net matches that in the net list.

Complementing Nets Verify is Tango's integrated design rule checker. The DRC operates on a board-wide basis, verifying both electrical connectivity and clearance gaps which you specify as design rules.

Running the design rule checker on your board is a two step process. First you run the Setup DRC command to establish the clearance gaps for pad-to-pad, pad-to-track and track-to-track checking on a per-layer basis. You also select the contents of the design rule check report, which may include: clearance violations, string violations, net list violations, single node routes and unconnected pins.

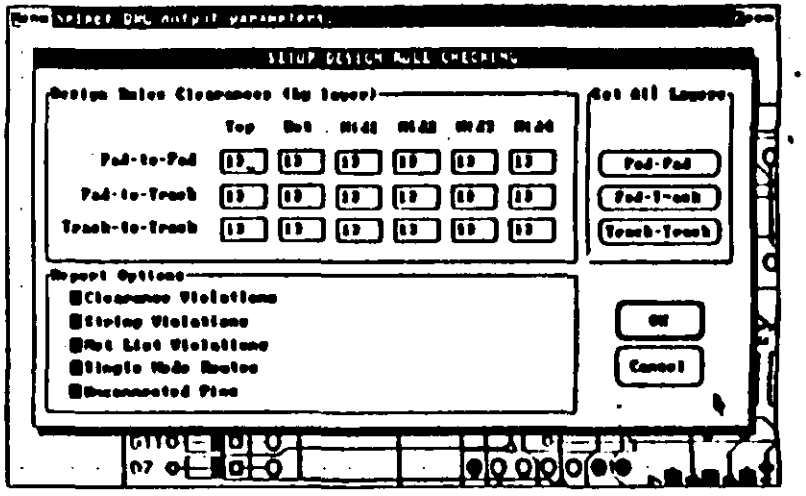


Figure 4-19. The Setup DRC dialog box.

Once the DRC options are set with the Setup DRC command, run the Output Reports command and enable the Design Rule Check report. You may print the report or write it out to a file on disk.

When you click on OK, the program will begin the design rule checking process, highlighting each connection as it is verified. When completed, the DRC report will print out or be written to a file.

The DRC is compute-intensive and can take a while on complex designs, though it is many times faster and much more accurate than checking a board by hand.

You don't have to have a net list loaded to produce a DRC report. In this case, however, the DRC will be limited to a check of clearance violations and string violations based on the rules you establish with the Setup DRC command.

4.18 Nets In A Nutshell

And so, to summarize, Tango-PCB PLUS includes powerful net list operations which allow you to display all nets (the *rat's nest*), individual nets, pins in a net, or all connections to a given component. You can also display *force vectors* to aid with placement. You are not required to maintain the validity of the net list during editing. Instead, you can verify the validity of your connections after drawing them.

The process of designing a board in Tango-PCB PLUS with the use of a net list follows these easy steps:

- Place the components on the board using the same reference designators (U1, U2, etc.) as in the net list.
- Load the net list, display all nets, and use the rat's nest or force vectors and the Nets Optimize and Move Component commands to optimize parts placement.
- Use Nets Display to display a single net.
- Use Nets Route to route each connection in the net.
- Use Nets Verify to check all connections in the net against the net list.
- Repeat the last three steps (display a net, route its connections, verify the net) until the board is completed.
- Run the Design Rule Check report on the entire design.

4.19 Output Options In Tango-PCB PLUS

It should be obvious by now that we're very proud of the ease-of-use and powerful editing features of Tango. There is no question that displaying a dense design on a 19-inch monitor running 1024 x 768 resolution is the sexy part of the CAD business. However, we've designed and built boards ourselves and we know that the most important function a PCB layout program must do is create crisp, accurate output for board production.

In Tango, we paid particular attention to generating the highest quality output, available on devices ranging from dot-matrix printers to Gerber-format photoplotters. We use our menus, dialog boxes, prompts and on-line help to take the mystery and frustration out of generating artwork, photoplot files, and even proper communications with pen plotters.

Let's review the output options included as standard features in Tango-PCB PLUS. Select the Output command from Tango's Main Menu. The Output Menu commands make it easy to:

- Setup photoplot aperture assignments.
- Create photoplot and N/C drill files.
- Pen plot multi-color check plots or final artwork at any scale.
- Generate check prints or even prototype-quality final artwork on your dot matrix or laser printer.
- Generate DXF and PostScript files for use with compatible mechanical CAD, desktop publishing and word processing software. You can even get high-quality, inexpensive final artwork on PostScript-compatible phototypesetters.
- Generate a selection of printed reports, ranging from the Bill of Materials to aperture assignments.

4.20 Printing And Plotting

We encourage you to take the time to print or plot a Tango file and see both our speed and quality of output. We've included the file RDEMO1.PCB with your Tango-PCB PLUS package, which may be plotted or printed.

Run the File Load command to load RDEMO1.PCB. Again, the program asks if you wish to save the changes to the current PCB file. Click on No Save.

NOTE

If you use a serial port for either printer or plotter, you must run the Setup Communications command to set options for baud rate, data bits, stop bits, parity, and handshake before running the Output Plot/Print command. Consult your printer or plotter manual for the proper settings. You do not need to run Setup Communications if your output device is connected to your computer by a parallel port.

Now run the Output Plot/Print command. The first dialog box which appears allows you to select which layers of the board you wish to print or plot (Figure 4-20). Other options toggled with this dialog box include single or multi-color artwork, draft or final artwork quality, mirror image, holes in pads and vias, and component reference designators and types.

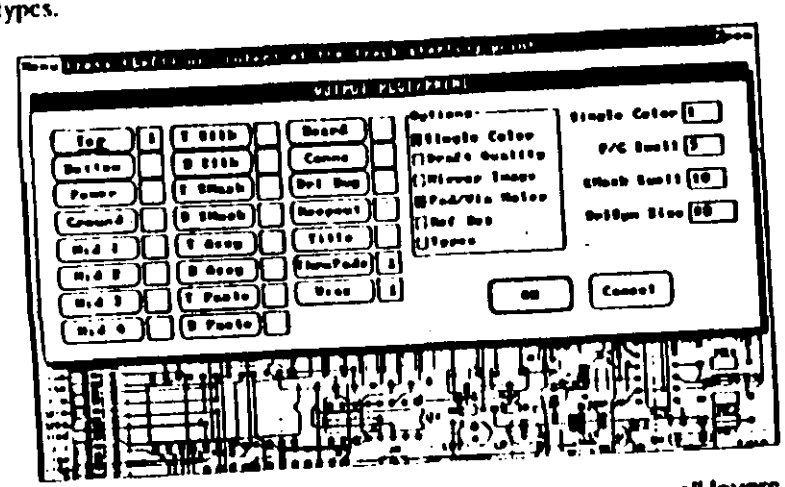


Figure 4-20. Produce draft or final artwork for any or all layers of your board.

You also use this dialog box to specify the pen number for single color plots, Power/Ground plane swell, Solder Mask swell and drill symbol size. All of these options are stored automatically for you in the initialization file PCB.INI to save you the trouble of resetting them each design session.

Choose the layer(s) of RDEMO1 you would like to print or plot, any other options which seem appropriate, and click OK.

A second dialog box appears which presents two list boxes, one for printer and plotter drivers, and one for output ports. First select from the list box the appropriate printer/plotter driver for the device you want to use (Figure 4-21). Consult your printer or plotter manual if you are unsure of its default driver. If your device is not displayed in the list box, check for a compatible driver. For instance, most plotters are either HP-GL or DM-PL compatible, and many printers are Epson FX compatible. The numerals beside the printer drivers indicate their resolution (in dots per inch).

The drivers used to generate DXF, PostScript and Encapsulated PostScript files are also selected from the driver list box.

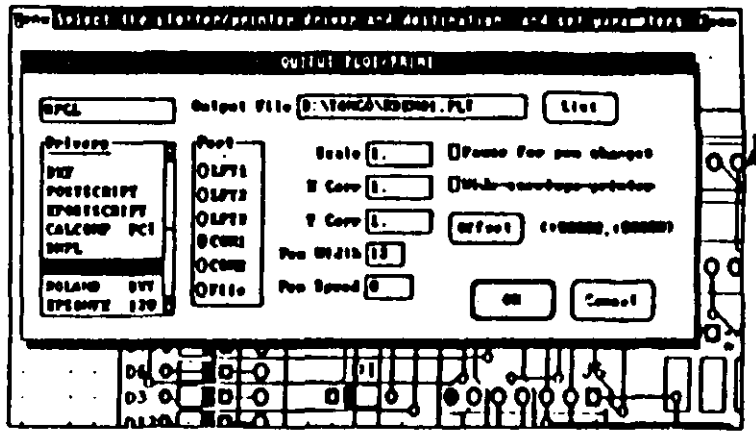


Figure 4-21. Tango supports a wide variety of printers and plotters, with more being added all the time.

Next click on the printer or plotter port you're going to use to output from your computer to the device. Other options which may be set with this dialog box include plotting or printing to a file, setting the artwork scale, X and Y correction values, pen width and speed, pause for pen changes, wide (15-inch) carriage printers, and offset dimensions. Again, any settings you make will be saved in PCB.INI.

After selecting your device driver and port, choose any other options which suit your fancy and click on OK. The program will begin to generate your artwork.

On narrow printers, dot matrix or laser, Tango-PCB PLUS will automatically print any artwork which is too wide for the printer in strips which may be taped together. If you wish to print or plot the artwork rotated 90 degrees, or mirrored, just click on those options in the Output Plot/Print dialog box.

Try experimenting by generating plots or prints for alternate layers, varying scale, draft and final artwork, assembly and drill drawings, and so on. We think you'll agree, Tango generates beautiful art, worthy of your best designs.

4.21 Viewing Photoplot Files

We have one more important feature of Tango-PCB PLUS that we would like to show off before we let you go out on your own. Maybe you have heard from friends or even experienced first-hand the problems which can sometimes arise when photoplotting your artwork. Tango-PCB PLUS takes a very logical approach to creating photoplot files from your design, but even still, a file on-disk is an invisible thing. Mistakes that may have been made along the way will not show up until your service bureau delivers your photoplots, which can be an expensive experience.

This is why we have built into Tango-PCB PLUS a photoplot file viewer. You can load in a photoplot file created with Tango and it will be displayed on-screen exactly as it will be photoplotted. Use all of Tango's zoom and pan functions to inspect the file, even print or plot out a copy for documentation and verification.

If you detect a problem, simply load the original PCB file, correct the error, generate a new photoplot file and load it for viewing. It's all done seamlessly in one integrated program.

Since you may not have yet learned how to generate a photoplot file, we have supplied one to help get you acquainted with the viewer. Run the File Load command and click on the Photoplot pushbutton. Now key in

VGADEMO.TOP in the file name entry box. When you click OK, Tango-PCB PLUS will load the photoplot file, which is the top layer of the VGADEMO printed circuit board design.

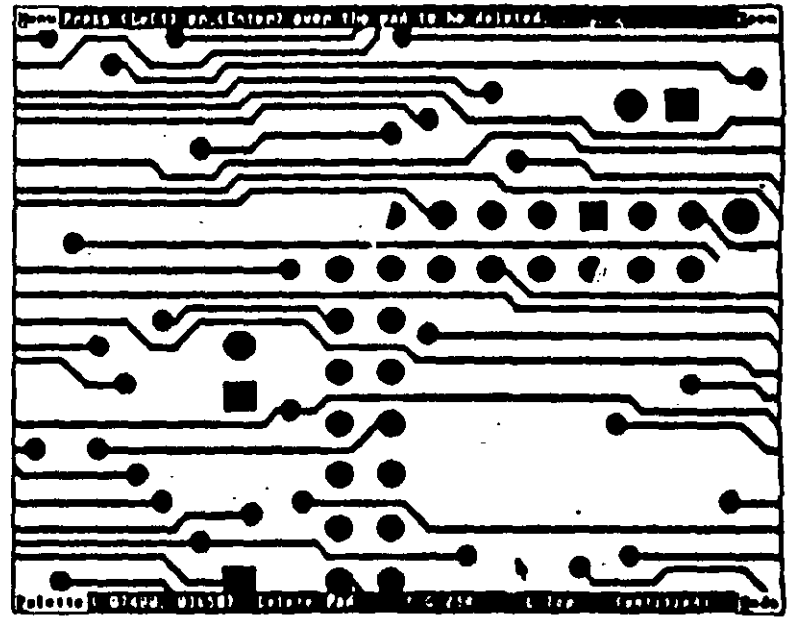


Figure 4-22. Viewing a photoplot file within Tango-PCB PLUS.

4.22 Summary

By now you should have a pretty good feel for what Tango-PCB PLUS is all about. We've tried to cover as many features as possible, and still not consume the better part of a day.

In review, you quickly learned how to operate the ACCEL Productivity Interface, with its pop-up menus, dialog boxes, hot spots, Speed Palettes, and on-line help. You placed components and text, manually routed connections, deleted a component, and used the Undo command to un-delete the component. You loaded a net list and used the rat's nest, net list optimizer, move component and force vectors functions to optimize parts placement. Then you displayed, routed, and verified

connections with net list support. Finally, you output final and/or draft artwork to your printer or plotter and viewed a photoplot file.

But no PCB design system worth its stuff can be adequately described in a 35-page tutorial. Here's a partial list of the dozens of features we haven't discussed. You can find out more about these features by reading the rest of the manual or by using Tango's extensive on-line help:

- **Block operations.** Besides saving and loading blocks, you can delete inside or outside blocks, and rotate, copy, and move blocks.
- **Global editing.** The Edit commands make it easy to change the characteristics of arcs, components, pads, strings, tracks, and vias on the board. You can edit any particular item or all matching items.
- **Move operations.** Moving previously placed tracks is facilitated by three commands: Move Track, Move Endpoint, and Move Reroute.
- **Jump commands.** These commands allow you to quickly locate and move to components, locations, nets, and strings.
- **Orthogonal routing.** When placing or re-routing tracks, type O to toggle between non-orthogonal mode and four different orthogonal routing styles (enabled using Setup Options).
- **Place commands.** Practice placing other elements in the design, such as pads, area fills, and arcs.
- **Nets Highlight.** This handy command will highlight all connected pads, tracks, vias, arcs, and fills, even without a net list loaded.
- **Nets Generate.** Generates a Tango-format net list from the currently loaded board design.
- **Print Reports.** Use Output Reports to print a Bill of Materials and other useful reports.

The Learning Tango-PCB PLUS tutorial introduced the following commands:

Command	Function
Current Layer	Set the current layer for editing
Delete Component	Delete a component on the PC-board
File Load	Load a PCB or block file
Library Browse	Display and list components in a library
Move Component	Move/rotate/flip a component on the PC-board
Nets Display	Select nets to be displayed
Nets Load	Load a net list
Nets Optimize	Create optimized connections for displayed nets
Nets Route	Replace connections with tracks
Nets Verify	Verify that the PC-board matches the net list
Output Plot/Print	Plot or print the current PCB file
Place Component	Place a component on the PC-board
Place String	Place a text string on the PC-board
Place Track	Place a track on the PC-board
Setup Display	Enable/disable and select colors for PC-board layers and items
Setup DRC	Set the design rules and report options for the design rule check report
Setup Grids	Set the absolute, relative, and visible grid sizes
Setup Options	Enable/disable Orthogonal modes and Drag Tracks With Components option
Setup Palette	Add or delete items on the custom Place Palettes
Undo	Undo the previous editing command
Zoom Board	Display the entire PC-board
Zoom Window	Zoom in or out on a section of the display

7 PC-Board Layers

7.1 Introduction

Tango-PCB PLUS provides 19 separate PC-board layers. You can display and print/plot/photoplot individual layers or a composite of two or more layers. You can only edit one layer at a time. The layer to edit is termed the *current layer*.

The program provides the following 19 PC-board layers:

Top
Bottom
Power
Ground
Middle Layer 1
Middle Layer 2
Middle Layer 3
Middle Layer 4
Top Silkscreen
Bottom Silkscreen
Top Solder Mask
Bottom Solder Mask
Top Assembly
Bottom Assembly
Board
Connections
Drill Drawing
Keepout
Title

A majority of the 19 layers -- all signal layers and the Top and Bottom Silkscreen -- are used directly as artwork for fabricating the PC-board. You can place pads, tracks, components, text, vias, arcs, and area fills on any of these layers.

It is the usual and recommended practice to lay out the PC-board as it is seen looking at the components on the board. This way text is displayed on the screen as it will appear on the Top Silkscreen layer (not mirror-imaged). You can think of the layers as stacked on one another with the Top Silkscreen Overlay on top, then the Top layer, the Middle Signal layers and Power/Ground planes, the Bottom layer, and the Bottom Silkscreen layer.

The remaining layers serve as guides for individual steps in the board fabrication process. For example, the Top and Bottom Assembly layers provide instructions for connecting and attaching components to the finished PC-board.

7.2 Top And Bottom Layers

The Top and Bottom layers correspond to the top and bottom sides of the PC-board. Before surface-mount technology, designers called the Top layer the *component side* and the Bottom layer the *solder side*. Though this terminology still holds true for designs that are exclusively through-hole, you can place surface-mount components and solder on *either* side of the board.

7.3 Power And Ground Planes

The Power and Ground Planes are different from the other signal layers in that they consist mostly of copper, with only small sections etched away. For this reason they are plotted in the negative. Connections to the Power and Ground planes are displayed using symbols placed on through hole pads. You cannot edit the Power and Ground planes individually or place items (such as tracks) on these planes.

You can connect component pins to the Power and Ground planes by *tagging* pads. When editing a pad, the program allows you to connect the pad to the Power or Ground plane either directly or through a thermal relief.

7.3.1 What Are Power And Ground Planes?

Tango-PCB PLUS offers true Power and Ground plane capabilities. Circuits using high clock speeds radiate a considerable amount of spurious noise. Power and Ground Planes are necessary to shield sensitive sections of the circuit from this noise. Poor shielding results in high speed flip-flops toggling randomly, leading to erratic circuit behavior. As well, there are now stringent FCC specifications for the amount of radiated energy allowed from electronic equipment. Power and Ground planes, in conjunction with proper equipment shielding techniques, minimize the radiated energy from electronic circuitry.

Some logic families draw a large transient current during state transitions; if the power and ground lines to those devices have a high impedance, large spikes are superimposed on the lines. These spikes often affect other devices down the line, and bypass capacitors can only go so far to alleviate these spikes. Power and Ground planes, in conjunction with bypass capacitors, deliver consistent low-impedance power to all devices on the PC-board.

Just what are the characteristics of Power and Ground planes? Imagine a plane of copper in the middle of your board, with holes in the copper wherever leads pass through the board. The holes are big enough to ensure clearance from the leads, but small enough to provide ample shielding around all closely spaced leads. Now suppose that the plane we are discussing is to be used for the Ground Plane. To connect a lead to the ground rail, fill the hole at that point with copper - the lead will now be in contact with the plane. Thus, the plane has holes in it at every point where a lead is not to be connected to the plane. The Power Plane is similar, with holes at every lead not to be connected to the power rail.

The Power and Ground planes are generally the innermost layers of a PC-board for two reasons. With the PC-board material sandwiched between them, the Power and Ground planes form a bypass capacitor for the supply rails with a low *Effective Series Resistance* (ESR). Recall that capacitance increases as the gap between the plates decreases, so the smaller the gap, the larger the capacitance. The second reason is that by having the planes interior to the signal layers, sensitive signal lines can be isolated from noisy lines by placing them on opposite sides of the planes.

7.3.2 Direct Connections And Thermal Reliefs

A lead is connected to a plane by having no clearance hole in the plane at that point. This provides good conduction between the lead and the entire plane, both electrically and thermally. The first is desirable, the second is not necessarily so good. When the board is soldered, any leads connected directly to a large area of copper will not rise in

temperature as quickly as other leads. This can either cause poor solder joints or require more heat, neither of which is desirable.

The solution is to connect the lead electrically but not thermally to the plane of copper, using a special symbol called a *thermal relief* (Figure 7-1). A thermal relief is a small island of copper around the lead, isolated from the plane by an annular gap. The plane is then connected to the island by four narrow bridges of copper (termed *spokes*). These spokes provide the electrical connection and the gap provides the thermal isolation.

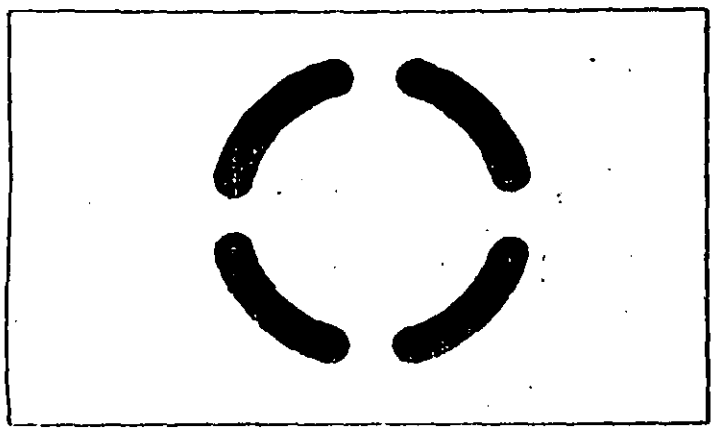


Figure 7-1. A thermal relief connects a component lead to a plane electrically but not thermally.

When running the Edit Pad command, you can tag a pad to the Power or Ground plane by means of either a direct connection or a thermal relief. A small cross (+) in the center of the pad indicates that the pin is connected to the Power or Ground plane with a thermal relief. A direct connection to a plane is indicated by an X in the center of a pad (Figure 7-2).

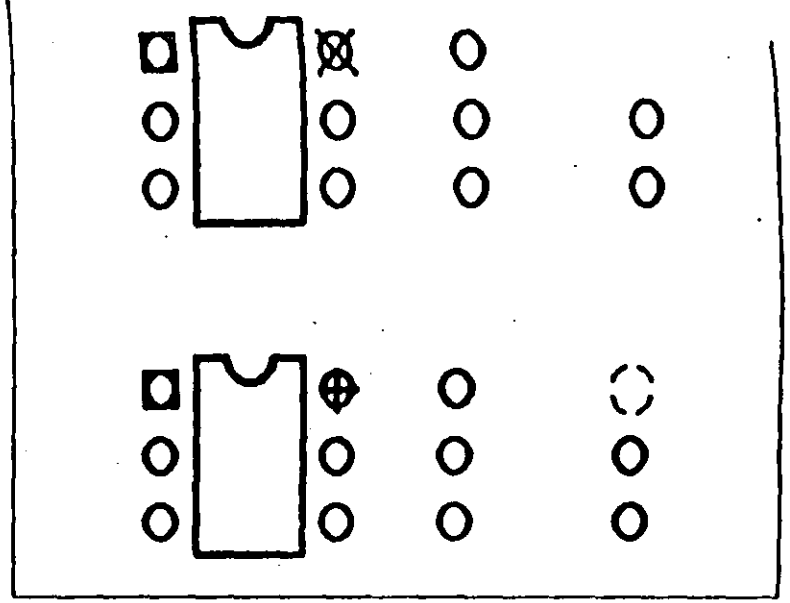


Figure 7-2. A direct connection (X) and thermal relief (+) as they appear on the Tango-PCB PLUS screen (left) and in the final artwork (right).

The small cross and the X let you tell at a glance whether a pad is connected to a plane with a thermal relief or direct connection. But how can you tell whether the pad is connected to the Power or Ground plane? By running the Setup Display command, you can assign separate colors to the Power and Ground planes. A good practice is to use red for the Power plane (red = hot = power) and green for the Ground plane (green often signifies ground connections).

There are three options for connections to the planes: no connection (signified by the pad only and no special symbol), a thermal relief (signified by a cross of the appropriate color in the center of a pad), or a direct connection to the plane (signified by an X of the appropriate color in the center of a pad). The program does not allow you to connect a pad to both planes. This may seem trivial, but it is amazing how many manually taped PC-boards end up with shorted Power and Ground planes!

When the planes are interior to the board, thermal reliefs are generally used. If you are designing a double-sided PC-board and you want a bare copper Ground plane for the Bottom layer (as is often the case for RF designs), then you can use direct connections to the Ground plane.

7.3.3 Connecting Nets To Power And Ground

When loading a net list (using the Nets Load command), you can direct the program to automatically tag all pads that are connected to the Power and Ground planes. In the Select Plane Nets dialog box (Figure 7-3), enter the name of the Power plane net and the name of the Ground plane net. You can also select either direct connections or thermal reliefs.

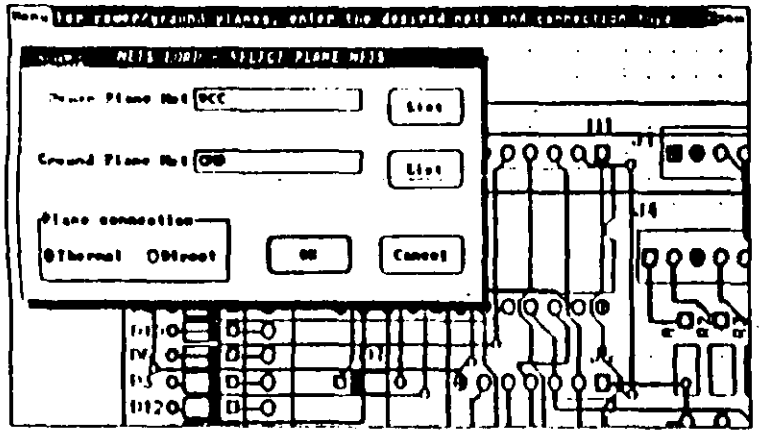


Figure 7-3. Tango-PCB PLUS automatically connects all pads in the specified Power/Ground plane nets to the correct planes.

For example, if your Power plane net has the name VCC, then specifying this net name connects all nodes within the net to the Power plane with either direct connections or thermal reliefs. Specifying the net name GND for the Ground plane net automatically connects all nodes within this net to the Ground plane. (For detailed information on loading net lists, see Chapter 14: Nets.)

7.4 Middle Signal Layers

The four Middle Signal layers are sandwiched between the Top and Bottom layers. You can place any Tango-PCB PLUS item on these layers. The Middle layers are additional signal layers available for multi-layer PC-boards.

7.5 Top And Bottom Silkscreen

The Top and Bottom Silkscreen layers produce the patterns printed on PC-boards that show such information as component outlines, reference designators, and the company name. For through-hole boards, you generally need only a Top Silkscreen layer. For surface-mount designs with components on both sides of the board, you will need both the Top and Bottom Silkscreen.

7.6 Top And Bottom Solder Mask

The Top and Bottom Solder Masks determine where solder mask is applied to the PC-board during fabrication. When the board is soldered, this mask prevents possible shorts by restricting the flow of solder. Tango-PCB PLUS provides Top and Bottom Solder Masks to support surface-mount designs with components on both sides of the board.

The program automatically generates the Top and Bottom Solder Masks from the board design. All pads on the board are *swollen* (enlarged) on the solder mask film to assure that they're kept free of solder mask. In addition, you can place area fills on the Top and Bottom Solder Masks to designate other areas of the board that will not receive solder mask.

For example, it's good practice to place area fills on the Top/Bottom Solder Mask over all edge connectors on the board. Though Tango-PCB PLUS automatically swells the edge connector pads to provide clearance from the solder mask, it's still possible for solder mask to be applied between the fingers of the edge connectors. This can cause problems. Plugging and unplugging the board may wear down the

solder mask, which can eventually interfere with connections to the fingers. By placing area fills on the Top/Bottom Solder Masks, you can assure that solder mask is not applied at all within the area of the edge connector.

Also, many board assembly shops recommend that the area beneath a surface-mount component be kept free of solder mask. If applied, the solder mask could blister during the heat of the soldering process, forcing the surface-mount component upwards and out of contact with the pads. You can prevent the application of solder mask to these board locations by placing area fills on the Top/Bottom Solder Masks under all surface-mount components.

NOTE

Tango-PCB PLUS enlarges all pads on the solder mask film. These pads are swollen when you print/plot/photoplot the board. The pads do not appear swollen on the screen. The area fills you place on the Top and Bottom Solder Masks will not be swollen on the screen or the solder mask film.

7.7 Top And Bottom Assembly

The Top and Bottom Assembly layers can be used, together with the Title layer, to create assembly drawings. These drawings guide the assembly shop during the board assembly procedure. The drawings can include the board dimensions and the locations of the components to be mounted, as well as any special instructions. For example, the drawings could show the location of test points on the board with instructions to keep these sites free of non-conducting conformal coat.

The Assembly drawings can be used together with the bill of materials to define the type of component that is to be mounted at each location. The Bottom Assembly drawing is generally needed only if the board contains surface-mount components on the Bottom layer.

7.8 Board

The Board layer is used to draw an outline of your PC-board. This layer is also useful for indenting the copper on the Power and Ground planes. If the copper extends to the edge of the board on these layers, it could cause a short if the board edge comes into contact with a piece of metal or another board connection.

To indent the Power and Ground planes and prevent shorts, we recommend you draw the board outline with a 100-mil track. If you then print/plot/photoplot the Board layer in composite with the Power and Ground planes, the resulting copper will be indented by 50 mils, half the thickness of the board outline.

7.9 Connections

The Connections layer helps you manually route the PC-board. When you load a net list for your design, all connections in the net list are stored and displayed on the Connections layer. The connections are *point-to-point*: the shortest distance between nodes in a net.

After you manually route a connection in Tango-PCB PLUS (using the Nets Route command), the connection is removed from the Connections layer. If you are editing a board that has been autorouted by Tango-Route, the Connections layer contains only the *no-routes*: connections that could not be autorouted. (For detailed information on net lists and routing, see Chapter 14: Nets.)

7.10 Drill Drawing

The Drill Drawing layer provides the service bureau with the location of every hole on the board and the bit size needed to drill the hole. Tango-PCB PLUS automatically generates a layer that shows every hole on the board. Together with the Title layer, this layer can be used to produce a drill drawing.

Tango-PCB PLUS automatically places a symbol at each hole location which indicates the drill tool required. In addition, you may wish to

place a table on the Drill Drawing which maps symbols to tool numbers/drill sizes.

Depending on your service bureau, a Drill Drawing may not be necessary if the bureau has an N/C drill machine that accepts the standard Excellon-compatible N/C drill file generated by Tango-PCB PLUS. (For more information on the Drill Drawing layer, see **Chapter 16: Prints, Plots, And Reports.**)

7.11 Keepout

The Keepout layer allows you to specify areas of the board where Tango-Route will not place traces. By placing a track segment or area fill on the Keepout layer, you are directing Tango-Route to avoid routing over these locations on all signal layers of the PC-board.

For example, it is good practice not to place vias beneath surface-mount discrete capacitors. During fabrication, solder could force its way up the via and knock the capacitor out of contact with its pads. To make sure Tango-Route does not place vias in these areas, place an area fill on the Keepout layer beneath each surface-mount discrete capacitor.

7.12 Title

The Title layer is used to document your artwork for the board fabrication procedure. This layer should contain such information as the company name, board name, part number, and revision number. The Title layer consists of borders and text strings located outside the outline of the PC-board. You can print or plot the Title layer in composite with the Top and Bottom Assembly and Drill Drawing layers.

The Tango-PCB PLUS package includes Title layer templates for A-size (8.5 x 11 inches), B-size (11 x 17 inches), and C-size (17 x 22 inches) sheets of paper. These templates are stored in the PCB files ASIZE.PCB, BSIZE.PCB, and CSIZE.PCB. You can use these templates or create your own Title layer from scratch.

Each of the Tango-PCB PLUS Title layer templates contain a sheet border and a title block (in the lower-right corner of the sheet (Figure 7-4). The title block provides space for such information as the board's name, identification number, revision number, sheet size, date, filename, and designer.

The Title layer borders are 0.25-inches wide. They are divided into segments which are labeled with numbers across the top and bottom (the columns) and with letters down the left and right sides (the rows). The borders provide a convenient way to locate information on the board. For example, a designer can describe the location of a resistor, R5 as the intersection of row B and column 3.

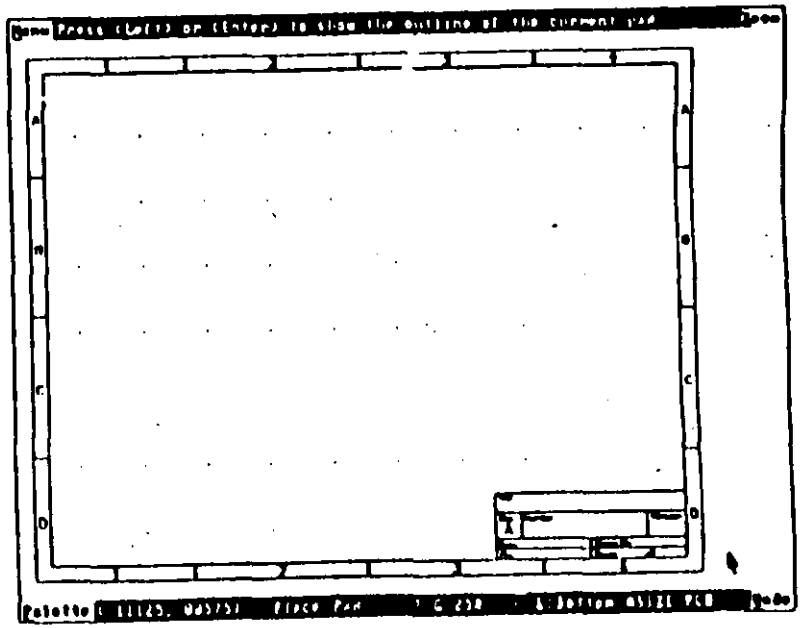


Figure 7-4. The Tango-PCB PLUS Title layer ASIZE.PCB.

7.13 Selecting Layers

The status line's Layer field displays the current layer for placing primitives. All editing takes place on the current layer. Thus, if you

place a track on the PC-board when the current layer is Top, the track is assigned to the Top layer. If you later want to delete this track, the current layer must again be set to Top.

The Layer field also shows the color of the current layer (in the small rectangle to the left of the L). When you place an arc, area fill, surface pad, text string, or track on the PC-board, the primitive is displayed in the color of the current layer. Individual colors can be selected for through-hole pads and vias, since these primitives belong to all layers of the board.

Clicking the mouse on the Layer field or typing L sets the current layer. All subsequent editing is performed on this layer. With each click of the mouse, the program cycles through a list of enabled layers and their colors. You can stop clicking the mouse when the desired layer is displayed. You can also set the current layer by selecting the Current Layer command from the Current Menu. For boards with only a few layers, clicking on the Layer field or typing L may be faster than using the menus.

7.14 Enabling And Disabling Layers

Before you select a current layer, the desired layer must be enabled. You can only edit and display enabled layers. It is useful to disable layers that you do not want to view or edit. Disabling these layers reduces the amount of PC-board information on the screen, allowing you to concentrate on the layer (or layers) that you're currently editing. Since less information is displayed, disabling layers also reduces the time it takes to redraw the screen.

Run the Setup Display command to enable and disable PC-board layers. In the Setup Display dialog box (Figure 7-5) there is a small box of color next to each layer field. This box shows the display color for the layer. If the color box is solid, the layer is enabled. If only the bottom half of the box is colored in (there is a dividing line across the center), the layer is disabled.

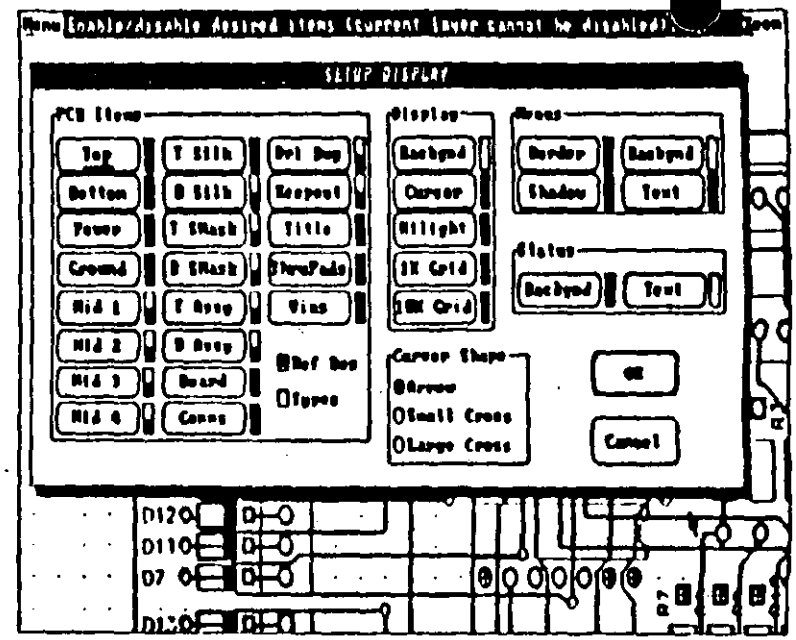


Figure 7-5. In the Setup Display dialog box, enabled layers are indicated by a solid box of color.

Clicking on the color box next to each layer toggles the layer on and off. For example, if Middle Layer 1 is disabled (only the bottom half of the box is colored in), click on the color box to enable the layer (the dialog box shows a solid box of color).

NOTE

When enabling or disabling a layer, make sure that the cursor is positioned within the color box *next to the layer's name. Positioning the cursor* on the layer name *allows you to change the color of the layer (see* Selecting Screen Colors *below).*

When you quit Tango-PCB PLUS, the settings in the Setup Display dialog box are saved in the file PCB.INI. These settings are automatically restored the next time you run the PCB program.

7.15 Selecting Screen Colors

Tango-PCB PLUS lets you have it your way. If you prefer purple pads and a pink cursor, you can have purple pads and a pink cursor. In addition to enabling and disabling PC-board layers, the Setup Display command lets you select the screen colors for individual layers and items (such as through pads and vias), the program menus, the status and prompt lines, and the workspace elements (including background, cursor, highlighting, and grids).

In the Setup Display dialog box, the current color is shown in a box next to each field (Figure 7-5). To change a color for a field, click the mouse on the field name. If your video card supports less than four colors, such as MCGA and Hercules, each click of the mouse cycles through the next available color.

If your video card supports four or more colors, such as EGA and VGA, the program displays a separate dialog box that shows all available colors. In this dialog box, select the desired color and then click on OK. The Setup Display field is updated to show the new color. Clicking on OK again removes the Setup Display dialog box and updates the screen colors.

The colors you select are saved in the file PCB.INI when you quit Tango-PCB PLUS and will be restored the next time you run the PCB program.

7.16 Summary

The following commands were discussed in this chapter:

Command	Function
Current Layer	Set the current layer for editing
Edit Pad	Edit a pad on the PC-board
Setup Display	Enable/disable and select colors for PC-board layers and items

8 Pads and Vias

8.1 Introduction

Tango-PCB PLUS provides user-definable pads and vias for PC-boards. This chapter describes how to define, place, edit, and delete pads and vias. Edge connectors, which consist of a series of surface pads, are also described.

8.2 Pads

A pad is a physical shape on the PC-board that generally corresponds to a component pin. Tango-PCB PLUS provides two types of pads: *through-hole pads* (which belong to all PC-board layers) and *surface pads* (which belong to either the Top or Bottom layer). The through-hole pads are used for component packages with leads that pass through all board layers. The surface pads are used for surface-mount components and edge connectors.

You can place or edit both through-hole pads and surface pads at any time regardless of the current layer setting. For example, if you want to delete a surface pad that belongs to the Top layer, you can do so whether or not the current layer is set to Top.

8.2.1 Selecting Pads

Before placing a pad on the PC-board, you need to run the Current Pad command to select the current pad. All subsequent Place Pad commands use the current pad settings. If you've added pad types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current pad by clicking the mouse on a pad entry in the

15 Verifying the Design

15.1 Introduction

No printed circuit board layout is complete until it has been checked to see that it matches the original electronic design and that, when manufactured, it has a reasonably good chance of working.

If you assume that the original electronic design, normally represented by a schematic, is correct, then you check to see that the PCB layout matches it on a component-by-component, connection-by-connection basis. In days past this task was accomplished with colored pencils and hours of tedious visual cross-checking. Now the process is greatly facilitated by the use of a net list, which is a list of all components and connections in the design.

Even if the layout matches the schematic electrically, the physical aspects of manufacturing the board can cause problems which will render it unusable. For example, tracks or pads that are too cl together could cause bridging of copper, creating a short. The l layout must be checked to see that clearances on the board exceed specified as your "design rules."

Tango-PCB PLUS offers two distinct, but complementary approaches to verifying the design.

15.1.1 Using Nets Verify

The Nets Verify command will check any nets which are currently displayed against an input net list. You use the Nets Display command to choose which nets to verify -- a single net, a collection of nets, or all nets.

This approach is especially useful if you are manually routing the board, but have an input net list. The recommended process is to 1) use Nets Display to show a single unrouted net, 2) route the net with the Nets Route command, 3) check the routed net with Nets Verify. Then use Nets Display to turn off the display of the routed net and to move onto the next net in the list.

15.1.2 Using The Design Rule Checker

The design rule checker in Tango-PCB PLUS has the ability to check the board electrically against the input net list, and to check for clearance gap violations against rules you establish with the Setup DRC command. Both checks are performed a board-wide basis and should be done when the layout is complete.

15.2 Net List Verification

The Nets Verify command automatically checks that the electrical connections for all displayed routed nets on the PC-board match the connections in the net list. The command verifies each net on a node-by-node basis. If it finds a short (a node that does not belong in the net) an open (a missing node), or an uncommitted component pin connected to the net, the program displays an error. (An uncommitted pin is not listed in the net list as part of any net.) If you are verifying more than one net, you have the option of continuing the verification process or stopping to correct the problem.

NOTE

The Nets Verify command verifies all currently displayed nets. *Before running this command, you need to run the Nets Display command to display (show) the net(s) that you want to verify.*

From the first component pin in the net list, Tango-PCB PLUS checks all connected tracks, area fills, arcs, vias, and pads. Each item is highlighted as it's checked.

If the program finds a component pin that does not belong to the net (a net short), it displays the error message:

Two nets shorted together.

This message includes the net names for the pins and the pin designators.

If the program finds an unconnected node in the net (an open net), it displays the error message:

Net not completely routed.

This message includes the pin designators for two of the unconnected nodes. Tango-PCB PLUS also highlights the sub-net (a group of connected nodes in the net) that includes the first of the unconnected pin designators.

If the program finds an uncommitted component pin in the net, it displays the error message:

Net connected to an uncommitted pin.

This message includes the pin designator of the uncommitted pin.

The Nets Verify command is designed to allow interactive net verification. When the command finds an error, it asks if you want to stop the verification process and fix the problem. Click on Continue to continue the verification process. Click on Cancel to stop the process.

If you choose to continue the verification process after the program reports a short or an open, Tango-PCB PLUS starts verifying the next displayed net. In this way, the program avoids displaying a long list of errors related to the one short or open. To make sure that there are no additional problems with the net, we recommend that you run the Nets Verify command again after you fix the short or open. If you choose to continue the verification process after the program reports an uncommitted component pin, Tango-PCB PLUS continues to verify the same net.

When continuing the verification process after error messages, jot down the errors as they occur. After Nets Verify is finished, you can then

all the problems on your list. Run the Nets Verify command again after modifying the board. If there are no error messages displayed, you can be assured that your net contains no open connections, shorts, or uncommitted component pins.

15.3 Design Rule Checking

After completing the layout, it's a good idea to do a board-wide check to make sure that all electrical connections in the PCB layout match the connections in the net list. This is especially important in Tango-PCB PLUS because the program does not hold nets "sacred". During the routing process, you may break nets without being warned or asked to rename the new net fragment. This speeds the revision process considerably since there are many times when you temporarily break a net. However, it also means that you can completely change the connections on the board.

Besides doing a board-wide electrical check, you should check the design to be sure that minimum clearances have been maintained throughout. Fortunately, both the electrical and clearance checking can be accomplished together with the integrated design rule checker in Tango-PCB PLUS.

To run the design rule checker, follow:

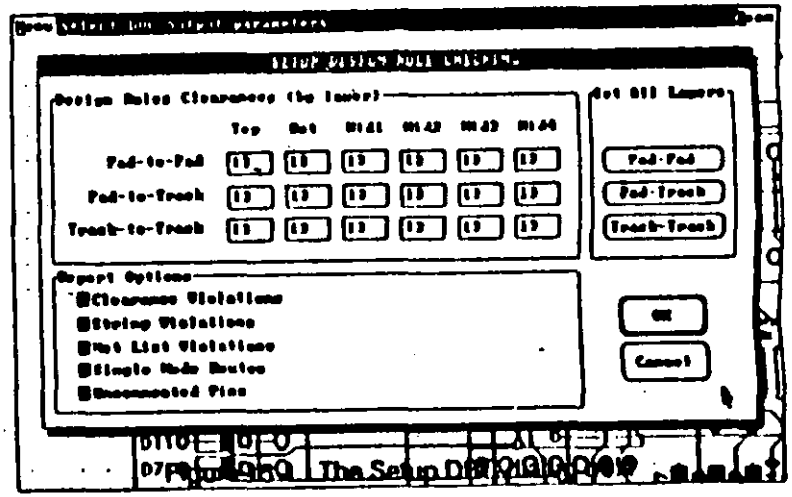
1. Load a net list with the Nets Load command. (This step may be skipped if no net list is available, as we'll explain below).

2. Establish your clearance gap rules with the Setup DRC command.

3. Start the design rule checker by selecting the Design Rule Check report in the Output Reports command.

15.2.1 The Setup DRC Command

Run the Setup DRC command to establish the design rule check parameters in preparation for generating a DRC report (using the Output Reports command). You can enter the minimum Pad-to-Pad, Pad-to-Track, and Track-to-Track clearances allowed on each of the six signal layers. There are also pushbuttons that allow you to set each of these clearances for all layers at once. All of these entries default to 13 mils (if you do not have a PCB.INI file).



The Setup DRC

You can also specify which conditions are to be checked for: Clearance Violations, String Violations, Net List Violations, Single Node Routes, and Unconnected Pins.

- CLEARANCE VIOLATIONS - Enables air-gap clearance checking. If disabled, no clearance errors will be reported.
- STRING VIOLATIONS - Enables air-gap clearance checking of strings on the signal layers. If you have placed strings on the signal layers, you should enable this option to make sure that the strings do not cross tracks. When checking for clearance violations, the bounding rectangle of the string is used. If the Clearance Violations option (above) has been disabled, this option is also disabled.

- NET LIST VIOLATIONS - Enables electrical checking against the net list. Items are considered to be connected if they overlap or have a clearance of less than 1 mil (just touching). Items that can be electrically connected to one another are arcs, fills, pads, tracks, and vias. Note that although strings can be checked for clearance violations, they are not considered to carry current. If a net list has not been loaded, this option is ignored.
- SINGLE NODE ROUTES - Enables the reporting of pins that are connected to other items on the board, but are not connected to any other pins. Note the use of the word "pin", which is a pad that is part of a component and has a pin designator (as opposed to a free pad, or a pad that is part of a component but does not have a pin designator). Again, items that can be electrically connected to one another are arcs, fills, pads, tracks, and vias.
- UNCONNECTED PINS - Enables the reporting of all pins that are not connected to other pins. This includes all of the Single Node Routes (described above) as well as pins that are not connected to anything at all.

15.3.2 The Design Rule Check Report

Once the DRC options are set with the Setup DRC command, run the Output Reports command and enable the Design Rule Check report. You may print the report or write it out to a file on disk.

When you click on OK, the program will begin the design rule checking process, highlighting each connection as it is verified. When completed, the DRC report will print out or be written to a file.

If you press <Esc> or <RightMouse>, you will be asked to verify your decision to halt the DRC. Should you decide to stop the DRC, the report will print anyway, with any violations encountered prior to the halt.

Running the DRC is a compute-intensive task which can take several hours on complex designs. Considering the alternatives, this seems a small price to pay compared to the benefits of design verification.

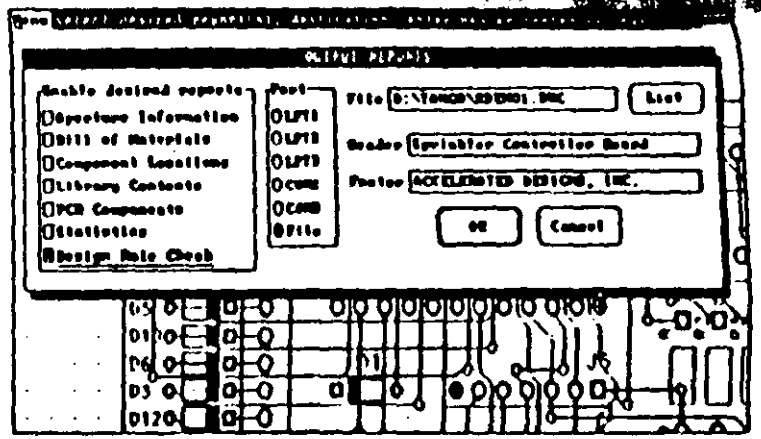


Figure 15-2. Select the Design Rule Check report with the Output Reports Command.

15.3.3 Running DRC Without a Net List

As mentioned above, you do not have to have a net list loaded to produce a DRC report. The DRC will be limited to a check of clearance violations and string violations based on the rules you establish with the Setup DRC command.

NOTE:

If you are running the DRC report without a net list, the design rule checker will report violations where the air-gap clearance is less than that specified. An actual short where two tracks are incorrectly connected will not be reported because the design rule checker will assume they are in the same net. This type of error can only be reported if a net list has been loaded.

15.4 Consideration for Mounting Holes

For mounting hole pads, both the Nets Verify command and the design rule checker consider only the drill hole dimension on inner board layers. This lets you place items such as tracks within the outer dimensions of the mounting hole pad on the inner layers (but not within the drill hole dimension). On the Top and Bottom layers, however, the Nets Verify does consider the outside dimensions of the mounting hole pad. This is because the program assumes the mounting hole pad's outer dimensions may be covered by items such as screw heads, nuts or washers which extend past the hole diameter on the Top and Bottom layers but which would have no effect on the inner layers.

15.5 Summary

Remember that the DRC report checks the entire board, as opposed to the Nets Verify command, which checks only the displayed nets (connections) for accuracy against the net list. Nets Verify is intended to be used repeatedly as the board is designed, so that errors can be fixed right away before more tracks are routed around them. Once you think the PC-board design is complete, generate the DRC report.

Check prints and multi-color check plots are also useful in verifying the PC-board. Tango-PCB PLUS's Nets Verify command and Design Rule Check report, however, can ensure the integrity of each net and clearances on the board, while sparing you the painful and frequently inaccurate task of visually inspecting the PCB artwork and checking connections against the schematic.

The following commands were discussed in this chapter:

Command	Function
Nets Verify	Verify the connections on the board match those in the net list
Setup DRC	Set up the clearance parameters for the physical design rule check
Output Plot/Print	Run the Design Rule Check report

16 Plots, Prints and Reports

16.1 Introduction

This chapter describes the Tango-PCB PLUS commands for printing, plotting, report generation, and special file output such as PostScript and DXF. The Output Plot/Print command lets you plot or print board. Whether you're plotting final artwork or making a quick check print, the program prompts you for all the necessary information with a series of dialog boxes.

The options for printing and plotting include the printer and plotter drivers, communications ports, plotter pen settings and printer colors, scale and X,Y correction values, board layer or layers (if printing a composite), output filename (if sending to a file), plot/print quality (final for artwork or draft for check prints), and the X,Y offsets for the plotter pen. The options you select are automatically saved in the file PCB.INI when you exit the program, then automatically re-loaded the next time you start the program.

In addition to printing and plotting, Tango-PCB PLUS provides the Output Reports command to generate a variety of reports on the PCB file. These reports can be output to a printer or file.

If your plotter or printer is connected to a serial port (COM1 or COM2), use the Setup Communications command to set the baud rate, parity, number of data bits, number of stop bits, and handshake protocol before running Output Plot/Print or Output Reports.

20 Commands

20.1 Introduction

This chapter provides a brief description of each Tango-PCB PLUS menu command and a cross-reference to where the command is discussed in the Reference Manual. It is designed to accommodate those of you who are already acquainted with Tango-PCB PLUS (or PCB design packages, in general) and, in most cases, require only an overview of the Tango-PCB PLUS functions.

20.2 Tango-PCB PLUS Commands

The Tango-PCB PLUS menu commands are briefly described in this section.

Current Layer

Description

Set the current layer. All subsequent editing is performed on the current layer. You can only choose from enabled layers when selecting the current layer. Use the Setup Display command to enable and disable layers.

The current layer and the color for the current layer are displayed in the status line's Layer field. You can also set the current layer by clicking on the Layer field or typing L, which toggles through the enabled layers. For boards with only a few layers, clicking on the Layer field or typing L may be faster than using the menus.

Cross-Reference

Section 7.13

Current Pad

Description

Set the current pad. You can choose from pre-defined pads or specify a new pad type. All subsequent Place Pad commands use the current pad settings.

The Pads list box shows all available pad definitions. The definitions are generated from the pads on the PC-board (these pad definitions are marked with an asterisk *) and in the Tango-PCB item definitions file PCB.DFN. If the desired pad type is not displayed in the Pads list box, you can define a new pad and add it to the list.

If you've added pad types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current pad by clicking the mouse on a pad entry in the palette.

Cross-Reference

Section 8.2.1

Current String

Description

Set the current text string. You can choose from pre-defined strings or specify a new string type. All subsequent Place String commands use the current string settings.

The Strings list box shows all available string definitions. If the desired string type is not displayed in the Strings list box, you can define a new string and add it to the list.

If you've added string types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current string by clicking the mouse on a string entry in the palette.

Cross-Reference

Section 10.2.1

Current Track

Description

Set the current track width. You can choose from pre-defined track widths or specify a new width. All subsequent Place Track, Place Arc, and Nets Route commands use the current track width.

The Tracks list box shows all available track definitions. If the desired track type is not displayed in the Tracks list box, define a new track and add it to the list.

If you've added track widths to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current track width by clicking the mouse on a track entry in the palette.

Cross-Reference

Section 9.2

Current Via

Description

Set the current via. You can choose from pre-defined vias or specify a new via type. All subsequent Place Via commands use the current via settings.

The Vias list box shows all available via definitions. The definitions are generated from the vias on the PC-board (these via definitions are marked with an asterisk *) and in the Tango-PCB item definitions file PCB.DFN. This file is automatically loaded when you run the PCB program. To select a current via type, click on the via definition in the Vias list box. Then click on OK.

If the desired via type is not displayed in the Vias list box, you can define a new via and add it to the list. To define a new via type, first select the shape. Specify the via size by entering values for the Dimension (even numbers from two through 250 mils) and Hole Diameter (from one through 250 mils) fields.

If you've added via types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current via by clicking the mouse on a via entry in the palette.

Cross-Reference

Section 8.3.1

Delete Arc

Description

Delete the selected arc on the current layer. If there is no arc selected on the current layer, the computer beeps.

Cross-Reference

Section 10.3.4

Delete Block

Description

Delete all items inside or outside a block. Tango-PCB prompts you to first define the block by marking two diagonally opposite corners of a rectangular area. The program then highlights the defined block.

You can select whether to delete items entirely inside (the default) or entirely outside the block and whether to delete items on the current layer or on all layers (the default). The program redraws the screen with the appropriate items deleted.

Cross-Reference

Section 13.4

Delete Component

Description

Delete the selected component. If there is no component selected, the computer beeps. If there is more than one component under the cursor (on a double-sided surface-mount board, for example), the program displays a list of all these components. You can then select the component to delete from the list.

Cross-Reference

Section 11.7

Delete Fill

Description

Delete the selected area fill on the current layer. If there is no area fill selected on the current layer, the computer beeps.

Cross-Reference

Section 10.4.3

Delete Highlight

Description

Delete all highlighted items, which include free tracks, pads, vias, arcs, and area fills. The items must have been previously highlighted using the Nets Highlight command. If a highlighted item belongs to a component, Tango-PCB will not delete that item. If there are no highlighted items, the computer beeps.

Cross-Reference

Section 14.7.1

Delete Pad

Description

Delete the selected pad. If there is no free pad selected, the computer beeps. This command has no effect on tracks that are connected to the pad.

If you attempt to delete a pad that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.2.5

Delete String

Description

Delete the selected text string on the current layer. If there is no text string selected on the current layer, the computer beeps.

If you attempt to delete a string that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 10.2.6

Delete Track

Description

Delete the selected track on the current layer. If there is no track selected on the current layer, the computer beeps.

If you attempt to delete a track that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 9.6

Delete Via

Description

Delete the selected via. If there is no via selected, the computer beeps. This command has no effect on tracks that are connected to the via.

If you attempt to delete a via that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.3.6

Edit Arc

Description

Edit the selected arc on the current layer. You can change the arc's radius, start angle, sweep angle, and line width. The radius is an even number from two through 16,000 mils. The start angle is an integer from 0 through 359 degrees. The sweep angle is an integer from one through 360 degrees. You can specify any line width from two through 250 mils (in two-mil increments). The line width cannot be more than twice the radius.

Tango-PCB makes it easy to edit a number of arcs on the board at one time. After modifying the arc, use the Arc(s) Edited options to determine whether the editing affects only the selected arc, a set of matching arcs, or all highlighted arcs.

Cross-Reference

Section 10.3.2

Edit Component

Description

Edit the selected component. You can change the component's reference designator, type, and value. You can also choose to release the component (which is similar to the *explode* funct common to most CAD programs). Releasing a component allows you to re-position and modify all the individual primitives in the component.

The Release option is especially useful when creating similar components. You can place a component on an unused area of the workspace, run the Edit Component command to release it, modify individual primitives, then run the Library Add command to define the modified pattern as a new component (see Chapter 12: Creating Library Components).

Cross-Reference

Section 11.5

Edit Pad

Description

Edit the selected pad. You can change the pad's shape, size, hole diameter, pin designator, layer, and plane. For the pad size, you can specify X (horizontal) and Y (vertical) dimensions of two through 4000 mils (in two-mil increments). You can specify any hole size from one through 250 mils.

Tango-PCB makes it easy to edit a number of pads on the board at one time. After modifying the pad, use the Pad(s) Edited options to determine whether the editing affects only the selected pad, a set of matching pads, or all highlighted pads. Matching pads have the same shape, X and Y dimensions, hole diameter, and layer as the selected pad.

Cross-Reference

Section 8.2.3

Edit String

Description

Edit the selected text string on the current layer. You can change the string's contents, height, and line width. You can specify any height from four through 1000 mils (in four-mil increments) and any line width from two through 250 mils (in two-mil increments).

Tango-PCB makes it easy to edit a number of strings on the board at one time. After modifying the string, use the String(s) Edited options to determine whether the editing affects only the selected string or a set of matching strings. Matching strings have the same height and line width as the selected string. If you choose any option other than This String, the Edit String command changes only the height and line width of the matching strings.

Cross-Reference

Section 10.2.4

Edit Track

Description

Edit the width of the selected track on the current layer. For the track width, enter an integer in the range of two through 250 mils (in two-mil increments).

Tango-PCB makes it easy to edit a number of tracks on the board at one time. After modifying the track, use the Track(s) Edited options to determine whether the editing affects only the selected track, a set of matching tracks, or all highlighted tracks. Matching tracks have the same width as the selected track.

Cross-Reference

Section 9.4

Edit Via

Description

Edit the selected via. You can change the via's shape, size, hole diameter, and Power/Ground plane connection. For the via size, you can specify a dimension of two through 250 mils (in two-mil increments). You can specify any hole size from one through 250 mils. The Plane field lets you connect vias to the Power or Ground plane by means of a direct connection or thermal relief.

Tango-PCB makes it easy to edit a number of vias on the board at one time. After modifying the via, use the Via(s) Edited options to determine whether the editing affects only the selected via, a set of matching vias, or all highlighted vias. Matching vias have the same shape, dimension, and hole diameter as the selected via.

Cross-Reference

Section 8.3.4

File Clear

Description

Clear the current PCB file from memory. If any changes have been made to the current PCB file during the editing session, the program prompts you to save the file, discard the changes to the file, or cancel the File Clear command.

Cross-Reference

Section 6.4

File DOS

Description

Execute DOS commands without quitting the Tango-PCB program. The program displays the standard DOS command prompt and you can now enter and execute any DOS command. To return to the Tango-PCB program from where you left off, at the DOS command prompt, enter:

```
exit
```

Cross-Reference

Section 6.7

File Load

Description

Load a PCB file (the default), block file, or a photoplot file. Loading a PCB file replaces the current PCB file with the specified file. Loading a block file inserts the specified file into the current PCB file. Photoplot files may be loaded for on-screen viewing.

Cross-Reference

Section 6.2

File Quit

Description

Quit the Tango-PCB program and return to DOS. If you have made changes to the current PCB during the editing session, the program prompts you to save the changes and exit, exit without saving the changes, or cancel the File Quit command.

Cross-Reference

Section 6.8

File Save

Description

Save the current PC-board or block to a file.

While marking a block during the File Save command, you can use the Zoom and Jump commands to move around on the workspace. You can also cancel the File Save command by pressing <RightMouse> or <Esc> or by clicking on Cancel in the File Save dialog box.

Cross-Reference

Section 6.3

Jump Component

Description

Jump to a specified component on the PCB. Enter the component's reference designator or select from a list of all reference designators on the PC-board. Clicking on OK moves the cursor to the reference point of the specified component (generally, pin 1). If the component is not currently displayed, the program redraws the screen at the same zoom level with the component's reference point at the center.

Cross-Reference

Section 6.5.2, 11.4

Jump Location

Description

Jump to a specified X,Y location on the PCB. Enter the X and Y coordinates of the location and click on OK. If the location is not currently displayed, the program re-draws the screen at the same zoom level with the specified location at the center.

Cross-Reference

Section 6.5.1

Jump Net

Description

Jump to the nearest component pin in a specified net. This command is useful when moving from one net to another during the routing procedure. Enter the net name or select a net from the Nets list box. Click on OK to remove the dialog box and jump to the specified net. If the nearest component pin in the net is not currently displayed, the program re-draws the screen at the same zoom level with the pin at the center.

The Jump Net command is only available if you have previously loaded a net list for the PC-board.

Cross-Reference

Section 6.5.4, 14.9

Jump String

Description

Jump to the nearest text string on the PC-board that matches a specified text string. Tango-PCB searches for an exact match of the specified string. The matching string must contain all and only all the characters in the specified text string.

Select **Current Layer** to search for a match on the current layer only (the default). Select **All Layers** to search for a match on all board layers. If the matching string is not currently displayed, the program redraws the screen at the same zoom level with the string at the center. The Jump String command is not case-sensitive (the characters can be either upper-case or lower-case).

Cross-Reference

Section 6.5.3, 10.2.3

Library Add

Description

Add a new component pattern to the current library. Enter the library name and the pattern name (of from one to 16 characters). After entering the pattern name, press <LeftMouse> or <Enter> to mark the first corner of a rectangle. The rectangular outline expands and contracts as you move the cursor. When the outline encloses the entire component pattern, again press <LeftMouse> or <Enter>. The program then prompts you to select a reference point for the pattern.

Cross-Reference

Section 12.5

Library Browse

Description

Display a component pattern in the specified library. In the Library Browse dialog box, the program displays a list of all patterns in the specified library. Selecting a pattern from this list displays the component on the right side of the dialog box.

Tango-PCB displays the component pattern as it would appear when placed on the PC-board, except for its actual size. The size of the component is scaled to fit within the dimensions of the dialog box. All primitives in the component are displayed. If a primitive belongs to a layer that is not currently enabled, the primitive still appears as part of the displayed pattern. Click on **Continue** to remove the Library Browse dialog box.

Cross-Reference

Section 11.2, 12.9

Library Delete

Description

Delete a component pattern from the specified library. To delete a pattern, highlight the pattern name in the list and click on the **Delete** pushbutton. Click on **Continue** to remove the Library Delete dialog box.

Cross-Reference

Section 12.8

Library Merge

Description

Merge (copy) a component pattern from a specified source library into a specified destination library. You can specify a new name for the pattern. If not, the program retains the source pattern name. Click on the Merge pushbutton to copy the source pattern into the destination library.

If a pattern with the same name exists in the current library, the program prompts you to enter a new pattern name, overwrite the existing pattern, or cancel the Library Merge command. You can continue to copy component patterns into the current library. Click on Continue to remove the Library Merge dialog box.

Cross-Reference

Section 12.6

Library Rename

Description

Rename a component pattern in the specified library. Select the current pattern name from the Patterns list box. Then enter the new pattern name. Click on the Rename pushbutton to rename the component pattern.

If a pattern with the new name exists in the library, the program prompts you to enter another new name, overwrite the existing pattern, or cancel the Library Rename command.

Cross-Reference

Section 12.7

Move Arc

Description

Move an arc on the current layer. First, position the cursor on the arc and press <LeftMouse> or <Enter>. If there is no arc selected on the current layer, the computer beeps. As you move the cursor, an outline of the arc moves across the screen. If you now change the current layer, the arc moves to the selected layer. Press <LeftMouse> or <Enter> to place the arc <RightMouse> or <Esc> to cancel the Move Arc command.

Cross-Reference

Section 10.3.3

Move Block

Description

Move all items contained entirely within a block. Tango-PCB prompts you to first define the block by marking two diagonally opposite corners of a rectangular area. The program highlights the defined block.

The program then prompts you to select a reference point for the block. Position the cursor on the reference point (generally, one of the corners of the block) and press <LeftMouse> or <Enter>.

If you move the block so that it overlaps any item on any layer of the PC-board, the program displays the Block Overlap Warning dialog box. Click on Retry to move the block to a different location. Click on Overlap to place the block with overlap in its current position. Click on Cancel to cancel the Move Block command.

Cross-Reference

Section 13.2

Move Component

Description

Move and rotate a component pattern on the PCB. First, position the cursor on the component and press <LeftMouse> or <Enter>. As you move the cursor, an outline of the component pattern moves across the screen. Press R to rotate the component 90 degrees. Press F to flip the component. Press <LeftMouse> or <Enter> to place the component and <RightMouse> or <Esc> to cancel the Move Component command.

Cross-Reference

Section 11.6

Move Endpoint

Description

Move the endpoint of a track on the current layer. This command is especially useful for moving a free pad or via on the PC-board while maintaining all routed connections to the pad or via.

When running the Move Endpoint command, first position the cursor on the endpoint of a track and press <LeftMouse> or <Enter>. As you move the cursor, the highlighted tracks stretch (expand and contract) with the endpoint. This process is called *rubberbanding*. Press <LeftMouse> or <Enter> to place the tracks. If there is a free pad or via at the endpoint, it moves to the new location. Press <RightMouse> or <Esc> to cancel the Move Endpoint command.

You cannot change the current layer during the Move Endpoint command.

Cross-Reference

Section 9.5.2

Move Fill

Description

Move an area fill on the current layer. First, position the cursor on the area fill and press <LeftMouse> or <Enter>. If there is no area fill selected on the current layer, the computer beeps. As you move the cursor, an outline of the fill moves across the screen. If you now change the current layer, the fill moves to the selected layer. Press <LeftMouse> or <Enter> to place the fill and <RightMouse> or <Esc> to cancel the Move Fill command.

Cross-Reference

Section 10.4.2

Move Pad

Description

Move and rotate a pad on the PC-board. First, position the cursor on the pad and press <LeftMouse> or <Enter>. If there is no pad selected, the computer beeps. As you move the cursor, an outline of the pad moves across the screen. Press R to rotate the pad 90 degrees. Press <LeftMouse> or <Enter> to place the pad and <RightMouse> or <Esc> to cancel the Move Pad command.

The Move Pad command has no effect on tracks that are connected to the pad. Run the Move Endpoint command to move a free pad and its connections.

If you attempt to move a pad that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.2.4

Move Reroute

Description

Reroute a track as a series of tracks and vias (if needed). This command is especially useful for cleaning up tracks that were dragged (rubberbanded) after running the Move Component command. First, position the cursor on the track and press <LeftMouse> or <Enter>. The endpoint of the track nearest to the cursor is termed the "pivot", the farthest endpoint is the "destination". As you move the cursor, a rubberbanding track outline is drawn from the pivot to the cursor. A rubberbanding line is also drawn from the destination to the cursor.

To place a track from the pivot to the cursor, press <LeftMouse> or <Enter>. The pivot now moves to the endpoint of this track. You can continue to place tracks by pressing <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to conclude the Move Reroute command and place a track from the destination to the cursor.

Cross-Reference

Section 9.5.3

Move String

Description

Move a text string on the current layer. First, position the cursor on the string and press <LeftMouse> or <Enter>. As you move the cursor, an outline of the text string moves across the screen. Press R to rotate the string 90 degrees. Press X to flip the component in the X direction. Press Y to flip the component in the Y direction. Press <LeftMouse> or <Enter> to place the string and <RightMouse> or <Esc> to cancel the Move String command.

Cross-Reference

Section 10.2.5

Move Track

Description

Move a track on the current layer. First, position the cursor on the track and press <LeftMouse> or <Enter>. If there is no track selected on the current layer, the computer beeps. As you move the cursor, an outline of the track moves across the screen. If you now change the current layer, the track moves to the selected layer. Press <LeftMouse> or <Enter> to place the track, <RightMouse> or <Esc> to cancel the Move Track command.

If you change the current layer *during* the Move Track command, the program automatically restores the previous current layer after the command ends. This allows you to move a series of tracks from one layer to another by running the Move Track command several times in succession.

Cross-Reference

Section 9.5.1

Move Via

Description

Move a via on the PC-board. First, position the cursor on the via and press <LeftMouse> or <Enter>. If there is no via selected, the computer beeps. As you move the cursor, an outline of the via moves across the screen. Press <LeftMouse> or <Enter> to place the via and <RightMouse> or <Esc> to cancel the Move Via command.

The Move Via command has no effect on tracks that connected to the via. Run the Move Endpoint command to a via and its connections.

Cross-Reference

Section 8.3.5

Nets Clear

Description

Clear the net list information. This command is useful if you want to clear a net list from memory without loading a new net list. If you run the Nets Load command to load a new net list file, the old net list is automatically cleared from memory.

The Nets Clear command clears all net list information, which includes the connections on the Connections layer and the net names associated with each pad. Clearing the net list (and not loading another one) disables the Nets Optimize, Nets Identify, and Jump Net commands.

Cross-Reference

Section 14.12

Nets Display

Description

Display the specified net list connections. The program displays a list box of all net names in the current net list. Displayed nets are marked with an asterisk. You can choose to show or hide individual nets, all nets connected to a specific component, or all nets. Note that if you have nets connected to the power or ground planes, these nets are marked with a "P" and "G", respectively.

This command also enables or disables the display of Force Vectors. Force vectors are the vector sum of the connections from a component, and are helpful in optimizing component placement.

Cross-Reference

Section 14.3, 14.5

Nets Generate

Description

Generates a Tango-format net list from the currently loaded PCB. The net list includes a listing of components, sorted by reference designator, and a listing of all nets. Each net is assigned a unique net name following the format "NET_*nnnn*" where *nnnn* is a four digit integer.Note that any connections to pads which are not part of a component, or do not have pin designators, will not appear on the net list.

Cross-Reference

Section 14.6, Appendix A

Nets Highlight

Description

Highlight a specified net. This command is useful for verifying manual routing, even if a net list has not been loaded. The Nets Highlight command works together with the Delete Highlight command to delete the items in a routed net on the board.

NOTE: The Highlight Nets command does not use (or require) a net list. The command highlights all items that are electrically connected on the board (generally, by means of tracks).

You can highlight only one net at a time. If a net is currently highlighted and you run the Nets Highlight command to highlight a different net, the program automatically removes the highlighting from the first net.

To un-highlight the net, press <LeftMouse> over a vacant portion of the workspace.

Cross-Reference

Section 14.7

Nets Identify

Description

Identify the net to which a pad belongs. The program prompts you to position the cursor on a pad and press <LeftMouse> or <Enter>. The net name for the pad is displayed in the Nets Identify dialog box. To remove the dialog box, click on OK or press <Enter> or <Esc>.

The Nets Identify command is disabled if there is no net list currently loaded.

Cross-Reference

Section 14.8

Nets Load

Description

Load a net list file. You can directly enter the net list filename in the File entry box of the Nets Load dialog box or you can click on the List pushbutton to select from a displayed list of net list files. The net list file must follow the Tango net list format described in Appendix A. The default filename extension for a net list file is .NET.

Cross-Reference

Section 14.4

Nets Optimize

Description

Create an optimized set of connections for the displayed nets. After you complete the component placement and load the net list, the Nets Optimize command provides a head start for routing the board. It is generally advisable to route the shortest traces first. The optimized connections show you the shortest traces at a glance.

In the Nets Optimize dialog box, select one of the displayed options: **Minimize X Length**, **Minimize Y Length**, or **Minimize Total Length**.

Selecting **Minimize Total Length** minimizes the total length, based on the Manhattan distance between pads. The Manhattan distance is the orthogonal distance between two points calculated as delta X plus delta Y.)

Cross-Reference

Section 14.10

Nets Route

Description

Route a connection interactively. This command lets you replace a displayed connection (which exists only as a routing aid) with a series of tracks and vias (if needed).

When running the Nets Route command, first position the cursor on the a displayed connection and press <LeftMouse> or <Enter>. If there is no connection at the specified location, the computer beeps. If there is a connection, Tango-PCB determines the nearest endpoint for the connection and checks if the endpoint is a surface pad.

Cross-Reference

Section 14.11

lets Verify

Description

Verify that the electrical connections for all displayed routed nets match the connections in the net list. The command verifies each net on a node-by-node basis. If it finds a short (a node that does not belong in the net) or an open (a missing node), the program displays an error. The verification process stops so you can correct the problem.

NOTE: The Nets Verify command verifies all currently displayed nets. Before running this command, you need to run the Nets Display command to display (show) the net(s) that you want to verify.

Cross-Reference

Section 15.2

utput Apertures

Description

Setup the aperture wheel and tool descriptions and then map the aperture and tool settings to items on the PC-board. The first dialog box lets you describe the aperture wheel (for photoplot files) and tools (for N/C drill files). For each aperture wheel position, enter the draft code, the shape, the X and Y dimensions, the hole diameter, and whether the aperture is to be flashed, drawn, or both. You can also enter a brief comment. For each tool, enter the tool number and the hole diameter.

After setting up the aperture wheel and tool descriptions, click on OK to display the Assign Apertures dialog box. In this box, you map the aperture and tool settings to items on the PC-board.

Cross-Reference

Section 17.3, 18.2

Output CAM

Description

Generate a Gerber-format photoplot file or Excellon-compatible N/C drill file for the current PC-board. The first Output CAM dialog box lets you configure the photoplot and N/C drill languages to match your bureau's equipment. In the second dialog box, you can choose from a variety of setup options for the files.

After setting up a file, click on the Add pushbutton to add the file to the CAM File Queue list box. Click on OK to generate the files marked by an asterisk in the CAM File Queue list box. If you select N/C Drill for the board layer/item, Tango-PCB generates an N/C drill file. If you select any other layers or items, the program generates a photoplot file.

Cross-Reference

Section 17.4, 18.4

Output Plot/Print

Description

Plot or print the current PCB file, or generate output files in PostScript or DXF format. You can select a variety of setup options, including: the printer and plotter drivers, communications ports, plotter pen settings and printer colors, scale, X and Y correction, board layer or layers (if printing a composite), output filename (if sending to a file), plot/print quality (final for artwork or draft for check prints), and the X and Y offsets for the plotter pen.

To interrupt plotting/printing, press <RightMouse> or <Esc>. The program then prompts you to continue or cancel the Output Plot/Print command.

Cross-Reference

Section 16.2

Output Reports

Description

Generate a variety of reports for the current PCB file. You can select one or more of the following types of reports: Aperture Information, Bill of Materials, Component Locations, Library Contents, PCB Components, Statistics, and Design Rule Check. At your request, the program sends the report(s) to a printer or file.

Click on OK to print the specified report(s). Click on Cancel to cancel the Output Reports command.

Cross-Reference

Section 16.6

Place Arc

Description

Place an arc on the current layer. To define the arc, the program prompts you to first position the cursor at the desired center point of the arc and press <LeftMouse> or <Enter>. The program draws a circle and radius at this point. Move the cursor to expand the circle to the desired radius of the arc. You can also move the line that indicates the radius to the start of the desired arc, called the start angle. (The start angle is measured counter-clockwise from 3 o'clock on the circle.) Press <LeftMouse> or <Enter> again to fix the radius and start angle. The program redraws the circle, this time displaying an outline of the arc's line width.

Move the cursor now to define the sweep of the arc, which is displayed dynamically on the screen.

Cross-Reference

Section 10.3.1

Place Block Copy

Description

Copy all items contained entirely within a block. Tango-PCB prompts you to first define the block by pressing <LeftMouse> or <Enter> to mark two diagonally opposite corners of a rectangular area. The program highlights the defined block.

After you select the reference point, use the mouse or arrow keys to move an outline of the block across the screen. Press R to rotate the block 90 degrees around the reference point. Each time you press <LeftMouse> or <Enter>, Tango-PCB places a copy of the block at the current cursor position. Press <RightMouse> or <Esc> to terminate the Place Block Copy command.

Cross-Reference

Section 13.3

Place Component

Description

Place a component pattern. Select the pattern from the specified library and enter its reference designator, type, and value (for example, U14, 0.25W RES, 4.7K). Press R to rotate the outline 90 degrees. Press F to flip (mirror) the pattern (which is useful for surface-mount designs). To fix the pattern in its current location and orientation, press <LeftMouse> or <Enter>.

Cross-Reference

Section 11.3

Place Designator

Description

Assign pin designators to a set of pads or reference designators to a set of components. When assigning pin designators, the Place Designator command is generally used after placing all the primitives in a new component pattern and before running the Library Add command to add the new pattern to the current library. When placing reference designators, run the Place Designator command after placing the component(s) on the board.

To assign pin/reference designators, first press <LeftMouse> or <Enter> to display the Place Designator dialog box. Select the Designator type (pin or reference designator). For the designator template, enter up to 15 alphanumeric characters and at least one # (number sign). When you assign pin/reference designators, these # symbols will be replaced by a value determined by the initial value and the increment.

After entering the dialog box values, click on OK. The program prompts you to click on the desired pad (for pin designators) or component (for reference designators).

Cross-Reference

Section 11.5.1, 12.4

Place Fill

Description

Place an area fill (a rectangular region of copper) on the current layer. Tango-PCB prompts you to press <LeftMouse> or <Enter> to mark two diagonally opposite corners of the area fill. The area fill is displayed as a solid rectangle. Press <RightMouse> or <Esc> to cancel the Place Fill command.

Cross-Reference

See Section 10.4.1

Place Pad

Description

Place a pad of the current pad type on the workspace. The current pad type, which is shown on the prompt line, is defined using the Current Pad command or by selecting a pad entry from one of the custom Place Palettes.

To place a pad, first press <LeftMouse> or <Enter> to display an outline of the current pad type at the cursor location. The pad outline moves with the cursor. Type R to rotate the pad 90 degrees. To fix the pad in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place Pad command.

Cross-Reference

Section 8.2.2

Place String

Description

Place a string of the current string type on the workspace. The current string type is defined using the Current String command or by selecting a string entry from one of the custom Place Palettes.

Press R to rotate the string 90 degrees counter-clockwise. Press X or Y to flip (mirror) the string along its X or Y axis (which is useful for surface-mount designs). To fix the string in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place String command.

Cross-Reference

Section 10.2.2

Place Track

Description

Place one or more tracks of the current track width on the workspace. The current track width is defined using the Current Track command or by selecting a track entry from one of the custom Place Palette.

To place a track, first press <LeftMouse> or <Enter> to fix a "pivot" point at the current cursor location. As you move the cursor, the program draws a rubberbanding line from the pivot to the cursor (see the section **Setting The Orthogonal Mode** in Chapter 9 for details). Press <LeftMouse> or <Enter> to place the track. You can continue to place tracks, each one starting at the endpoint of the previous track. Press <RightMouse> or <Esc> to terminate the Place Track command.

Cross-Reference

Section 9.3

Place Via

Description

Place a via of the current via type on the workspace. The current via type, which is shown on the prompt line, is defined using the Current Via command or by selecting a via entry from one of the custom Place Palettes.

To place a via, first press <LeftMouse> or <Enter> to display an outline of the current via type at the cursor location. The via outline moves with the cursor. To fix the via in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place Via command.

Cross-Reference

Section 8.3.2

Setup Communications

Description

Configure the serial communications ports (COM1 and COM2) for printing and plotting. You can select the **baud rate** (in the range of 300 through 9600), **parity** (None, Even, or Odd), number of **data bits** (7 Bits or 8 Bits), number of **stop bits** (1 Bit or 2 Bits), and the **handshake** protocol (Hardwire or XON/XOFF)

The serial port settings will be in effect for all subsequent output operations. When you exit Tango-PCB, these settings are automatically saved in the file PCB.INI and loaded the next time you start the program. You only have to change the settings if you change plotters or printers.

Cross-Reference

Section 16.3

Setup DRC

Description

Setup the design rule check (DRC) parameters, in preparation of generating a DRC report (using the Output Reports command). You can enter the minimum Pad-to-Pad, Pad-to-Track, and Track-to-Track clearances allowed on each of the six signal layers.

You can also specify which conditions are to be checked for. Once the parameters for the DRC are established with Setup DRC, run the Output Reports command and enable the Design Rule Check report.

You do not have to have a net list loaded to produce a DRC report. However, without a net list loaded, the DRC report will not contain any Net List Violations, since there is not a net list for comparison to the board.

Cross-Reference

Section 15.3.1

Setup Display

Description

Enable and disable the display of individual PC-board layers and items (including through pads and vias); turn the visible grid on or off; and, select the cursor shape (arrow, small cross, or large cross).

In the Setup Display dialog box there is a small box of color next to each layer field. This box shows the display color for the layer. If the color box is solid, the layer is enabled. To change a color for a field, click the mouse on the field name.

Cross-Reference

Section 7.14, 7.15

Setup Grids

Description

Set the size for the three workspace grids (absolute, relative, and visible) and set the snap grid to absolute (the default) or relative. As an alternative to the Setup Grids command, you can also set the snap grid by clicking the mouse on the status line's Grid field or by typing G.

You can only move the cursor to a point on the snap grid. When the snap grid is set to absolute, the X,Y coordinates are displayed in parentheses on the status line with the origin (0,0) at the lower-left corner of the workspace. When the snap grid is set to relative, the program prompts you to select the relative grid origin by positioning the cursor and pressing <LeftMouse> or <Enter>.

The visible grid is for reference only.

Cross-Reference

ion 5.8.2

Setup Options

Description

Enable or disable a variety of Tango-PCB options, including Orthogonal modes and Drag Signal Tracks options.

The Orthogonal modes determine the mode for placing tracks on the board. With the Orthogonal modes, you can only place tracks that are horizontal, vertical, or at 45-degree angles. These modes are in effect for the Place Tracks, Move Reroute, and Nets Route commands.

You can also specify whether or not signal tracks are to be dragged (rubberbanded) with the Move Block, Move Component, or Move Track commands.

Cross-Reference

Section 9.5, 11.6, 13.2

Setup Palette

Description

Set up the custom Place Palettes. Tango-PCB provides up to five custom Place Palettes, labeled PLACE1 through PLACE5. You can add pad, string, track, and via information to these palettes. This allows you to have a number of item types, such as pad sizes and track widths, at your fingertips for quick placement.

The number of custom Place Palettes is determined by the number of items you add to the palettes. Each palette is one line in size. If you add more items than will fit on one line, Tango-PCB automatically creates another custom Place Palette.

Cross-Reference

Section 10.2

Undo

Description

Undo the previous editing command. The Undo command restores the PCB to its status prior to the last Delete, Edit, File Load (loading a block only), Move, Nets Route, or Place command. You can only undo the last command. The Undo command makes it easy to change your mind or to recover from a mistake.

You can also undo the previous editing command by clicking the mouse on the Undo hot spot or typing U.

Cross-Reference

Section 5.6

Zoom All

Description

Display the entire 32-inch by 32-inch workspace.

Cross-Reference

Section 6.6.1

Zoom Board

Description

Display the entire PC-board. The zoom level is adjusted so that the PC-board fills the screen. The program displays only the enabled layers of the board.

Cross-Reference

Section 6.6.2

Zoom Center

Description

Re-center the display. The program first displays a rectangular zoom window that indicates the screen area at the current zoom level. This window is the same size as the screen. By moving the cursor, the borders of the window can be moved off the screen, letting you zoom sections of the workspace that aren't currently displayed.

You can initiate a quick Zoom Center at any time by simply pressing the "C" key on your keyboard. This is especially handy for panning quickly across the board.

This command is useful if you want to display a section of the workspace that is currently off-screen. Press <RightMouse> or <Esc> to cancel the Zoom Center command.

Cross-Reference

Section 6.6.3

Zoom In

Description

Zoom in on the display. The program first displays a rectangular zoom window that indicates the screen area at the next highest zoom level. Move the cursor to re-position the window. The borders of the window can be moved off the screen, letting you zoom in on sections of the workspace that aren't currently displayed.

This command is useful if you want to view a section of the workspace in greater detail. Press <RightMouse> or <Esc> to cancel the Zoom In command.

Cross-Reference

Section 6.6.4

Zoom Out

Description

Zoom out on the display. The program prompts you to position the cursor on the desired center of the display, then press <LeftMouse> or <Enter>. The screen is re-drawn at a lower zoom level with the cursor at the center of the screen. This is useful if you want to view a wider area of the workspace (though in less detail than previously displayed). Press <RightMouse> or <Esc> to cancel the Zoom Out command.

Cross-Reference

Section 6.6.5

Zoom Redraw

Description

Re-draw the display at the current center position and zoom level. This is useful if extensive editing (including deletions and moves) has left gaps in the display.

Cross-Reference

Section 6.6.6

Zoom Window

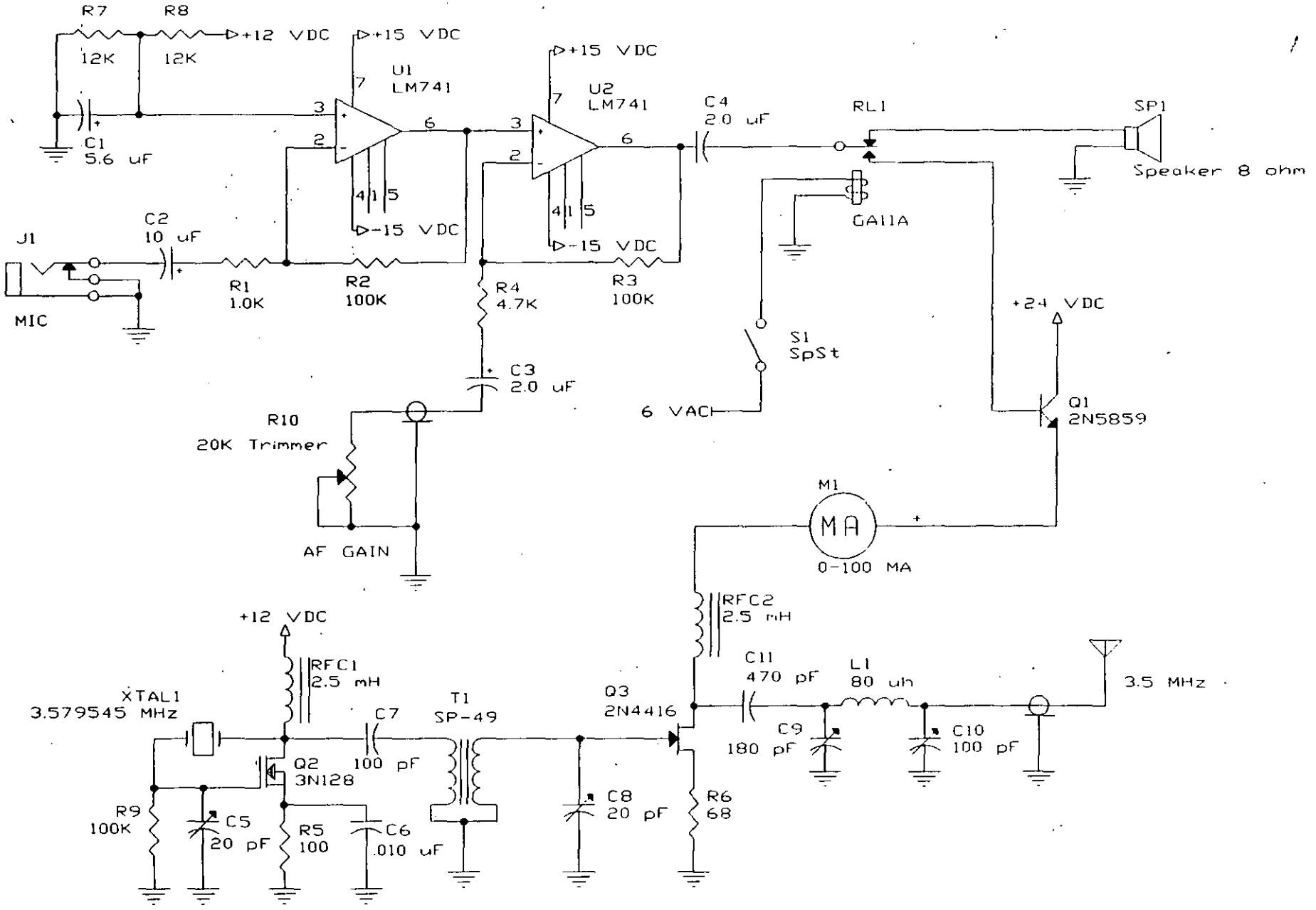
Description

Zoom in or out on a specified section of the workspace. The program first displays a rectangular zoom window that indicates the screen area at the highest zoom level. To mark the center of the zoom window, position the cursor and press <LeftMouse> or <Enter>. The program displays an X at this spot. To display the section of the workspace inside the window at the highest zoom level, again press <LeftMouse> or <Enter> without moving the cursor.

If you want to display a larger area of the workspace, you can expand the window by moving the cursor up or to the right. Contract the window by moving the cursor down or to the left. The borders of the window can be moved off the screen, letting you zoom sections of the workspace that aren't currently displayed. When the window is the desired size, again press <LeftMouse> or <Enter>. The section of the workspace inside the window is redrawn to fill the screen.

Cross-Reference

Section 6.6.7



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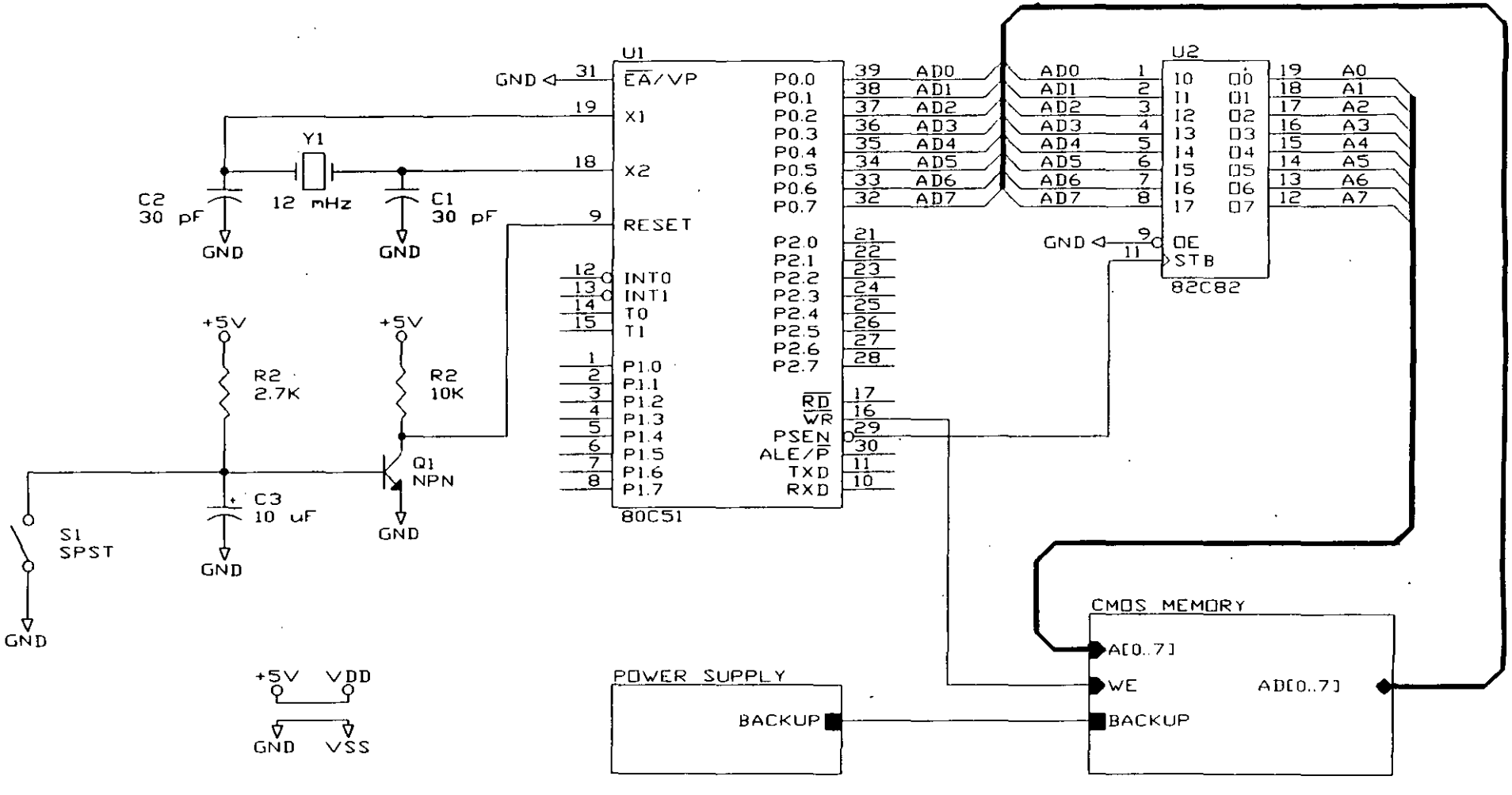
Item	Quantity	Reference	Part
1	1	BOS	1
2	1	C1	5.6 uF
3	1	C2	10 uF
4	2	C3,C4	2.0 uF
5	2	C5,C8	20 pF
6	1	C6	.010 uF
7	2	C7,C10	100 pF
8	1	C9	180 pF
9	1	C11	470 pF
10	1	J1	MIC
11	1	L1	80 uh
12	1	M1	0-100 MA
13	1	Q1	2N5859
14	1	Q2	3N128
15	1	Q3	2N4416
16	1	R1	1.0K
17	3	R2,R3,R9	100K
18	1	R4	4.7K
19	1	R5	100
20	1	R6	68
21	2	R7,R8	12K
22	1	R10	20K Trimmer
23	2	RFC1,RFC2	2.5 mH
24	1	RL1	GA11A
25	1	S1	SpSt
26	1	SP1	Speaker 8 ohm
27	1	T1	SP-49

Item	Quantity	Reference	Part
28	2	U1,U2	LM741
29	1	XTAL1	3.579545 MHz



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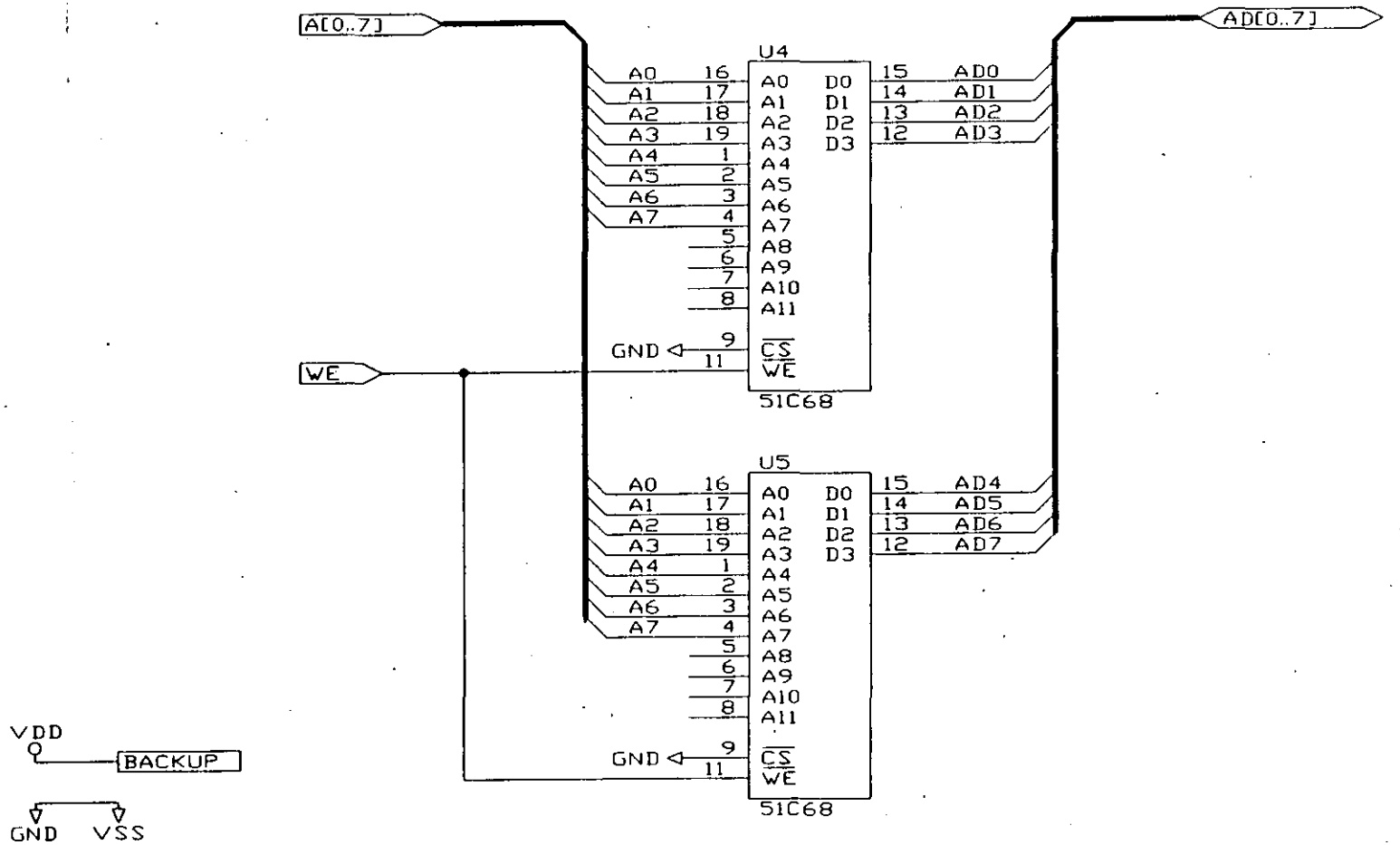

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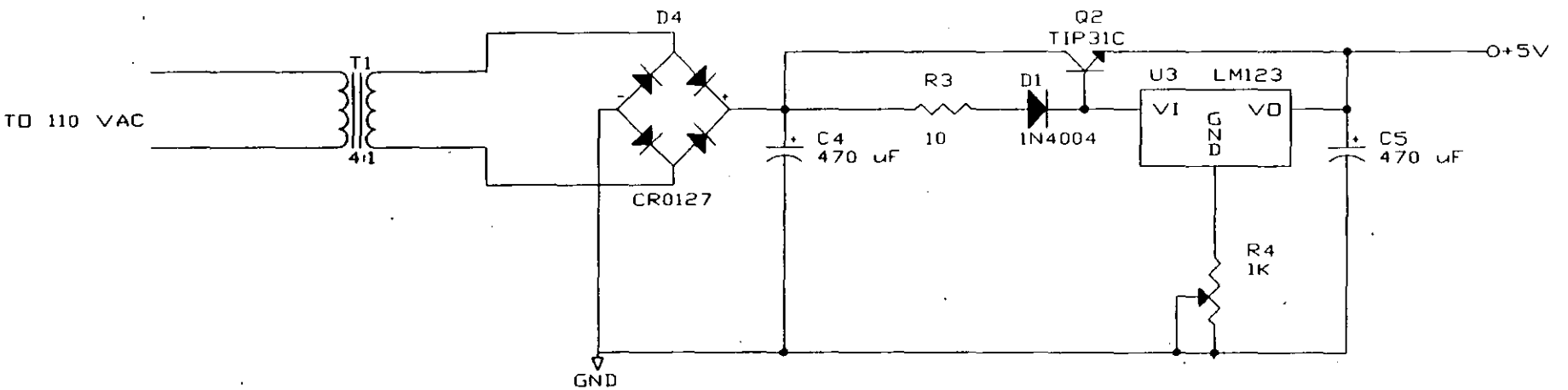
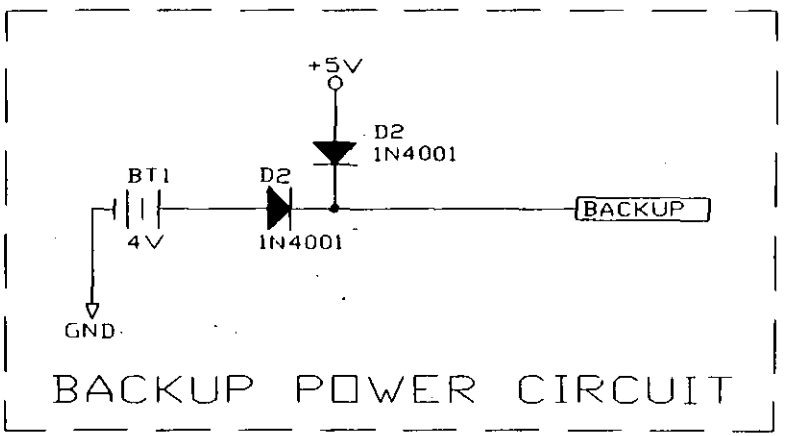




BACKUP POWER CIRCUIT

4.12 Net List Operations

Whether you've drawn your electronic circuit in a sophisticated schematic capture system or on the back of an envelope, generating a net list will help with your PCB design. The benefits include faster layout, because Tango-PCB PLUS displays nets and their nodes for easy routing, and higher quality, and because Tango's Nets Verify command and integrated design rule checker conduct electrical connectivity as well as clearance gap checks to ensure the integrity of the design.

For the uninitiated, a net list is simply a list of all components and connections in the circuit. Tango-PCB PLUS supports a simple, ASCII net list format which may be generated by hand with a text editor or by popular schematic capture systems including Tango-Schematic, OrCAD/SDT, and Schema. We're adding support for additional programs, so call us if you wish to check on another.

As noted above, an important distinction between Tango and other net-list-based PCB design software is that while Tango-PCB PLUS *supports* net lists, it does not *require* them. This means you can load a net list and take advantage of several productivity enhancing features in the program, while you are still free to make or break any connection at any time without updating the net list information.

Besides speeding up board design in Tango-PCB PLUS, the net list also feeds component and connection information to our powerful autorouter, Tango-Route PLUS. If you don't have a net list, you can still use the powerful *what-you-see-is-what-you-get* editing capability of Tango-PCB PLUS to lay out your circuit by hand.

In the next few pages, we'll load a net list, display a *rat's nest* and *force vectors*, then display, route, and verify individual nets.

The net list is loaded after all components have been placed on the board. Since we know your time is valuable, we have supplied a PCB file with 100+ components already placed. Pop-up the menus to run the File Load command. Key in, or select from the list box, DEMO1.PCB and click on OK. Tango prompts you to save the changes to our current board. Let's leave IBMCARD.PCB as-is. Click on No Save.

4.13 Loading A Net List

Next, pop-up the menus again and run the Nets Load command. The Tango-PCB PLUS package includes an associated net list called DEMO1.NET. In the Nets Load dialog box, either key in the name DEMO1.NET or select it from the list box. Click on OK to load the net list. After a few moments, Tango will prompt you for the names of the nets to be assigned to power and ground planes, if so desired. Key in, or select from the list box, VCC for the Power Plane Net and GND for the Ground Plane Net. For the Plane Connection, select Thermal and click on OK.

Tango-PCB PLUS redraws the screen with all point-to-point connections in the net list displayed on a special Connections layer. This representation is appropriately called the *rat's nest* (Figure 4-13). The rat's nest, along with force vectors to be discussed below, provide a visual cue as to the quality of our parts placement.

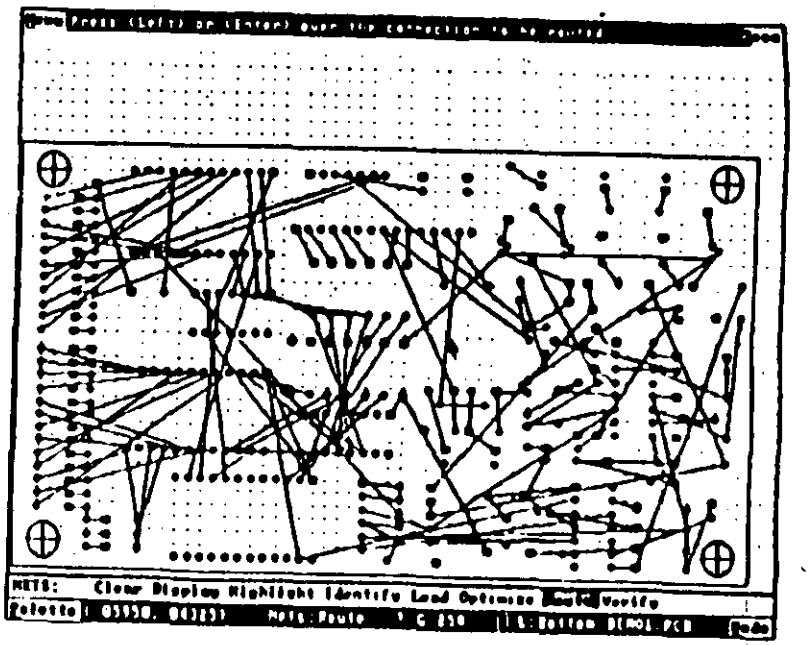


Figure 4-13. The rat's nest is displayed on a special Connections layer.

4.14 Optimizing Nets

Whether you intend to manually route the design or use Tango-Route to autoroute the board, optimal component placement is crucial to your success. Tango-PCB PLUS include three powerful features to aid in component optimization: the Nets Optimize and Move Component commands, and force vectors.

When you first loaded the net list, Tango-PCB PLUS connected all the nodes in the order they were connected in the schematic, which may not make any sense on the PCB. Therefore, it almost always pays to first run the Nets Optimize command, which re-connects the nets using a shortest distance, X-bias, or Y-bias strategy. Run the command now, either selecting it from the menus or from the Nets Speed Palette. Choose the Minimize Total Length option and click on OK.

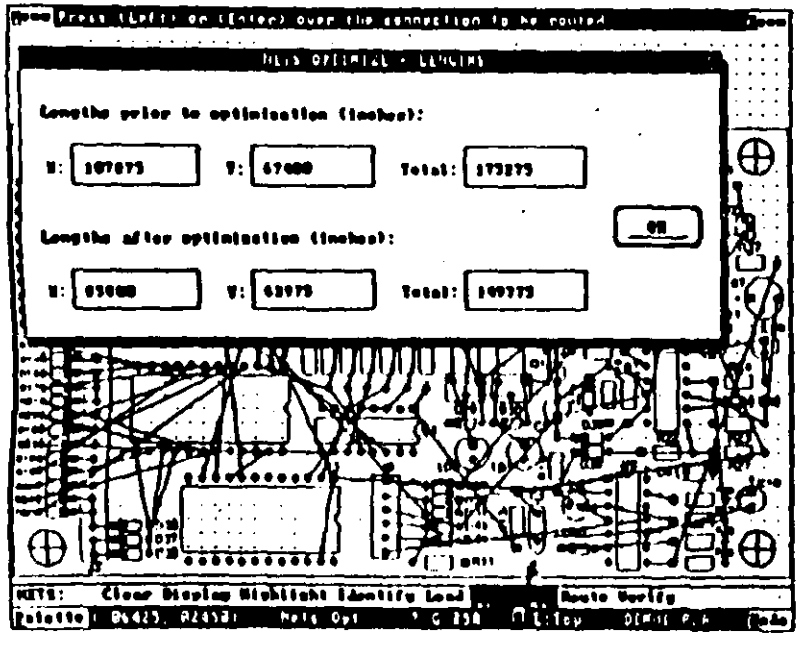


Figure 4-14. Use the Nets Optimize command to help clean up the rat's nest.

Tango-PCB PLUS takes a few moments to recalculate all connections and, prior to redrawing the new rat's nest, displays the reduction in connection inches. In this case, the length prior to optimization is 175.275 inches and the length after optimization is 149.775 inches (Figure 4-14). Click on OK to view the rat's nest.

With the nets now optimized, you get a visual cue to the effectiveness of your initial component placement. Parts which might be better placed are identified by long connections flung to disparate locations on the board. The Move Component command provides an effective tool for highlighting and moving components and their connections.

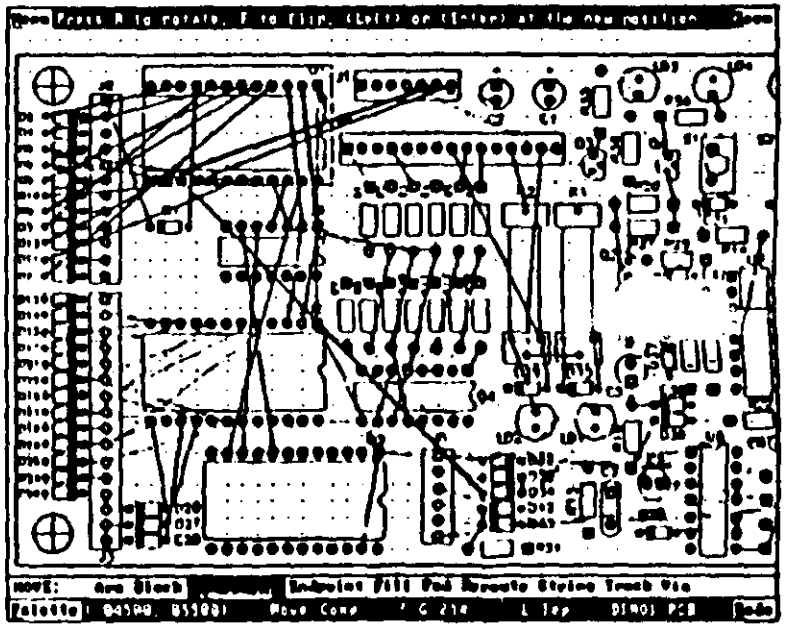


Figure 4-15. When you run the Move Components command, Tango-PCB PLUS highlights and dynamically rubberbands connections to the component.

Change to Move Component mode now by selecting the command from the menus or the Move Speed Palette. Place the cursor over an IC, U1, (located at 4500,5500 in the top left portion of the board), and press <LeftMouse> or <Enter>. The component and its connections are highlighted for easy viewing. Move the part in any direction, flip or rotate it, and its connections are dynamically rubberbanded (Figure 4-15). As it turns out, this component is fairly well place press

<RightMouse> or <Esc> to cancel the operation and return the part to its original position.

Now place the cursor over the diode D1, (located at 3400,4600, just below U1), and press <LeftMouse> or <Enter>. Both connections to this component lead to the top of the board, indicating it should be moved up. Practice rubberbanding other components with Move Component.

While the rat's nest and Move Component operations help you visually see the density of connections on the board, they can become overwhelming on boards of average or greater complexity. A cleaner, easier way to see what's going on is to use Tango's force vector display. Force vectors are arrows emanating from each component which represent the weighted average of all connections to that component. They give an indication of where the component should be moved to reduce the connection length to that component.

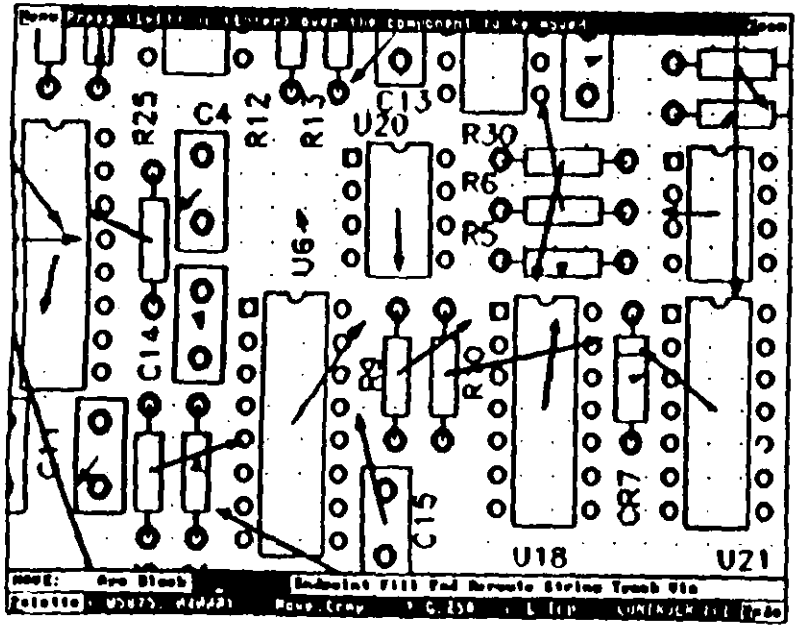


Figure 4-16. Force vectors aid component placement.

To display force vectors, enable their display in the Nets Display dialog box. Generally, you will want to hide all connections (the rat's nest) during the display of force vectors.

If you move a component, its force vector is updated as it is moved; once you place the component, the force vectors for all components connected to the component just moved are also updated.

Another handy feature for getting a feel for the overall effect of each component move is to toggle Undo several times (just press U or click on the Undo hot spot), before accepting the move or trying again.

Good component placement is still more of an art than a science, but Tango's placement tools augment your own judgment and experience to make the job go faster.

4.15 Routing Nets

Assume now that the component placement is optimal. The next step is to begin routing actual traces on the board. If you were a Tango-Route owner, at this point you would simply save the design to a PCB file and load the board and its net list into Tango-Route for autorouting. Should Tango-Route not complete 100% of the connections, you would come back to Tango-PCB PLUS for manual routing of the remaining connections, which are displayed in rat's nest fashion on the Connections layer.

Without the aid of Tango-Route, you are faced with the task of manually routing traces in Tango-PCB PLUS. But keep your chin up, because Tango's powerful editing tools again come through to make this task easier. With the net list loaded, you can use the Nets Display command to display individual connections for easy manual routing.

Selecting a connection to work on can be a difficult task with the entire rat's nest displayed, even on smaller boards. Average designs can easily contain hundreds of nets, making the ability to selectively display a subset of them an important feature.

To selectively display individual nets, we'll use the Nets Display command. Since you are going to use several of the Nets commands in

the component pins of all nodes in a particular net (the Nets Highlight command).

4.16 Verifying Nets

Since you're free to make or break any connection in any net, you should verify that all connections have been made properly. You can wait and perform a board-wide check at the end of the design with Tango-PCB PLUS' integrated design rule checker. Or better yet, verify on a net-by-net basis during the layout process, *and* run Tango's DRC at the end for a final measure of confidence.

To verify the net we just completed (RESET), run the Nets Verify command. This command performs an electrical design rule check on all nets currently displayed using the Nets Display command. Since RESET, and only RESET, is displayed, its connections as shown on the screen will be checked against the net list. Any incorrectly connected or missing pins will be flagged with an error message which is displayed on the screen. You have the option of continuing the verification process or stopping to fix the problem.

If there were other nets on the board displayed with Nets Display, they too would undergo the net list verification. Late in the design, you may find it necessary to break connections, which were previously completed and verified, to make room for a subsequent trace. Even though you diligently re-connected the broken nets, a final and complete DRC can greatly enhance your peace of mind.

4.17 Checking the Entire Design

The Nets Verify command is designed to be used interactively during layout and manual routing. Its verification is limited to making sure the connectivity of a routed net matches that in the net list.

Complementing Nets Verify is Tango's integrated design rule checker. The DRC operates on a board-wide basis, verifying both electrical connectivity and clearance gaps which you specify as design rules.

Running the design rule checker on your board is a two step process. First you run the Setup DRC command to establish the clearance gaps for pad-to-pad, pad-to-track and track-to-track checking on a per-layer basis. You also select the contents of the design rule check report, which may include: clearance violations, string violations, net list violations, single node routes and unconnected pins.

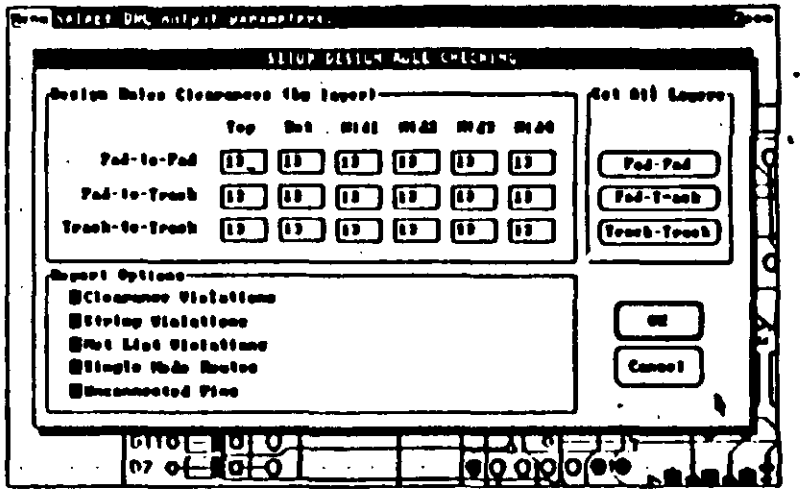


Figure 4-19. The Setup DRC dialog box.

Once the DRC options are set with the Setup DRC command, run the Output Reports command and enable the Design Rule Check report. You may print the report or write it out to a file on disk.

When you click on OK, the program will begin the design rule checking process, highlighting each connection as it is verified. When completed, the DRC report will print out or be written to a file.

The DRC is compute-intensive and can take a while on complex designs, though it is many times faster and much more accurate than checking a board by hand.

You don't have to have a net list loaded to produce a DRC report. In this case, however, the DRC will be limited to a check of clearance violations and string violations based on the rules you establish with the Setup DRC command.

4.18 Nets In A Nutshell

And so, to summarize, Tango-PCB PLUS includes powerful net list operations which allow you to display all nets (the *rat's nest*), individual nets, pins in a net, or all connections to a given component. You can also display *force vectors* to aid with placement. You are not required to maintain the validity of the net list during editing. Instead, you can verify the validity of your connections after drawing them.

The process of designing a board in Tango-PCB PLUS with the use of a net list follows these easy steps:

- Place the components on the board using the same reference designators (U1, U2, etc.) as in the net list.
- Load the net list, display all nets, and use the rat's nest or force vectors and the Nets Optimize and Move Component commands to optimize parts placement.
- Use Nets Display to display a single net.
- Use Nets Route to route each connection in the net.
- Use Nets Verify to check all connections in the net against the net list.
- Repeat the last three steps (display a net, route its connections, verify the net) until the board is completed.
- Run the Design Rule Check report on the entire design.

4.19 Output Options In Tango-PCB PLUS

It should be obvious by now that we're very proud of the ease-of-use and powerful editing features of Tango. There is no question that displaying a dense design on a 19-inch monitor running 1024 x 768 resolution is the sexy part of the CAD business. However, we've designed and built boards ourselves and we know that the most important function a PCB layout program must do is create crisp, accurate output for board production.

In Tango, we paid particular attention to generating the highest quality output, available on devices ranging from dot-matrix printers to Gerber-format photoplotters. We use our menus, dialog boxes, prompts and on-line help to take the mystery and frustration out of generating artwork, photoplot files, and even proper communications with pen plotters.

Let's review the output options included as standard features in Tango-PCB PLUS. Select the Output command from Tango's Main Menu. The Output Menu commands make it easy to:

- Setup photoplot aperture assignments.
- Create photoplot and N/C drill files.
- Pen plot multi-color check plots or final artwork at any scale.
- Generate check prints or even prototype-quality final artwork on your dot matrix or laser printer.
- Generate DXF and PostScript files for use with compatible mechanical CAD, desktop publishing and word processing software. You can even get high-quality, inexpensive final artwork on PostScript-compatible phototypesetters.
- Generate a selection of printed reports, ranging from the Bill of Materials to aperture assignments.

4.20 Printing And Plotting

We encourage you to take the time to print or plot a Tango file and see both our speed and quality of output. We've included the RDEMO1.PCB with your Tango-PCB PLUS package, which ma[illegible] plotted or printed.

Run the File Load command to load RDEMO1.PCB. Again, the program asks if you wish to save the changes to the current PCB file. Click on No Save.

NOTE

If you use a serial port for either printer or plotter, you must run the Setup Communications command to set options for baud rate, data bits, stop bits, parity, and handshake before running the Output Plot/Print command. Consult your printer or plotter manual for the proper settings. You do not need to run Setup Communications if your output device is connected to your computer by a parallel port.

Now run the Output Plot/Print command. The first dialog box which appears allows you to select which layers of the board you wish to print or plot (Figure 4-20). Other options toggled with this dialog box include single or multi-color artwork, draft or final artwork quality, mirror image, holes in pads and vias, and component reference designators and types.

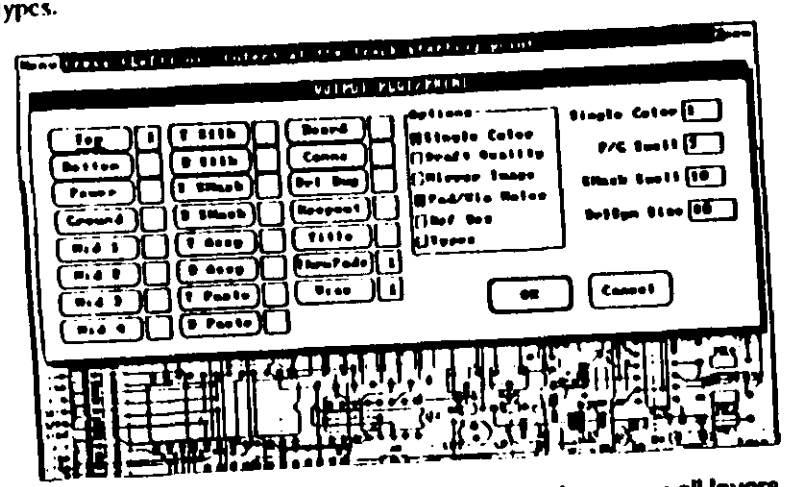


Figure 4-20. Produce draft or final artwork for any or all layers of your board.

You also use this dialog box to specify the pen number for single color plots, Power/Ground plane swell, Solder Mask swell and drill symbol size. All of these options are stored automatically for you in the initialization file PCB.INI to save you the trouble of resetting them each design session.

Choose the layer(s) of RDEMO1 you would like to print or plot, any other options which seem appropriate, and click OK.

A second dialog box appears which presents two list boxes, one for printer and plotter drivers, and one for output ports. First select from the list box the appropriate printer/plotter driver for the device you want to use (Figure 4-21). Consult your printer or plotter manual if you are unsure of its default driver. If your device is not displayed in the list box, check for a compatible driver. For instance, most plotters are either HP-GL or DM-PL compatible, and many printers are Epson FX compatible. The numerals beside the printer drivers indicate their resolution (in dots per inch).

The drivers used to generate DXF, PostScript and Encapsulated PostScript files are also selected from the driver list box.

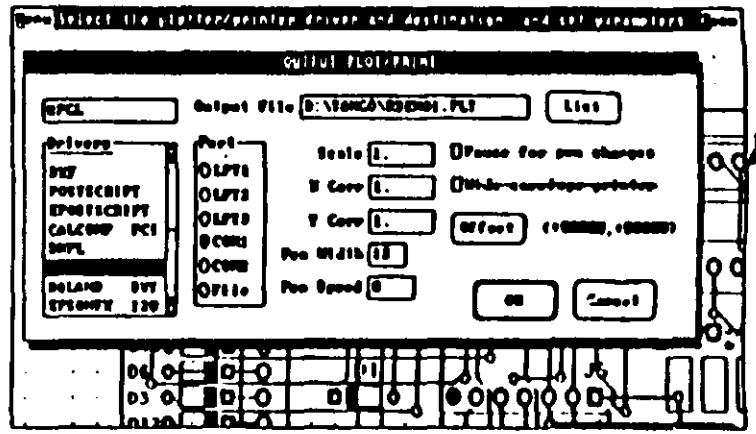


Figure 4-21. Tango supports a wide variety of printers and plotters, with more being added all the time.

Next click on the printer or plotter port you're going to use to output from your computer to the device. Other options which may be set with this dialog box include plotting or printing to a file, setting the artwork scale, X and Y correction values, pen width and speed, pause for pen changes, wide (15-inch) carriage printers, and offset dimensions. Again, any settings you make will be saved in PCB.INI.

After selecting your device driver and port, choose any other options which suit your fancy and click on OK. The program will begin to generate your artwork.

On narrow printers, dot matrix or laser, Tango-PCB PLUS will automatically print any artwork which is too wide for the printer in strips which may be taped together. If you wish to print or plot the artwork rotated 90 degrees, or mirrored, just click on those options in the Output Plot/Print dialog box.

Try experimenting by generating plots or prints for alternate layers, varying scale, draft and final artwork, assembly and drill drawings, and so on. We think you'll agree, Tango generates beautiful art, worthy of your best designs.

4.21 Viewing Photoplot Files

We have one more important feature of Tango-PCB PLUS that we would like to show off before we let you go out on your own. Maybe you have heard from friends or even experienced first-hand the problems which can sometimes arise when photoplotting your artwork. Tango-PCB PLUS takes a very logical approach to creating photoplot files from your design, but even still, a file on-disk is an invisible thing. Mistakes that may have been made along the way will not show up until your service bureau delivers your photoplots, which can be an expensive experience.

This is why we have built into Tango-PCB PLUS a photoplot file viewer. You can load in a photoplot file created with Tango and it will be displayed on-screen exactly as it will be photoplotted. Use all of Tango's zoom and pan functions to inspect the file, even print or plot out a copy for documentation and verification.

If you detect a problem, simply load the original PCB file, correct the error, generate a new photoplot file and load it for viewing. It's all done seamlessly in one integrated program.

Since you may not have yet learned how to generate a photoplot file, we have supplied one to help get you acquainted with the viewer. Run the File Load command and click on the Photoplot pushbutton. Now key in

VGADEMO.TOP in the file name entry box. When you click OK, Tango-PCB PLUS will load the photoplot file, which is the top layer of the VGADEMO printed circuit board design.

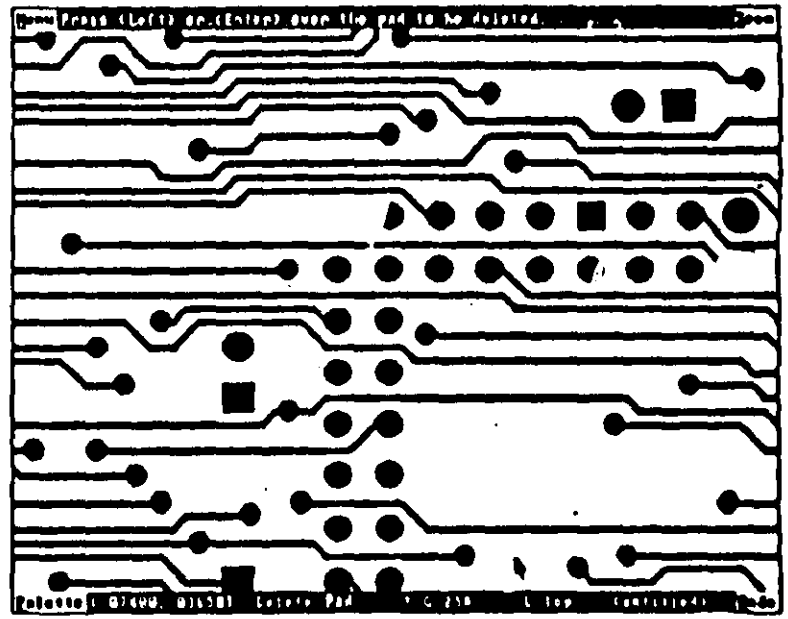


Figure 4-22. Viewing a photoplot file within Tango-PCB PLUS.

4.22 Summary

By now you should have a pretty good feel for what Tango-PCB PLUS is all about. We've tried to cover as many features as possible, and still not consume the better part of a day.

In review, you quickly learned how to operate the ACCEL Productivity Interface, with its pop-up menus, dialog boxes, hot spots, Speed Palettes, and on-line help. You placed components and text, manually routed connections, deleted a component, and used the Undo command to un-delete the component. You loaded a net list and used the rat's nest, net list optimizer, move component and force vectors functions to optimize parts placement. Then you displayed, routed, and verified

connections with net list support. Finally, you output final and/or draft artwork to your printer or plotter and viewed a photoplot file.

But no PCB design system worth its stuff can be adequately described in a 35-page tutorial. Here's a partial list of the dozens of features we haven't discussed. You can find out more about these features by reading the rest of the manual or by using Tango's extensive on-line help:

- **Block operations.** Besides saving and loading blocks, you can delete inside or outside blocks, and rotate, copy, and move blocks.
- **Global editing.** The Edit commands make it easy to change the characteristics of arcs, components, pads, strings, tracks, and vias on the board. You can edit any particular item or all matching items.
- **Move operations.** Moving previously placed tracks is facilitated by three commands: Move Track, Move Endpoint, and Move Reroute.
- **Jump commands.** These commands allow you to quickly locate and move to components, locations, nets, and strings.
- **Orthogonal routing.** When placing or re-routing tracks, type O to toggle between non-orthogonal mode and four different orthogonal routing styles (enabled using Setup Options).
- **Place commands.** Practice placing other elements in the design, such as pads, area fills, and arcs.
- **Nets Highlight.** This handy command will highlight all connected pads, tracks, vias, arcs, and fills, even without a net list loaded.
- **Nets Generate.** Generates a Tango-format net list from the currently loaded board design.
- **Print Reports.** Use Output Reports to print a Bill of Materials and other useful reports.

The Learning Tango-PCB PLUS tutorial introduced the following commands:

Command	Function
Current Layer	Set the current layer for editing
Delete Component	Delete a component on the PC-board
File Load	Load a PCB or block file
Library Browse	Display and list components in a library
Move Component	Move/rotate/flip a component on the PC-board
Nets Display	Select nets to be displayed
Nets Load	Load a net list
Nets Optimize	Create optimized connections for displayed nets
Nets Route	Replace connections with tracks
Nets Verify	Verify that the PC-board matches the net list
Output Plot/Print	Plot or print the current PCB file
Place Component	Place a component on the PC-board
Place String	Place a text string on the PC-board
Place Track	Place a track on the PC-board
Setup Display	Enable/disable and select colors for PC-board layers and items
Setup DRC	Set the design rules and report options for the design rule check report
Setup Grids	Set the absolute, relative, and visible grid sizes
Setup Options	Enable/disable Orthogonal modes and Drag Tracks With Components option
Setup Palette	Add or delete items on the custom Place Palettes
Undo	Undo the previous editing command
Zoom Board	Display the entire PC-board
Zoom Window	Zoom in or out on a section of the display

7 PC-Board Layers

7.1 Introduction

Tango-PCB PLUS provides 19 separate PC-board layers. You can display and print/plot/photoplot individual layers or a composite of two or more layers. You can only edit one layer at a time. The layer to edit is termed the *current layer*.

The program provides the following 19 PC-board layers:

Top
Bottom
Power
Ground
Middle Layer 1
Middle Layer 2
Middle Layer 3
Middle Layer 4
Top Silkscreen
Bottom Silkscreen
Top Solder Mask
Bottom Solder Mask
Top Assembly
Bottom Assembly
Board
Connections
Drill Drawing
Keepout
Title

A majority of the 19 layers -- all signal layers and the Top and Bottom Silkscreen -- are used directly as artwork for fabricating the PC-board. You can place pads, tracks, components, text, vias, arcs, and area fills on any of these layers.

It is the usual and recommended practice to lay out the PC-board as it is seen looking at the components on the board. This way text is displayed on the screen as it will appear on the Top Silkscreen layer (not mirror-imaged). You can think of the layers as stacked on one another with the Top Silkscreen Overlay on top, then the Top layer, the Middle Signal layers and Power/Ground planes, the Bottom layer, and the Bottom Silkscreen layer.

The remaining layers serve as guides for individual steps in the board fabrication process. For example, the Top and Bottom Assembly layers provide instructions for connecting and attaching components to the finished PC-board.

7.2 Top And Bottom Layers

The Top and Bottom layers correspond to the top and bottom sides of the PC-board. Before surface-mount technology, designers called the Top layer the *component side* and the Bottom layer the *solder side*. Though this terminology still holds true for designs that are exclusively through-hole, you can place surface-mount components and solder on *either* side of the board.

7.3 Power And Ground Planes

The Power and Ground Planes are different from the other signal layers in that they consist mostly of copper, with only small sections etched away. For this reason they are plotted in the negative. Connections to the Power and Ground planes are displayed using symbols placed on through hole pads. You cannot edit the Power and Ground planes individually or place items (such as tracks) on these planes.

You can connect component pins to the Power and Ground planes by *tagging* pads. When editing a pad, the program allows you to connect the pad to the Power or Ground plane either directly or through a thermal relief.

7.3.1 What Are Power And Ground Planes?

Tango-PCB PLUS offers true Power and Ground plane capabilities. Circuits using high clock speeds radiate a considerable amount of spurious noise. Power and Ground Planes are necessary to shield sensitive sections of the circuit from this noise. Poor shielding results in high speed flip-flops toggling randomly, leading to erratic circuit behavior. As well, there are now stringent FCC specifications for the amount of radiated energy allowed from electronic equipment. Power and Ground planes, in conjunction with proper equipment shielding techniques, minimize the radiated energy from electronic circuitry.

Some logic families draw a large transient current during state transitions; if the power and ground lines to those devices have a high impedance, large spikes are superimposed on the lines. These spikes often affect other devices down the line, and bypass capacitors can only go so far to alleviate these spikes. Power and Ground planes, in conjunction with bypass capacitors, deliver consistent low-impedance power to all devices on the PC-board.

Just what are the characteristics of Power and Ground planes? Imagine a plane of copper in the middle of your board, with holes in the copper wherever leads pass through the board. The holes are big enough to ensure clearance from the leads, but small enough to provide ample shielding around all closely spaced leads. Now suppose that the plane we are discussing is to be used for the Ground Plane. To connect a lead to the ground rail, fill the hole at that point with copper - the lead will now be in contact with the plane. Thus, the plane has holes in it at every point where a lead is not to be connected to the plane. The Power Plane is similar, with holes at every lead not to be connected to the power rail.

The Power and Ground planes are generally the innermost layers of a PC-board for two reasons. With the PC-board material sandwiched between them, the Power and Ground planes form a bypass capacitor for the supply rails with a low *Effective Series Resistance* (ESR). Recall that capacitance increases as the gap between the plates decreases, so the smaller the gap, the larger the capacitance. The second reason is that by having the planes interior to the signal layers, sensitive signal lines can be isolated from noisy lines by placing them on opposite sides of the planes.

7.3.2 Direct Connections And Thermal Reliefs

A lead is connected to a plane by having no clearance hole in the plane at that point. This provides good conduction between the lead and the entire plane, both electrically and thermally. The first is desirable, the second is not necessarily so good. When the board is soldered, any leads connected directly to a large area of copper will not rise in

temperature as quickly as other leads. This can either cause poor solder joints or require more heat, neither of which is desirable.

The solution is to connect the lead electrically but not thermally to the plane of copper, using a special symbol called a *thermal relief* (Figure 7-1). A thermal relief is a small island of copper around the lead, isolated from the plane by an annular gap. The plane is then connected to the island by four narrow bridges of copper (termed *spokes*). These spokes provide the electrical connection and the gap provides the thermal isolation.

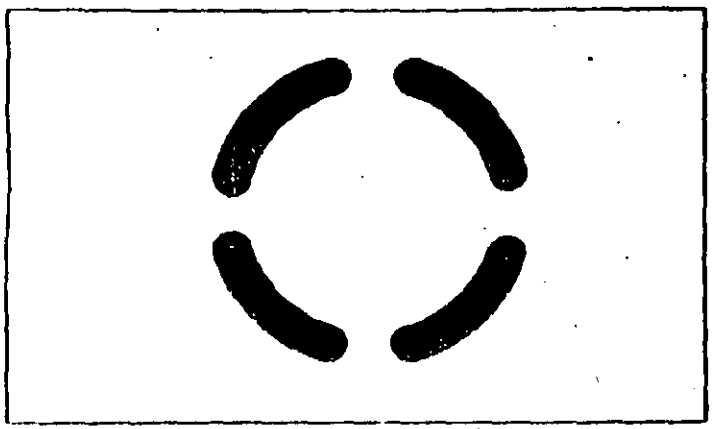


Figure 7-1. A thermal relief connects a component lead to a plane electrically but not thermally.

When running the Edit Pad command, you can tag a pad to the Power or Ground plane by means of either a direct connection or a thermal relief. A small cross (+) in the center of the pad indicates that the pin is connected to the Power or Ground plane with a thermal relief. A direct connection to a plane is indicated by an X in the center of a pad (Figure 7-2).

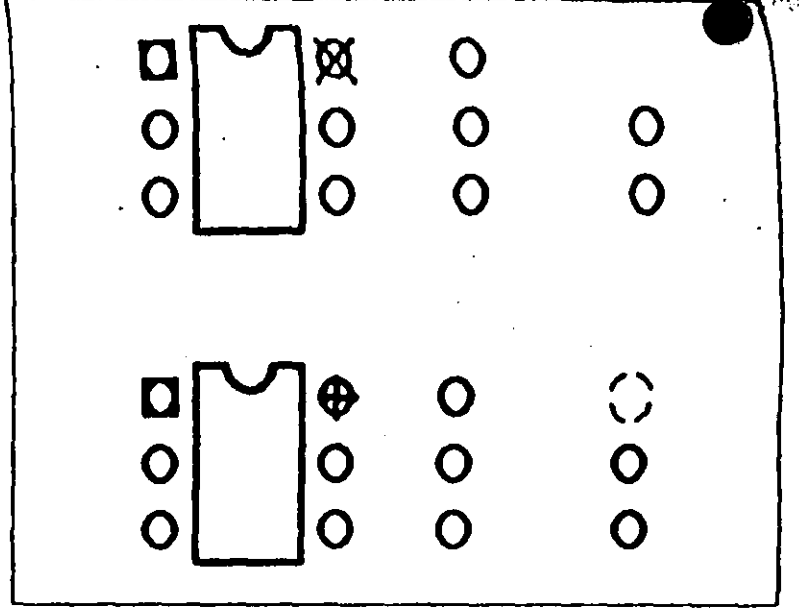


Figure 7-2. A direct connection (X) and thermal relief (+) as they appear on the Tango-PCB PLUS screen (left) and in the final artwork (right).

The small cross and the X let you tell at a glance whether a pad is connected to a plane with a thermal relief or direct connection. But how can you tell whether the pad is connected to the Power or Ground plane? By running the Setup Display command, you can assign separate colors to the Power and Ground planes. A good practice is to use red for the Power plane (red = hot = power) and green for the Ground plane (green often signifies ground connections).

There are three options for connections to the planes: no connection (signified by the pad only and no special symbol), a thermal relief (signified by a cross of the appropriate color in the center of a pad), or a direct connection to the plane (signified by an X of the appropriate color in the center of a pad). The program does not allow you to connect a pad to both planes. This may seem trivial, but it is amazing how many manually taped PC-boards end up with shorted Power and Ground planes!

When the planes are interior to the board, thermal reliefs are generally used. If you are designing a double-sided PC-board and you want a bare copper Ground plane for the Bottom layer (as is often the case for RF designs), then you can use direct connections to the Ground plane.

7.3.3 Connecting Nets To Power And Ground

When loading a net list (using the Nets Load command), you can direct the program to automatically tag all pads that are connected to the Power and Ground planes. In the Select Plane Nets dialog box (Figure 7-3), enter the name of the Power plane net and the name of the Ground plane net. You can also select either direct connections or thermal reliefs.

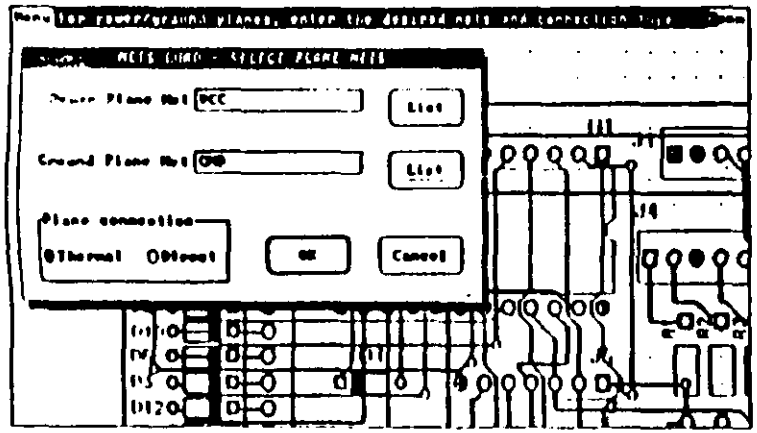


Figure 7-3. Tango-PCB PLUS automatically connects all pads in the specified Power/Ground plane nets to the correct planes.

For example, if your Power plane net has the name VCC, then specifying this net name connects all nodes within the net to the Power plane with either direct connections or thermal reliefs. Specifying the net name GND for the Ground plane net automatically connects all nodes within this net to the Ground plane. (For detailed information on loading net lists, see Chapter 14: Nets.)

7.4 Middle Signal Layers

The four Middle Signal layers are sandwiched between the Top and Bottom layers. You can place any Tango-PCB PLUS item on these layers. The Middle layers are additional signal layers available for multi-layer PC-boards.

7.5 Top And Bottom Silkscreen

The Top and Bottom Silkscreen layers produce the patterns printed on PC-boards that show such information as component outlines, reference designators, and the company name. For through-hole boards, you generally need only a Top Silkscreen layer. For surface-mount designs with components on both sides of the board, you will need both the Top and Bottom Silkscreen.

7.6 Top And Bottom Solder Mask

The Top and Bottom Solder Masks determine where solder mask is applied to the PC-board during fabrication. When the board is soldered, this mask prevents possible shorts by restricting the flow of solder. Tango-PCB PLUS provides Top and Bottom Solder Masks to support surface-mount designs with components on both sides of the board.

The program automatically generates the Top and Bottom Solder Masks from the board design. All pads on the board are *swollen* (enlarged) on the solder mask film to assure that they're kept free of solder mask. In addition, you can place area fills on the Top and Bottom Solder Masks to designate other areas of the board that will not receive solder mask.

For example, it's good practice to place area fills on the Top/Bottom Solder Mask over all edge connectors on the board. Though Tango-PCB PLUS automatically swells the edge connector pads to provide clearance from the solder mask, it's still possible for solder mask to be applied between the fingers of the edge connectors. This can cause problems. Plugging and unplugging the board may wear down the

solder mask, which can eventually interfere with connections to the fingers. By placing area fills on the Top/Bottom Solder Masks, you can assure that solder mask is not applied at all within the area of the edge connector.

Also, many board assembly shops recommend that the area beneath a surface-mount component be kept free of solder mask. If applied, the solder mask could blister during the heat of the soldering process, forcing the surface-mount component upwards and out of contact with the pads. You can prevent the application of solder mask to these board locations by placing area fills on the Top/Bottom Solder Masks under all surface-mount components.

NOTE

Tango-PCB PLUS enlarges all pads on the solder mask film. These pads are swollen when you print/plot/photoplot the board. The pads do not appear swollen on the screen. The area fills you place on the Top and Bottom Solder Masks will not be swollen on the screen or the solder mask film.

7.7 Top And Bottom Assembly

The Top and Bottom Assembly layers can be used, together with the Title layer, to create assembly drawings. These drawings guide the assembly shop during the board assembly procedure. The drawings can include the board dimensions and the locations of the components to be mounted, as well as any special instructions. For example, the drawings could show the location of test points on the board with instructions to keep these sites free of non-conducting conformal coat.

The Assembly drawings can be used together with the bill of materials to define the type of component that is to be mounted at each location. The Bottom Assembly drawing is generally needed only if the board contains surface-mount components on the Bottom layer.

7.8 Board

The Board layer is used to draw an outline of your PC-board. This layer is also useful for indenting the copper on the Power and Ground planes. If the copper extends to the edge of the board on these layers, it could cause a short if the board edge comes into contact with a piece of metal or another board connection.

To indent the Power and Ground planes and prevent shorts, we recommend you draw the board outline with a 100-mil track. If you then print/plot/photoplot the Board layer in composite with the Power and Ground planes, the resulting copper will be indented by 50 mils, half the thickness of the board outline.

7.9 Connections

The Connections layer helps you manually route the PC-board. When you load a net list for your design, all connections in the net list are stored and displayed on the Connections layer. The connections are *point-to-point*: the shortest distance between nodes in a net.

After you manually route a connection in Tango-PCB PLUS (using the Nets Route command), the connection is removed from the Connections layer. If you are editing a board that has been autorouted by Tango-Route, the Connections layer contains only the *no-routes*: connections that could not be autorouted. (For detailed information on net lists and routing, see Chapter 14: Nets.)

7.10 Drill Drawing

The Drill Drawing layer provides the service bureau with the location of every hole on the board and the bit size needed to drill the hole. Tango-PCB PLUS automatically generates a layer that shows every hole on the board. Together with the Title layer, this layer can be used to produce a drill drawing.

Tango-PCB PLUS automatically places a symbol at each hole location which indicates the drill tool required. In addition, you may wish to

place a table on the Drill Drawing which maps symbols to tool numbers/drill sizes.

Depending on your service bureau, a Drill Drawing may not be necessary if the bureau has an N/C drill machine that accepts the standard Excellon-compatible N/C drill file generated by Tango-PCB PLUS. (For more information on the Drill Drawing layer, see **Chapter 16: Prints, Plots, And Reports.**)

7.11 Keepout

The Keepout layer allows you to specify areas of the board where Tango-Route will not place traces. By placing a track segment or area fill on the Keepout layer, you are directing Tango-Route to avoid routing over these locations on all signal layers of the PC-board.

For example, it is good practice not to place vias beneath surface-mount discrete capacitors. During fabrication, solder could force its way up the via and knock the capacitor out of contact with its pads. To make sure Tango-Route does not place vias in these areas, place an area fill on the Keepout layer beneath each surface-mount discrete capacitor.

7.12 Title

The Title layer is used to document your artwork for the board fabrication procedure. This layer should contain such information as the company name, board name, part number, and revision number. The Title layer consists of borders and text strings located outside the outline of the PC-board. You can print or plot the Title layer in composite with the Top and Bottom Assembly and Drill Drawing layers.

The Tango-PCB PLUS package includes Title layer templates for A-size (8.5 x 11 inches), B-size (11 x 17 inches), and C-size (17 x 22 inches) sheets of paper. These templates are stored in the PCB files ASIZE.PCB, BSIZE.PCB, and CSIZE.PCB. You can use these templates or create your own Title layer from scratch.

Each of the Tango-PCB PLUS Title layer templates contain a sheet border and a title block (in the lower-right corner of the sheet (Figure 7-4). The title block provides space for such information as the board's name, identification number, revision number, sheet size, date, filename, and designer.

The Title layer borders are 0.25-inches wide. They are divided into segments which are labeled with numbers across the top and bottom (the columns) and with letters down the left and right sides (the rows). The borders provide a convenient way to locate information on the board. For example, a designer can describe the location of a resistor, R5 as the intersection of row B and column 3.

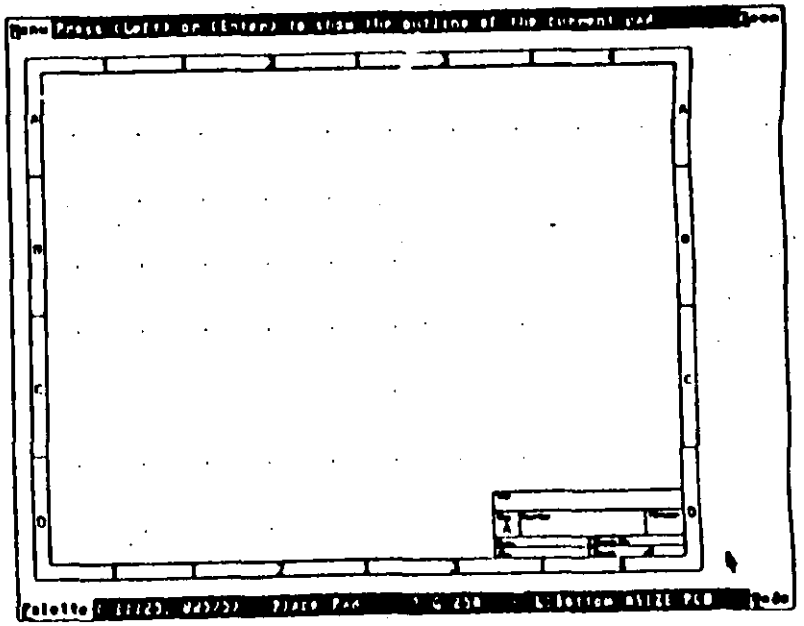


Figure 7-4. The Tango-PCB PLUS Title layer ASIZE.PCB.

7.13 Selecting Layers

The status line's Layer field displays the current layer for placing primitives. All editing takes place on the current layer. Thus, if you

place a track on the PC-board when the current layer is Top, the track is assigned to the Top layer. If you later want to delete this track, the current layer must again be set to Top.

The Layer field also shows the color of the current layer (in the small rectangle to the left of the L). When you place an arc, area fill, surface pad, text string, or track on the PC-board, the primitive is displayed in the color of the current layer. Individual colors can be selected for through-hole pads and vias, since these primitives belong to all layers of the board.

Clicking the mouse on the Layer field or typing L sets the current layer. All subsequent editing is performed on this layer. With each click of the mouse, the program cycles through a list of enabled layers and their colors. You can stop clicking the mouse when the desired layer is displayed. You can also set the current layer by selecting the Current Layer command from the Current Menu. For boards with only a few layers, clicking on the Layer field or typing L may be faster than using the menus.

7.14 Enabling And Disabling Layers

Before you select a current layer, the desired layer must be enabled. You can only edit and display enabled layers. It is useful to disable layers that you do not want to view or edit. Disabling these layers reduces the amount of PC-board information on the screen, allowing you to concentrate on the layer (or layers) that you're currently editing. Since less information is displayed, disabling layers also reduces the time it takes to redraw the screen.

Run the Setup Display command to enable and disable PC-board layers. In the Setup Display dialog box (Figure 7-5) there is a small box of color next to each layer field. This box shows the display color for the layer. If the color box is solid, the layer is enabled. If only the bottom half of the box is colored in (there is a dividing line across the center), the layer is disabled.

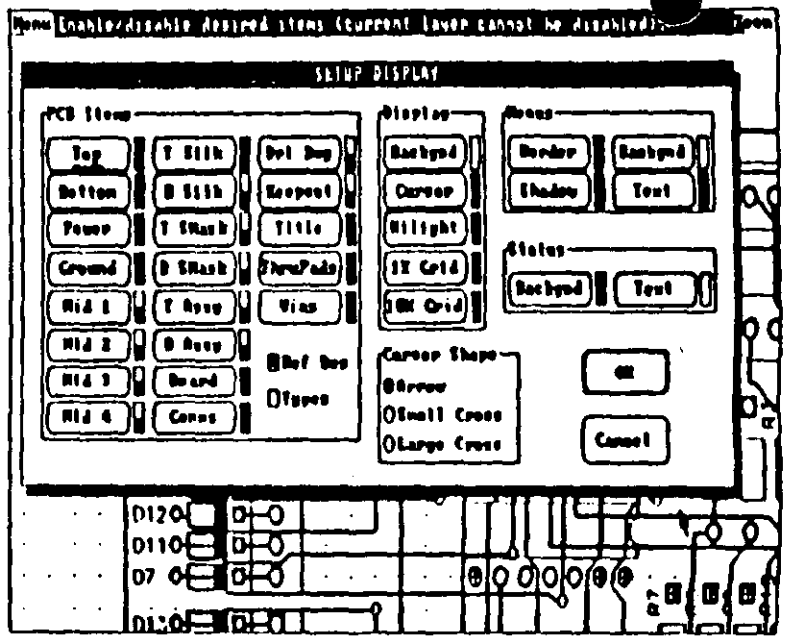


Figure 7-5. In the Setup Display dialog box, enabled layers are indicated by a solid box of color.

Clicking on the color box next to each layer toggles the layer on and off. For example, if Middle Layer 1 is disabled (only the bottom half of the box is colored in), click on the color box to enable the layer (the dialog box shows a solid box of color).

NOTE

When enabling or disabling a layer, make sure that the cursor is positioned **within the color box** *next to the layer's name. Positioning the cursor* **on the layer name** *allows you to change the color of the layer (see* **Selecting Screen Colors** *below).*

When you quit Tango-PCB PLUS, the settings in the Setup Display dialog box are saved in the file PCB.INI. These settings are automatically restored the next time you run the PCB program.

7.15 Selecting Screen Colors

Tango-PCB PLUS lets you have it your way. If you prefer purple pads and a pink cursor, you can have purple pads and a pink cursor. In addition to enabling and disabling PC-board layers, the Setup Display command lets you select the screen colors for individual layers and items (such as through pads and vias), the program menus, the status and prompt lines, and the workspace elements (including background, cursor, highlighting, and grids).

In the Setup Display dialog box, the current color is shown in a box next to each field (Figure 7-5). To change a color for a field, click the mouse on the field name. If your video card supports less than four colors, such as MCGA and Hercules, each click of the mouse cycles through the next available color.

If your video card supports four or more colors, such as EGA and VGA, the program displays a separate dialog box that shows all available colors. In this dialog box, select the desired color and then click on OK. The Setup Display field is updated to show the new color. Clicking on OK again removes the Setup Display dialog box and updates the screen colors.

The colors you select are saved in the file PCB.INI when you quit Tango-PCB PLUS and will be restored the next time you run the PCB program.

7.16 Summary

The following commands were discussed in this chapter:

Command	Function
Current Layer	Set the current layer for editing
Edit Pad	Edit a pad on the PC-board
Setup Display	Enable/disable and select colors for PC-board layers and items

8 Pads and Vias

8.1 Introduction

Tango-PCB PLUS provides user-definable pads and vias for PC-boards. This chapter describes how to define, place, edit, and delete pads and vias. Edge connectors, which consist of a series of surface pads, are also described.

8.2 Pads

A pad is a physical shape on the PC-board that generally corresponds to a component pin. Tango-PCB PLUS provides two types of pads: *through-hole pads* (which belong to all PC-board layers) and *surface pads* (which belong to either the Top or Bottom layer). The through-hole pads are used for component packages with leads that pass through all board layers. The surface pads are used for surface-mount components and edge connectors.

You can place or edit both through-hole pads and surface pads at any time regardless of the current layer setting. For example, if you want to delete a surface pad that belongs to the Top layer, you can do so whether or not the current layer is set to Top.

8.2.1 Selecting Pads

Before placing a pad on the PC-board, you need to run the Current Pad command to select the current pad. All subsequent Place Pad commands use the current pad settings. If you've added pad types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current pad by clicking the mouse on a pad entry in the

15 Verifying the Design

15.1 Introduction

No printed circuit board layout is complete until it has been checked to see that it matches the original electronic design and that, when manufactured, it has a reasonably good chance of working.

If you assume that the original electronic design, normally represented by a schematic, is correct, then you check to see that the PCB layout matches it on a component-by-component, connection-by-connection basis. In days past this task was accomplished with colored pencils and hours of tedious visual cross-checking. Now the process is greatly facilitated by the use of a net list, which is a list of all components connections in the design.

Even if the layout matches the schematic electrically, the physical aspects of manufacturing the board can cause problems which will render it unusable. For example, tracks or pads that are too together could cause bridging of copper, creating a short. The final layout must be checked to see that clearances on the board exceed th specified as your "design rules."

Tango-PCB PLUS offers two distinct, but complementary approaches to verifying the design.

15.1.1 Using Nets Verify

The Nets Verify command will check any nets which are currently displayed against an input net list. You use the Nets Display command to choose which nets to verify -- a single net, a collection of nets, or all nets.

This approach is especially useful if you are manually routing the board, but have an input net list. The recommended process is to 1) use Nets Display to show a single unrouted net, 2) route the net with the Nets Route command, 3) check the routed net with Nets Verify. Then use Nets Display to turn off the display of the routed net and to move onto the next net in the list.

15.1.2 Using The Design Rule Checker

The design rule checker in Tango-PCB PLUS has the ability to check the board electrically against the input net list, and to check for clearance gap violations against rules you establish with the Setup DRC command. Both checks are performed a board-wide basis and should be done when the layout is complete.

15.2 Net List Verification

The Nets Verify command automatically checks that the electrical connections for all displayed routed nets on the PC-board match the connections in the net list. The command verifies each net on a node-by-node basis. If it finds a short (a node that does not belong in the net) an open (a missing node), or an uncommitted component pin connected to the net, the program displays an error. (An uncommitted pin is not listed in the net list as part of any net.) If you are verifying more than one net, you have the option of continuing the verification process or stopping to correct the problem.

NOTE

The Nets Verify command verifies all currently displayed nets. *Before running this command, you need to run the Nets Display command to display (show) the net(s) that you want to verify.*

From the first component pin in the net list, Tango-PCB PLUS checks all connected tracks, area fills, arcs, vias, and pads. Each item is highlighted as it's checked.

If the program finds a component pin that does not belong to the net (a net short), it displays the error message:

Two nets shorted together.

This message includes the net names for the pins and the pin designators.

If the program finds an unconnected node in the net (an open net), it displays the error message:

Net not completely routed.

This message includes the pin designators for two of the unconnected nodes. Tango-PCB PLUS also highlights the sub-net (a group of connected nodes in the net) that includes the first of the unconnected pin designators.

If the program finds an uncommitted component pin in the net, it displays the error message:

Net connected to an uncommitted pin.

This message includes the pin designator of the uncommitted pin.

The Nets Verify command is designed to allow interactive net verification. When the command finds an error, it asks if you want to stop the verification process and fix the problem. Click on Continue to continue the verification process. Click on Cancel to stop the process.

If you choose to continue the verification process after the prog reports a short or an open, Tango-PCB PLUS starts verifying the next displayed net. In this way, the program avoids displaying a long list of errors related to the one short or open. To make sure that there are no additional problems with the net, we recommend that you run the Nets Verify command again after you fix the short or open. If you choose to continue the verification process after the program reports an uncommitted component pin, Tango-PCB PLUS continues to verify the same net.

When continuing the verification process after error messages, jot d the errors as they occur. After Nets Verify is finished, you can then fix

all the problems on your list. Run the Nets Verify command again after modifying the board. If there are no error messages displayed, you can be assured that your net contains no open connections, shorts, or uncommitted component pins.

15.3 Design Rule Checking

After completing the layout, it's a good idea to do a board-wide check to make sure that all electrical connections in the PCB layout match the connections in the net list. This is especially important in Tango-PCB PLUS because the program does not hold nets "sacred". During the routing process, you may break nets without being warned or asked to rename the new net fragment. This speeds the revision process considerably since there are many times when you temporarily break a net. However, it also means that you can completely change the connections on the board.

Besides doing a board-wide electrical check, you should check the design to be sure that minimum clearances have been maintained throughout. Fortunately, both the electrical and clearance checking can be accomplished together with the integrated design rule checker in Tango-PCB PLUS.

To run the design rule checker, do:

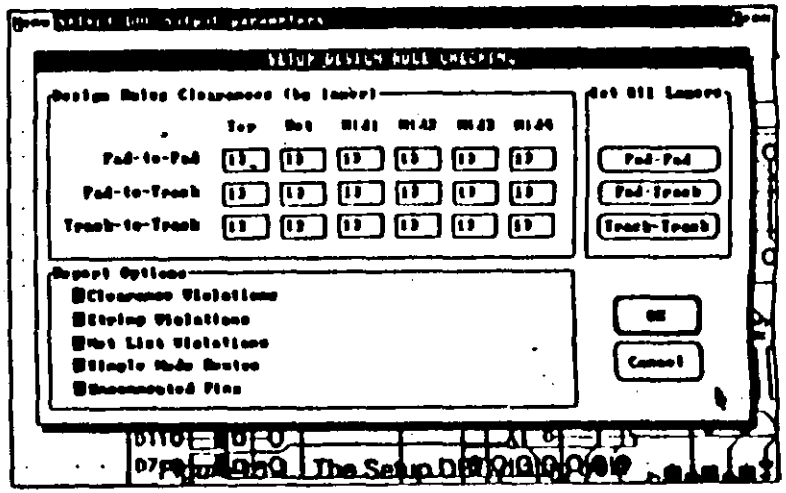
1. Load a net list with the Nets Load command. (This step may be skipped if no net list is available, as we'll explain below).

2. Establish your clearance gap rules with the Setup DRC command.

3. Start the design rule checker by selecting the Design Rule Check report in the Output Reports command.

15.2.1 The Setup DRC Command

Run the Setup DRC command to establish the design rule check parameters in preparation for generating a DRC report (using the Output Reports command). You can enter the minimum Pad-to-P Pad-to-Track, and Track-to-Track clearances allowed on each of the six signal layers. There are also pushbuttons that allow you to set each of these clearances for all layers at once. All of these entries default to 13 mils (if you do not have a PCB.INI file).



You can also specify which conditions are to be checked for: Clearance Violations, String Violations, Net List Violations, Single Node Routes, and Unconnected Pins.

- CLEARANCE VIOLATIONS - Enables air-gap clearance checking. If disabled, no clearance errors will be reported.
- STRING VIOLATIONS - Enables air-gap clearance checking of strings on the signal layers. If you have placed strings on the signal layers, you should enable this option to make sure that the strings do not cross tracks. When checking for clearance violations, the bounding rectangle of the string is used. If the Clearance Violations option (above) has been disabled, this option is also disabled.

- NET LIST VIOLATIONS - Enables electrical checking against the net list. Items are considered to be connected if they overlap or have a clearance of less than 1 mil (just touching). Items that can be electrically connected to one another are arcs, fills, pads, tracks, and vias. Note that although strings can be checked for clearance violations, they are not considered to carry current. If a net list has not been loaded, this option is ignored.
- SINGLE NODE ROUTES - Enables the reporting of pins that are connected to other items on the board, but are not connected to any other pins. Note the use of the word "pin", which is a pad that is part of a component and has a pin designator (as opposed to a free pad, or a pad that is part of a component but does not have a pin designator). Again, items that can be electrically connected to one another are arcs, fills, pads, tracks, and vias.
- UNCONNECTED PINS - Enables the reporting of all pins that are not connected to other pins. This includes all of the Single Node Routes (described above) as well as pins that are not connected to anything at all.

15.3.2 The Design Rule Check Report

Once the DRC options are set with the Setup DRC command, run the Output Reports command and enable the Design Rule Check report. You may print the report or write it out to a file on disk.

When you click on OK, the program will begin the design rule checking process, highlighting each connection as it is verified. When completed, the DRC report will print out or be written to a file.

If you press <Esc> or <RightMouse>, you will be asked to verify your decision to halt the DRC. Should you decide to stop the DRC, the report will print anyway, with any violations encountered prior to the halt.

Running the DRC is a compute-intensive task which can take several hours on complex designs. Considering the alternatives, this seems a small price to pay compared to the benefits of design verification.

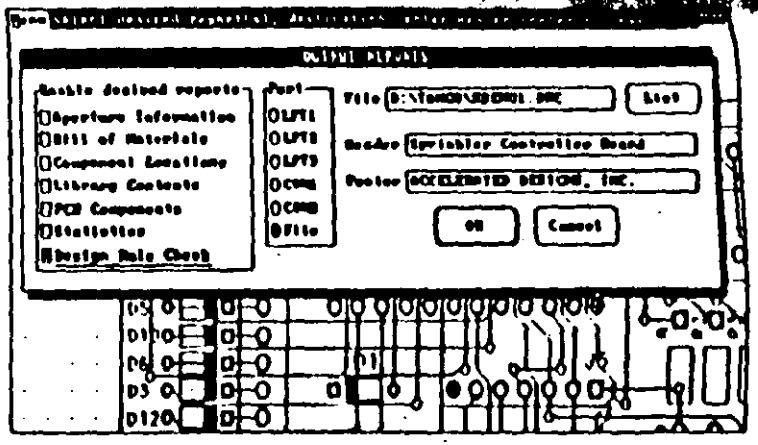


Figure 15-2. Select the Design Rule Check report with the Output Reports Command.

15.3.3 Running DRC Without a Net List

As mentioned above, you do not have to have a net list loaded to produce a DRC report. The DRC will be limited to a check of clearance violations and string violations based on the rules you establish with the Setup DRC command.

NOTE:

If you are running the DRC report without a net list, the design rule checker will report violations where the air-gap clearance is less than that specified. An actual short where two tracks are incorrectly connected will not be reported because the design rule checker will assume they are in the same net. This type of error can only be reported if a net list has been loaded.

15.4 Consideration for Mounting Holes

For mounting hole pads, both the Nets Verify command and the design rule checker consider only the drill hole dimension on inner board layers. This lets you place items such as tracks within the outer dimensions of the mounting hole pad on the inner layers (but not within the drill hole dimension). On the Top and Bottom layers, however, the Nets Verify does consider the outside dimensions of the mounting hole pad. This is because the program assumes the mounting hole pad's outer dimensions may be covered by items such as screw heads, nuts or washers which extend past the hole diameter on the Top and Bottom layers but which would have no effect on the inner layers.

15.5 Summary

Remember that the DRC report checks the entire board, as opposed to the Nets Verify command, which checks only the displayed nets (connections) for accuracy against the net list. Nets Verify is intended to be used repeatedly as the board is designed, so that errors can be fixed right away before more tracks are routed around them. Once you think the PC-board design is complete, generate the DRC report.

Check prints and multi-color check plots are also useful in verifying the PC-board. Tango-PCB PLUS's Nets Verify command and Design Rule Check report, however, can ensure the integrity of each net and clearances on the board, while sparing you the painful and frequently inaccurate task of visually inspecting the PCB artwork and checking connections against the schematic.

The following commands were discussed in this chapter:

Command	Function
Nets Verify	Verify the connections on the board match those in the net list
Setup DRC	Set up the clearance parameters for the physical design rule check
Output Plot/Print	Run the Design Rule Check report

16 Plots, Prints and Reports

16.1 Introduction

This chapter describes the Tango-PCB PLUS commands for printing, plotting, report generation, and special file output such as PostScript and DXF. The Output Plot/Print command lets you plot or print board. Whether you're plotting final artwork or making a quick check print, the program prompts you for all the necessary information with a series of dialog boxes.

The options for printing and plotting include the printer and plotter drivers, communications ports, plotter pen settings and printer colors, scale and X,Y correction values, board layer or layers (if printing a composite), output filename (if sending to a file), plot/print quality (final for artwork or draft for check prints), and the X,Y offsets for the plotter pen. The options you select are automatically saved in the file PCB.INI when you exit the program, then automatically re-loaded the next time you start the program.

In addition to printing and plotting, Tango-PCB PLUS provides the Output Reports command to generate a variety of reports on the PC file. These reports can be output to a printer or file.

If your plotter or printer is connected to a serial port (COM1 or COM2), use the Setup Communications command to set the baud rate, parity, number of data bits, number of stop bits, and handshake protocol before running Output Plot/Print or Output Reports.

20 Commands

20.1 Introduction

This chapter provides a brief description of each Tango-PCB PLUS menu command and a cross-reference to where the command is discussed in the Reference Manual. It is designed to accommodate those of you who are already acquainted with Tango-PCB PLUS (or PCB design packages, in general) and, in most cases, require only an overview of the Tango-PCB PLUS functions.

20.2 Tango-PCB PLUS Commands

The Tango-PCB PLUS menu commands are briefly described in this section.

Current Layer

Description

Set the current layer. All subsequent editing is performed on the current layer. You can only choose from enabled layers when selecting the current layer. Use the Setup Display command to enable and disable layers.

The current layer and the color for the current layer are displayed in the status line's Layer field. You can also set the current layer by clicking on the Layer field or typing L, which toggles through the enabled layers. For boards with only a few layers, clicking on the Layer field or typing L may be faster than using the menus.

Cross-Reference

Section 7.13

Current Pad

Description

Set the current pad. You can choose from pre-defined pads or specify a new pad type. All subsequent Place Pad commands use the current pad settings.

The Pads list box shows all available pad definitions. The definitions are generated from the pads on the PC-board (these pad definitions are marked with an asterisk *) and in the Tango-PCB item definitions file PCB.DFN. If the desired pad type is not displayed in the Pads list box, you can define a new pad and add it to the list.

If you've added pad types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current pad by clicking the mouse on a pad entry in the palette.

Cross-Reference

Section 8.2.1

Current String

Description

Set the current text string. You can choose from pre-defined strings or specify a new string type. All subsequent Place String commands use the current string settings.

The Strings list box shows all available string definitions. If the desired string type is not displayed in the Strings list box, you can define a new string and add it to the list.

If you've added string types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current string by clicking the mouse on a string entry in the palette.

Cross-Reference

Section 10.2.1

Current Track

Description

Set the current track width. You can choose from pre-defined track widths or specify a new width. All subsequent Place Track, Place Arc, and Nets Route commands use the current track width.

The Tracks list box shows all available track definitions. If the desired track type is not displayed in the Tracks list box, you can define a new track and add it to the list.

If you've added track widths to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current track width by clicking the mouse on a track entry in the palette.

Cross-Reference

Section 9.2

Current Via

Description

Set the current via. You can choose from pre-defined vias or specify a new via type. All subsequent Place Via commands use the current via settings.

The Vias list box shows all available via definitions. The definitions are generated from the vias on the PC-board (these via definitions are marked with an asterisk *) and in the Tango-PCB item definitions file PCB.DFN. This file is automatically loaded when you run the PCB program. To select a current via type, click on the via definition in the Vias list box. Then click on OK.

If the desired via type is not displayed in the Vias list box, you can define a new via and add it to the list. To define a new via type, first select the shape. Specify the via size by entering values for the Dimension (even numbers from two through 250 mils) and Hole Diameter (from one through 250 mils) fields.

If you've added via types to the custom Place Palettes, labeled PLACE1 through PLACE5, you can also select the current via by clicking the mouse on a via entry in the palette.

Cross-Reference

Section 8.3.1

Delete Arc

Description

Delete the selected arc on the current layer. If there is no arc selected on the current layer, the computer beeps.

Cross-Reference

Section 10.3.4

Delete Block

Description

Delete all items inside or outside a block. Tango-PCB prompts you to first define the block by marking two diagonally opposite corners of a rectangular area. The program then highlights the defined block.

You can select whether to delete items entirely inside (the default) or entirely outside the block and whether to delete items on the current layer or on all layers (the default). The program redraws the screen with the appropriate items deleted.

Cross-Reference

Section 13.4

Delete Component

Description

Delete the selected component. If there is no component selected, the computer beeps. If there is more than one component under the cursor (on a double-sided surface-mount board, for example), the program displays a list of all these components. You can then select the component to delete from the list.

Cross-Reference

Section 11.7

Delete Fill

Description

Delete the selected area fill on the current layer. If there is no area fill selected on the current layer, the computer beeps.

Cross-Reference

Section 10.4.3

Delete Highlight

Description

Delete all highlighted items, which include free tracks, pads, vias, arcs, and area fills. The items must have been previously highlighted using the Nets Highlight command. If a highlighted item belongs to a component, Tango-PCB will not delete that item. If there are no highlighted items, the computer beeps.

Cross-Reference

Section 14.7.1

Delete Pad

Description

Delete the selected pad. If there is no free pad selected, the computer beeps. This command has no effect on tracks that are connected to the pad.

If you attempt to delete a pad that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.2.5

Delete String

Description

Delete the selected text string on the current layer. If there is no text string selected on the current layer, the computer beeps.

If you attempt to delete a string that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 10.2.6

Delete Track

Description

Delete the selected track on the current layer. If there is no track selected on the current layer, the computer beeps.

If you attempt to delete a track that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 9.6

Delete Via

Description

Delete the selected via. If there is no via selected, the computer beeps. This command has no effect on tracks that are connected to the via.

If you attempt to delete a via that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.3.6

Edit Arc

Description

Edit the selected arc on the current layer. You can change the arc's radius, start angle, sweep angle, and line width. The radius is an even number from two through 16,000 mils. The start angle is an integer from 0 through 359 degrees. The sweep angle is an integer from one through 360 degrees. You can specify any line width from two through 250 mils (in two-mil increments). The line width cannot be more than twice the radius.

Tango-PCB makes it easy to edit a number of arcs on the board at one time. After modifying the arc, use the Arc(s) Edited options to determine whether the editing affects only the selected arc, a set of matching arcs, or all highlighted arcs.

Cross-Reference

Section 10.3.2

Edit Component

Description

Edit the selected component. You can change the component's reference designator, type, and value. You can also choose to release the component (which is similar to the *explode* functi common to most CAD programs). Releasing a component allows you to re-position and modify all the individual primitives in the component.

The Release option is especially useful when creating similar components. You can place a component on an unused area of the workspace, run the Edit Component command to release it, modify individual primitives, then run the Library Add command to define the modified pattern as a new component (see Chapter 12: Creating Library Components).

Cross-Reference

Section 11.5

Edit Pad

Description

Edit the selected pad. You can change the pad's shape, size, hole diameter, pin designator, layer, and plane. For the pad size, you can specify X (horizontal) and Y (vertical) dimensions of two through 4000 mils (in two-mil increments). You can specify any hole size from one through 250 mils.

Tango-PCB makes it easy to edit a number of pads on the board at one time. After modifying the pad, use the Pad(s) Edited options to determine whether the editing affects only the selected pad, a set of matching pads, or all highlighted pads. Matching pads have the same shape, X and Y dimensions, hole diameter, and layer as the selected pad.

Cross-Reference

Section 8.2.3

Edit String

Description

Edit the selected text string on the current layer. You can change the string's contents, height, and line width. You can specify any height from four through 1000 mils (in four-mil increments) and any line width from two through 250 mils (in two-mil increments).

Tango-PCB makes it easy to edit a number of strings on the board at one time. After modifying the string, use the String(s) Edited options to determine whether the editing affects only the selected string or a set of matching strings. Matching strings have the same height and line width as the selected string. If you choose any option other than This String, the Edit String command changes only the height and line width of the matching strings.

Cross-Reference

Section 10.2.4

Edit Track

Description

Edit the width of the selected track on the current layer. F the track width, enter an integer in the range of two through 250 mils (in two-mil increments).

Tango-PCB makes it easy to edit a number of tr :ks on the board at one time. After modifying the track, use the Track(s) Edited options to determine whether the editing affects only the selected track, a set of matching tracks, or all highlighted tracks. Mat tracks have the same width as the selected track.

Cross-Reference

Section 9.4

Edit Via

Description

Edit the selected via. You can change the via's shape, size, hole diameter, and Power/Ground plane connection. For the via size, you can specify a dimension of two through 250 mils (in two- increments). You can specify any hole size from one through 250 mils. The Plane field lets you connect vias to the Power or Ground plane by means of a direct connection or thermal relief.

Tango-PCB makes it easy to edit a number of vias on the board at one time. After modifying the via, use the Via(s) Edited opti to determine whether the editing affects only the selected via, a set of matching vias, or all highlighted vias. Matching vias have the shape, dimension, and hole diameter as the selected via.

Cross-Reference

Section 8.3.4

File Clear

Description

Clear the current PCB file from memory. If any changes have been made to the current PCB file during the editing session, the program prompts you to save the file, discard the changes to the file, or cancel the File Clear command.

Cross-Reference

Section 6.4

File DOS

Description

Execute DOS commands without quitting the Tango-PCB program. The program displays the standard DOS command prompt and you can now enter and execute any DOS command. To return to the Tango-PCB program from where you left off, at the DOS command prompt, enter:

```
exit
```

Cross-Reference

Section 6.7

File Load

Description

Load a PCB file (the default), block file, or a photoplot file. Loading a PCB file replaces the current PCB file with the specified file. Loading a block file inserts the specified file into the current PCB file. Photoplot files may be loaded for on-screen viewing.

Cross-Reference

Section 6.2

File Quit

Description

Quit the Tango-PCB program and return to DOS. If you have made changes to the current PCB during the editing session, the program prompts you to save the changes and exit, exit without saving the changes, or cancel the File Quit command.

Cross-Reference

Section 6.8

File Save

Description

Save the current PC-board or block to a file.

While marking a block during the File Save command, you can use the Zoom and Jump commands to move around on the workspace. You can also cancel the File Save command by pressing <RightMouse> or <Esc> or by clicking on Cancel in the File Save dialog box.

Cross-Reference

Section 6.3

Jump Component

Description

Jump to a specified component on the PCB. Enter the component's reference designator or select from a list of all reference designators on the PC-board. Clicking on OK moves the cursor to the reference point of the specified component (generally, pin 1). If the component is not currently displayed, the program redraws the screen at the same zoom level with the component's reference point at the center.

Cross-Reference

Section 6.5.2, 11.4

Jump Location

Description

Jump to a specified X,Y location on the PCB. Enter the X and Y coordinates of the location and click on OK. If the location is not currently displayed, the program re-draws the screen at the same zoom level with the specified location at the center.

Cross-Reference

Section 6.5.1

Jump Net

Description

Jump to the nearest component pin in a specified net. This command is useful when moving from one net to another during the routing procedure. Enter the net name or select a net from the Nets list box. Click on OK to remove the dialog box and jump to the specified net. If the nearest component pin in the net is not currently displayed, the program re-draws the screen at the same zoom level with the pin at the center.

The Jump Net command is only available if you have previously loaded a net list for the PC-board.

Cross-Reference

Section 6.5.4, 14.9

Jump String

Description

Jump to the nearest text string on the PC-board that matches a specified text string. Tango-PCB searches for an exact match of the specified string. The matching string must contain all and only all the characters in the specified text string.

Select **Current Layer** to search for a match on the current layer only (the default). Select **All Layers** to search for a match on all board layers. If the matching string is not currently displayed, the program redraws the screen at the same zoom level with the string at the center. The Jump String command is not case-sensitive (the characters can be either upper-case or lower-case).

Cross-Reference

Section 6.5.3, 10.2.3

Library Add

Description

Add a new component pattern to the current library. Enter the library name and the pattern name (of from one to 16 characters). After entering the pattern name, press <LeftMouse> or <Enter> to mark the first corner of a rectangle. The rectangular outline expands and contracts as you move the cursor. When the outline encloses the entire component pattern, again press <LeftMouse> or <Enter>. The program then prompts you to select a reference point for the pattern.

Cross-Reference

Section 12.5

Library Browse

Description

Display a component pattern in the specified library. In the Library Browse dialog box, the program displays a list of all patterns in the specified library. Selecting a pattern from this list displays the component on the right side of the dialog box.

Tango-PCB displays the component pattern as it would appear when placed on the PC-board, except for its actual size. The size of the component is scaled to fit within the dimensions of the dialog box. All primitives in the component are displayed. If a primitive belongs to a layer that is not currently enabled, the primitive still appears as part of the displayed pattern. Click on **Continue** to remove the Library Browse dialog box.

Cross-Reference

Section 11.2, 12.9

Library Delete

Description

Delete a component pattern from the specified library. To delete a pattern, highlight the pattern name in the list and click on the **Delete** pushbutton. Click on **Continue** to remove the Library Delete dialog box.

Cross-Reference

Section 12.8

Library Merge

Description

Merge (copy) a component pattern from a specified source library into a specified destination library. You can specify a new name for the pattern. If not, the program retains the source pattern name. Click on the Merge pushbutton to copy the source pattern into the destination library.

If a pattern with the same name exists in the current library, the program prompts you to enter a new pattern name, overwrite the existing pattern, or cancel the Library Merge command. You can continue to copy component patterns into the current library. Click on Continue to remove the Library Merge dialog box.

Cross-Reference

Section 12.6

Library Rename

Description

Rename a component pattern in the specified library. Select the current pattern name from the Patterns list box. Then enter the new pattern name. Click on the Rename pushbutton to rename the component pattern.

If a pattern with the new name exists in the library, the program prompts you to enter another new name, overwrite the existing pattern, or cancel the Library Rename command.

Cross-Reference

Section 12.7

Move Arc

Description

Move an arc on the current layer. First, position the cursor on the arc and press <LeftMouse> or <Enter>. If there is no arc selected on the current layer, the computer beeps. As you move the cursor, an outline of the arc moves across the screen. If you now change the current layer, the arc moves to the selected layer. Press <LeftMouse> or <Enter> to place the arc and <RightMouse> or <Esc> to cancel the Move Arc command.

Cross-Reference

Section 10.3.3

Move Block

Description

Move all items contained entirely within a block. Tango-PCB prompts you to first define the block by marking two diagonally opposite corners of a rectangular area. The program highlights the defined block.

The program then prompts you to select a reference point for the block. Position the cursor on the reference point (generally, one of the corners of the block) and press <LeftMouse> or <Enter>.

If you move the block so that it overlaps any item on any layer of the PC-board, the program displays the Block Overlap Warning dialog box. Click on Retry to move the block to a different location. Click on Overlap to place the block with overlap in its current position. Click on Cancel to cancel the Move Block command.

Cross-Reference

Section 13.2

Move Component

Description

Move and rotate a component pattern on the PCB. First, position the cursor on the component and press <LeftMouse> or <Enter>. As you move the cursor, an outline of the component pattern moves across the screen. Press R to rotate the component 90 degrees. Press F to flip the component. Press <LeftMouse> or <Enter> to place the component and <RightMouse> or <Esc> to cancel the Move Component command.

Cross-Reference

Section 11.6

Move Endpoint

Description

Move the endpoint of a track on the current layer. This command is especially useful for moving a free pad or via on the PC-board while maintaining all routed connections to the pad or via.

When running the Move Endpoint command, first position the cursor on the endpoint of a track and press <LeftMouse> or <Enter>. As you move the cursor, the highlighted tracks stretch (expand and contract) with the endpoint. This process is called *rubberbanding*. Press <LeftMouse> or <Enter> to place the tracks. If there is a free pad or via at the endpoint, it moves to the new location. Press <RightMouse> or <Esc> to cancel the Move Endpoint command.

You cannot change the current layer during the Move Endpoint command.

Cross-Reference

Section 9.5.2

Move Fill

Description

Move an area fill on the current layer. First, position the cursor on the area fill and press <LeftMouse> or <Enter>. If there is no area fill selected on the current layer, the computer beeps. As you move the cursor, an outline of the fill moves across the screen. If you now change the current layer, the fill moves to the selected layer. Press <LeftMouse> or <Enter> to place the fill and <RightMouse> or <Esc> to cancel the Move Fill command.

Cross-Reference

Section 10.4.2

Move Pad

Description

Move and rotate a pad on the PC-board. First, position the cursor on the pad and press <LeftMouse> or <Enter>. If there is no pad selected, the computer beeps. As you move the cursor, an outline of the pad moves across the screen. Press R to rotate the pad 90 degrees. Press <LeftMouse> or <Enter> to place the pad and <RightMouse> or <Esc> to cancel the Move P command.

The Move Pad command has no effect on tracks that are connected to the pad. Run the Move Endpoint command to move a free pad and its connections.

If you attempt to move a pad that is part of a component pattern, the program displays an error message.

Cross-Reference

Section 8.2.4

Move Reroute

Description

Reroute a track as a series of tracks and vias (if needed). This command is especially useful for cleaning up tracks that were dragged (rubberbanded) after running the Move Component command. First, position the cursor on the track and press <LeftMouse> or <Enter>. The endpoint of the track nearest to the cursor is termed the "pivot", the farthest endpoint is the "destination". As you move the cursor, a rubberbanding track outline is drawn from the pivot to the cursor. A rubberbanding line is also drawn from the destination to the cursor.

To place a track from the pivot to the cursor, press <LeftMouse> or <Enter>. The pivot now moves to the endpoint of this track. You can continue to place tracks by pressing <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to conclude the Move Reroute command and place a track from the destination to the cursor.

Cross-Reference

Section 9.5.3

Move String

Description

Move a text string on the current layer. First, position the cursor on the string and press <LeftMouse> or <Enter>. As you move the cursor, an outline of the text string moves across the screen. Press R to rotate the string 90 degrees. Press X to flip the component in the X direction. Press Y to flip the component in the Y direction. Press <LeftMouse> or <Enter> to place the string and <RightMouse> or <Esc> to cancel the Move String command.

Cross-Reference

Section 10.2.5

Move Track

Description

Move a track on the current layer. First, position the cursor on the track and press <LeftMouse> or <Enter>. If there is no track selected on the current layer, the computer beeps. As you move the cursor, an outline of the track moves across the screen. If you now change the current layer, the track moves to the selected layer. Press <LeftMouse> or <Enter> to place the track and <RightMouse> or <Esc> to cancel the Move Track command.

If you change the current layer *during* the Move Track command, the program automatically restores the previous current layer after the command ends. This allows you to move a series of tracks from one layer to another by running the Move Track command several times in succession.

Cross-Reference

Section 9.5.1

Move Via

Description

Move a via on the PC-board. First, position the cursor on the via and press <LeftMouse> or <Enter>. If there is no via selected, the computer beeps. As you move the cursor, an outline of the moves across the screen. Press <LeftMouse> or <Enter> place the via and <RightMouse> or <Esc> to cancel the Move Via command.

The Move Via command has no effect on tracks that are connected to the via. Run the Move Endpoint command to move a via and its connections.

Cross-Reference

Section 8.3.5

Nets Clear

Description

Clear the net list information. This command is useful if you want to clear a net list from memory without loading a new net list. If you run the Nets Load command to load a new net list file, the old net list is automatically cleared from memory.

The Nets Clear command clears all net list information, which includes the connections on the Connections layer and the net names associated with each pad. Clearing the net list (and not loading another one) disables the Nets Optimize, Nets Identify, and Jump Net commands.

Cross-Reference

Section 14.12

Nets Display

Description

Display the specified net list connections. The program displays a list box of all net names in the current net list. Displayed nets are marked with an asterisk. You can choose to show or hide individual nets, all nets connected to a specific component, or all nets. Note that if you have nets connected to the power or ground planes, these nets are marked with a "P" and "G", respectively.

This command also enables or disables the display of Force Vectors. Force vectors are the vector sum of the connections from a component, and are helpful in optimizing component placement.

Cross-Reference

Section 14.3, 14.5

Nets Generate

Description

Generates a Tango-format net list from the currently loaded PCB. The net list includes a listing of components, sorted by reference designator, and a listing of all nets. Each net is assigned a unique net name following the format "NET_*nnnn*" where *nnnn* is a four digit integer.Note that any connections to pads which are not part of a component, or do not have pin designators, will not appear on the net list.

Cross-Reference

Section 14.6, Appendix A

Nets Highlight

Description

Highlight a specified net. This command is useful for verifying manual routing, even if a net list has not been loaded. The Nets Highlight command works together with the Delete Highlight command to delete the items in a routed net on the board.

NOTE: The Highlight Nets command does not use (or require) a net list. The command highlights all items that are electrically connected on the board (generally, by means of tracks).

You can highlight only one net at a time. If a net is currently highlighted and you run the Nets Highlight command to highlight a different net, the program automatically removes the highlighting from the first net.

To un-highlight the net, press <LeftMouse> over a vacant portion of the workspace.

Cross-Reference

Section 14.7

Nets Identify

Description

Identify the net to which a pad belongs. The program prompts you to position the cursor on a pad and press <LeftMouse> or <Enter>. The net name for the pad is displayed in the Nets Identify dialog box. To remove the dialog box, click on OK or press <Enter> or <Esc>.

The Nets Identify command is disabled if there is no net list currently loaded.

Cross-Reference

Section 14.8

Nets Load

Description

Load a net list file. You can directly enter the net list filename in the File entry box of the Nets Load dialog box or you can click on the List pushbutton to select from a displayed list of net list files. The net list file must follow the Tango net list format described in Appendix A. The default filename extension for a net list file is .NET.

Cross-Reference

Section 14.4

Nets Optimize

Description

Create an optimized set of connections for the displayed nets. After you complete the component placement and load the net list, the Nets Optimize command provides a head start for routing the board. It is generally advisable to route the shortest traces first. The optimized connections show you the shortest traces at a glance.

In the Nets Optimize dialog box, select one of the displayed options: **Minimize X Length**, **Minimize Y Length**, or **Minimize Total Length**.

Selecting **Minimize Total Length** minimizes the total length, based on the Manhattan distance between pads. The Manhattan distance is the orthogonal distance between two points calculated as delta X plus delta Y.)

Cross-Reference

Section 14.10

Nets Route

Description

Route a connection interactively. This command lets you replace a displayed connection (which exists only as a routing aid) with a series of tracks and vias (if needed).

When running the Nets Route command, first position the cursor on the a displayed connection and press <LeftMouse> or <Enter>. If there is no connection at the specified location, the computer beeps. If there is a connection, Tango-PCB determines the nearest endpoint for the connection and checks if the endpoint is a surface pad.

Cross-Reference

Section 14.11

lets Verify

Description

Verify that the electrical connections for all displayed routed nets match the connections in the net list. The command verifies each net on a node-by-node basis. If it finds a short (a node that does not belong in the net) or an open (a missing node), the program displays an error. The verification process stops so you can correct the problem.

NOTE: The Nets Verify command verifies all currently displayed nets. Before running this command, you need to run the Nets Display command to display (show) the net(s) that you want to verify.

Cross-Reference

Section 15.2

utput Apertures

Description

Setup the aperture wheel and tool descriptions and then map the aperture and tool settings to items on the PC-board. The first dialog box lets you describe the aperture wheel (for photoplot files) and tools (for N/C drill files). For each aperture wheel position, enter the draft code, the shape, the X and Y dimensions, the hole diameter, and whether the aperture is to be flashed, drawn, or both. You can also enter a brief comment. For each tool, enter the tool number and the hole diameter.

After setting up the aperture wheel and tool descriptions, click on OK to display the Assign Apertures dialog box. In this box, you map the aperture and tool settings to items on the PC-board.

Cross-Reference

Section 17.3, 18.2

Output CAM

Description

Generate a Gerber-format photoplot file or Excellon-compatible N/C drill file for the current PC-board. The first Output CAM dialog box lets you configure the photoplot and N/C drill languages to match your bureau's equipment. In the second dialog box, you can choose from a variety of setup options for the files.

After setting up a file, click on the Add pushbutton to add the file to the CAM File Queue list box. Click on OK to generate the files marked by an asterisk in the CAM File Queue list box. If you select N/C Drill for the board layer/item, Tango-PCB generates an N/C drill file. If you select any other layers or items, the program generates a photoplot file.

Cross-Reference

Section 17.4, 18.4

Output Plot/Print

Description

Plot or print the current PCB file, or generate output files in PostScript or DXF format. You can select a variety of setup options, including: the printer and plotter drivers, communications ports, plotter pen settings and printer colors, scale, X and Y correction, board layer or layers (if printing a composite), output filename (if sending to a file), plot/print quality (final for artwork or draft for check prints), and the X and Y offsets for the plotter pen.

To interrupt plotting/printing, press <RightMouse> or <Esc>. The program then prompts you to continue or cancel the Output Plot/Print command.

Cross-Reference

Section 16.2

Output Reports

Description

Generate a variety of reports for the current PCB file. You can select one or more of the following types of reports: Aperture Information, Bill of Materials, Component Locations, Library Contents, PCB Components, Statistics, and Design Rule Check. At your request, the program sends the report(s) to a printer or file.

Click on OK to print the specified report(s). Click on Cancel to cancel the Output Reports command.

Cross-Reference

Section 16.6

Place Arc

Description

Place an arc on the current layer. To define the arc, the program prompts you to first position the cursor at the desired center point of the arc and press <LeftMouse> or <Enter>. The program draws a circle and radius at this point. Move the cursor to expand the circle to the desired radius of the arc. You can also move the line that indicates the radius to the start of the desired arc, called the start angle. (The start angle is measured counter-clockwise from 3 o'clock on the circle.) Press <LeftMouse> or <Enter> again to fix the radius and start angle. The program redraws the circle, this time displaying an outline of the arc's line width.

Move the cursor now to define the sweep of the arc, which is displayed dynamically on the screen.

Cross-Reference

Section 10.3.1

Place Block Copy

Description

Copy all items contained entirely within a block. Tango-PCB prompts you to first define the block by pressing <LeftMouse> or <Enter> to mark two diagonally opposite corners of a rectangular area. The program highlights the defined block.

After you select the reference point, use the mouse or arrow keys to move an outline of the block across the screen. Press R to rotate the block 90 degrees around the reference point. Each time you press <LeftMouse> or <Enter>, Tango-PCB places a copy of the block at the current cursor position. Press <RightMouse> or <Esc> to terminate the Place Block Copy command.

Cross-Reference

Section 13.3

Place Component

Description

Place a component pattern. Select the pattern from the specified library and enter its reference designator, type, and value (for example, U14, 0.25W RES, 4.7K). Press R to rotate the outline 90 degrees. Press F to flip (mirror) the pattern (which is useful for surface-mount designs). To fix the pattern in its current location and orientation, press <LeftMouse> or <Enter>.

Cross-Reference

Section 11.3

Place Designator

Description

Assign pin designators to a set of pads or reference designators to a set of components. When assigning pin designators, the Place Designator command is generally used after placing all the primitives in a new component pattern and before running the Library Add command to add the new pattern to the current library. When placing reference designators, run the Place Designator command after placing the component(s) on the board.

To assign pin/reference designators, first press <LeftMouse> or <Enter> to display the Place Designator dialog box. Select the Designator type (pin or reference designator). For the designator template, enter up to 15 alphanumeric characters and at least one # (number sign). When you assign pin/reference designators, these # symbols will be replaced by a value determined by the initial value and the increment.

After entering the dialog box values, click on OK. The program prompts you to click on the desired pad (for pin designators) or component (for reference designators).

Cross-Reference

Section 11.5.1, 12.4

Place Fill

Description

Place an area fill (a rectangular region of copper) on the current layer. Tango-PCB prompts you to press <LeftMouse> or <Enter> to mark two diagonally opposite corners of the area fill. The area fill is displayed as a solid rectangle. Press <RightMouse> or <Esc> to cancel the Place Fill command.

Cross-Reference

Section 10.4.1

Place Pad

Description

Place a pad of the current pad type on the workspace. The current pad type, which is shown on the prompt line, is defined using the Current Pad command or by selecting a pad entry from one of the custom Place Palettes.

To place a pad, first press <LeftMouse> or <Enter> to display an outline of the current pad type at the cursor location. The pad outline moves with the cursor. Type R to rotate the pad 90 degrees. To fix the pad in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place Pad command.

Cross-Reference

Section 8.2.2

Place String

Description

Place a string of the current string type on the workspace. The current string type is defined using the Current String command or by selecting a string entry from one of the custom Place Palettes.

Press R to rotate the string 90 degrees counter-clockwise. Press X or Y to flip (mirror) the string along its X or Y axis (which is useful for surface-mount designs). To fix the string in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place String command.

Cross-Reference

Section 10.2.2

Place Track

Description

Place one or more tracks of the current track width on the workspace. The current track width is defined using the Current Track command or by selecting a track entry from one of the custom Place Palette.

To place a track, first press <LeftMouse> or <Enter> to fix a "pivot" point at the current cursor location. As you move the cursor, the program draws a rubberbanding line from the pivot to the cursor (see the section **Setting The Orthogonal Mode** in Chapter 9 for details). Press <LeftMouse> or <Enter> to place the track. You can continue to place tracks, each one starting at the endpoint of the previous track. Press <RightMouse> or <Esc> to terminate the Place Track command.

Cross-Reference

Section 9.3

Place Via

Description

Place a via of the current via type on the workspace. The current via type, which is shown on the prompt line, is defined using the Current Via command or by selecting a via entry from one of the custom Place Palettes.

To place a via, first press <LeftMouse> or <Enter> to display an outline of the current via type at the cursor location. The via outline moves with the cursor. To fix the via in its current location and orientation, press <LeftMouse> or <Enter>. Press <RightMouse> or <Esc> to cancel the Place Via command.

Cross-Reference

Section 8.3.2

Setup Communications

Description

Configure the serial communications ports (COM1 and COM2) for printing and plotting. You can select the baud rate (in the range of 300 through 9600), parity (None, Even, or Odd), number of data bits (7 Bits or 8 Bits), number of stop bits (1 Bit or 2 Bits), and the handshake protocol (Hardwire or XON/XOFF)

The serial port settings will be in effect for all subsequent output operations. When you exit Tango-PCB, these settings are automatically saved in the file PCB.INI and loaded the next time you start the program. You only have to change the settings if you change plotters or printers.

Cross-Reference

Section 16.3

Setup DRC

Description

Setup the design rule check (DRC) parameters, in preparation of generating a DRC report (using the Output Reports command). You can enter the minimum Pad-to-Pad, Pad-to-Track, and Track-to-Track clearances allowed on each of the six signal layers.

You can also specify which conditions are to be checked for. Once the parameters for the DRC are established with Setup DRC, run the Output Reports command and enable the Design Rule Check report.

You do not have to have a net list loaded to produce a DRC report. However, without a net list loaded, the DRC report will not contain any Net List Violations, since there is not a net list for comparison to the board.

Cross-Reference

Section 15.3.1

Setup Display

Description

Enable and disable the display of individual PC-board layers and items (including through pads and vias); turn the visible grid on or off; and, select the cursor shape (arrow, small cross, or large cross).

In the Setup Display dialog box there is a small box of color next to each layer field. This box shows the display color for the layer. If the color box is solid, the layer is enabled. To change a color for a field, click the mouse on the field name.

Cross-Reference

Section 7.14, 7.15

Setup Grids

Description

Set the size for the three workspace grids (absolute, relative, and visible) and set the snap grid to absolute (the default) or relative. As an alternative to the Setup Grids command, you can also set the snap grid by clicking the mouse on the status line's Grid field or by typing G.

You can only move the cursor to a point on the snap grid. When the snap grid is set to absolute, the X,Y coordinates are displayed in parentheses on the status line with the origin (0,0) at the lower-left corner of the workspace. When the snap grid is set to relative, the program prompts you to select the relative grid origin by positioning the cursor and pressing <LeftMouse> or <Enter>.

The visible grid is for reference only.

Cross-Reference

ion 5.8.2

Setup Options

Description

Enable or disable a variety of Tango-PCB options, including Orthogonal modes and Drag Signal Tracks options.

The Orthogonal modes determine the mode for placing tracks on the board. With the Orthogonal modes, you can only place tracks that are horizontal, vertical, or at 45-degree angles. These modes are in effect for the Place Tracks, Move Reroute, and Nets Route commands.

You can also specify whether or not signal tracks are to be dragged (rubberbanded) with the Move Block, Move Component, or Move Track commands.

Cross-Reference

Section 9.5, 11.6, 13.2

Setup Palette

Description

Set up the custom Place Palettes. Tango-PCB provides up to five custom Place Palettes, labeled PLACE1 through PLACE5. You can add pad, string, track, and via information to these palettes. This allows you to have a number of item types, such as pad sizes and track widths, at your fingertips for quick placement.

The number of custom Place Palettes is determined by the number of items you add to the palettes. Each palette is one line in size. If you add more items than will fit on one line, Tango-PCB automatically creates another custom Place Palette.

Cross-Reference

Section 10.2

Undo

Description

Undo the previous editing command. The Undo command restores the PCB to its status prior to the last Delete, Edit, File Load (loading a block only), Move, Nets Route, or Place command. You can only undo the last command. The Undo command makes it easy to change your mind or to recover from a mistake.

You can also undo the previous editing command by clicking the mouse on the Undo hot spot or typing U.

Cross-Reference

Section 5.6

Zoom All

Description

Display the entire 32-inch by 32-inch workspace.

Cross-Reference

Section 6.6.1

Zoom Board

Description

Display the entire PC-board. The zoom level is adjusted so that the PC-board fills the screen. The program displays only the enabled layers of the board.

Cross-Reference

Section 6.6.2

Zoom Center

Description

Re-center the display. The program first displays a rectangular zoom window that indicates the screen area at the current zoom level. This window is the same size as the screen. By moving the cursor, the borders of the window can be moved off the screen, letting you zoom sections of the workspace that aren't currently displayed.

You can initiate a quick Zoom Center at any time by simply pressing the "C" key on your keyboard. This is especially handy for panning quickly across the board.

This command is useful if you want to display a section of the workspace that is currently off-screen. Press <RightMouse> or <Esc> to cancel the Zoom Center command.

Cross-Reference

Section 6.6.3

Zoom In

Description

Zoom in on the display. The program first displays a rectangular zoom window that indicates the screen area at the next highest zoom level. Move the cursor to re-position the window. The borders of the window can be moved off the screen, letting you zoom in on sections of the workspace that aren't currently displayed.

This command is useful if you want to view a section of the workspace in greater detail. Press <RightMouse> or <Esc> to cancel the Zoom In command.

Cross-Reference

Section 6.6.4

Zoom Out

Description

Zoom out on the display. The program prompts you to position the cursor on the desired center of the display, then press <LeftMouse> or <Enter>. The screen is re-drawn at a lower zoom level with the cursor at the center of the screen. This is useful if you want to view a wider area of the workspace (though in less detail than previously displayed). Press <RightMouse> or <Esc> to cancel the Zoom Out command.

Cross-Reference

Section 6.6.5

Zoom Redraw

Description

Re-draw the display at the current center position and zoom level. This is useful if extensive editing (including deletions and moves) has left gaps in the display.

Cross-Reference

Section 6.6.6

Zoom Window

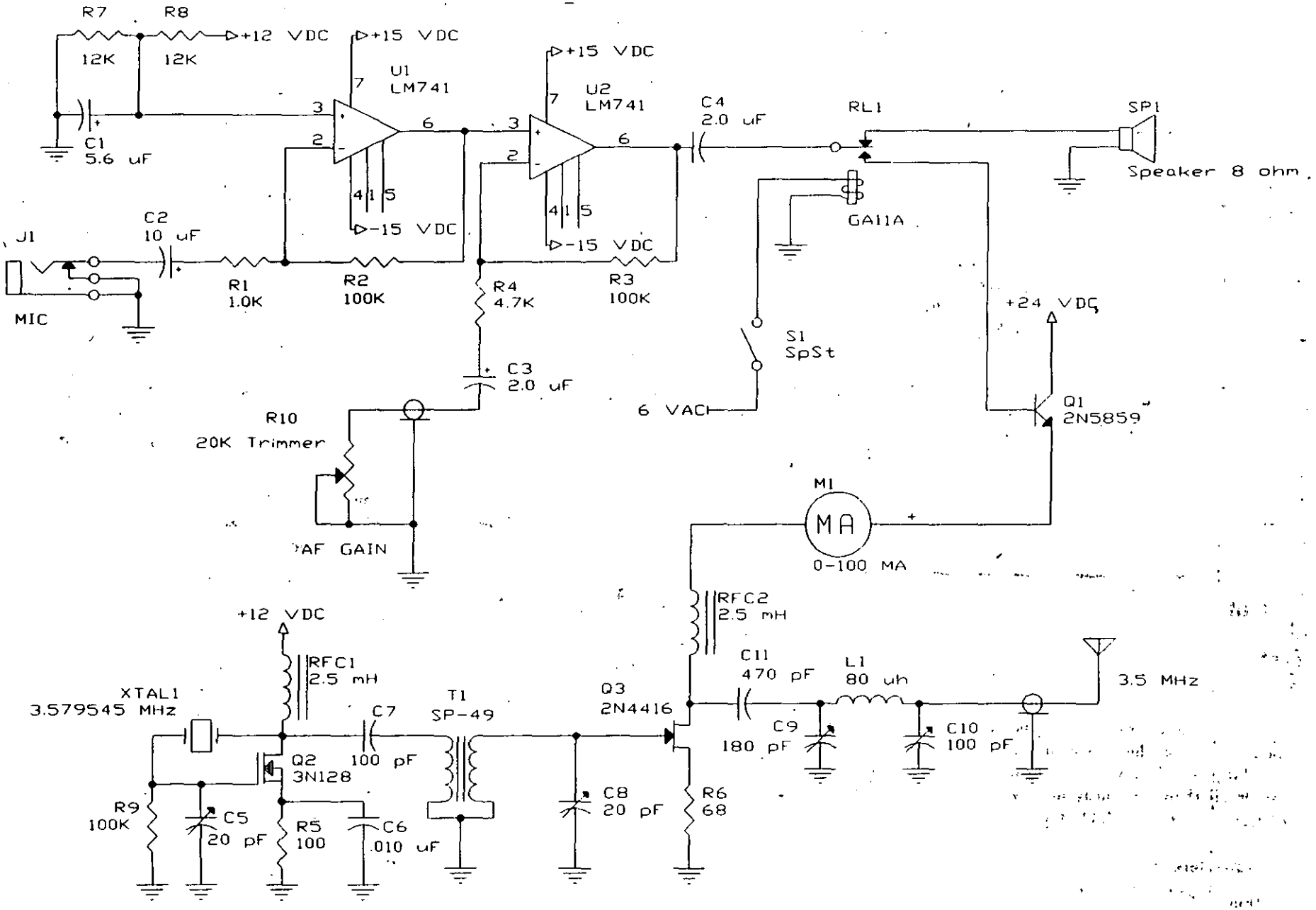
Description

Zoom in or out on a specified section of the workspace. The program first displays a rectangular zoom window that indicates the screen area at the highest zoom level. To mark the center of the zoom window, position the cursor and press <LeftMouse> or <Enter>. The program displays an X at this spot. To display the section of the workspace inside the window at the highest zoom level, again press <LeftMouse> or <Enter> without moving the cursor.

If you want to display a larger area of the workspace, you can expand the window by moving the cursor up or to the right. Contract the window by moving the cursor down or to the left. The borders of the window can be moved off the screen, letting you zoom sections of the workspace that aren't currently displayed. When the window is the desired size, again press <LeftMouse> or <Enter>. The section of the workspace inside the window is redrawn to fill the screen.

Cross-Reference

Section 6.6.7



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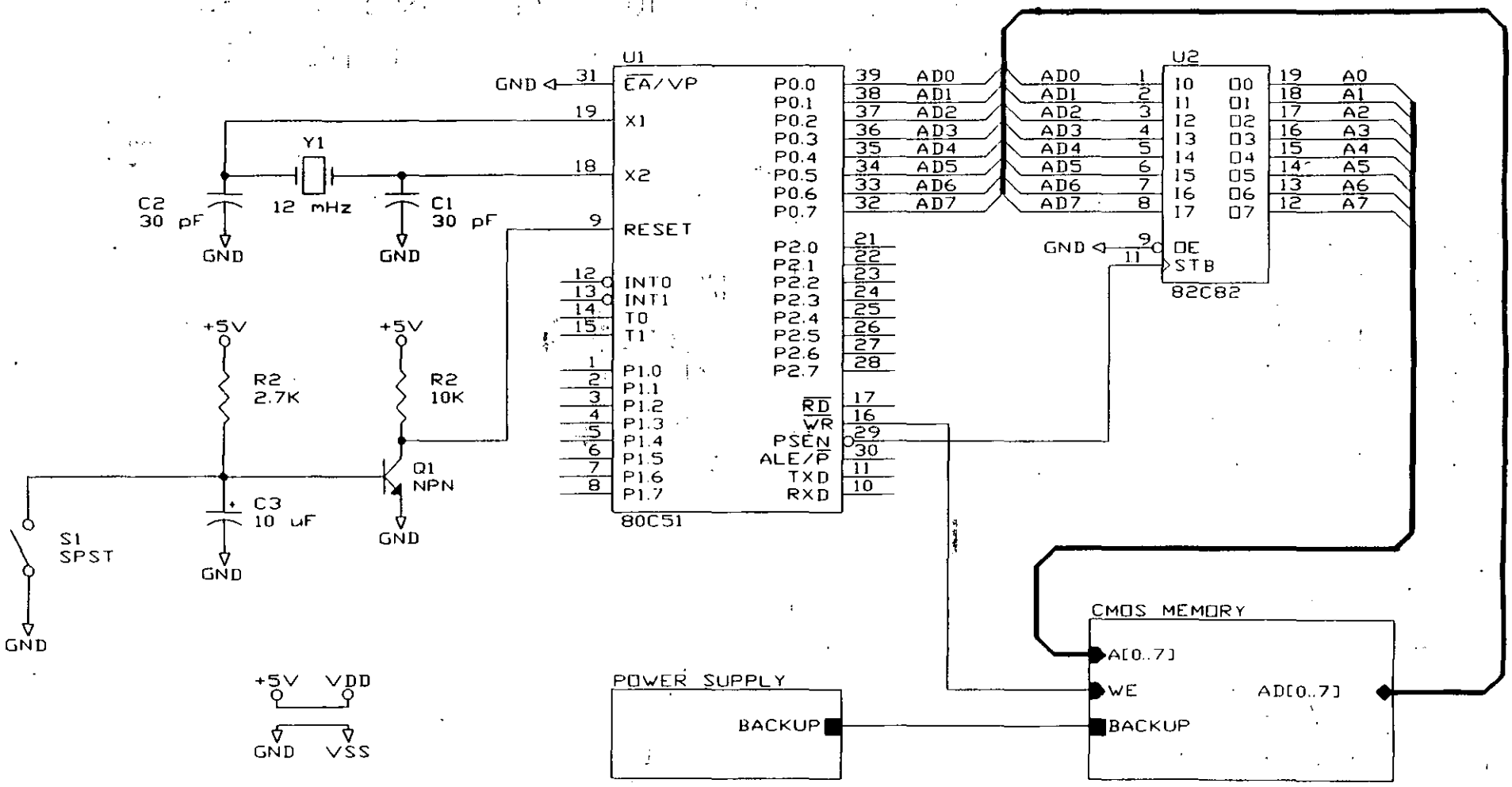
Item	Quantity	Reference	Part
1	1	BOS	1
2	1	C1	5.6 uF
3	1	C2	10 uF
4	2	C3,C4	2.0 uF
5	2	C5,C8	20 pF
6	1	C6	.010 uF
7	2	C7,C10	100 pF
8	1	C9	180 pF
9	1	C11	470 pF
10	1	J1	MIC
11	1	L1	80 uh
12	1	M1	0-100 MA
13	1	Q1	2N5859
14	1	Q2	3N128
15	1	Q3	2N4416
16	1	R1	1.0K
17	3	R2,R3,R9	100K
18	1	R4	4.7K
19	1	R5	100
20	1	R6	68
21	2	R7,R8	12K
22	1	R10	20K Trimmer
23	2	RFC1,RFC2	2.5 mH
24	1	RL1	GA11A
25	1	S1	SpSt
26	1	SP1	Speaker 8 ohm
27	1	T1	SP-49

Item	Quantity	Reference	Part
28	2	U1,U2	LM741
29	1	XTAL1	3.579545 MHz



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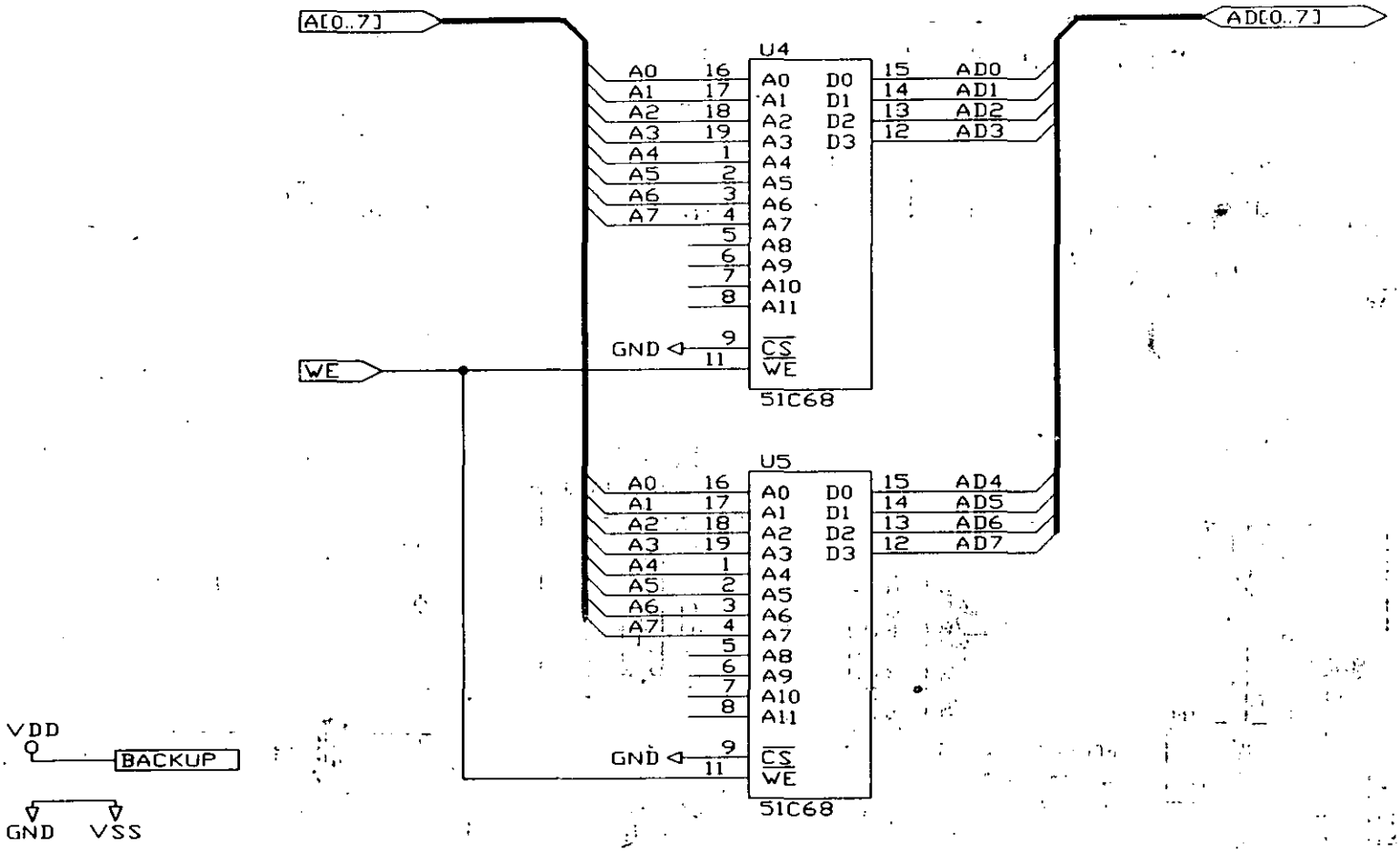

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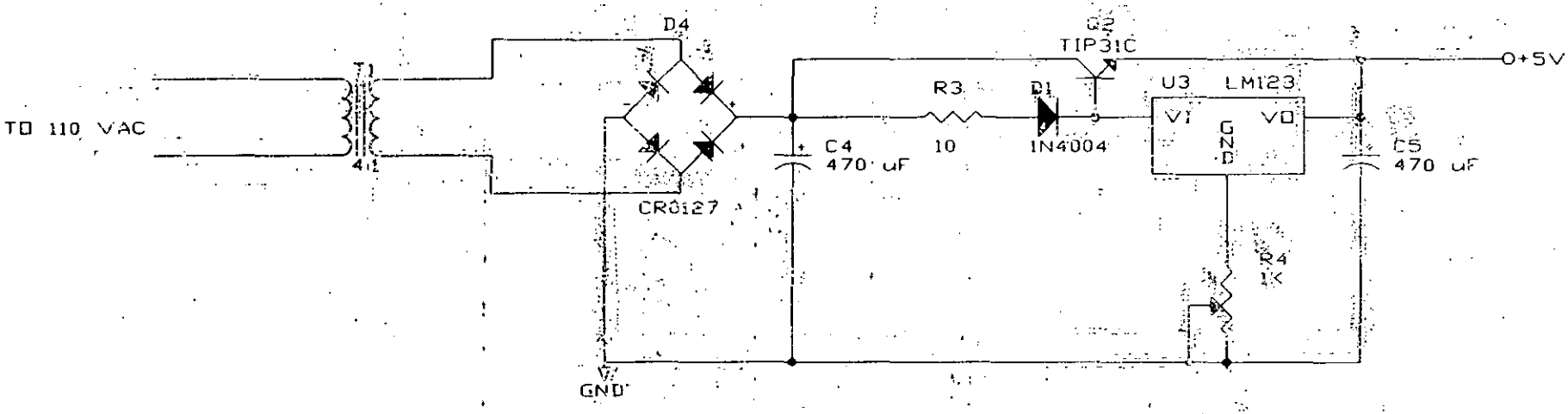

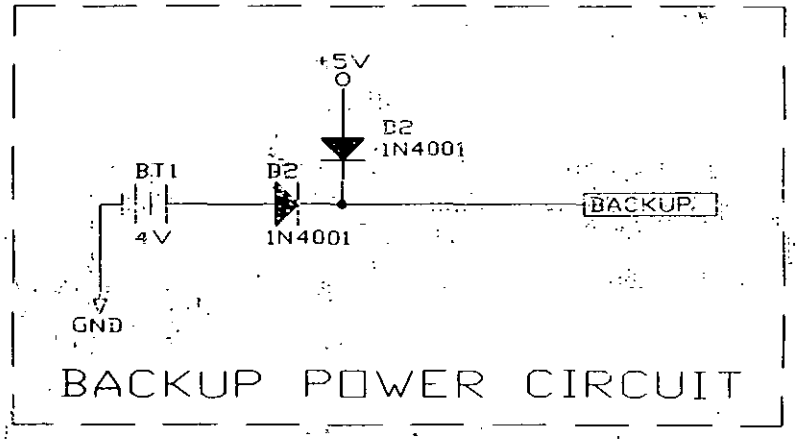

BACKUP POWER CIRCUIT