

A P É N D I C E S

Lista de componentes

Tarjeta de Potencia

Resistores (5%, 250 mW, salvo indicación contraria)

R1= 15 Ω	R7= 1M Ω	R12=1.8 k Ω
R2= 1.8 Ω , 1W	R8= 68 k Ω	
R3= 150 Ω	R9=6.8 k Ω , 1 W	
R4= 12 Ω	R10= 2.2 k Ω	
R5,R6= 47 Ω	R11= 150 k Ω	

Pot 1 = Resistencia ajustable de alambre 10 k Ω

Condensadores

C1= 2200 μ F
C2,C4= 300 nF
C3= 2200 μ F
C5,C6,C7= 1 μ F

Semiconductores

U1= TL783 (Texas Instruments).
U2= 78L05
U3= MOC3031
U4= 7805
D1= Diodo Zener 1N4733A 5.1V/ 1W
Q1= 2N2907
Q2= TIP32C
Q3= PN2222
Q4= IRF1110

Varios

TR1= Transformador 60V/1A
TR2= Transformador 6V / 1A
BR1= Puente rectificador 1.2 A, 100V
BR2= Puente rectificador de Diodos.
F1= Fusible rápido 1A /125 V
F2= Fusible rápido 0.75 A /125 V
F3= Fusible rápido 0.5 A /125 V
K10= Conector horizontal 3 vías con paso de 100 mm .
K11= Conector horizontal 2 vías con paso de 100 mm.
K12= Conector horizontal 2 vías con paso de 100 mm.
K13= Conector horizontal 2 vías con paso de 150 mm.
K14= Conector horizontal 2 vías con paso de 150 mm.

Placa de Control

Resistores

R14,R22=470 Ω

R15= 10 k Ω

R16,R17= 220 Ω

R18,R19= 4.7 k Ω

R20=3.9 k Ω

R21=1 k Ω

POT 2 = Resistencia ajustable 2.4 k Ω horizontal.

Condensadores

C9,C10,C11,C12= 22 pF

C13= 10 nF

Semiconductores

U5= PIC18F452 (Microchip).

U6= 24C256F (Microchip).

U7=DS1307 (Maxim).

Varios

K1= Conector 10 terminales vertical.

K2= Conector 10 terminales vertical.

K3= Conector 6 vías con paso de 100 mm.

K4= Conector 3 vías con paso de 100 mm.

K5= Conector 2 vías con paso de 100 mm.

K6= Conector 2 vías con paso de 100 mm.

K7= Conector 10 terminales vertical

K8= Conector 10 terminales vertical

K9= Conector 2 vías con paso de 100 mm.

BUZ1 Buzzer

X1= Cristal de cuarzo de 10 Mhz

X2= Cristal de cuarzo de 32.768 Khz

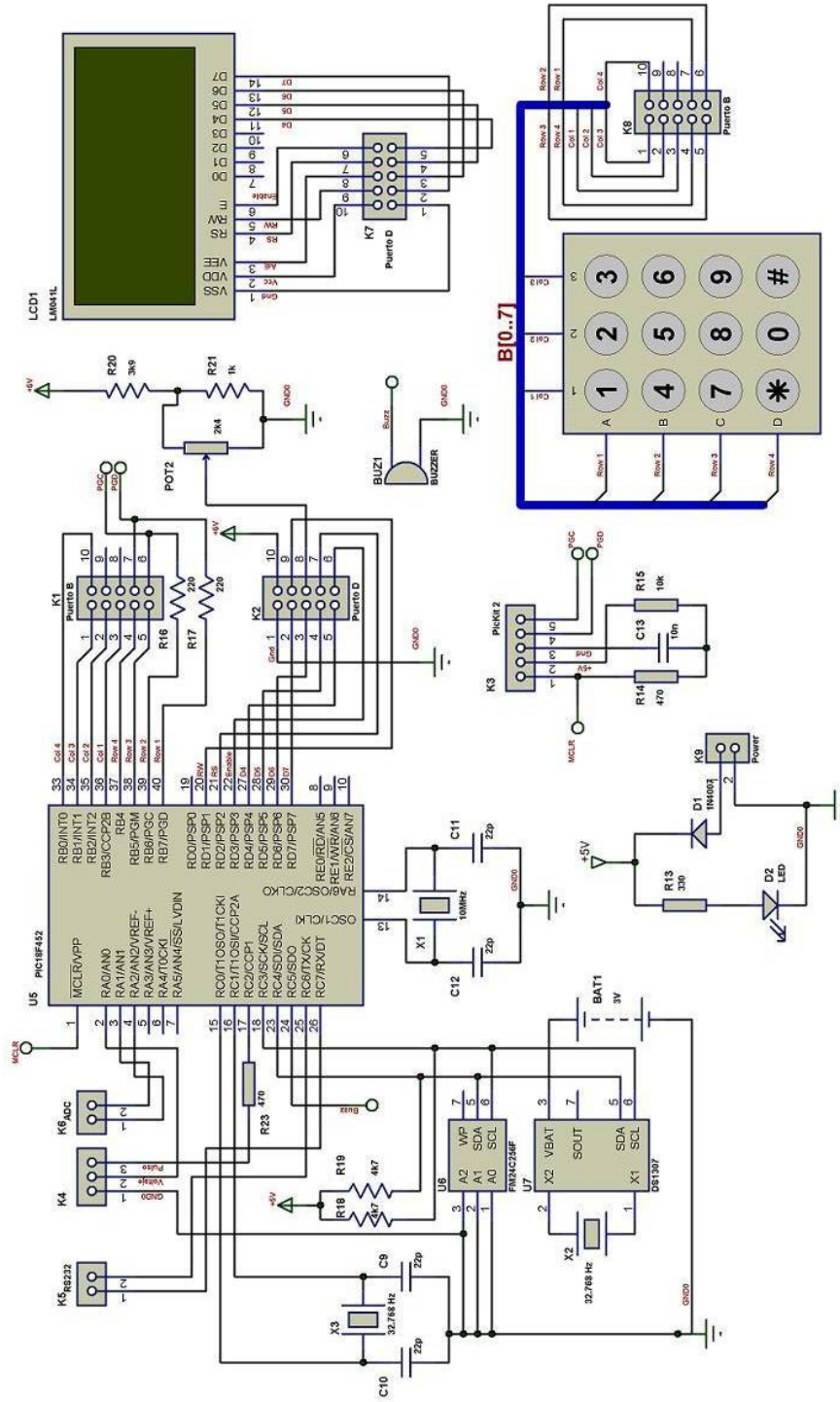
X3= Cristal de cuarzo de 32.768 Khz

BAT1=Zócalo para pila

LCD1 = Visualizador alfanumérico de 4 líneas x 16 caracteres (EPS 050176-73)

S1-S12 = Botón-pulsador, SPN

Esquema Electrónico de Control





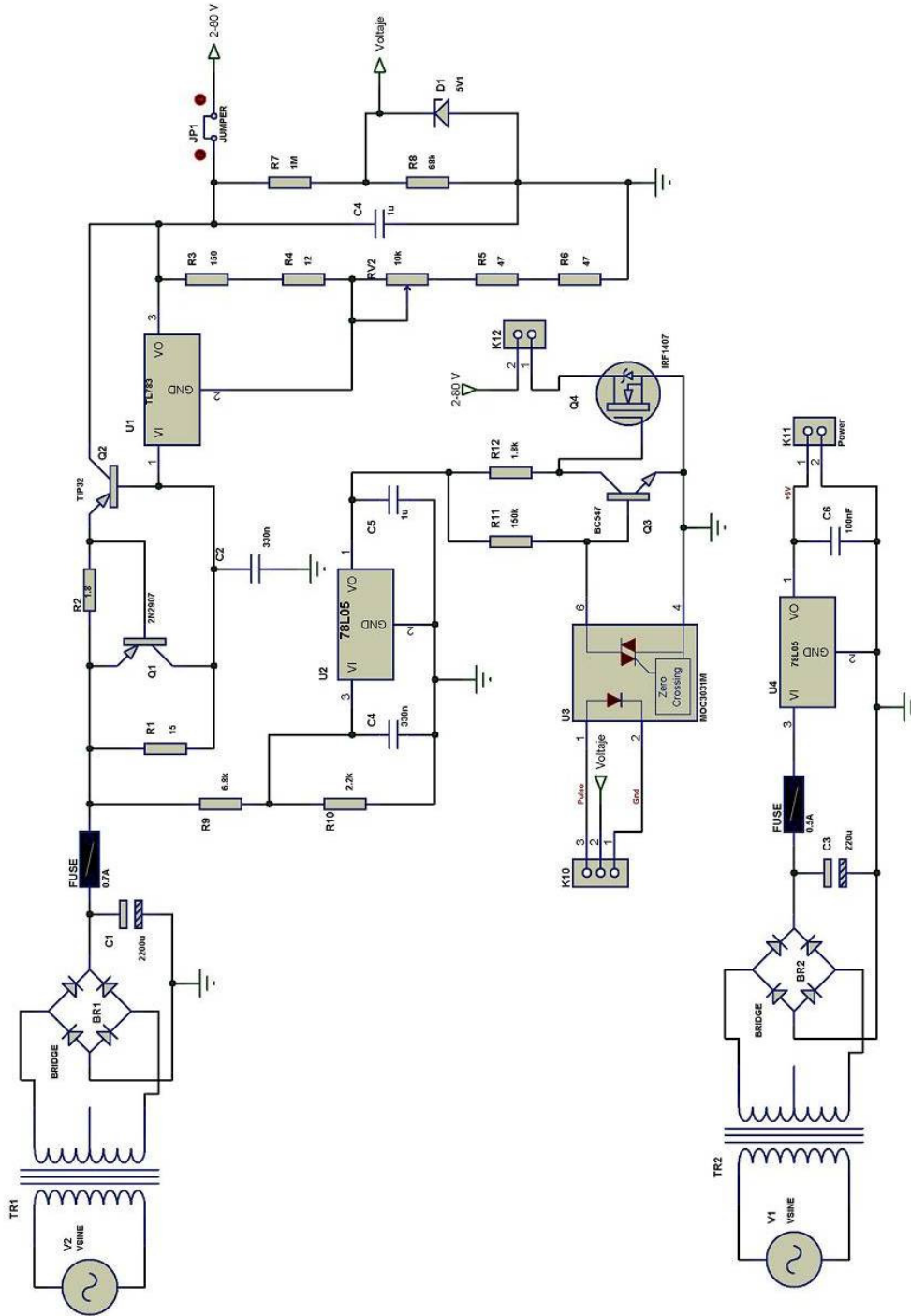
Diseño y Desarrollo de un Electroplador Digital

Unidad de Control

Autor: Gutiérrez Ruiz, Jorge Octavio



Esquema Electrónico de Potencia





Diseño y Desarrollo de un Electropotador Digital

Unidad de Potencia

Autor: Gutiérrez Ruiz, Jorge Octavio



Firmware

Electroporador.c

C:\ProgramMicro\C compiler\Electroporador\electroporador.c

```

1  /*electroporador.c -Codigo principal de la Unidad de Control
2     que realiza todas las funciones del Electroporador
3     Creada por Jorge O. Gutiérrez Ruiz, Julio 13, 2010
4     Código liberado para el dominio público.
5  */
6  #include "LCD_PIC.c"      // Manejo del LCD
7  #include "electroporador.h" //Archivo de cabecera del electroporador
8  #include "teclado.c"     //Manejo del Teclado
9  #include "funciones.c"
10 #include <stdlib.h>      //
11 #include <p18cxxx.h>     //Libreria que especifica puertos del PIC
12 //Registro que maneja el control del programa
13 #define Read      regis_0.b0
14 #define ancho    regis_0.b1
15 #define t_bajo   regis_0.b2
16 #define numero   regis_0.b3
17 #define pulso    regis_0.b4
18 #define fin      regis_0.b5
19 #define wait     regis_0.b6
20 #define start    regis_0.b7
21 /*-----
22     Subroutine: Interrupt_High_Vector
23     Synopsys: Inicializa las Interrupciones de alta prioridad
24 -----*/
25 #pragma code Interrupt_High_Vector = 0x08 //Define la direccion=0008h
26 void Interrupt (void) //para high interruption
27 {
28     _asm
29     goto Interrupt_Handler // Salto a la rutina de Interrupción
30     _endasm
31 }
32 #pragma code
33 /*-----
34     Subroutine: main
35     Synopsys: Rutina principal
36 -----*/
37 void main (void)
38 {
39     INIT_PORTS (); //Inicializacion de puertos principales
40     regis_0._byte=0;
41     LCD_COM (CLR_DISP); //Limpia pantalla del LCD
42     INTCON=0b11100000; //Inicializa TMRO
43     TOCON=0b01000101;
44     T1CON=0b10100000;
45     TMR0L=61; //Desbordamiento del TMRO cada 5ms
46     LCD_write(1,1,"Electroporador"); //Mensaje de bienvenida al sistema
47     LCD_write(2,2,"UNAM-CCADET");
48     LCD_write(3,5,"V 1.5");
49     delay_5s();
50     start=1; //Primera etapa del programa
51
52     while (1)
53     {
54         if (start) //Mensajes del tratamiento
55         {
56             LCD_COM(CLR_DISP); //Limpia pantalla del LCD
57             LCD_write (1,0,"Voltaje V"); //Mensajes al LCD
58             LCD_write (2,0,"Ancho ms");

```

```

59     LCD_write (3,0,"Separacion  ms");
60     LCD_write (4,0,"No. pulsos  ");
61     regis_0._byte=0x01;          //Pasa el control del programa a Read
62 }
63 if (Read) //Lectura del ADC
64 {
65     TOCON&=0X7F;                //Deshabilita interrupcion TMRO
66     LCD_COM (BLINK_OFF);        //Deshabilita cursor del LCD
67     do
68     { read_voltage (); }        //Fin de do
69     while (get_key()!='');      //Espera el enter del voltaje deseado
70     regis_0._byte= 0x02;        //Pasa el control del programa a ancho
71     LCD_COM (BLINK_ON);         //Habilita parpadeo del cursor
72     TOCON^=0X80;                //Habilita Interrupcion de TMRO
73 }//Fin de Read
74 if (ancho) // Recepción del ancho del pulso Tiempo en Alto
75 {
76     do
77     {
78         cursor=0xCB;
79         LCD_COM(cursor);        //Cursor listo para recibir Ancho de pulso
80         ancho_p=in_data(3);     //Se ingresan tres digitos para el ancho de pulso
81         if (ancho_p==0)         //El ancho de pulso no puede ser igual a cero
82         {
83             LCD_COM(CLR_DISP);   //Limpia pantalla del LCD
84             INTCONbits.GIE =0;   //Deshabilitando Interrupciones globa
85             LCD_write (1,0,"El ancho de "); //Error
86             LCD_write (2,0,"pulso no puede");
87             LCD_write (3,0,"ser cero.");
88             buzzer ();           //Aviso auditivo para el usuario
89             while (get_key()!='') //Espera a que se oprima el Enter
90             /* Nothing */ ;
91             LCD_COM(CLR_DISP);   //Limpia pantalla del LCD
92             LCD_write (1,0,"Voltaje  V"); //Mensajes al LCD
93             LCD_write (2,0,"Ancho  ms");
94             LCD_write (3,0,"Separacion  ms");
95             LCD_write (4,0,"No. pulsos  ");
96             if (voltaje>9999)    //Escribe el voltaje ya seleccionado
97             {
98                 LCD_COM (0X88);
99                 LCD_DAT(disp_val[0]); //Escribe en LCD la parte entera
100                LCD_DAT(disp_val[1]); //Escribe en LCD la parte entera
101                LCD_DAT(0X2E);        //Escribe le punto decimal
102                LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
103            }
104            else
105            {
106                LCD_COM (0X88);
107                LCD_DAT(disp_val[0]); //Escribe en LCD la parte entera
108                LCD_DAT(0X2E);        //Escribe le punto decimal
109                LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
110            }
111            INTCONbits.GIE =1;        //Habilitando Interrupciones globales.
112        }
113    }
114    while(ancho_p==0);              //Regresa a pedir ancho de pulso
115    regis_0._byte= 0x04;           //Pasa el control del programa a t_bajo
116    ky=0xff;                       //Evita que la siguiente etapa lea el enter anterior.

```

```

117 }//Fin de if(ancho)
118 if (t_bajo) // Recepción del tren del pulso Tiempo en Bajo
119 {
120     do
121     {
122         cursor=0x9B;
123         LCD_COM(cursor); //Cursor listo para recibir frecuencia
124         hz=in_data(3); //Se ingresan dos digitos para la frecuencia del pulso
125         if ((hz ==0) || (hz%50!=0)) //El ancho de pulso no puede ser igual a cero
126         {
127             //y debe ser divisible entre 50
128             INTCONbits.GIE =0; //Deshabilitando Interrupciones globales.
129             LCD_COM(CLR_DISP); //Limpia pantalla del LCD
130             LCD_write (1,0,"Solo multiples ");
131             LCD_write (2,0,"de 50.");
132             buzzer (); //Aviso auditivo para el usuario
133             while (get_key()!=' '); //Espera a que se oprima el Enter
134             LCD_COM(CLR_DISP); //Limpia pantalla del LCD
135             LCD_write (1,0,"Voltaje V"); //Mensajes al LCD
136             LCD_write (2,0,"Ancho ms");
137             LCD_write (3,0,"Separacion ms");
138             LCD_write (4,0,"No. pulsos ");
139             if (voltaje>9999) //Voltaje mayor a 9.999V
140             {
141                 //Escribe el voltaje ya seleccionado
142                 LCD_COM (0X88);
143                 LCD_DAT(displ_val[0]); //Escribe en LCD la parte entera
144                 LCD_DAT(displ_val[1]); //Escribe en LCD la parte entera
145                 LCD_DAT(0X2E); //Escribe el punto decimal
146                 LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
147             }
148             else
149             {
150                 LCD_COM (0X88);
151                 LCD_DAT(displ_val[0]); //Escribe en LCD la parte entera
152                 LCD_DAT(0X2E); //Escribe el punto decimal
153                 LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
154             }
155             disp_val_ptr=&data[0]; //Escribe el ancho ya seleccionado
156             itoa(ancho_p,disp_val_ptr); //Convierte el varlo de ancho a un string
157             LCD_COM(0xCB); //Ubica al LCD en el renglon de A.pulso
158             LCD_ascii(disp_val_ptr); //Escribe en LCD el ancho de pulso
159             INTCONbits.GIE =1; //Habilita interrupciones
160         }
161     }
162     while((hz==0) || (hz%50!=0)); //Regresa a pedir la frecuencia del pulso
163     regis_0_byte=0x08 ; //Pasa el control del programa a pedir el No. de pulsos
164     ky=0xff; //Evita que la siguiente etapa lea el enter anterior.
165 }//Fin de if(t_bajo)
166 if (numero) //Recepción del Numero de pulsos
167 {
168     do
169     {
170         cursor=0xDB;
171         LCD_COM(cursor); //Cursor listo para recibir frecuencia
172         num_pulso=in_data(2); //Se ingresan dos digitos para la frecuencia del pulso
173         if (num_pulso==0) //El ancho de pulso no puede ser igual a cero
174         {
175             //y debe ser divisible entre 50
176             INTCONbits.GIE =0; //Habilitando Interrupciones globales.
177             LCD_COM(CLR_DISP); //Limpia pantalla del LCD

```



```

175 LCD_write (1,0,"El intervalo de");
176 LCD_write (2,0,"pulsos es de ");
177 LCD_write (3,0,"1-99.");
178 buzzer (); //Aviso auditivo para el usuario
179 while (get_key()!=' ');
180 //Espera a que se oprima el Enter
181 LCD_COM(CLR_DISP); //Limpia pantalla del LCD
182 LCD_write (1,0,"Voltaje V"); //Mensajes al LCD
183 LCD_write (2,0,"Ancho ms");
184 LCD_write (3,0,"Separacion ms");
185 LCD_write (4,0,"No. pulsos ");
186 if (voltaje>9999)
187 { //Escribe el voltaje ya seleccionado
188 LCD_COM (0X88);
189 LCD_DAT(displ_val[0]); //Escribe en LCD la parte entera
190 LCD_DAT(displ_val[1]); //Escribe en LCD la parte entera
191 LCD_DAT(0X2E); //Escribe le punto decimal
192 LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
193 }
194 else
195 {
196 LCD_COM (0X88);
197 LCD_DAT(displ_val[0]); //Escribe en LCD la parte entera
198 LCD_DAT(0X2E); //Escribe le punto decimal
199 LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
200 }
201 displ_val_ptr=&data[0];
202 itoa(ancho_p,displ_val_ptr); //Escribe el ancho ya seleccionado
203 LCD_COM(0xCB);
204 LCD_ascii(displ_val_ptr); //Escribe en LCD la parte entera
205 displ_val_ptr=&data[0];
206 itoa(hz,displ_val_ptr); //Escribe el tren de pulso ya seleccionado
207 LCD_COM(0x9B);
208 LCD_ascii(displ_val_ptr); //Escribe en LCD la parte entera
209 INTCONbits.GIE =1; //Habilitando Interrupciones globales.
210 } //Fin de if (num_pulso==0)
211 } // Fin de do
212 while(num_pulso==0); //Regresa a pedir No. de pulsos
213 } // Fin de if(numero)
214
215 LCD_COM(CLR_DISP); //Limpia pantalla del LCD
216 LCD_write (1,0,"Los parametros"); //Permiso de realizar el tratamiento
217 LCD_write (2,0,"son correctos ?");
218 LCD_write (3,0,"SI: Enter");
219 LCD_write (4,0,"NO: Borrar");
220 while((ky!=' ')&&(ky!='*'));
221 if (ky==' ')
222 {
223 INTCONbits.GIE =0; //Deshabilitando Interrupciones globales.
224 do
225 {
226 LCD_COM(CLR_DISP); //Limpia pantalla del LCD
227 for (cont2=1; cont2<=num_pulso;cont2++)
228 temp1s(); //Realiza el tratamiento ingresado
229 buzzer (); //Aviso auditivo Fin del Tratamiento
230 INTCONbits.GIE =1; //Deshabilitando Interrupciones globales.
231 LCD_write (1,0,"Voltaje V"); //Mensajes al LCD
232 LCD_write (2,0,"Ancho ms");

```

```

233         LCD_write (3,0,"Separacion  ms");
234         LCD_write (4,0,"No. pulsos  ");
235         if (voltaje>9999)          // Escribe los parametros del tratamiento
236         {
237             LCD_COM (0X88);
238             LCD_DAT(disp_val[0]); //Escribe en LCD la parte entera
239             LCD_DAT(disp_val[1]); //Escribe en LCD la parte entera
240             LCD_DAT(0X2E);        //Escribe le punto decimal
241             LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
242         }
243         else
244         {
245             LCD_COM (0X88);
246             LCD_DAT(disp_val[0]); //Escribe en LCD la parte entera
247             LCD_DAT(0X2E);        //Escribe le punto decimal
248             LCD_ascii (val_frac); //Escribe la parte fraccionaria en LCD
249         }
250         disp_val_ptr=&data[0];      //Variable que guarda parametros
251         itoa(ancho_p,disp_val_ptr); //Se guarda A.pulso para desplegar a LCD
252         LCD_COM(0xCB);
253         LCD_ascii(disp_val_ptr);    //Escribe en LCD A.Pulso
254         disp_val_ptr=&data[0];
255         itoa(hz,disp_val_ptr);      //Se guarda tiempo en bajo para desplegar a LCD
256         LCD_COM(0x9B);
257         LCD_ascii(disp_val_ptr);    //Escribe en LCD tren de pulsos
258         disp_val_ptr=&data[0];
259         itoa(num_pulso,disp_val_ptr); //Se guarda num_pulso para desplegar a LCD
260         LCD_COM(0xDB);
261         LCD_ascii(disp_val_ptr);    //Escribe en LCD numero de pulsos
262         while (ky!=' ');            //Espera a que se oprima el Enter
263         LCD_COM(CLR_DISP);          //Limpia pantalla del LCD
264         LCD_write (1,0,"Repetir ?"); //Permiso de realizar el tratamiento
265         LCD_write (3,0,"Si: Enter");
266         LCD_write (4,0,"No: Borrar");
267         while((ky!=' ')&&(ky!='*'));
268     }
269     while (ky==' ');
270     regis_0_byte=0x80 ; //Pasa el control del programa a start
271 }
272 else // Se ha opreso Borrar
273 { regis_0_byte=0x80 ; //Pasa el control del programa a start
274   INTCONbits.GIE =1; //Habilita Interrupciones globales
275 }
276
277 } // Fin de while (1)
278 } // Fin de main
279
280 /*-----*/
281     Subroutine: Interrupt_Handler
282     Synopsys: Maneja todas las interrupciones del programa
283     -----*/
284 #pragma interrupt Interrupt_Handler //La funcion ADCVoltage se especifica como high-priority ISR
285 void Interrupt_Handler (void) //No transfiere parametros por ser ISR
286 {
287     if (INTCONbits.TMROIF)
288     {
289         ky=get_key(); //Obtiene la tecla pulsada
290         TMR0L=61; //Desbordamiento del TMR0 cada 5 ms

```

```

291     INTCONbits.TMR0IF =0;    //Limpia bandera de interrupcion del TMRO
292 }
293 } //Final de Interrupt Handler
294
295
296 /*-----
297     Subroutine: INIT_PORTS
298     Synopsys: Inicializa todos los registros y funciones asociados con la aplicacion.
299 -----*/
300
301 void INIT_PORTS (void)
302 {
303     INI_ADC ();    //Inicializa el ADC
304     INI_LCD ();    //Inicializa el LCD
305     INI_keypad ();    //Inicializa el teclado
306     INI_BUZZER ();//Inicializa el buzzer
307     bitclr(TRISC,2);    //Inicializa la salida del pin del tratamiento
308     bitclr(PORTC,2);
309 }
310

```

Electroporador.h

C:\ProgramMicro\C compiler\Electroporador\electroporador.h

```
1  /*electroporador.h - Libreria de cabecera para el manejo del Electroporador
2   Creada por Jorge O. Gutiérrez Ruiz, Julio 13, 2010
3   Código liberado para el dominio público.
4  */
5
6  #include "boolean.h"    /* funciones booleanas */
7  #include <adc.h>        //Libreria de conversión AD
8  #include <delays.h>     //Libreria de retardos por software
9  #include <stdlib.h>     //
10 #include <timers.h>     //Libreria de temporizador
11 #include <p18cxxx.h>    //Libreria que especifica puertos del PIC
12
13 // Configuración de fuses del PIC
14 #pragma config OSC = OFF
15 #pragma config OSC = HS    // - set HSPLL oscilador
16 #pragma config WDT = OFF  // -disable watchdog timer
17 #pragma config LVP = OFF  // -disabel low voltage programming
18 #pragma config DEBUG = ON // -enable background debugging
19
20 #define bitset(Var,bitno) ((Var) |= 1 << (bitno))
21 #define bitclr(Var,bitno) ((Var) &= ~(1 << (bitno)))
22 #define ON    1           //Definicion de booleanos
23 #define OFF   0
24 #define BASE  4.169      // Voltaje Max a la entrada del AD (4.176/1023)
25
26
27
28 //Definicion de Prototipos de Funcion
29 void INIT_PORTS (void);    //Inializa todos los puertos principales y aplicaciones
30 void delay_5s (void);     //Retardo de 5 segundos por software
31 void delay_1s (void);     //Retardo de 1 segundo por software
32 void INI_ADC (void);      //Inicializa ADC
33 void INI_BUZZER (void);   //Inicializa Buzzer
34 unsigned int x_read(int no); //Variable con Oversampling del ADC
35 unsigned int ADC_READ (void); //Activación y Lectura del ADC
36 void buzzer (void);       //Aviso auditivo del buzzer
37 int in_data ( int n);     //Recepción de parametros del tratamiento
38 void temp1s (void);       //Ejecución del tratamiento
39 void Interrupt_Handler (void); //Maneja todas las Interrupciones del PIC
40 void read_voltage (void); //Lee el voltaje del ADC y despliega en pantalla
41 // Creacion de un Registro de 8 bits
42 typedef union _BYTE
43 {
44     unsigned char _byte;
45     struct
46     {
47         unsigned b0:1;
48         unsigned b1:1;
49         unsigned b2:1;
50         unsigned b3:1;
51         unsigned b4:1;
52         unsigned b5:1;
53         unsigned b6:1;
54         unsigned b7:1;
55     };
56 } BYTE;
57
58 //Definicion de Variables globales           //near:indica que la variable es puesta en Access RAM
```

```

59 int multi1=1000; //volatile:El contenido de la variable puede cambiar
60 char *disp_val_ptr;
61 #pragma udata access var_glob //udata: locates uninitialised user variables in data memory
62 near volatile char addr,val_high,val_low,data[3], enter,ky;
63 near volatile char cont, cont2, i, disp_val [6], val_frac[4];
64 near volatile int tmp,ADC,integer,frac,cursor,ADC_current,idx;
65 near volatile long int voltaje, x;
66 near volatile int ancho_p, hz,bajo;
67 near volatile int num_pulso;
68 near BYTE regis_0,regis_temp;
69 #pragma udata
70

```

Hojas de Especificaciones

TL783



TL783

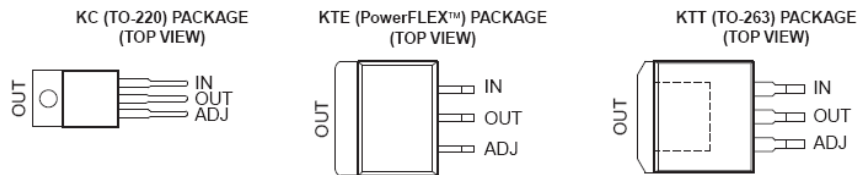
www.ti.com

SLVS036M – SEPTEMBER 1981 – REVISED APRIL 2008

HIGH-VOLTAGE ADJUSTABLE REGULATOR

FEATURES

- Output Adjustable From 1.25 V to 125 V When Used With an External Resistor Divider
- 700-mA Output Current
- Full Short-Circuit, Safe-Operating-Area, and Thermal-Shutdown Protection
- 0.001%/V Typical Input Voltage Regulation
- 0.15% Typical Output Voltage Regulation
- 76-dB Typical Ripple Rejection



DESCRIPTION/ORDERING INFORMATION

The TL783 is an adjustable three-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip, to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary-breakdown and thermal-runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if ADJ is disconnected inadvertently, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

ORDERING INFORMATION⁽¹⁾

T _J	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	PowerFLEX™ – KTE	Reel of 2000	TL783CKTER	TL783
	TO-263 – KTT	Reel of 500	TL783CKTTR	TL783C
	TO-220 – KC	Tube of 50	TL783CKC	TL783C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



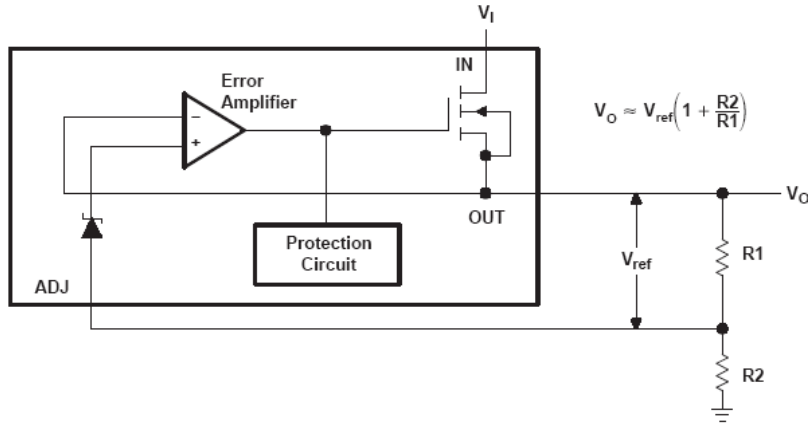
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FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage		125	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data⁽¹⁾

PACKAGE	BOARD	θ_{JC}	$\theta_{JP}^{(2)}$	θ_{JA}
PowerFLEX (KTE)	High K, JESD 51-5		2.7°C/W	23°C/W
TO-263 (KTT)	High K, JESD 51-5	18°C/W	1.94°C/W	25.3°C/W
TO-220 (KC)	High K, JESD 51-5	17°C/W	3°C/W	19°C/W

- (1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
- (2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage		125	V
I_O	Output current	15	700	mA
T_J	Operating virtual junction temperature	0	125	°C

Electrical Characteristics
 $V_I - V_O = 25\text{ V}$, $I_O = 0.5\text{ A}$, $T_J = 0^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
Input voltage regulation ⁽²⁾	$V_I - V_O = 20\text{ V}$ to 125 V , $P \leq$ rated dissipation	$T_J = 25^\circ\text{C}$	0.001	0.01	%/ V
		$T_J = 0^\circ\text{C}$ to 125°C	0.004	0.02	
Ripple rejection	$\Delta V_{I(PP)} = 10\text{ V}$, $V_O = 10\text{ V}$, $f = 120\text{ Hz}$	66	76		dB
Output voltage regulation	$I_O = 15\text{ mA}$ to 700 mA , $T_J = 25^\circ\text{C}$	$V_O \leq 5\text{ V}$	7.5	25	mV
		$V_O \geq 5\text{ V}$	0.15	0.5	%
	$I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation	$V_O \leq 5\text{ V}$	20	70	mV
		$V_O \geq 5\text{ V}$	0.3	1.5	%
Output voltage change with temperature			0.4		%
Output voltage long-term drift	1000 hours at $T_J = 125^\circ\text{C}$, $V_I - V_O = 125\text{ V}$		0.2		%
Output noise voltage	$f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$		0.003		%
Minimum output current to maintain regulation	$V_I - V_O = 125\text{ V}$			15	mA
Peak output current	$V_I - V_O = 25\text{ V}$, $t = 1\text{ ms}$		1100		mA
	$V_I - V_O = 15\text{ V}$, $t = 30\text{ ms}$		715		
	$V_I - V_O = 25\text{ V}$, $t = 30\text{ ms}$	700	900		
	$V_I - V_O = 125\text{ V}$, $t = 30\text{ ms}$	100	250		
ADJ input current			83	110	μA
Change in ADJ input current	$V_I - V_O = 15\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation		0.5	5	μA
Reference voltage (OUT to ADJ) ⁽³⁾	$V_I - V_O = 10\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation	1.2	1.27	1.3	V

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
- (2) Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input
- (3) Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.



LM78LXX Series 3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment.

The LM78LXX is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area pro-

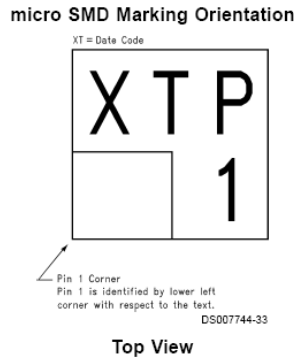
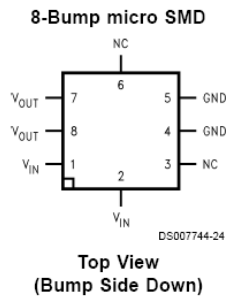
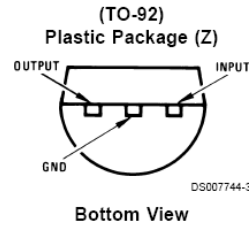
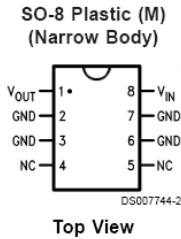
tection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of $\pm 5\%$ over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components
- Output voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V

LM78LXX Series 3-Terminal Positive Regulators

Connection Diagrams



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	Internally Limited
Input Voltage	35V
Storage Temperature	-65°C to +150°C

Operating Junction Temperature	SO-8	0°C to 125°C
	micro SMD	-40°C to 85°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C (lead time)
ESD Susceptibility (Note 2)		1kV

LM78LXX Electrical Characteristics Limits in standard typeface are for $T_J = 25^\circ\text{C}$, **Bold typeface applies over 0°C to 125°C for SO-8 package and -40°C to 85°C for micro SMD package.** Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $I_O = 40\text{ mA}$, $C_I = 0.33\ \mu\text{F}$, $C_O = 0.1\ \mu\text{F}$.

LM78L05

Unless otherwise specified, $V_{IN} = 10\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		4.8	5	5.2	V
		$7\text{V} \leq V_{IN} \leq 20\text{V}$ $1\text{ mA} \leq I_O \leq 40\text{ mA}$ (Note 3)	4.75		5.25	
		$1\text{ mA} \leq I_O \leq 70\text{ mA}$ (Note 3)	4.75		5.25	
ΔV_O	Line Regulation	$7\text{V} \leq V_{IN} \leq 20\text{V}$		18	75	mV
		$8\text{V} \leq V_{IN} \leq 20\text{V}$		10	54	
ΔV_O	Load Regulation	$1\text{ mA} \leq I_O \leq 100\text{ mA}$		20	60	mV
		$1\text{ mA} \leq I_O \leq 40\text{ mA}$		5	30	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	$8\text{V} \leq V_{IN} \leq 20\text{V}$ $1\text{ mA} \leq I_O \leq 40\text{ mA}$			1.0 0.1	
V_n	Output Noise Voltage	$f = 10\text{ Hz to } 100\text{ kHz}$ (Note 4)		40		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120\text{ Hz}$ $8\text{V} \leq V_{IN} \leq 16\text{V}$	47	62		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	$I_O = 5\text{ mA}$		-0.65		mV/°C
$V_{IN}(\text{Min})$	Minimum Value of Input Voltage Required to Maintain Line Regulation			6.7	7	V
θ_{JA}	Thermal Resistance (8-Bump micro SMD)			230.9		°C/W



**TIP31A/31C
TIP32A/32B/32C**

**COMPLEMENTARY SILICON POWER
TRANSISTORS**

APPLICATION

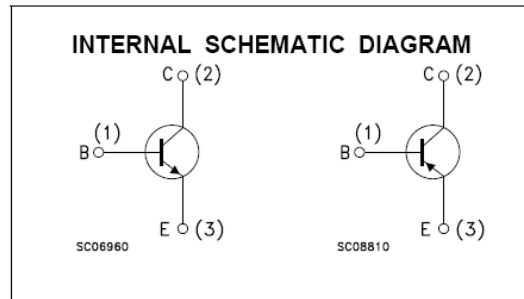
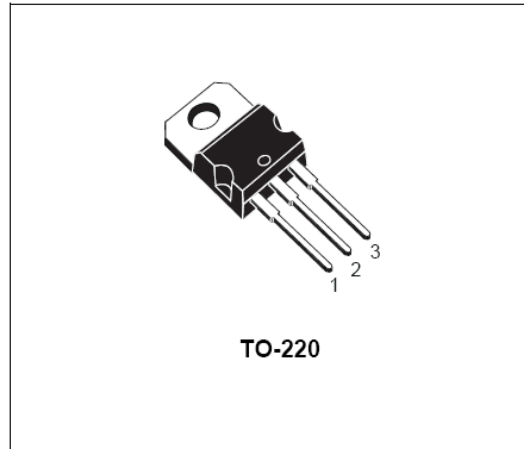
- LINEAR AND SWITCHING INDUSTRIAL EQUIPMENT

DESCRIPTION

The TIP31A and TIP31C are silicon Epitaxial-Base NPN transistors mounted in Jedec TO-220 plastic package. They are intended for use in medium power linear and switching applications.

The complementary PNP types are TIP32A and TIP32C respectively.

Also TIP32B is a PNP type.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit	
		NPN	TIP31A	TIP31C		
		PNP	TIP32A	TIP32C		
V _{CB0}	Collector-Base Voltage (I _E = 0)		60	80	100	V
V _{CE0}	Collector-Emitter Voltage (I _B = 0)		60	80	100	V
V _{EBO}	Emitter-Base Voltage (I _C = 0)		5			V
I _C	Collector Current		3			A
I _{CM}	Collector Peak Current		5			A
I _B	Base Current		1			A
P _{tot}	Total Dissipation at T _{case} ≤ 25 °C T _{amb} ≤ 25 °C		40			W
			2			W
T _{stg}	Storage Temperature		-65 to 150			°C
T _j	Max. Operating Junction Temperature		150			°C

For PNP types voltage and current values are negative

TIP31A/TIP31C/TIP32A/TIP32B/TIP32C

THERMAL DATA

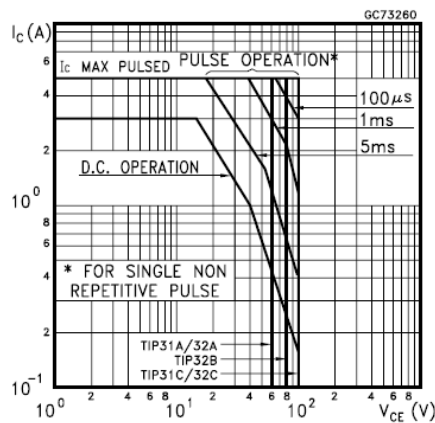
$R_{thj-case}$	Thermal Resistance Junction-case	Max	3.12	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

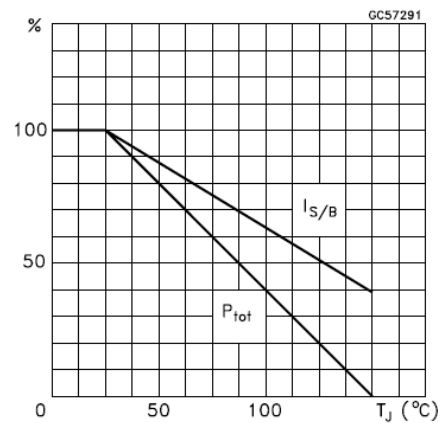
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current ($I_B = 0$)	for TIP31A/32A $V_{CE} = 30 V$ for TIP31C/32B/32C $V_{CE} = 60 V$			0.3 0.3	mA mA
I_{CES}	Collector Cut-off Current ($V_{BE} = 0$)	for TIP31A/32A $V_{CE} = 60 V$ for TIP32B $V_{CE} = 80 V$ for TIP31C/32C $V_{CE} = 100 V$			0.2 0.2 0.2	mA mA mA
I_{EBO}	Emitter Cut-off Current ($I_C = 0$)	$V_{EB} = 5 V$			1	mA
$V_{CEO(sus)*}$	Collector-Emitter Sustaining Voltage ($I_B = 0$)	$I_C = 30 mA$ for TIP31A/32A for TIP32B for TIP31C/32C	60 80 100			V V V
$V_{CE(sat)*}$	Collector-Emitter Saturation Voltage	$I_C = 3 A$ $I_B = 375 mA$			1.2	V
$V_{BE(on)*}$	Base-Emitter Voltage	$I_C = 3 A$ $V_{CE} = 4 V$			1.8	V
h_{FE*}	DC Current Gain	$I_C = 1 A$ $V_{CE} = 4 V$ $I_C = 3 A$ $V_{CE} = 4 V$	25 10		50	
h_{fe}	Small Signal Current Gain	$I_C = 0.5 A$ $V_{CE} = 10 V$ $f = 1 KHz$ $I_C = 0.5 A$ $V_{CE} = 10 V$ $f = 1 MHz$	20 3			

* Pulsed : pulse duration = 300 μs , duty cycle $\leq 2\%$
For PNP types voltage and current values are negative.

Safe Operating Area




Derating Curves

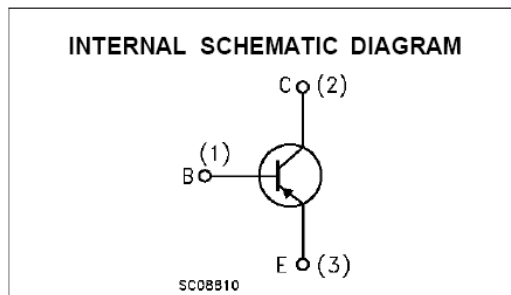
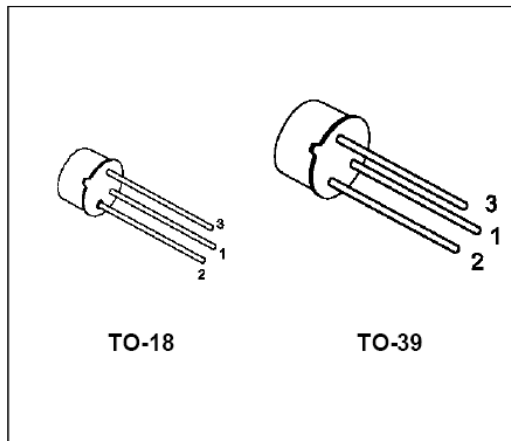


GENERAL PURPOSE AMPLIFIERS AND SWITCHES

DESCRIPTION

The 2N2905 and 2N2907 are silicon planar epitaxial PNP transistors in Jedec TO-39 (for 2N2905) and in Jedec TO-18 (for 2N2907) metal case. They are designed for high speed saturated switching and general purpose application.

 2N2905 approved to CECC 50002-102,
 2N2907 approved to CECC 50002-103
 available on request.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CB0}	Collector-Base Voltage ($I_E = 0$)	-60	V
V_{CE0}	Collector-Emitter Voltage ($I_B = 0$)	-40	V
V_{EB0}	Emitter-Base Voltage ($I_C = 0$)	-5	V
I_C	Collector Current	-0.6	A
P_{tot}	Total Dissipation at $T_{amb} \leq 25^\circ\text{C}$ for 2N2905 for 2N2907 at $T_{case} \leq 25^\circ\text{C}$ for 2N2905 for 2N2907	0.6	W
		0.4	W
		3	W
		1.8	W
T_{stg}	Storage Temperature	-65 to 200	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature	200	$^\circ\text{C}$

THERMAL DATA

		TO-39	TO-18	
R _{thj-case}	Thermal Resistance Junction-Case	Max	58.3	97.3 °C/W
R _{thj-amb}	Thermal Resistance Junction-Ambient	Max	292	437.5 °C/W

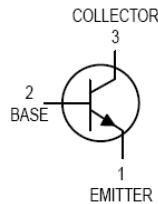
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{CBO}	Collector Cut-off Current (I _E = 0)	V _{CB} = -50 V V _{CB} = -50 V T _{case} = 150 °C			-20 -20	nA μA
I _{CEX}	Collector Cut-off Current (V _{BE} = -0.5V)	V _{CE} = -30 V			-50	nA
I _{BEX}	Base Cut-off Current (V _{BE} = -0.5V)	V _{CE} = -30 V			-50	nA
V _{(BR)CBO} *	Collector-Base Breakdown Voltage (I _E = 0)	I _C = -10 μA	-60			V
V _{(BR)CEO} *	Collector-Emitter Breakdown Voltage (I _B = 0)	I _C = -10 mA	-40			V
V _{(BR)EBO} *	Emitter-Base Breakdown Voltage (I _C = 0)	I _E = -10 μA	-5			V
V _{CE(sat)} *	Collector-Emitter Saturation Voltage	I _C = -150 mA I _B = -15 mA I _C = -500 mA I _B = -50 mA			-0.4 -1.6	V V
V _{BE(sat)} *	Base-Emitter Saturation Voltage	I _C = -150 mA I _B = -15 mA I _C = -500 mA I _B = -50 mA			-1.3 -2.6	V V
h _{FE} *	DC Current Gain	I _C = -0.1 mA V _{CE} = -10 V I _C = -1 mA V _{CE} = -10 V I _C = -10 mA V _{CE} = -10 V I _C = -150 mA V _{CE} = -10 V I _C = -500 mA V _{CE} = -10 V	35 50 75 100 30		300	
f _T	Transition Frequency	V _{CE} = -20 V f = 100 MHz I _C = -50 mA	200			MHz
C _{EBO}	Emitter Base Capacitance	I _C = 0 V _{EB} = -2 V f = 1MHz			30	pF
C _{CBO}	Collector Base Capacitance	I _E = 0 V _{CB} = -10 V f = 1MHz			8	pF
t _d	Delay Time	V _{CC} = -30 V I _C = -150 mA I _{B1} = -15 mA			10	ns
t _r	Rise Time	V _{CC} = -30 V I _C = -150 mA I _{B1} = -15 mA			40	ns
t _s	Storage Time	V _{CC} = -6 V I _C = -150 mA I _{B1} = -I _{B2} = -15 mA			80	ns
t _f	Fall Time	V _{CC} = -6 V I _C = -150 mA I _{B1} = -I _{B2} = -15 mA			30	ns

* Pulsed: Pulse duration = 300 μs, duty cycle ≤ 1%

General Purpose Transistors

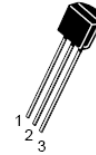
NPN Silicon



MPS2222

MPS2222A*

*Motorola Preferred Device


 CASE 29-04, STYLE 1
 TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	MPS2222	MPS2222A	Unit
Collector–Emitter Voltage	V_{CE0}	30	40	Vdc
Collector–Base Voltage	V_{CBO}	60	75	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	6.0	Vdc
Collector Current — Continuous	I_C	600		mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625	5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5	12	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = 10\text{ mAdc}, I_E = 0$)	MPS2222 MPS2222A	$V_{(BR)CEO}$	30 40	— —	Vdc
Collector–Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{Adc}, I_E = 0$)	MPS2222 MPS2222A	$V_{(BR)CBO}$	60 75	— —	Vdc
Emitter–Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{Adc}, I_C = 0$)	MPS2222 MPS2222A	$V_{(BR)EBO}$	5.0 6.0	— —	Vdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}, V_{EB(off)} = 3.0\text{ Vdc}$)	MPS2222A	I_{CEX}	—	10	nAdc
Collector Cutoff Current ($V_{CB} = 50\text{ Vdc}, I_E = 0$) ($V_{CB} = 60\text{ Vdc}, I_E = 0$) ($V_{CB} = 50\text{ Vdc}, I_E = 0, T_A = 125^\circ\text{C}$) ($V_{CB} = 50\text{ Vdc}, I_E = 0, T_A = 125^\circ\text{C}$)	MPS2222 MPS2222A MPS2222 MPS2222A	I_{CBO}	— — — —	0.01 0.01 10 10	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0\text{ Vdc}, I_C = 0$)	MPS2222A	I_{EBO}	—	100	nAdc
Base Cutoff Current ($V_{CE} = 60\text{ Vdc}, V_{EB(off)} = 3.0\text{ Vdc}$)	MPS2222A	I_{BL}	—	20	nAdc

Preferred devices are Motorola recommended choices for future use and best overall value.

MPS2222 MPS2222A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (I _C = 0.1 mA, V _{CE} = 10 Vdc) (I _C = 1.0 mA, V _{CE} = 10 Vdc) (I _C = 10 mA, V _{CE} = 10 Vdc) (I _C = 10 mA, V _{CE} = 10 Vdc, T _A = -55°C) (I _C = 150 mA, V _{CE} = 10 Vdc) ⁽¹⁾ (I _C = 150 mA, V _{CE} = 1.0 Vdc) ⁽¹⁾ (I _C = 500 mA, V _{CE} = 10 Vdc) ⁽¹⁾	h _{FE}	35 50 75 35 100 50 30 40	— — — — 300 — — —	—
Collector–Emitter Saturation Voltage ⁽¹⁾ (I _C = 150 mA, I _B = 15 mA) (I _C = 500 mA, I _B = 50 mA)	V _{CE(sat)}	— — — —	0.4 0.3 1.6 1.0	Vdc
Base–Emitter Saturation Voltage ⁽¹⁾ (I _C = 150 mA, I _B = 15 mA) (I _C = 500 mA, I _B = 50 mA)	V _{BE(sat)}	— 0.6 — —	1.3 1.2 2.6 2.0	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current–Gain — Bandwidth Product ⁽²⁾ (I _C = 20 mA, V _{CE} = 20 Vdc, f = 100 MHz)	f _T	250 300	— —	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{obo}	—	8.0	pF
Input Capacitance (V _{EB} = 0.5 Vdc, I _C = 0, f = 1.0 MHz)	C _{ibo}	— —	30 25	pF
Input Impedance (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz) (I _C = 10 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{ie}	2.0 0.25	8.0 1.25	kΩ
Voltage Feedback Ratio (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz) (I _C = 10 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{re}	— —	8.0 4.0	X 10 ⁻⁴
Small–Signal Current Gain (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz) (I _C = 10 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	50 75	300 375	—
Output Admittance (I _C = 1.0 mA, V _{CE} = 10 Vdc, f = 1.0 kHz) (I _C = 10 mA, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{oe}	5.0 25	35 200	μmhos
Collector Base Time Constant (I _E = 20 mA, V _{CB} = 20 Vdc, f = 31.8 MHz)	rb'C _C	—	150	ps
Noise Figure (I _C = 100 μA, V _{CE} = 10 Vdc, R _S = 1.0 kΩ, f = 1.0 kHz)	NF	—	4.0	dB

SWITCHING CHARACTERISTICS MPS2222A only

Delay Time	(V _{CC} = 30 Vdc, V _{BE(off)} = -0.5 Vdc, I _C = 150 mA, I _{B1} = 15 mA) (Figure 1)	t _d	—	10	ns
Rise Time		t _r	—	25	ns
Storage Time	(V _{CC} = 30 Vdc, I _C = 150 mA, I _{B1} = I _{B2} = 15 mA) (Figure 2)	t _s	—	225	ns
Fall Time		t _f	—	60	ns

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

2. f_T is defined as the frequency at which |h_{fe}| extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

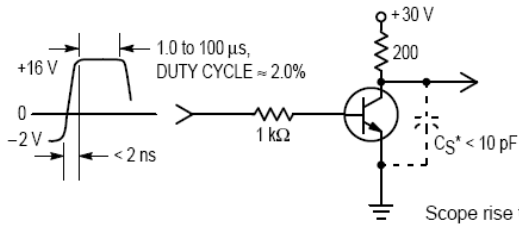


Figure 1. Turn-On Time

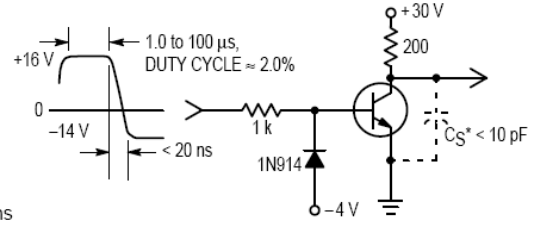


Figure 2. Turn-Off Time

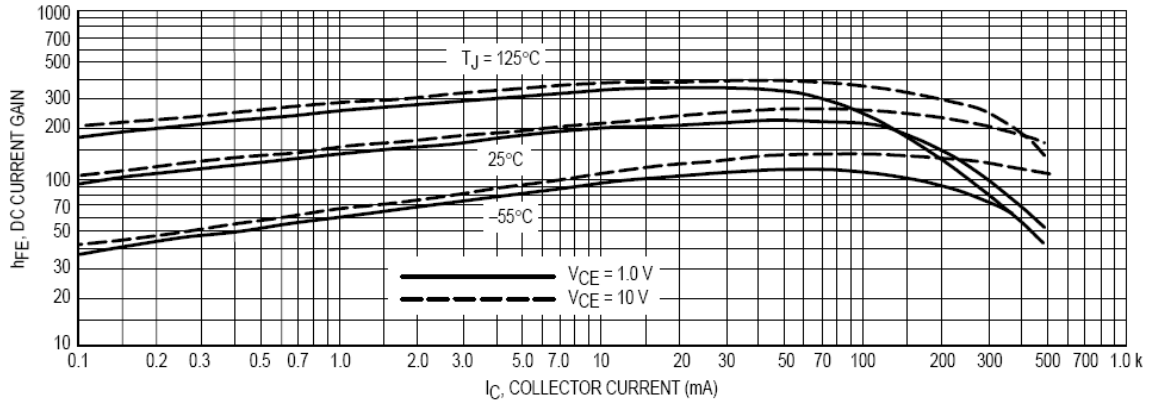


Figure 3. DC Current Gain

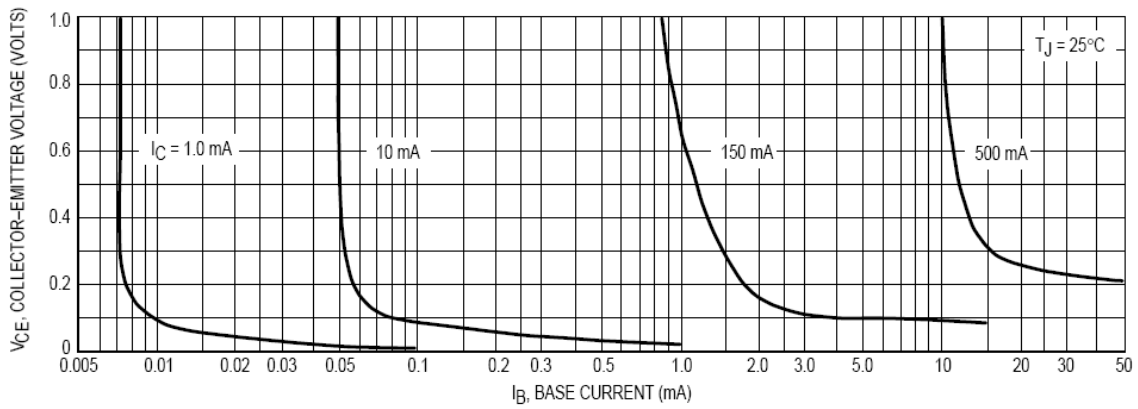


Figure 4. Collector Saturation Region



6-Pin DIP Random-Phase Optoisolators Triac Driver Output (250 Volts Peak)

The MOC3010 Series consists of gallium arsenide infrared emitting diodes, optically coupled to silicon bilateral switch and are designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 Vac peak), high detector standoff voltage, small size, and low cost.

- To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.

Recommended for 115 Vac(rms) Applications:

- Solenoid/Valve Controls
- Lamp Ballasts
- Interfacing Microprocessors to 115 Vac Peripherals
- Motor Controls
- Static ac Power Switch
- Solid State Relays
- Incandescent Lamp Dimmers

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
--------	--------	-------	------

INFRARED EMITTING DIODE

Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Negligible Power in Transistor Derate above 25°C	P_D	100	mW
		1.33	mW/ $^\circ\text{C}$

OUTPUT DRIVER

Off-State Output Terminal Voltage	V_{DRM}	250	Volts
Peak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300	mW
		4	mW/ $^\circ\text{C}$

TOTAL DEVICE

Isolation Surge Voltage ⁽¹⁾ (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	330	mW
		4.4	mW/ $^\circ\text{C}$
Junction Temperature Range	T_J	-40 to +100	$^\circ\text{C}$
Ambient Operating Temperature Range ⁽²⁾	T_A	-40 to +85	$^\circ\text{C}$
Storage Temperature Range ⁽²⁾	T_{stg}	-40 to +150	$^\circ\text{C}$
Soldering Temperature (10 s)	T_L	260	$^\circ\text{C}$

1. Isolation surge voltage, V_{ISO} , is an internal device dielectric breakdown rating.

For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.

GlobalOptoisolator is a trademark of Motorola, Inc.

(Replaces MOC3009/D)

MOC3010
[IFT = 15 mA Max]
MOC3011
[IFT = 10 mA Max]
MOC3012*
[IFT = 5 mA Max]

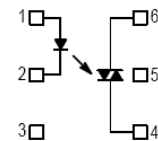
*Motorola Preferred Device

STYLE 6 PLASTIC



**STANDARD THRU HOLE
CASE 730A-04**

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
DO NOT CONNECT
6. MAIN TERMINAL

MOC3010 MOC3011 MOC3012

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT LED					
Reverse Leakage Current (V _R = 3 V)	I _R	—	0.05	100	μA
Forward Voltage (I _F = 10 mA)	V _F	—	1.15	1.5	Volts
OUTPUT DETECTOR (I_F = 0 unless otherwise noted)					
Peak Blocking Current, Either Direction (Rated V _{DRM} ⁽¹⁾)	I _{DRM}	—	10	100	nA
Peak On-State Voltage, Either Direction (I _{TM} = 100 mA Peak)	V _{TM}	—	1.8	3	Volts
Critical Rate of Rise of Off-State Voltage (Figure 7, Note 2)	dv/dt	—	10	—	V/μs
COUPLED					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V ⁽³⁾)	I _{FT}	—	8	15	mA
MOC3010	—	—	5	10	
MOC3011	—	—	3	5	
Holding Current, Either Direction	I _H	—	100	—	μA

1. Test voltage must be applied within dv/dt rating.
2. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.
3. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3010, 10 mA for MOC3011, 5 mA for MOC3012) and absolute max I_F (60 mA).

TYPICAL ELECTRICAL CHARACTERISTICS T_A = 25°C

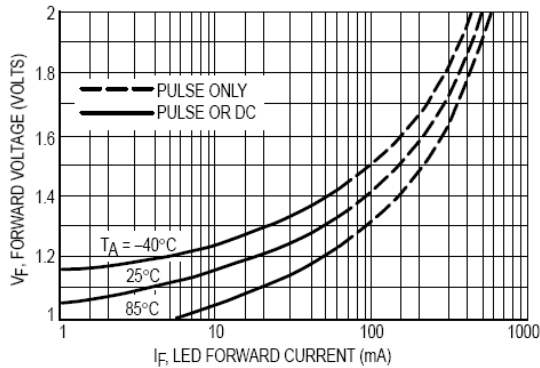


Figure 1. LED Forward Voltage versus Forward Current

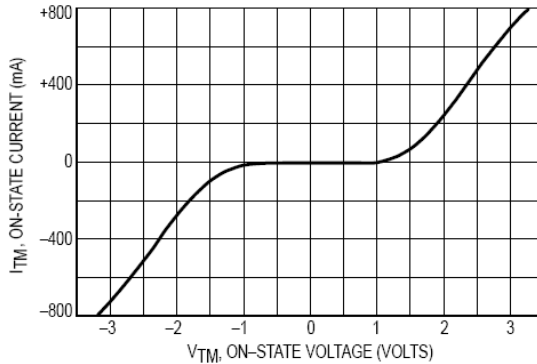


Figure 2. On-State Characteristics

1A, 100V, 0.600 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17441.

Ordering Information

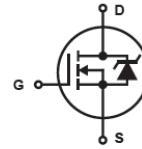
PART NUMBER	PACKAGE	BRAND
IRFD110	HEXDIP	IRFD110

NOTE: When ordering, use the entire part number.

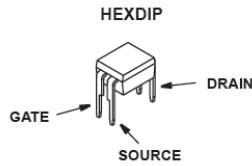
Features

- 1A, 100V
- $r_{DS(ON)} = 0.600\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging



IRFD110

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

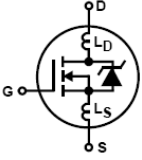
	IRFD110	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	100 V
Continuous Drain Current	I_D	1.0 A
Pulsed Drain Current (Note 3)	I_{DM}	8.0 A
Gate to Source Voltage	V_{GS}	± 20 V
Maximum Power Dissipation	P_D	1.0 W
Linear Derating Factor (See Figure 1)		0.008 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 3)	E_{AS}	19 mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 9)	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	1.0	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 0.8\text{A}, V_{GS} = 10\text{V}$ (Figures 7, 8)	-	0.5	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, I_D = 0.8\text{A}$ (Figure 11)	0.8	1.2	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 0.5 \times \text{Rated } BV_{DSS}, I_D \approx 1.0\text{A}, R_G = 9.1\Omega, R_L = 50\Omega$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	10	20	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	15	25	ns
Fall Time	t_f		-	10	20	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$		$V_{GS} = 10\text{V}, I_D \approx 1.0\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, I_{g(REF)} = 1.5\text{mA}$ (Figure 13) Gate Charge is Essentially Independent of Operating Temperature	-	5.0	7.0
Gate to Source Charge	Q_{gs}		-	2.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	3.0	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ (Figure 10)	-	135	-	pF
Output Capacitance	C_{OSS}		-	80	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Internal Drain Inductance	L_D	Measured from the Drain Lead, 2mm (0.08in) from Package to Center of Die	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 2mm (0.08in) from Header to Source Bonding Pad	-	6.0	-	nH
		Modified MOSFET Symbol Showing the Internal Device's Inductances 				
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	120	$^\circ\text{C/W}$

IRFD110

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	1.0	A
Pulse Source to Drain Current (Note 4)	I_{SDM}		-	-	8.0	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 1.0\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	100	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^\circ\text{C}$, $I_{SD} = 1.0\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	0.2	-	μC

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. $V_{DD} = 25\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 28.5\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 1.0\text{A}$.
4. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

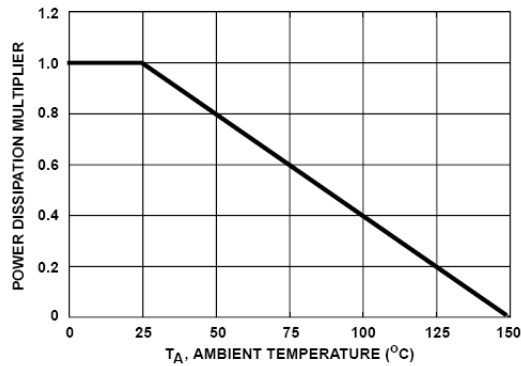


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

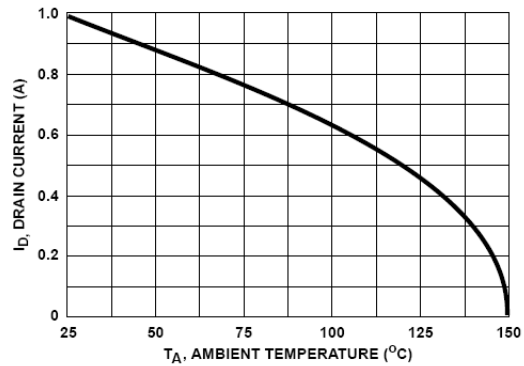


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

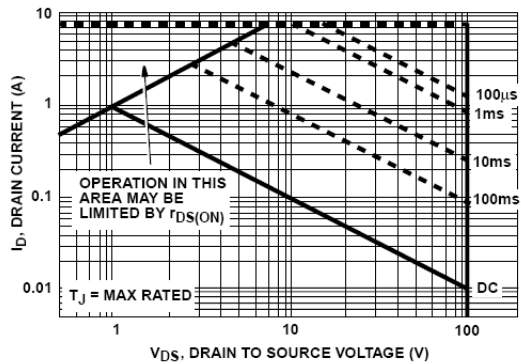


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

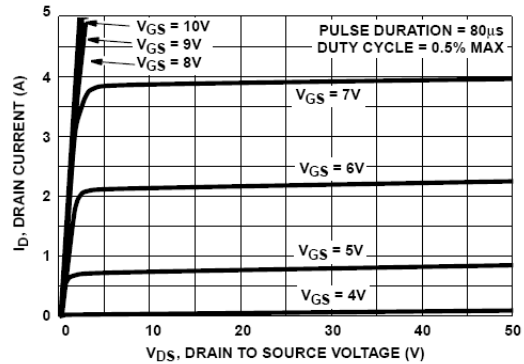


FIGURE 4. OUTPUT CHARACTERISTICS

Zener 1N4733A



1N4728A THRU 1N4764A
1W ZENER DIODE



FEATURES

- * 3.3 thru 100 volt voltage range
- * High surge current rating
- * Higher voltages available, see 1EZ series

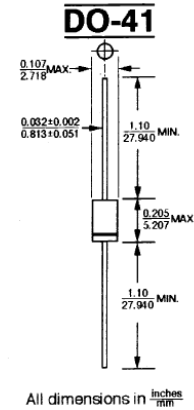
MECHANICAL CHARACTERISTICS

- * CASE: Molded encapsulation, axial lead package (DO - 41).
- * FINISH: Corrosion resistant. Leads are solderable.
- * THERMAL RESISTANCE: 45°C/Watt junction to lead at 0.375 inches from body.
- * POLARITY: banded end is cathode.
- * WEIGHT: 0.4 grams (Typical).

MAXIMUM RATINGS

Junction and Storage temperature: - 65°C to + 200°C
 DC Power Dissipation: 1 Watt
 Power Derating: 10mW/°C, from 100°C
 Forward Voltage @ 200mA: 1.2 Volts

VOLTAGE RANGE
3.3 to 100 Volts



* **ELECTRICAL CHARACTERISTICS @ 25°C**

JEDEC TYPE NUMBER (Note 1)	ZENER VOLTAGE (VZ) (Note 4)	TEST CURRENT IZT	MAXIMUM DYNAMIC IMPEDANCE ZZT @ IZT (Note 2)	MAXIMUM REVERSE CURRENT IR @ VR	TEST VOLTAGE (VR)	MAXIMUM REGULATOR CURRENT (IZM) @ TA = 50°C	MAXIMUM KNEE IMPEDANCE (Zzk @ Izk) (Note 2)	TEST CURRENT (Izk)	MAXIMUM (SURGE) CURRENT (IS) (Note 3)
	VOLTS	mA	OHMS	µA	VOLTS	mA	OHMS	mA	mA
1N4728A	3.3	76	10	100	1	276	400	1.0	1380
1N4728A	3.6	69	10	100	1	252	400	1.0	1250
1N4730A	3.9	64	9	50	1	234	400	1.0	1190
1N4731A	4.3	58	9	10	1	217	400	1.0	1070
1N4732A	4.7	53	8	10	1	193	500	1.0	970
1N4733A	5.1	49	7	10	1	178	550	1.0	890
1N4734A	5.6	45	5	10	2	162	600	1.0	810
1N4735A	6.2	41	2	10	3	146	700	1.0	730
1N4736A	6.8	37	3.5	10	4	133	700	1.0	660
1N4737A	7.5	34	4.0	10	5	121	700	0.5	605
1N4738A	8.2	31	4.5	10	6	110	700	0.5	560
1N4739A	9.1	28	5.0	10	7	100	700	0.5	500
1N4740A	10	25	7	10	7.6	91	700	0.25	454
1N4741A	11	23	8	5	8.4	83	700	0.25	414
1N4742A	12	21	9	5	9.1	76	700	0.25	380
1N4743A	13	19	10	5	9.9	69	700	0.25	344
1N4744A	15	17	14	5	11.4	61	700	0.25	304
1N4745A	16	15.5	16	5	12.2	57	700	0.25	285
1N4746A	18	14	20	5	13.7	50	750	0.25	250
1N4747A	20	12.5	22	5	15.2	45	750	0.25	225
1N4748A	22	11.5	23	5	16.7	41	750	0.25	205
1N4749A	24	10.5	25	5	18.2	38	750	0.25	190
1N4750A	27	9.5	35	5	20.6	34	750	0.25	170
1N4751A	30	8.5	40	5	22.8	30	1000	0.25	150
1N4752A	33	7.5	45	5	25.1	27	1000	0.25	135
1N4753A	36	7.0	50	5	27.4	25	1000	0.25	125
1N4754A	39	6.5	60	5	29.7	23	1000	0.25	115
1N4755A	43	6.0	70	5	32.7	22	1500	0.25	110
1N4756A	47	5.5	80	5	35.8	19	1500	0.25	95
1N4757A	51	5.0	96	5	38.8	18	1500	0.25	90
1N4758A	56	4.5	110	5	42.6	16	2000	0.25	80
1N4759A	62	4.0	125	5	47.1	14	2000	0.25	70
1N4760A	68	3.7	150	5	51.7	13	2000	0.25	65
1N4761A	75	3.3	175	5	56.0	12	2000	0.25	60
1N4762A	82	3.0	200	5	62.2	11	3000	0.25	55
1N4763A	91	2.8	250	5	69.2	10	3000	0.25	50
1N4764A	100	2.5	350	5	76.0	9	3000	0.25	45

NOTE 1 The JEDEC type numbers shown have a 5% tolerance on nominal zener voltage. No suffix signifies a 10% tolerance, C signifies 2%, and D signifies 1% tolerance.

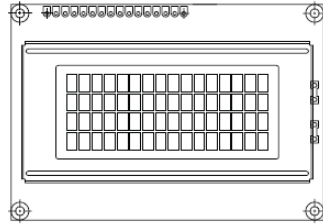
NOTE 2 The Zener impedance is derived from the 60 Hz ac voltage, which results when an ac current having an rms value equal to 10% of the DC Zener current (IZT or IZK) is superimposed on IZT or IZK. Zener impedance is measured at two points to insure a sharp knee on the breakdown curve and eliminate unstable units.

NOTE 3 The zener surge current is measured at 25°C ambient using a 1/2 square wave or equivalent sine wave pulse 1/120 second duration superimposed on IZT.

NOTE 4 Voltage measurements to be performed 90 seconds after application of DC current.



16 x 4 Character LCD



FEATURES

- 5 x 8 dots includes cursor
- Built-in controller (KS 0066 or Equivalent)
- + 5V power supply (Also available for + 3V)
- 1/16 duty cycle
- B/L to be driven by pin 1, pin 2 or pin 15, pin 16 or A and K (LED)
- N.V. optional for + 3V power supply

MECHANICAL DATA		
ITEM	STANDARD VALUE	UNIT
Module Dimension	87.0 x 60.0	mm
Viewing Area	62.0 x 26.0	mm
Dot Size	0.55 x 0.55	mm
Character Size	2.95 x 4.75	mm

ABSOLUTE MAXIMUM RATING					
ITEM	SYMBOL	STANDARD VALUE			UNIT
		MIN.	TYP.	MAX.	
Power Supply	VDD-VSS	- 0.3	-	7.0	V
Input Voltage	VI	- 0.3	-	VDD	V

NOTE: VSS = 0 Volt, VDD = 5.0 Volt

ELECTRICAL SPECIFICATIONS						
ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
Input Voltage	VDD	VDD = + 5V	4.7	5.0	5.3	V
		VDD = + 3V	2.7	3.0	5.3	V
Supply Current	IDD	VDD = + 5V	-	1.0	1.2	mA
Recommended LC Driving Voltage for Normal Temp. Version Module	VDD - V0	- 20 °C	5.0	5.1	5.7	V
		0 °C	4.6	4.8	5.2	
		25 °C	4.1	4.5	4.7	
		50 °C	3.9	4.2	4.5	
		70 °C	3.7	3.9	4.3	
LED Forward Voltage	VF	25 °C	-	4.2	4.6	V
LED Forward Current	IF	25 °C	-	220	440	mA
EL Power Supply Current	IEL	Vel = 110VAC:400Hz	-	-	5.0	mA

DISPLAY CHARACTER ADDRESS CODE:																
Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F
DD RAM Address	10	11														1F
DD RAM Address	50	51														5F



Intelligent Alphanumeric Application Notes

Character Position and Character Address

For each device, the relationship between character position and character address is straightforward. A hexadecimal code for each character position in each device is given in the following charts. Character positions are numbered from left to right beginning in the top left corner as you view the device from the front.

AND671

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

AND491, 481, 471

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Character Position	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

AND501

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Character Position	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

AND731

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Character Position	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM (Hex) Add.	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
Character Position	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	Character Position	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	DD RAM (Hex) Add.	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

AND771

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
Character Position	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57

AND591

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

AND721

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Character Position	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
DD RAM (Hex) Add.	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	6	62	63	64	65	66	67

AND791

Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67
Character Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
DD RAM (Hex) Add.	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0E	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
Character Position	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
DD RAM (Hex) Add.	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

Note: Address locations for Lines 1 & 2 are controlled by E1, and lines 3 & 4 are controlled by E2.



Timing

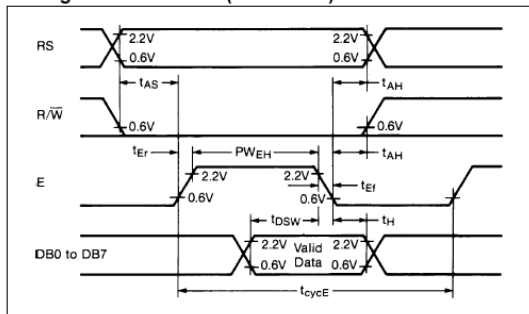
Timing Characteristics (TA = 25°C) Data Write

Item	Symbol	Value		Unit
		Min.	Max.	
Enable Cycle Time	t_{CYCE}	1000	-	
Enable Pulse Width	PW_{EH}	450		
Enable Rise/Fall Time	t_{Er}, t_{Ef}		25	
Set Up Time	t_{AS}	140		ns
Address Hold Time	t_{AH}	10		
Data Set Up Time	t_{DSW}	195		
Data Hold Time	t_H	10		

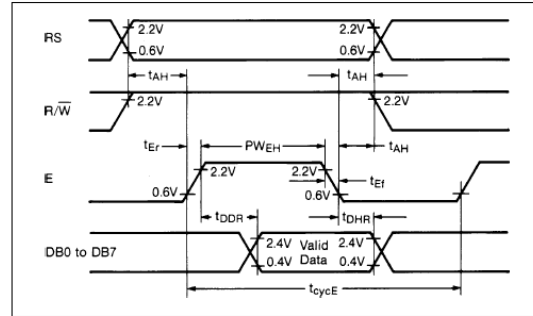
Data Read

Item	Symbol	Value		Unit
		Min.	Max.	
Enable Cycle Time	t_{CYCE}	1000		
Enable Pulse Width	PW_{EH}	450		
Enable Rise/Fall Time	t_{Er}, t_{Ef}		25	
Set Up Time	t_{AS}	140		ns
Address Hold Time	t_{AH}	10		
Data Delay Time	t_{DDR}		320	
Data Hold Time	t_{DHR}	20		

Timing Characteristics (Data Write)



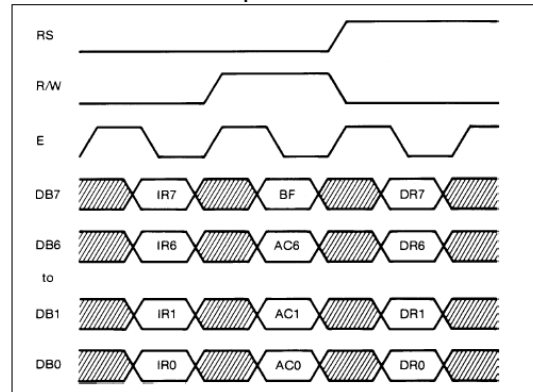
Timing Characteristics (Data Read)



Data Transfer Example

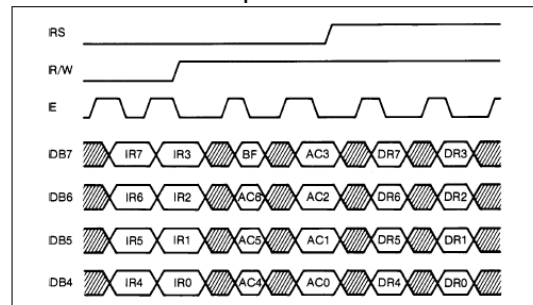
Data can be sent in either two cycles of 4-bit data or one cycle of 8-bit data, a scheme that suits 4-bit or 8-bit CPUs. Data that is 8-bits long is transferred using 8 data lines of DB0 to DB7.

8-Bit Data Transfer Example



Data that is 4 bits long is transferred by using only 4 lines of DB7 to DB4—DB3 to DB0 are not used. Data transfer between the module and a 4-bit CPU is completed when the high order 4 bits are transferred first, followed by the low order 4 bits.

4-Bit Data Transfer Example





Intelligent Alphanumeric Application Notes

Command List

Command	Command Code										Description	Execution Time (Max.) ⁽¹⁾	Execution Time (Max.) ⁽²⁾
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display ⁽³⁾	0	0	0	0	0	0	0	0	0	1	Clear display and return cursor to home position (Address 0).	1.64ms	4.9ms
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home position (Address 0). Also return display being shifted to original position. DD RAM contents remain the same.	1.64ms	4.8ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Set cursor move direction and specify whether to shift display. These operations are performed during data write.	40μs	120μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set ON/OFF of entire display (D), dresser ON/OFF (C), and blinking of cursor position B	40μs	120μs
Cursor and Display Shift ⁽⁴⁾	0	0	0	0	0	1	S/C	R/L	X	X	Move cursor and shift display without changing DD RAM contents.	40μs	120μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL) number of display lines (L) and character font (F).	40μs	120μs
Set RAM Address	0	0	0	1	ACG						Set CG RAM address, CG RAM data is sent and received after this setting.	40μs	120μs
Set DD RAM Address	0	0	1	ADD						Set DD RAM address, DD RAM data is sent and received after this setting.	40μs	120μs	
Read Busy Flag & Address	0	1	BF	AC						Read Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μs	120μs	
Write Data to CG or DD RAM	1	0	Write Data						Write Data from DD RAM or CG RAM.	40μs	120μs		
Read Data to CG or DD RAM	1	1	Read Data						Read Data from DD RAM or CG RAM.	40μs	120μs		
	I/D = 1 : Increment I/D = 0 Decrement S = 1 : Accompanies display shift S/C = 1 : Display shift S/C = 0 Cursor move R/L = 1 : Shift to the right R/L = 0 : Shift to the left DL = 1 : 8 bits DL = 0: 4 bits N = 1 : 2 lines N = 0: 1 line F = 1 : 5 x 10 dots F = 0: 5 x 7 dots BF = 1 : Internally operating BF = 0 : Can accept instruction										DD RAM : Display Data RAM CG RAM : Character Gen RAM ACG : CG RAM Address ADD : DD RAM Address corresponds to Cursor Address AC : Address Counter used for DD and CG RAM Address.		

X = Don't Care

Notes:

1. Applies to AND491, AND481, AND491, and AND501.
2. Applies to AND591, AND731, AND721, AND771.
3. The repeat time interval of command Clear Display must be 13ms minimum (5 x 7 dot font) and 18ms minimum (5 x 10 dot font).
4. Commands "Cursor and Display Shift" are invalid for the AND671.



Function of Registers

The following paragraphs describe the function of the registers.

Instruction Register and Data Register

The built-in controller has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The IR stores commands such as display clear and cursor shift, or address information of display data RAM (DD RAM), and character generator RAM (CG RAM). The IR can be written to by a CPU, but a CPU cannot read this register.

The DR temporarily stores data to be written into the DD RAM or the CG RAM. Data written into the DR is automatically sent to the DD RAM or the CG RAM as an internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is transferred to the DR from the DD RAM or the CG RAM as an internal operation. Then, the CPU reads the DR and data transfer is completed. After the CPU reads the DR, data of the DD RAM or the CG RAM at the next address is sent to DR for the next reading. Register Selector (RS) signals select these two registers.

Register Selection

RS	R/W	Operation	Enable (E)
0	0	Write commands to IR.	
0	1	Read of a Busy Flag (DB7) and Address Counter (DB0 to DB6)	
1	0	DR Write as internal operations (DR → DD or CG RAM)	
1	1	DR Read as internal operations (DD or CG RAM → DR)	

Busy Flag (BF)

When the Busy Flag is "1", the LCD module is in the internal operation mode, and the next instruction is not accepted at this time. As shown in the "Command List" on page 5 of this section, the Busy Flag is shown in DB7 when RS = 0 and R/W = 1. The next instruction must be written after checking that the Busy Flag is "0".

Address Counter (AC)

The address counter (AC) assigns DD and CG RAM address. When an instruction for address setting is written in IR, the address information is sent from IR to AC.

Selection of either the DD or CG RAM is also determined by an instruction. After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by 1 (or decremented by 1). Data in address counters (AC) are in DB6 to DBO when RS = 0 and R/W = 1, as shown in the table entitled "Command List" on page 5 of this section.

Display Data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. The relationship between the DD RAM address and display position on the LCD Display is described by a series of tables under the paragraph "Character Position and Character Address" on page 3 of this section.

Commands

The command code is the signal through which the LCD module is accessed through the CPU. The LCD module begins operation upon receipt of the code input. Because the internal processing operation of the LCD module is started with a timing that does not affect the LCD display, the busy status continues longer than the CPU cycle time.

Under the busy status (when the busy flag is set to "1"), the LCD module does not execute any commands other than the busy flag read. Accordingly, the CPU has to verify that the busy flag is set to "0" prior to the input of the command code.

Clear Display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Write space code "20" (hexadecimal) into all the DD RAM addresses. The cursor returns to address "0" (DD RAM Address = "00H") and the display, if it has been shifted, returns to the original position. In other words, the display disappears and the cursor goes to the left edge of the first line.

Return Home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Return the cursor to character position 1 (DD RAM Address = "00H") and returns the display to the original position if it has been shifted (S in the instruction register is 1). The DD RAM contents remain unchanged.

X = Don't care

Entry Mode Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increment (I/D = 1) or decrement (I/D = 0) the DD RAM address by one upon writing a character code into the DD RAM or reading a character code from the DD RAM. The cursor moves to the right when I/D = 1, and to the left when I/D = 0.

S: When writing to the DD RAM, shift the entire display to the right (when I/D = 0, S = 1) or to the left (when I/D = 1, S = 1). Therefore, the cursor looks as if it stood still and only the display moves. Display is not shifted when reading from the DD RAM. Display is not shifted when S = 0.



Intelligent Alphanumeric Application Notes

Display ON/OFF Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

- D: Display is turned ON when D = 1 and OFF when D = 0. When display is turned off due to D = 0, the display data remains in the DD RAM and they can be displayed immediately by setting D = 1.
- C: The cursor is displayed when C = 1 and not displayed when C = 0. Even if the cursor disappears, the function of I/D does not change during "display data write." The cursor is displayed at the 8th line when the 5 x 7 dots character font is selected.
- B: The character at the cursor position blinks when B = 1. The blink is done by switching between all black dots and display characters at 0.4 second interval. The cursor and the blink can be set concurrently.

Cursor or Display Shift

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

Shift the cursor position or display position to the right or the left without writing or reading the display data. This function can be used for correction or search of display.

S/C	R/L	Function
0	0	Shift the cursor position to the left. (AC is decremented by one.)
0	1	Shift the cursor position to the right. (AC is incremented by one.)
1	0	Shift the entire display to the left. The cursor follows the display shift.
1	1	Shift the entire display to the right. The Cursor follows the display shift.

Function Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

- DL: Sets the interface data length. Data is sent or received in 8-bit length (DB7 to DB0) when DL = 1 and 4-bit length (DB7 to DB4) when DL = 0. When 4-bit length is selected, data must be sent or received in two cycles.
- N: Set number of display lines.
- F: Set character font. The 5 x 7 dots character font is selected when F = 0. While 5 x 10 dots character font is selected when F = 1 and N = 0.

Module Type Number

N	F	No. of Display Lines	Character Font	Duty Ratio	AND Model No.
1	0	2	5 x 7 Dots	1/16	AND471, AND481, AND491, AND501, AND591, AND671, AND771
1	0	4	5 x 7 Dots	1/16	AND721, AND731, AND791

Set CG RAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	A	A	A	A	A	A

Set the CG RAM address to a binary number of AAAAAA in the address counter. After execution of this instruction, all the data from MPU is written into the CG RAM and all the data is read from CG RAM.

Set DD RAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	An	A	A	A	A	A	A

Set the DD RAM address to a binary number of AnAAAAA in the address counter (An = 0 for the first line, An = 1 for the second line). After execution of this instruction, all the data from MPU is written into the DD RAM and all the data is read from DD RAM.

Read Busy Flag and Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	091	DB0
Code	0	1	BF	A	A	A	A	A	A	A

Read Busy Flag (BF) and the value of the address counter (AAAAAA). The condition BF = 1 indicates that an internal operation is going on and the next command is not accepted until BF becomes "0." You must check the BF status before the next write operation. The address counter generates the CG or DD RAM address.

Write Data to CG RAM or DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	D	D	D	D	D	D	D	D	D

Write binary 8-bit data DDDDDDDD to the CG RAM or the DD RAM. Whether the CG RAM or the DD RAM is to be written is determined by the previous designation (CG RAM address setting or DD RAM address setting). After writing, the address is automatically incremented or decremented by one according to entry mode. Display shift also follows the entry mode.



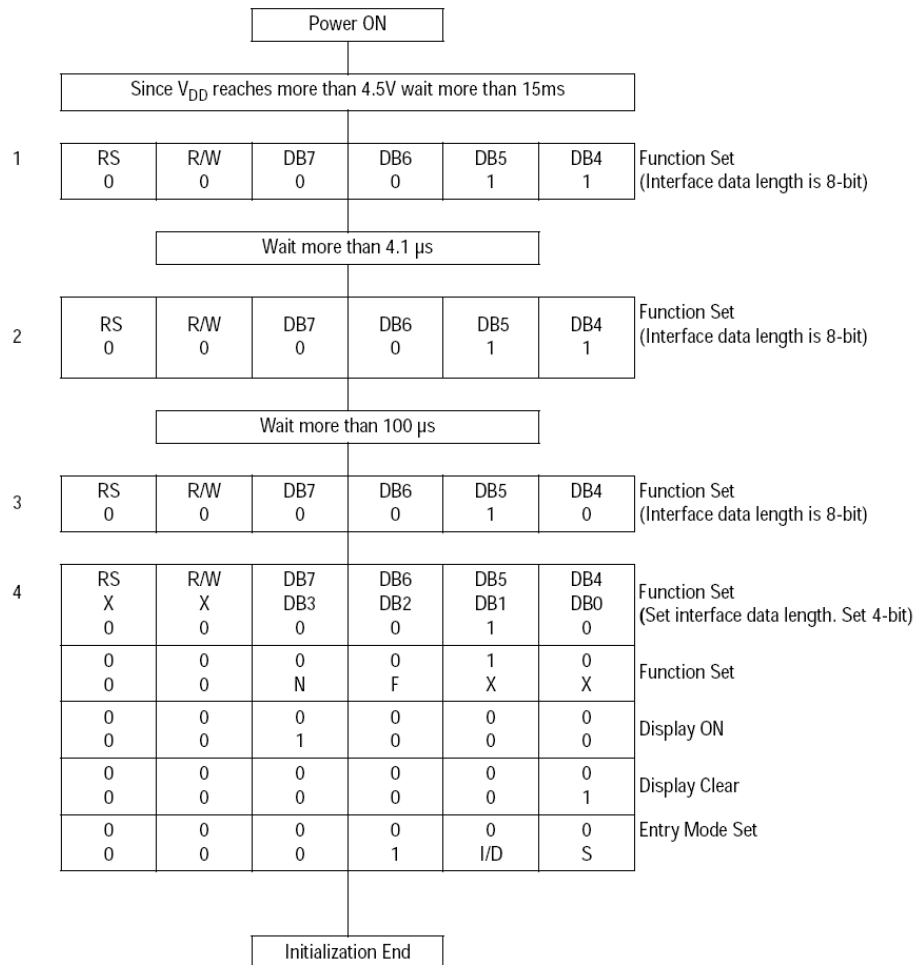
Character Pattern and Character Code

Upper 4 bit Lower 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
XXXX0000	CG RAM (1)		0	a	P	\	P	-	9	3	0	p	
XXXX0001	(2)	!	1	0	a	4	7	7	4	a	q		
XXXX0010	(3)	"	2	R	b	r	"	4	W	x	p	0	
XXXX0011	(4)	#	3	C	S	c	s	.	7	t	e	e	*
XXXX0100	(5)	\$	4	O	T	d	t	.	I	k	t	p	a
XXXX0101	(6)	%	5	E	U	e	u	.	7	+	1	e	0
XXXX0110	(7)	&	6	F	V	f	v	9	n	c	a	p	z
XXXX0111	(8)	'	7	G	W	g	w	7	+	7	9	g	n
XXXX1000	(1)	<	8	H	X	h	x	4	7	+	7	7	7
XXXX1001	(2)	>	9	I	Y	i	y	7	+	7	7	7	7
XXXX1010	(3)	*	:	J	Z	j	z	7	+	7	7	7	7
XXXX1011	(4)	+	:	K	L	k	l	7	+	7	7	7	7
XXXX1100	(5)	,	<	L	*	l	7	+	7	7	7	7	7
XXXX1101	(6)	-	=	M	I	m	i	7	+	7	7	7	7
XXXX1110	(7)	.	>	N	^	n	7	+	7	7	7	7	7
XXXX1111	(8)	/	?	O	_	o	7	+	7	7	7	7	7



Manual Initialization Procedure

The following diagram applies when the interface data length is 4-bits.



X = Don't care

Notes:

1. Before initialize step 1, 2, and 3, cannot check busy flag.
2. After initialize step 4, cannot change function set mode, number of display lines and character font.



PIC18FXX2

28/40-pin High Performance, Enhanced FLASH Microcontrollers with 10-Bit A/D

High Performance RISC CPU:

- C compiler optimized architecture/instruction set
 - Source code compatible with the PIC16 and PIC17 instruction sets
- Linear program memory addressing to 32 Kbytes
- Linear data memory addressing to 1.5 Kbytes

Device	On-Chip Program Memory		On-Chip RAM (bytes)	Data EEPROM (bytes)
	FLASH (bytes)	# Single Word Instructions		
PIC18F242	16K	8192	768	256
PIC18F252	32K	16384	1536	256
PIC18F442	16K	8192	768	256
PIC18F452	32K	16384	1536	256

- Up to 10 MIPs operation:
 - DC - 40 MHz osc./clock input
 - 4 MHz - 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier

Peripheral Features:

- High current sink/source 25 mA/25 mA
- Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter with 8-bit period register (time-base for PWM)
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option - Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules. CCP pins that can be configured as:
 - Capture input: capture is 16-bit, max. resolution 6.25 ns ($T_{CY}/16$)
 - Compare is 16-bit, max. resolution 100 ns (T_{CY})
 - PWM output: PWM resolution is 1- to 10-bit, max. PWM freq. @: 8-bit resolution = 156 kHz
10-bit resolution = 39 kHz
- Master Synchronous Serial Port (MSSP) module, Two modes of operation:
 - 3-wire SPI™ (supports all 4 SPI modes)
 - I²C™ Master and Slave mode

Peripheral Features (Continued):

- Addressable USART module:
 - Supports RS-485 and RS-232
- Parallel Slave Port (PSP) module

Analog Features:

- Compatible 10-bit Analog-to-Digital Converter module (A/D) with:
 - Fast sampling rate
 - Conversion available during SLEEP
 - Linearity ≤ 1 LSb
- Programmable Low Voltage Detection (PLVD)
 - Supports interrupt on-Low Voltage Detection
- Programmable Brown-out Reset (BOR)

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced FLASH program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory
- FLASH/Data EEPROM Retention: > 40 years
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options including:
 - 4X Phase Lock Loop (of primary oscillator)
 - Secondary Oscillator (32 kHz) clock input
- Single supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins

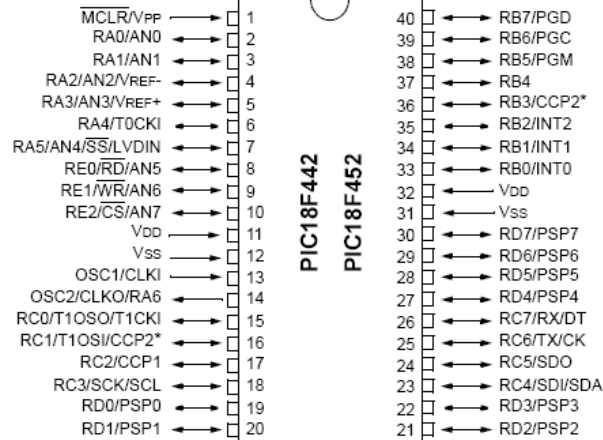
CMOS Technology:

- Low power, high speed FLASH/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption:
 - < 1.6 mA typical @ 5V, 4 MHz
 - 25 μ A typical @ 3V, 32 kHz
 - < 0.2 μ A typical standby current

PIC18FXX2

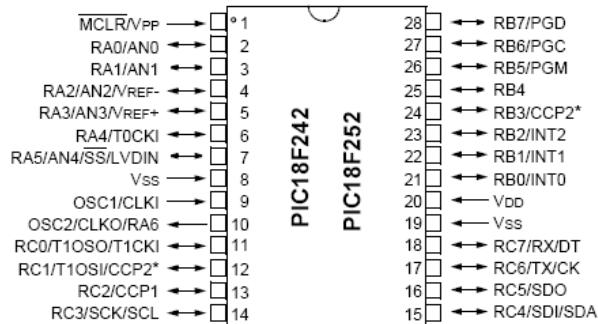
Pin Diagrams (Cont.'d)

DIP



Note: Pin compatible with 40-pin PIC16C7X devices.

DIP, SOIC



* RB3 is the alternate pin for the CCP2 pin multiplexing.

PIC18FXX2

1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F242
- PIC18F252
- PIC18F442
- PIC18F452

These devices come in 28-pin and 40/44-pin packages. The 28-pin devices do not have a Parallel Slave Port (PSP) implemented and the number of Analog-to-Digital (A/D) converter input channels is reduced to 5. An overview of features is shown in Table 1-1.

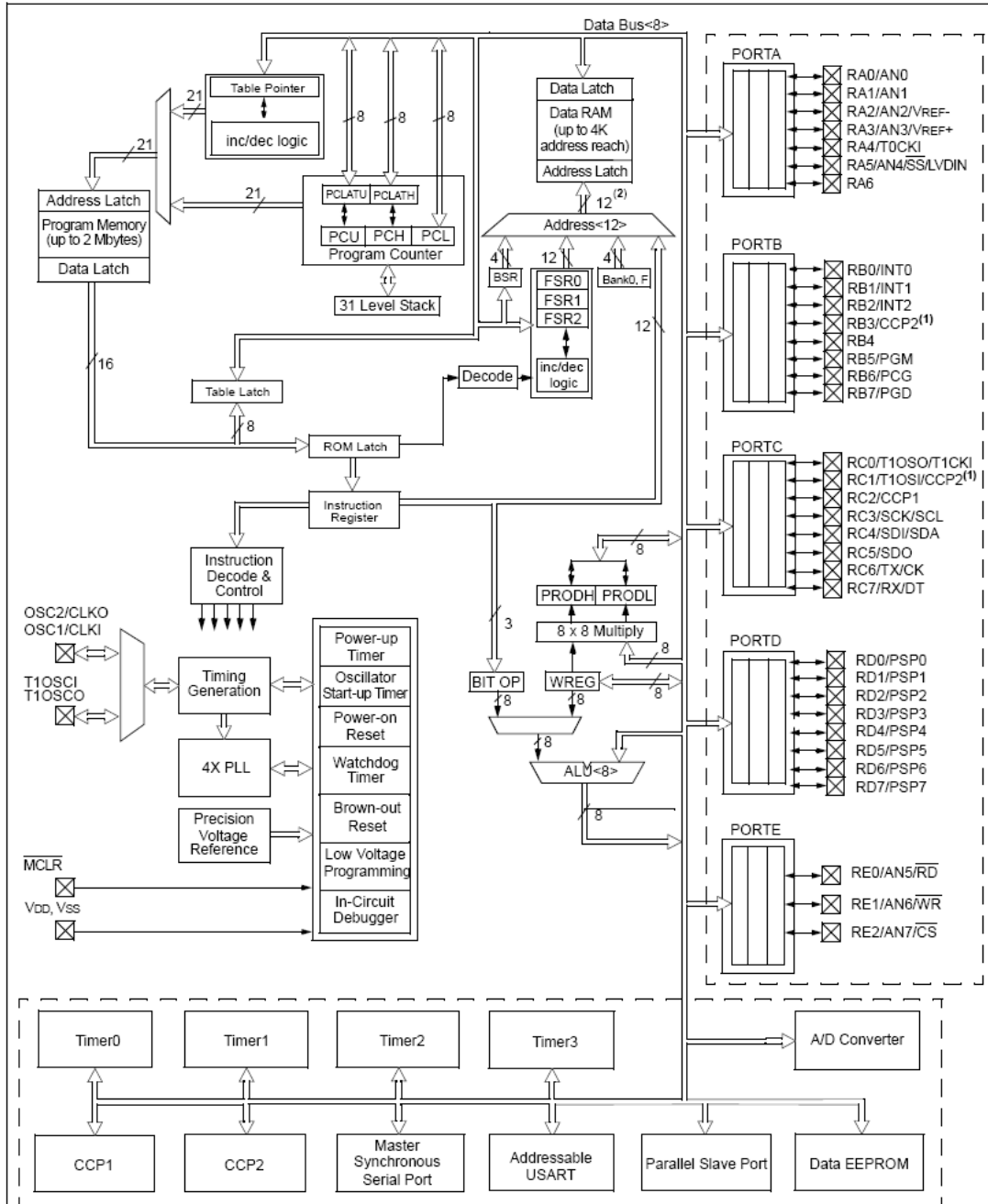
The following two figures are device block diagrams sorted by pin count: 28-pin for Figure 1-1 and 40/44-pin for Figure 1-2. The 28-pin and 40/44-pin pinouts are listed in Table 1-2 and Table 1-3, respectively.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F242	PIC18F252	PIC18F442	PIC18F452
Operating Frequency	DC - 40 MHz	DC - 40 MHz	DC - 40 MHz	DC - 40 MHz
Program Memory (Bytes)	16K	32K	16K	32K
Program Memory (Instructions)	8192	16384	8192	16384
Data Memory (Bytes)	768	1536	768	1536
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	17	17	18	18
I/O Ports	Ports A, B, C	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART
Parallel Communications	—	—	PSP	PSP
10-bit Analog-to-Digital Module	5 input channels	5 input channels	8 input channels	8 input channels
RESETS (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)
Programmable Low Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions	75 Instructions	75 Instructions	75 Instructions
Packages	28-pin DIP 28-pin SOIC	28-pin DIP 28-pin SOIC	40-pin DIP 44-pin PLCC 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin TQFP

PIC18FXX2

FIGURE 1-2: PIC18F4X2 BLOCK DIAGRAM



- Note**
- 1: Optional multiplexing of CCP2 input/output with RB3 is enabled by selection of configuration bit.
 - 2: The high order bits of the Direct Address for the RAM are from the BSR register (except for the `MOVWF` instruction).
 - 3: Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations are device dependent.

PIC18FXX2

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	PLCC	TQFP			
MCLR/VPP	1	2	18			Master Clear (input) or high voltage ICSP programming enable pin. Master Clear (Reset) input. This pin is an active low RESET to the device. High voltage ICSP programming enable pin.
$\overline{\text{MCLR}}$				I	ST	
VPP				I	ST	
NC	—			—	—	These pins should be left unconnected.
OSC1/CLKI OSC1	13	14	30	I	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
CLKI				I	CMOS	
OSC2/CLKO/RA6 OSC2	14	15	31	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General Purpose I/O pin.
CLKO				O	—	
RA6				I/O	TTL	
RA0/AN0 RA0 AN0	2	3	19	I/O I	TTL Analog	PORTA is a bi-directional I/O port. Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	4	20	I/O I	TTL Analog	
RA2/AN2/VREF- RA2 AN2 VREF-	4	5	21	I/O I I	TTL Analog Analog	Digital I/O. Analog input 2. A/D Reference Voltage (Low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	6	22	I/O I I	TTL Analog Analog	
RA4/T0CKI RA4 T0CKI	6	7	23	I/O I	ST/OD ST	Digital I/O. Open drain when configured as output. Timer0 external clock input.
RA5/AN4/ $\overline{\text{SS}}$ /LVDIN RA5 AN4 $\overline{\text{SS}}$ LVDIN	7	8	24	I/O I I I	TTL Analog ST Analog	Digital I/O. Analog input 4. SPI Slave Select input. Low Voltage Detect Input. (See the OSC2/CLKO/RA6 pin.)
RA6						

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
OD = Open Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
I = Input
P = Power

PIC18FXX2

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	PLCC	TQFP			
RB0/INT0 RB0 INT0	33	36	8	I/O I	TTL ST	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External Interrupt 0.
RB1/INT1 RB1 INT1	34	37	9	I/O I	TTL ST	External Interrupt 1.
RB2/INT2 RB2 INT2	35	38	10	I/O I	TTL ST	Digital I/O. External Interrupt 2.
RB3/CCP2 RB3 CCP2	36	39	11	I/O I/O	TTL ST	Digital I/O. Capture2 input, Compare2 output, PWM2 output.
RB4	37	41	14	I/O	TTL	Digital I/O. Interrupt-on-change pin.
RB5/PGM RB5 PGM	38	42	15	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. Low Voltage ICSP programming enable pin.
RB6/PGC RB6 PGC	39	43	16	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/PGD RB7 PGD	40	44	17	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 O = Output
 OD = Open Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
 I = Input
 P = Power

PIC18FXX2

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	PLCC	TQFP			
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	PORTC is a bi-directional I/O port. Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC0				O	—	
T1OSO				I	ST	
T1CKI						
RC1/T1OSI/CCP2	16	18	35	I/O	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC1				I	CMOS	
T1OSI CCP2				I/O	ST	
RC2/CCP1	17	19	36	I/O	ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.
RC2				I/O	ST	
CCP1						
RC3/SCK/SCL	18	20	37	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode.
RC3				I/O	ST	
SCK						
SCL				I/O	ST	
RC4/SDI/SDA	23	25	42	I/O	ST	Digital I/O. SPI Data In. I ² C Data I/O.
RC4				I	ST	
SDI SDA				I/O	ST	
RC5/SDO	24	26	43	I/O	ST	Digital I/O. SPI Data Out.
RC5				O	—	
RC6/TX/CK	25	27	44	I/O	ST	Digital I/O. USART Asynchronous Transmit. USART Synchronous Clock (see related RX/DT).
RC6				O	—	
TX CK				I/O	ST	
RC7/RX/DT	26	29	1	I/O	ST	Digital I/O. USART Asynchronous Receive. USART Synchronous Data (see related TX/CK).
RC7				I	ST	
RX DT				I/O	ST	

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 O = Output
 OD = Open Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
 I = Input
 P = Power



MICROCHIP 24AA256/24LC256/24FC256

256K I²C™ CMOS Serial EEPROM

Device Selection Table

Part Number	VCC Range	Max. Clock Frequency	Temp. Ranges
24AA256	1.8-5.5V	400 kHz ⁽¹⁾	I
24LC256	2.5-5.5V	400 kHz	I, E
24FC256	1.8-5.5V	1 MHz ⁽²⁾	I

Note 1: 100 kHz for VCC < 2.5V.
Note 2: 400 kHz for VCC < 2.5V.

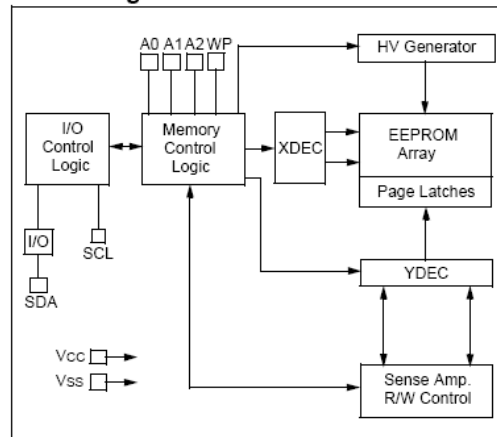
Features:

- Low-power CMOS technology:
 - Maximum write current 3 mA at 5.5V
 - Maximum read current 400 µA at 5.5V
 - Standby current 100 nA, typical at 5.5V
- 2-wire serial interface bus, I²C™ compatible
- Cascadable for up to eight devices
- Self-timed erase/write cycle
- 64-byte Page Write mode available
- 5 ms max. write cycle time
- Hardware write-protect for entire array
- Output slope control to eliminate ground bounce
- Schmitt Trigger inputs for noise suppression
- 1,000,000 erase/write cycles
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP, SOIC, TSSOP, MSOP and DFN packages, 14-lead TSSOP package
- Pb-free finishes available
- Temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

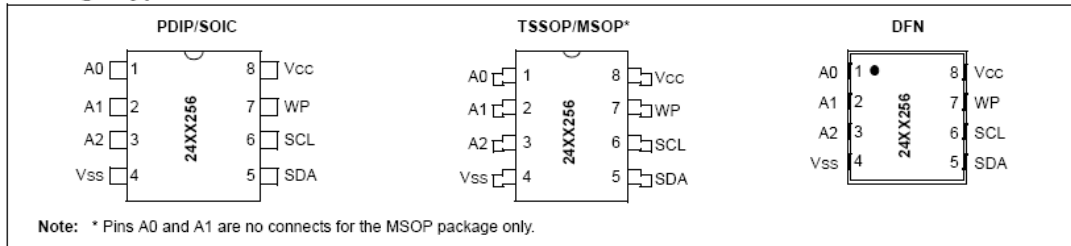
Description:

The Microchip Technology Inc. 24AA256/24LC256/24FC256 (24XX256*) is a 32K x 8 (256 Kbit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.8V to 5.5V). It has been developed for advanced, low-power applications such as personal communications or data acquisition. This device also has a page write capability of up to 64 bytes of data. This device is capable of both random and sequential reads up to the 256K boundary. Functional address lines allow up to eight devices on the same bus, for up to 2 Mbit address space. This device is available in the standard 8-pin plastic DIP, SOIC, TSSOP, MSOP and DFN packages.

Block Diagram



Package Types



*24XX256 is used in this document as a generic part number for the 24AA256/24LC256/24FC256 devices.

24AA256/24LC256/24FC256

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature.....	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins.....	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics:			
			Industrial (I): V _{CC} = +1.8V to 5.5V		T _A = -40°C to +85°C	
			Automotive (E): V _{CC} = +2.5V to 5.5V		T _A = -40°C to +125°C	
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Conditions
D1	—	A0, A1, A2, SCL, SDA and WP pins:	—	—	—	—
D2	V _{IH}	High-level input voltage	0.7 V _{CC}	—	V	—
D3	V _{IL}	Low-level input voltage	—	0.3 V _{CC} 0.2 V _{CC}	V V	V _{CC} ≥ 2.5V V _{CC} < 2.5V
D4	V _{HYS}	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 V _{CC}	—	V	V _{CC} ≥ 2.5V (Note)
D5	V _{OL}	Low-level output voltage	—	0.40	V	I _{OL} = 3.0 ma @ V _{CC} = 4.5V I _{OL} = 2.1 ma @ V _{CC} = 2.5V
D6	I _{LI}	Input leakage current	—	±1	μA	V _{IN} = V _{SS} or V _{CC} , WP = V _{SS} V _{IN} = V _{SS} or V _{CC} , WP = V _{CC}
D7	I _{LO}	Output leakage current	—	±1	μA	V _{OUT} = V _{SS} or V _{CC}
D8	C _{IN} , C _{OUT}	Pin capacitance (all inputs/outputs)	—	10	pF	V _{CC} = 5.0V (Note) T _A = 25°C, F _{CLK} = 1 MHz
D9	I _{CC} Read	Operating current	—	400	μA	V _{CC} = 5.5V, SCL = 400 kHz
	I _{CC} Write		—	3	mA	V _{CC} = 5.5V
D10	I _{CCS}	Standby current	—	1	μA	T _A = -40°C to +85°C SCL = SDA = V _{CC} = 5.5V A0, A1, A2, WP = V _{SS}
			—	5	μA	T _A = -40°C to +125°C SCL = SDA = V _{CC} = 5.5V A0, A1, A2, WP = V _{SS}

Note: This parameter is periodically sampled and not 100% tested.



DS1307 64 X 8 Serial Real Time Clock

www.dalsemi.com

FEATURES

- Real time clock counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 56 byte nonvolatile RAM for data storage
- 2-wire serial interface
- Programmable squarewave output signal
- Automatic power-fail detect and switch circuitry
- Consumes less than 500 nA in battery backup mode with oscillator running
- Optional industrial temperature range -40°C to +85°C
- Available in 8-pin DIP or SOIC
- Recognized by Underwriters Laboratory

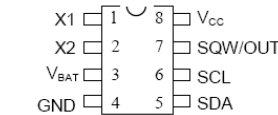
ORDERING INFORMATION

DS1307	8-Pin DIP
DS1307Z	8-Pin SOIC (150 mil)
DS1307N	8-Pin DIP (Industrial)
DS1307ZN	8-Pin SOIC (Industrial)

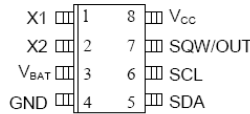
DESCRIPTION

The DS1307 Serial Real Time Clock is a low power, full BCD clock/calendar plus 56 bytes of nonvolatile SRAM. Address and data are transferred serially via a 2-wire bi-directional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1307 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply.

PIN ASSIGNMENT



DS1307 8-Pin DIP (300 mil)



DS1307Z 8-Pin SOIC (150 mil)

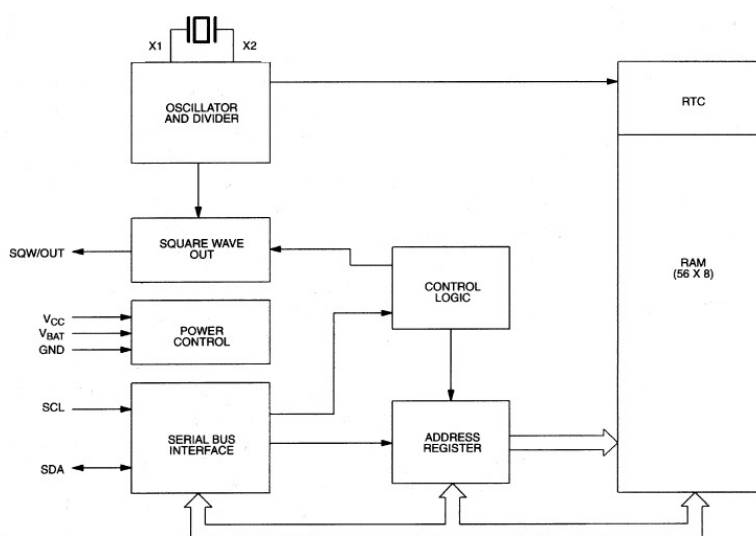
PIN DESCRIPTION

V _{CC}	- Primary Power Supply
X1, X2	- 32.768 kHz Crystal Connection
V _{BAT}	- +3V Battery Input
GND	- Ground
SDA	- Serial Data
SCL	- Serial Clock
SQW/OUT	- Square wave/Output Driver

OPERATION

The DS1307 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When V_{CC} falls below $1.25 \times V_{BAT}$ the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device switches into a low current battery backup mode. Upon power up, the device switches from battery to V_{CC} when V_{CC} is greater than $V_{BAT} + 0.2V$ and recognizes inputs when V_{CC} is greater than $1.25 \times V_{BAT}$. The block diagram in Figure 1 shows the main elements of the Serial Real Time Clock.

DS1307 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC} , **GND** - DC power is provided to the device on these pins. V_{CC} is the +5 volt input. When 5 volts is applied within normal limits, the device is fully accessible and data can be written and read. When a 3-volt battery is connected to the device and V_{CC} is below $1.25 \times V_{BAT}$, reads and writes are inhibited. However, the Timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{BAT} the RAM and timekeeper are switched over to the external power supply (nominal 3.0V DC) at V_{BAT} .

V_{BAT} - Battery input for any standard 3-volt lithium cell or other energy source. Battery voltage must be held between 2.0 and 3.5 volts for proper operation. The nominal write protect trip point voltage at which access to the real time clock and user RAM is denied is set by the internal circuitry as $1.25 \times V_{BAT}$ nominal. A lithium battery with 48 mAh or greater will back up the DS1307 for more than 10 years in the absence of power at 25 degrees C.

SCL (Serial Clock Input) - SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) - SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open drain which requires an external pullup resistor.

SQW/OUT (Square Wave/ Output Driver) - When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square wave frequencies (1 Hz, 4 kHz, 8 kHz, 32 kHz). The SQW/OUT pin is open drain which requires an external pullup resistor. SQW/OUT will operate with either Vcc or Vbat applied.

X1, X2 - Connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5 pF.

For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks." The DS1307 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

Please review Application Note 95, "Interfacing the DS1307 with a 8051-Compatible Microcontroller" for additional information.

RTC AND RAM ADDRESS MAP

The address map for the RTC and RAM registers of the DS1307 is shown in Figure 2. The real time clock registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multi-byte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

DS1307 ADDRESS MAP Figure 2

00H	SECONDS
	MINUTES
	HOURS
	DAY
	DATE
	MONTH
	YEAR
07H	CONTROL
08H	RAM
3FH	56 x 8

Acronimos

ACK	A cknowledgement
ADC	A nalog-to- D igital Converter
ALU	A rithmetic L ogic U nit
ASCII	A merican S tandard C ode for I nformation I nterchange
BCD	B inary- C oded D ecima
CAN	C ontroller A rea N etwork
CCP	C apture- C ompare and P wm M ode
CI	C ircuito I ntegrado
CISC	C ompleted I nstruction S et C omputer
CPU	C entral P rocessing U nit
DCOM	D istributed C omponent O bject M odel
DNA	D eoxyribo N ucleic A cid
EEPROM	E lectrically E rasable P rogrammable R ead O nly M emory
FPGA	F ield P rogrammable G ate A rray
GFP	G reen F luorescent P rotein
GPR	G eneral P urpose R egisters
IDE	I ntegrated D evelopment E nviroment
ISR	I nterrupt S ervice R outine
I ² C	I nter- I ntegrated C ircuit
LCD	L iquid C ristal D isplay
LVD	L ow V oltage D etection
MSSP	M aster S ynchronous S erial P ort
μC	M icro C ontrolador
PCB	P rinted C ircuit B oard
PIC	P eripheral I nterface C ontroller
POR	P ower- O n R eset
PSP	P arallel S lave P ort
PWRT	P ower-up T imer
PWM	P ulse- W idth M odulation
RAM	R andom A ccess M emory
ROM	R ead- O nly M emory
RISC	R educed I nstruction S et C omputer
RTC	R eal T ime C lock
SQW	S quare W ave
SCL	S erial C lock
SPI	S erial P eripheral I nterface
SDA	S erial D ata
TCP/IP	T ransfer C ontrol P rotocol / I nternet P rotocol
TCY	T imes the processor C lock period
UART	U niversal A synchronous R eceiver- T ransmitter
USB	U niversal S erial B us
USART	U niversal S ynchronous/ A synchronous R eceiver T ransmitter
WDT	W atch D og T imer
WP	W ire P rotect