Apéndices

A. Descripción del PLD

La descripción completa del comportamiento de la máquina de estados del Sistema de Seguridad se presenta a continuación. Esta desarrollada con base al diagrama de estados del Capítulo 2. Con doble guión se presentan los comentarios.

```
Library IEEE;
use IEEE.std_logic_1164.all;
entity bueno is                                    --nombre de la entidad--
port(Entrada: in integer range 0 to 15;            --declaracion de señales--
     clk,V,R: in std_logic;
     P,L,I: out bit;
     Salida: out integer range 0 to 15);
end entity;                                        --fin de la entidad--

Architecture algo of bueno is --descripcion algoritmica de la arquitectura--
type estado is(inicio,A,B,C,D,E,F,G,cortado);--declaracion de estados--
signal presente: estado:=inicio;     --señal interna, condicion nicial--
begin
process(clk,R) —ASM--          --señales que generan un cambio de estado--
  begin

    if R='0' then                                  --etapa secuencial--
       presente<=inicio;
    elsif clk'event and clk='1' then
    case presente is

        when inicio=>if V='1' then                 --estado inicio--
                        presente<=cortado;
                     elsif Entrada=0 then
                        presente<=A;
                     elsif Entrada=1 then
                        presente<=B;
                     elsif Entrada=2 then
                        presente<=C;
                     elsif Entrada=5 then
                        presente<=D;
                     elsif Entrada=9 then
                        presente<=E;
                     elsif Entrada=10 then
                        presente<=F;
                     else
                        presente<=G;
                     end if;

        when A=>if V='1' then                       --estado A--
                    presente<=cortado;
                elsif Entrada=0 then
                    presente<=A;
                else
                    presente<=inicio;
                end if;

        when B=>if V='1' then                      --estado B--
                    presente<=cortado;
                elsif Entrada=1 then
```

```
               presente<=B;
            else
               presente<=inicio;
            end if;

when C=>if V='1' then                    --estado C--
               presente<=cortado;
            elsif Entrada=2 then
               presente<=C;
            else
               presente<=inicio;
            end if;

  when D=>if V='1' then                   --estado D--
               presente<=cortado;
            elsif Entrada=5 then
               presente<=D;
            else
               presente<=inicio;
            end if;

  when E=>if V='1' then                   --estado E--
               presente<=cortado;
            elsif Entrada= 9 then
               presente<=E;
            else
               presente<=inicio;
            end if;

when F=>if V='1' then                    --estado F--
               presente<=cortado;
            elsif Entrada=10 then
               presente<=F;
            else
               presente<=inicio;
            end if;

when G=>if V='1' then                    --estado G--
               presente<=cortado;
            elsif Entrada=3 then
               presente<=G;
            elsif Entrada=4 then
               presente<=G;
            elsif Entrada=6 then
               presente<=G;
            elsif Entrada=7 then
               presente<=G;
            elsif Entrada=8 then
               presente<=G;
            elsif Entrada=11 then
               presente<=G;
            elsif Entrada=12 then
               presente<=G;
            elsif Entrada=13 then
               presente<=G;
            elsif Entrada=14 then
               presente<=G;
            elsif Entrada=15 then
               presente<=G;
```

```
                  else
                     presente<=inicio;
                  end if;

      when cortado=>presente<=cortado;    --estado cortado--
      when others=>presente<=inicio;
      end case;
end if;
end process;                              --fin etapa secuencial--
process(presente)--asignacion de salidas --etapa combinacional--
     begin
      case presente is
        when inicio=>Salida<=15; --asignacion de salidas en estado inicio--
                 P<='1';
                 L<='0';
                 I<='0';
        when A=> Salida<=15;
                 P<='1';
                 L<='0';
                 I<='0';
        when B=> Salida<=14;
                 P<='1';
                 L<='0';
                 I<='0';
        when C=> Salida<=13;
                 P<='1';
                 L<='0';
                 I<='0';
        when D=> Salida<=10;
                 P<='1';
                 L<='0';
                 I<='0';
        when E=> Salida<=6;
                 P<='1';
                 L<='0';
                 I<='0';
        when F=> Salida<=5;
                 P<='1';
                 L<='0';
                 I<='0';
        when G=> Salida<=15;
                 P<='1';
                 L<='0';
                 I<='1';
        when cortado=>Salida<=15;
                 P<='0';
                 L<='1';
                 I<='0';
        when others=>Salida<=15;
                 P<='1';
                 L<='0';
                 I<='0';                  --fin de asignaciones--
      end case;
end process;                              --fin etapa combinacional--

end algo;                                 --fin arquitectura--
```

B. Reporte de síntesis del PLD.

Una vez descrito el comportamiento del SS, el paso siguiente es sintetizarlo lo cual consiste en obtener la mínima expresión de las ecuaciones lógicas que representan a la máquina de estados, en este sentido existen herramientas de software que lo realizan de manera automática, entre ellos esta el programa Warp de Cypress, como resultado de la síntesis se producen entre otros archivos el de extensión PIN que resume información importante como la asignación de pines en el PLD y la cantidad de macroceldas utilizadas. A continuación se presenta tal archivo.

```
     | | | | | | |
   _________________
  -|                 |-
  -|                 |-
  -|                 |-
  -|    CYPRESS      |-
  -|                 |-
  -|                 |-   Warp VHDL Synthesis Compiler: Version 6.3 IR 35
  -|                 |-   Copyright (C) 1991-2001 Cypress Semiconductor
   |_________________|
     | | | | | | |

========================================================================
Compiling:  buenogalaxy.vhd
Options:    -yu -e10 -w100 -o2 -ygs -fP -v10 -dc22v10 -ppalc22v10d-25pc -b
buenogalaxy.vhd -u buenogalaxy.hie
========================================================================

vhdlfe V6.3 IR 35:  VHDL parser
Mon Mar 02 15:21:06 2009

Library 'work' => directory 'lc22v10'
Linking 'C:\Archivos de programa\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\work\cypress.vif'.
Library 'ieee' => directory 'C:\Archivos de programa\Cypress\Warp\lib\ieee\work'
Linking 'C:\Archivos de programa\Cypress\Warp\lib\ieee\work\stdlogic.vif'.

vhdlfe:  No errors.

tovif V6.3 IR 35:  High-level synthesis
Mon Mar 02 15:21:08 2009

Linking 'C:\Archivos de programa\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\work\cypress.vif'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\ieee\work\stdlogic.vif'.

tovif:  No errors.

topld V6.3 IR 35:  Synthesis and optimization
Mon Mar 02 15:21:08 2009

Linking 'C:\Archivos de programa\Cypress\Warp\bin\std.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\cypress.vhd'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\common\work\cypress.vif'.
Linking 'C:\Archivos de programa\Cypress\Warp\lib\ieee\work\stdlogic.vif'.
State variable 'presente' is represented by a Bit_vector (0 to 2).
State encoding (sequential) for 'presente' is:
      inicio :=    b"000";
```

```
       a :=   b"001";
       b :=   b"010";
       c :=   b"011";
       d :=   b"100";
       e :=   b"101";
       cortado :=   b"110";
buenogalaxy.vhd (line 82, col 16):  Warning: (W508) No exit from state 'cortado' of
'presente'.
-------------------------------------------------------------
Detecting unused logic.
-------------------------------------------------------------
-----------------------------------------------------
Alias Detection
-----------------------------------------------------
-----------------------------------------------------
Aliased 0 equations, 5 wires.
-----------------------------------------------------
-------------------------------------------------------------
Circuit simplification
-------------------------------------------------------------
-------------------------------------------------------------
Circuit simplification results:
       Expanded 0 signals.
       Turned 0 signals into soft nodes.
       Maximum default expansion cost was set at 10.
-------------------------------------------------------------
Created 28 PLD nodes.
topld:  No errors.  1 warning.
-------------------------------------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    31/03/2000  [v4.02 ] 6.3 IR 35
DESIGN HEADER INFORMATION  (15:21:11)
Input File(s): buenogalaxy.pla
Device       : C22V10
Package      : palc22v10d-25pc
ReportFile   : buenogalaxy.rpt

Program Controls:
    COMMAND LANGUAGE_VHDL
    COMMAND PROPERTY BUS_HOLD ENABLE

Signal Requests:
    GROUP USEPOL ALL
    GROUP FAST_SLEW ALL

Completed Successfully
-------------------------------------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    31/03/2000  [v4.02 ] 6.3 IR 35
OPTIMIZATION OPTIONS       (15:21:11)
Messages:
  Information: Process virtual 'presenteSBV_2D'presenteSBV_2D ... expanded.
  Information: Process virtual 'presenteSBV_1D'presenteSBV_1D ... expanded.
  Information: Process virtual 'presenteSBV_0D'presenteSBV_0D ... expanded.
  Information: Process virtual 'presenteSBV_2' ... converted to NODE.
  Information: Process virtual 'presenteSBV_1' ... converted to NODE.
  Information: Process virtual 'presenteSBV_0' ... converted to NODE.
  Information: Optimizing logic using best output polarity for signals:
         presenteSBV_0.D presenteSBV_1.D presenteSBV_2.D reset salida_IBV(0)
         salida_IBV(1) salida_IBV(2)
  Information: Selected logic optimization OFF for signals:
         aviso presenteSBV_0.AR presenteSBV_0.C presenteSBV_1.AR
         presenteSBV_1.C presenteSBV_2.AR presenteSBV_2.C salida_IBV(3)

Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
```

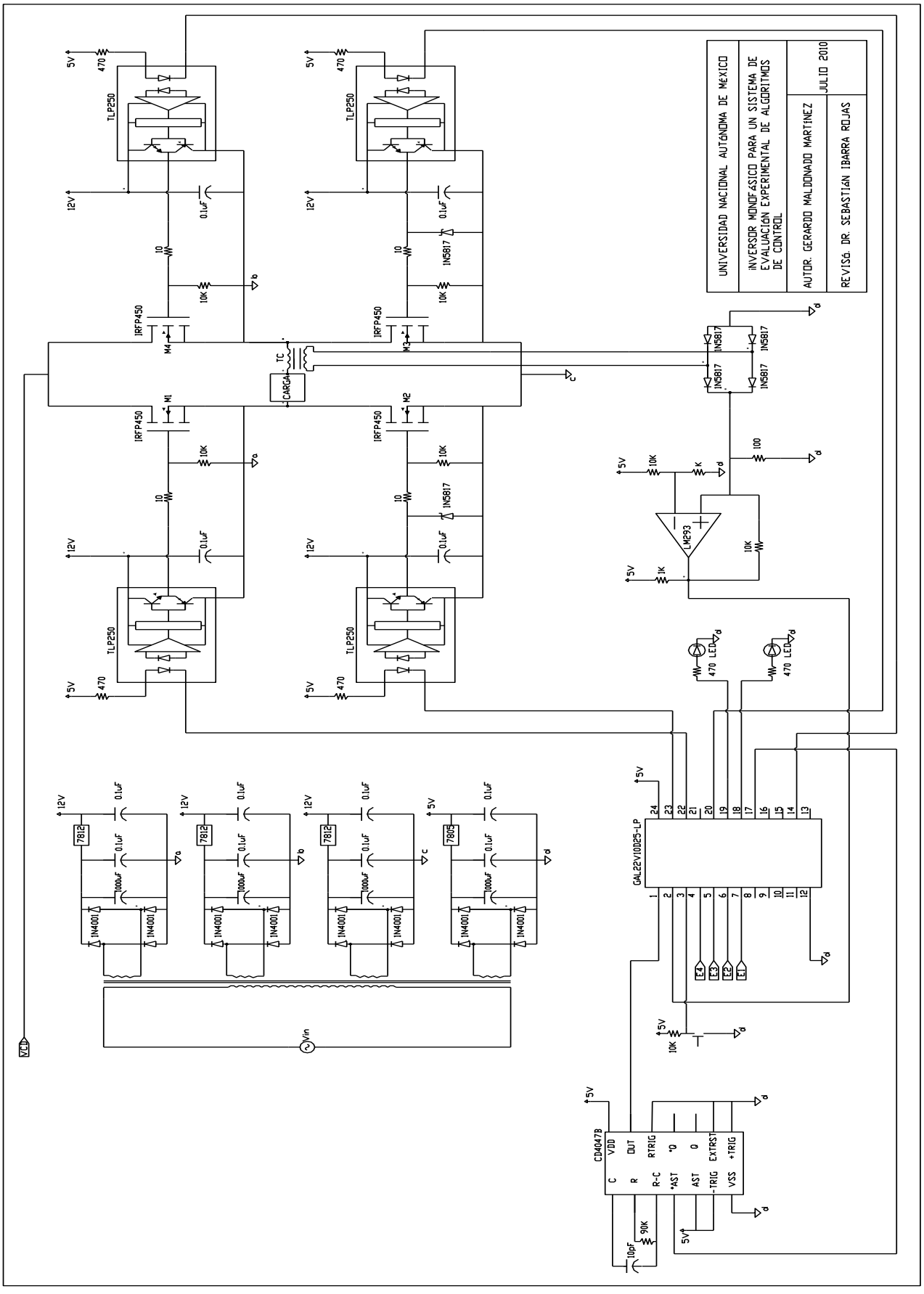
```
--------------------------------------------------------------------------------
PLD Optimizer Software:       MINOPT.EXE     01/NOV/1999  [v4.02 ] 6.3 IR 35
LOGIC MINIMIZATION         ()

Messages:
Summary:
                 Error Count = 0      Warning Count = 0
Completed Successfully
--------------------------------------------------------------------------------
PLD Optimizer Software:       DSGNOPT.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

OPTIMIZATION OPTIONS       (15:21:11)

Messages:
  Information: Optimizing Banked Preset/Reset requirements.
Summary:
                 Error Count = 0      Warning Count = 0
Completed Successfully
--------------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

<CYPRESSTAG name="Equations" icon=FILE_RPT_EQUATION>
DESIGN EQUATIONS           (15:21:12)
</CYPRESSTAG>

    aviso =
          presenteSBV_0.Q * presenteSBV_1.Q
    presenteSBV_0.D =
          /presenteSBV_0.Q * /presenteSBV_1.Q * /presenteSBV_2.Q *
          /salida_IBV(0) * salida_IBV(1) * /salida_IBV(2) * salida_IBV(3)
        + presenteSBV_0.Q * presenteSBV_2.Q * /entrada_IBV(0) * salida_IBV(1) *
          /entrada_IBV(2) * entrada_IBV(3)
        + /presenteSBV_1.Q * /presenteSBV_2.Q * entrada_IBV(0) * /entrada_IBV(1) *
          /entrada_IBV(2) * entrada_IBV(3)
        + presenteSBV_0.Q * presenteSBV_1.Q
        + v
    presenteSBV_0.AR =
          r
    presenteSBV_0.SP =
          GND
    presenteSBV_0.C =
          clk
    presenteSBV_1.D =
          /presenteSBV_0.Q * /presenteSBV_1.Q * /presenteSBV_2.Q *
          entrada_IBV(0) * /entrada_IBV(1) * entrada_IBV(2) * /entrada_IBV(3)
        + presenteSBV_1.Q * presenteSBV_2.Q * entrada_IBV(0) * /entrada_IBV(1) *
          entrada_IBV(2) * /entrada_IBV(3)
        + /presenteSBV_0.Q * /presenteSBV_2.Q * /entrada_IBV(0) * entrada_IBV(1) *
          /entrada_IBV(2) * /entrada_IBV(3)
        + presenteSBV_0.Q * presenteSBV_1.Q
        + v
    presenteSBV_1.AR =
          r
    presenteSBV_1.SP =
          GND
    presenteSBV_1.C =
          clk
    presenteSBV_2.D =
          /corto * /presenteSBV_0.Q * /presenteSBV_1.Q * /presenteSBV_2.Q *
          /entrada_IBV(0) * entrada_IBV(1) * /entrada_IBV(2) * entrada_IBV(3)
        + /v * presenteSBV_0.Q * presenteSBV_2.Q * /entrada_IBV(0) *
          entrada_IBV(1) * /entrada_IBV(2) * entrada_IBV(3)
        + /v * presenteSBV_1.Q * presenteSBV_2.Q * entrada_IBV(0) *
          /entrada_IBV(1) * entrada_IBV(2) * /entrada_IBV(3)
        + /v * /presenteSBV_0.Q * /presenteSBV_1.Q * /presenteSBV_2.Q *
          entrada_IBV(0) * /entrada_IBV(1) * /entrada_IBV(3)
```

```
        + /v * /presenteSBV_0.Q * /presenteSBV_1.Q * entrada_IBV(0) *
          /entrada_IBV(1) * /entrada_IBV(2) * /entrada_IBV(3)
    presenteSBV_2.AR =
          r
    presenteSBV_2.SP =
          GND
    presenteSBV_2.C =
          clk
    /rt =
          presenteSBV_0.Q * presenteSBV_1.Q
    salida_IBV(0) =
          presenteSBV_0.Q * /presenteSBV_1.Q * /presenteSBV_2.Q
        + /presenteSBV_0.Q * presenteSBV_2.Q
    /salida_IBV(1) =
          /presenteSBV_0.Q * presenteSBV_1.Q * /presenteSBV_2.Q
        + presenteSBV_0.Q * presenteSBV_2.Q
    /salida_IBV(2) =
          presenteSBV_1.Q * presenteSBV_2.Q
    salida_IBV(3) =
          presenteSBV_0.Q * /presenteSBV_1.Q

Completed Successfully
-------------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

DESIGN RULE CHECK          (15:21:12)

Messages:
                None.
Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

<CYPRESSTAG name="Pinout" icon=FILE_RPT_PINOUT>
PINOUT INFORMATION   (15:21:12)
</CYPRESSTAG>
Messages:
  Information: Checking for duplicate NODE logic.
                None.
                              C22V10
                _____________________________________________
            clk =| 1|                                     |24|*not used
              r =| 2|                                     |23|=presenteSBV..
 entrada_IBV(3) =| 3|                                     |22|=salida_IBV(1)
 entrada_IBV(2) =| 4|                                     |21|=salida_IBV(3)
 entrada_IBV(1) =| 5|                                     |20|=p
 entrada_IBV(0) =| 6|                                     |19|*not used
              v =| 7|                                     |18|=l
       not used *| 8|                                     |17|=salida_IBV(2)
       not used *| 9|                                     |16|=salida_IBV(0)
       not used *|10|                                     |15|=presenteSBV..
       not used *|11|                                     |14|=presenteSBV..
       not used *|12|                                     |13|*not used
                _____________________________________________

Summary:
                Error Count = 0      Warning Count = 0

Completed Successfully
-------------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

<CYPRESSTAG name="Utilization" icon=FILE_RPT_UTILIZATION>
```

```
RESOURCE UTILIZATION (15:21:12)
</CYPRESSTAG>
  Information: Macrocell Utilization.

                    Description        Used     Max
                  ___________________________________
                  | Dedicated Inputs   |    6  |   11  |
                  | Clock/Inputs       |    1  |    1  |
                  | I/O Macrocells     |    9  |   10  |
                  ___________________________________
                                      16  /   22   = 72  %
  Information: Output Logic Product Term Utilization.

                   Node#  Output Signal Name  Used   Max
                  ___________________________________________
                  | 14  |  presenteSBV_2   |   5  |   8  |
                  | 15  |  presenteSBV_0   |   5  |  10  |
                  | 16  |  salida_IBV(0)   |   2  |  12  |
                  | 17  |  salida_IBV(2)   |   1  |  14  |
                  | 18  |  l               |   1  |  16  |
                  | 19  |  Unused          |   0  |  16  |
                  | 20  |  p               |   1  |  14  |
                  | 21  |  salida_IBV(3)   |   1  |  12  |
                  | 22  |  salida_IBV(1)   |   2  |  10  |
                  | 23  |  presenteSBV_1   |   5  |   8  |
                  | 25  |  Unused          |   0  |   1  |
                  ___________________________________________
                                         23  / 121   = 19  %

Completed Successfully
------------------------------------------------------------------------------
PLD Compiler Software:        PLA2JED.EXE    31/03/2000  [v4.02 ] 6.3 IR 35

JEDEC ASSEMBLE             (15:21:12)

Messages:
  Information: Output file 'buenogalaxy.pin' created.
  Information: Output file 'buenogalaxy.jed' created.

  Usercode:
  Checksum:    95E0

Summary:
                 Error Count = 0      Warning Count = 0

Completed Successfully at 15:21:12
```

C. Diagramas

En esta parte del trabajo se presenta el diagrama esquemático del inversor monofásico implementado, los valores del Sistema de Medición son para la corriente nominal del inversor de 10 [A], el diagrama fue desarrollado con el programa Autocad.


UNIVERSIDAD NACIONAL AUTÓNOMA DE MÉXICO
INVERSOR MONOFÁSICO PARA UN SISTEMA DE EVALUACIÓN EXPERIMENTAL DE ALGORITMOS DE CONTROL
AUTOR. GERARDO MALDONADO MARTÍNEZ
REVISÓ. DR. SEBASTIÁN IBARRA ROJAS
JULIO 2010
TLP250
IRFP450
IN5817
LM293
CAL22V10D25-LP
CD4047B
7812
7805
IN4001
TC
CARGA
Vin
VCD

D. Hojas de datos

En éste apéndice se presentan algunos datos técnicos de los elementos principales del sistema. Las hojas de datos en forma completa se pueden encontrar en el sitio web del fabricante.

- GAL 22V1025-LP.
- MOSFET IRFP450.
- TLP 250.

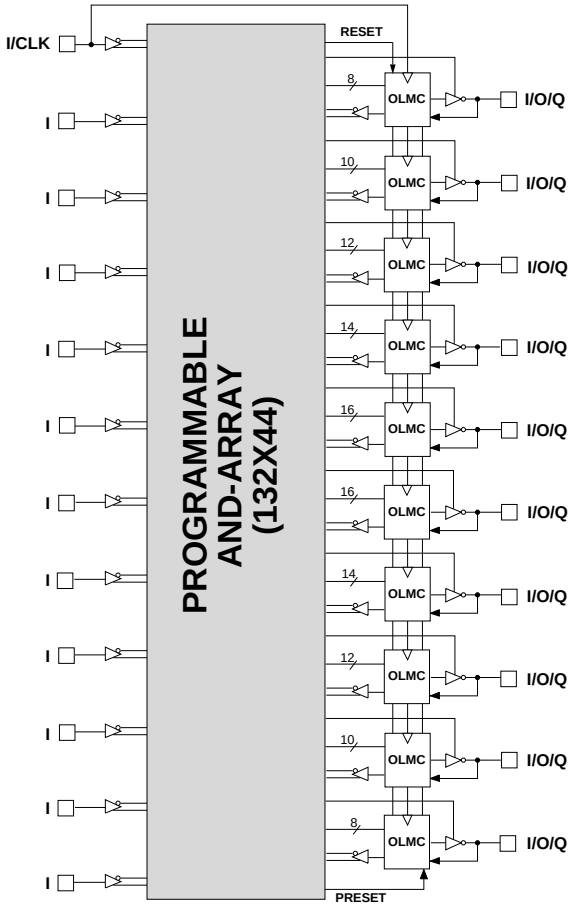
GAL22V10

High Performance E²CMOS PLD
Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 4 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 3.5 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices**
- **50% to 75% REDUCTION IN POWER VERSUS BIPOLAR**
  - **— 90mA Typical Icc on Low Power Device**
  - **— 45mA Typical Icc on Quarter Power Device**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Functional Block Diagram



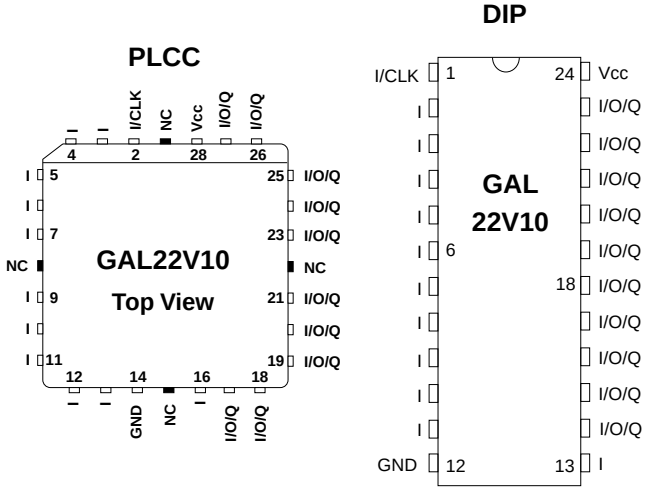
Description

The GAL22V10, at 4ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E^2 technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

August 2000

22v10_06

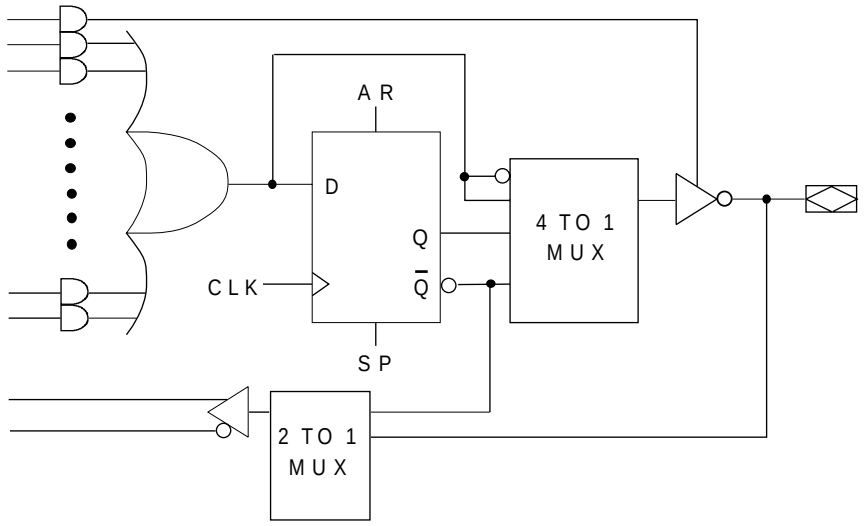
Output Logic Macrocell (OLMC)

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23, DIP pinout), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

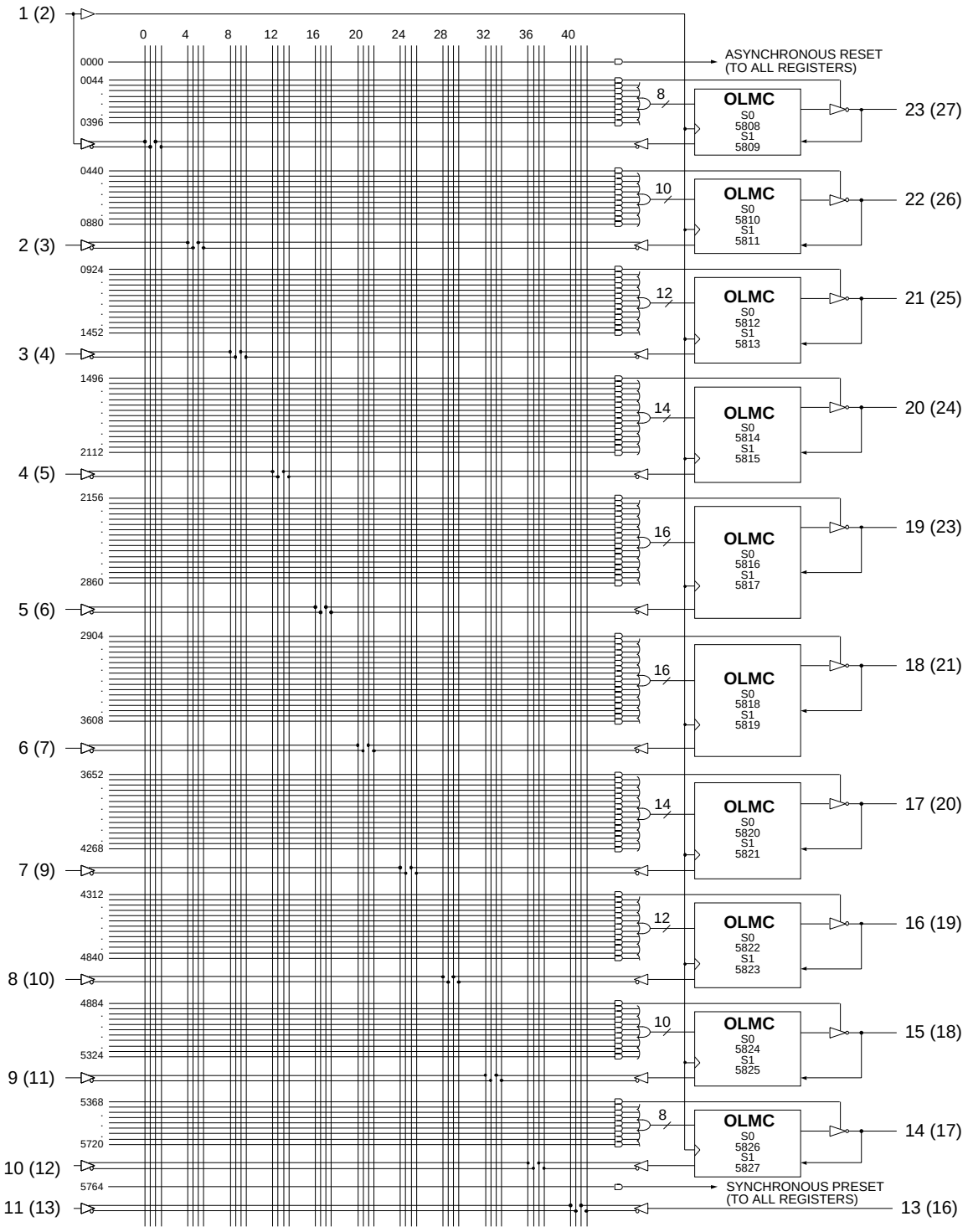
NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

GAL22V10 Logic Diagram / JEDEC Fuse Map

DIP (PLCC) Package Pinouts



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

Absolute Maximum Ratings[1]

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied..... -2.5 to V_{CC} +1.0V
Storage Temperature..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	16	mA
I_{OH}	High Level Output Current			—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–130	mA
COMMERCIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-4/-5/-7	—	90	140	mA
			L-10	—	90	130	mA
			L-15/-25	—	75	90	mA
			Q-10/-15/-25	—	45	55	mA
INDUSTRIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7/-10	—	90	160	mA
			L-15/-20/-25	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

Electronic Signature

An electronic signature (ES) is provided in every GAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

Security Cell

A security cell is provided in every GAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

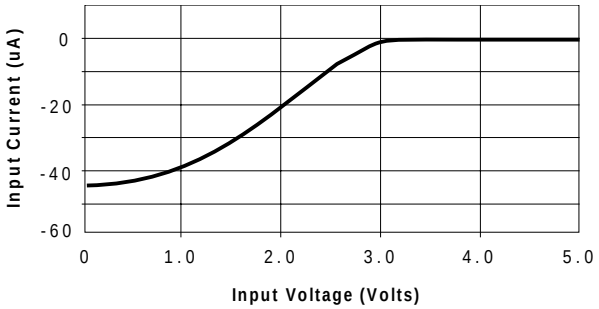
The GAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

Input Buffers

GAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current



14A, 500V, 0.400 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17435.

Ordering Information

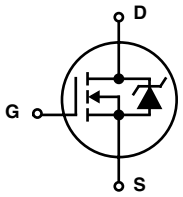
PART NUMBER	PACKAGE	BRAND
IRFP450	TO-247	IRFP450

NOTE: When ordering, use the entire part number.

Features

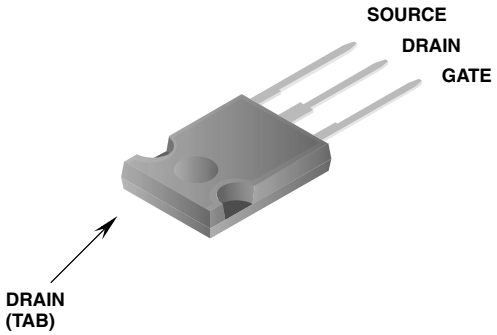
- 14A, 500V
- $r_{DS(ON)} = 0.400\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC STYLE TO-247



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

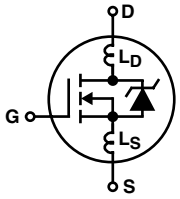
		IRFP450	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	500	V
Continuous Drain Current	I_D	14	A
$T_C = 100^oC$	I_D	8.8	A
Pulsed Drain Current (Note 3)	I_{DM}	56	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	180	W
Linear Derating Factor		1.44	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	860	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

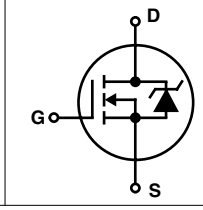
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 10)		500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$		-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V		14	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 7.9A, V_{GS} = 10V (Figures 8, 9)		-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 7.9A (Figure 12)		9.3	13.8	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \approx$ 14A, V_{GS} = 10V, R_{GS} = 6.1Ω, R_L = 17.4Ω MOSFET Switching Times are Essentially Independent of Operating Temperature		-	16	27	ns
Rise Time	t_r			-	45	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	68	100	ns
Fall Time	t_f			-	41	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, $I_D \approx$ 14A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{G(REF)}$ = 1.5mA (Figure 14) Gate Charge is Essentially Independent of OperatingTemperature		-	82	130	nC
Gate to Source Charge	Q_{gs}			-	12	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	42	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	2000	-	pF
Output Capacitance	C_{OSS}			-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Internal Drain Inductance	L_D	Measured from the Contact Screw on Header Closer to Source and Gate Pins to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6.0mm (0.25in) from Header to Source Bonding Pad		-	12.5	-	nH
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	0.70	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 	-	-	14	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	56	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 14A$, $V_{GS} = 0V$ (Figure 13)	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = 13A$, $dI_{SD}/dt = 100A/\mu s$	-	1300	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = 13A$, $dI_{SD}/dt = 100A/\mu s$	-	7.4	-	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, L = 7.9mH, $R_G = 25\Omega$, peak $I_{AS} = 14A$.

Typical Performance Curves Unless Otherwise Specified

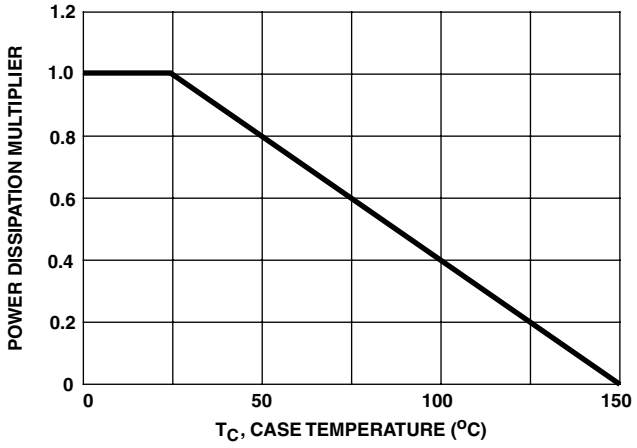


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

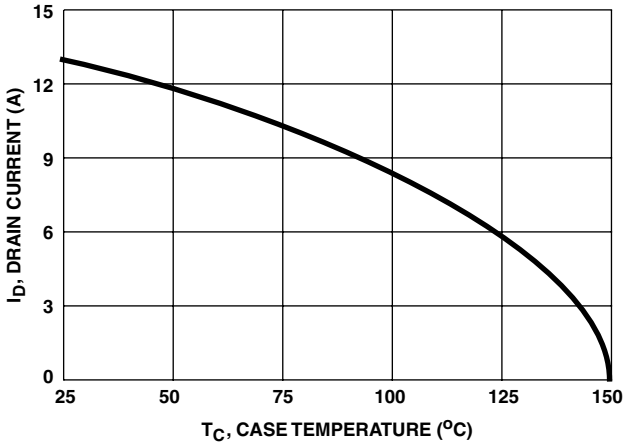


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

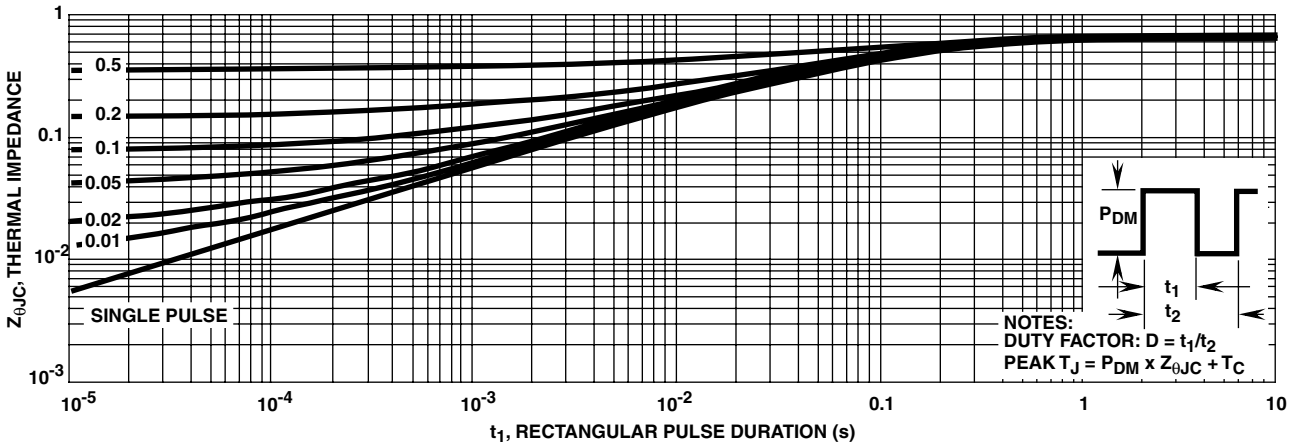


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

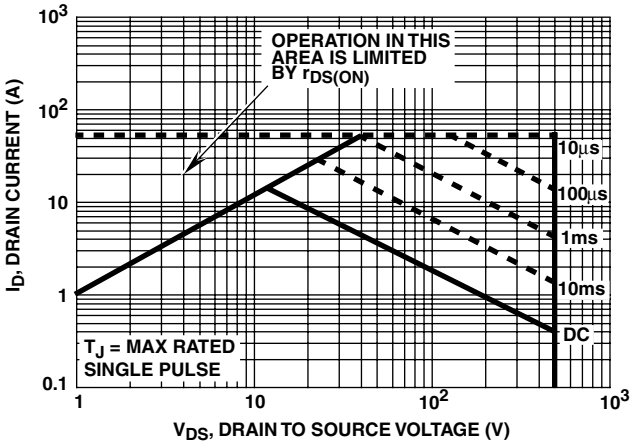


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

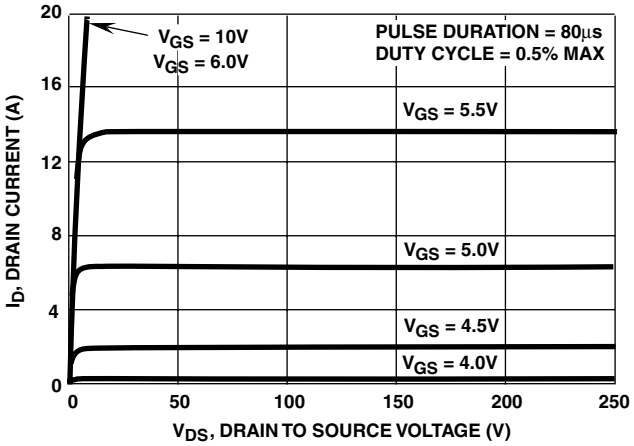


FIGURE 5. OUTPUT CHARACTERISTICS

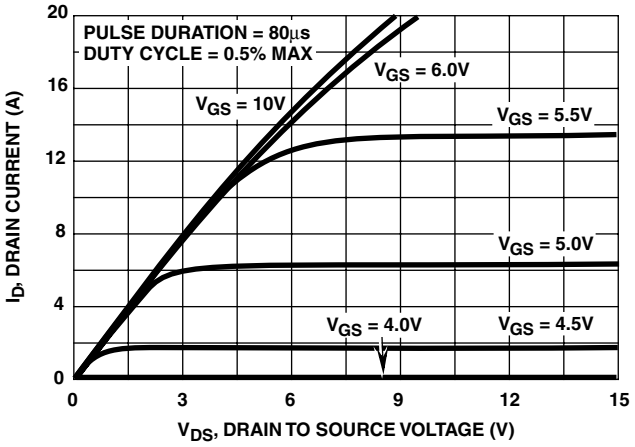


FIGURE 6. SATURATION CHARACTERISTICS

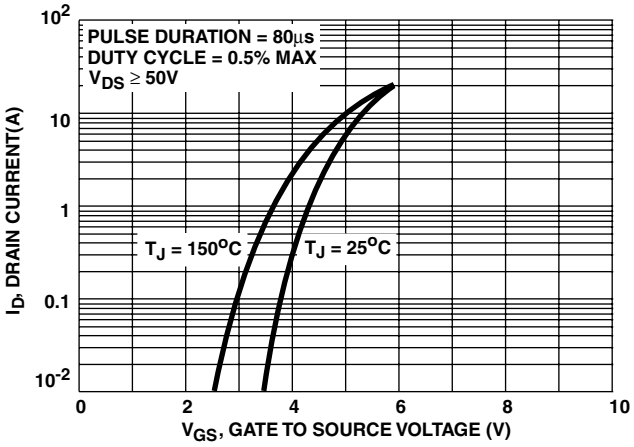
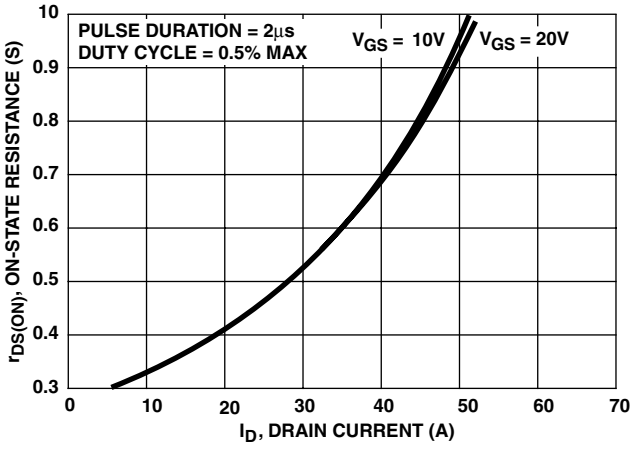


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

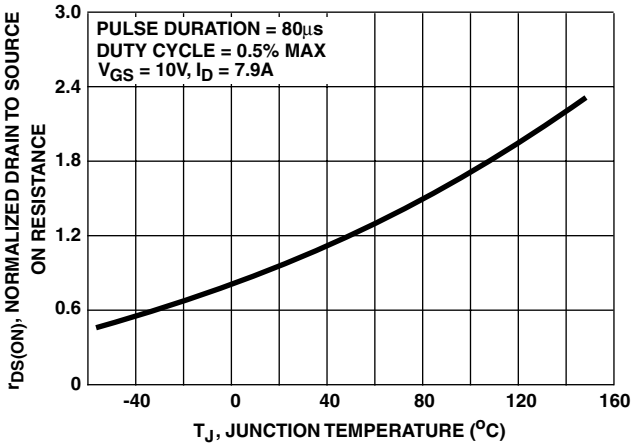


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

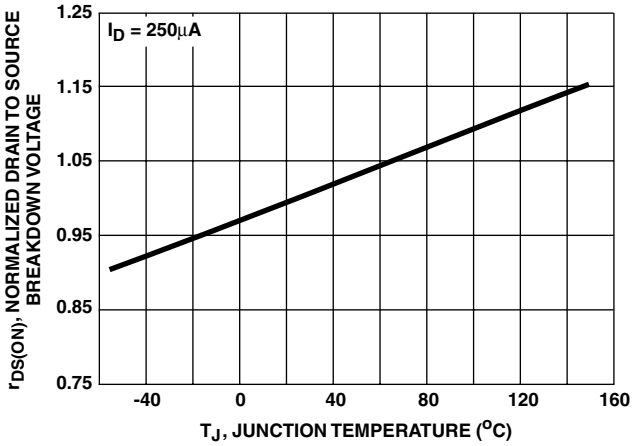


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

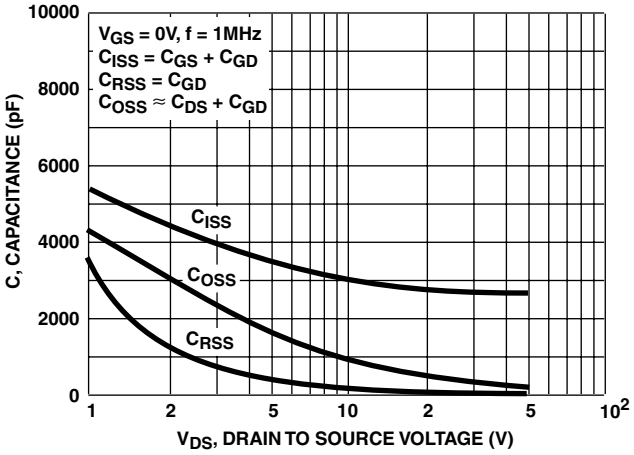


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

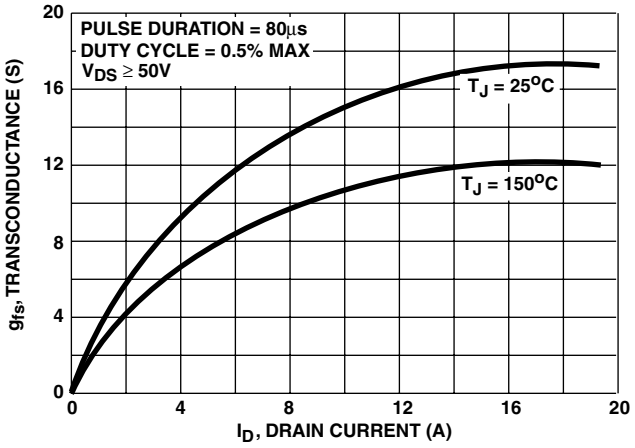


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

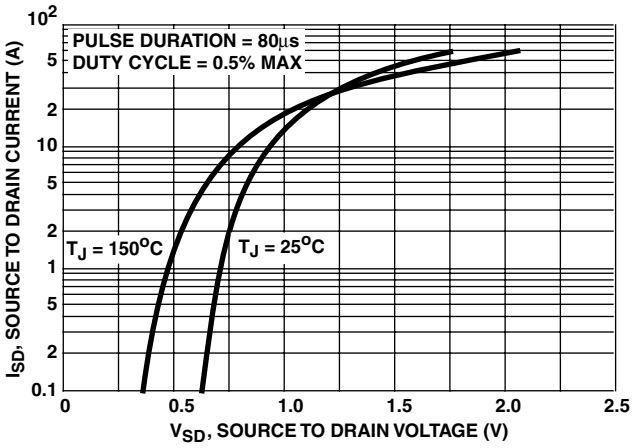


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

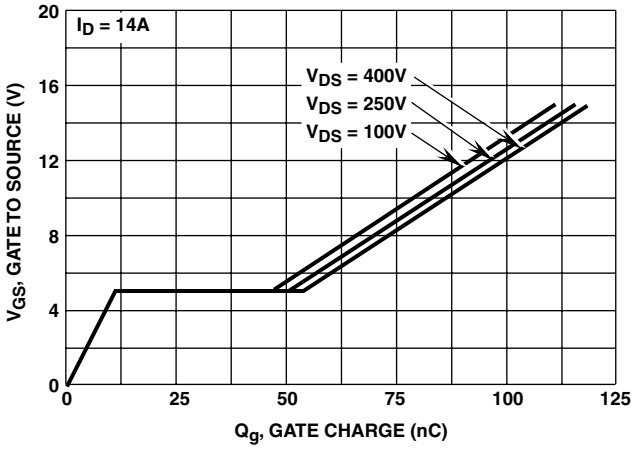


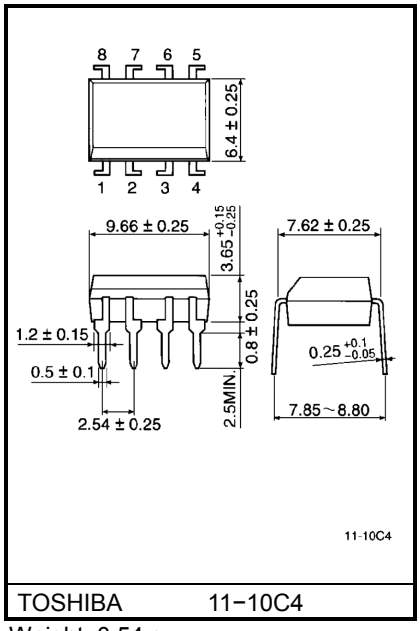
FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

TOSHIBA Photocoupler GaAlAs Ired & Photo−IC

TLP250

Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

Unit in mm



TOSHIBA 11−10C4

Weight: 0.54 g

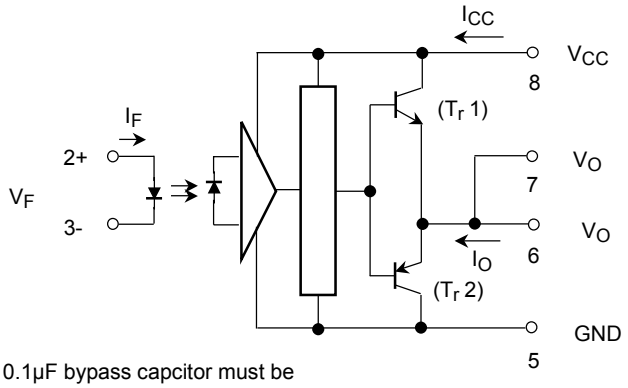
The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8−lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10−35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"

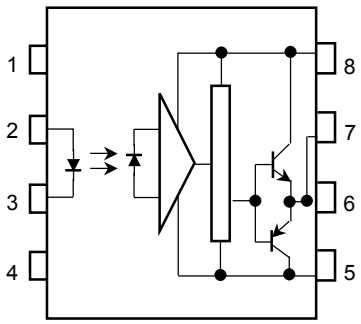
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
	Peak transient forward curent	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Junction temperature		Tj	125	°C
Detector	"H"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPH}	−1.5	A
	"L"peak output current (P_W ≤ 2.5μs,f ≤ 15kHz)	(Note 2)	I_{OPL}	+1.5	A
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta = 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta = 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
	Junction temperature		Tj	125	°C
Operating frequency		(Note 3)	f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s)			T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%)		(Note 4)	BV_S	2500	Vrms

(Note 1) Pulse width P_W ≤ 1μs, 300pps

(Note 2) Exporenential wavefom

(Note 3) Exporenential wavefom, I_{OPH} ≤ −1.0A(≤ 2.5μs), I_{OPL} ≤ +1.0A(≤ 2.5μs)

(Note 4) Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

(Note 5) A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.		Unit
Input current, on	$I_{F(ON)}$	7	8	10		mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8		V
Supply voltage	V_{CC}	15	—	30	20	V
Peak output current	I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature	T_{opr}	−20	25	70	85	°C

Electrical Characteristics (Ta = −20~70°C, unless otherwise specified)

Characteristic		Symbol	Test Cir−cuit	Test Condition		Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C			1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA		—	−2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C			—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C		—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1)	I_F = 10 mA V_{8-6} = 4V	−0.5	−1.5	—	A
	"L" level	I_{OPL}	2		I_F = 0 V_{6-5} = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, I_F = 5mA		11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_F = 0.8V		—	−14.2	−12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA Ta = 25°C		—	7	—	mA
				V_{CC} = 30V, I_F = 10mA		—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA Ta = 25°C		—	7.5	—	
				V_{CC} = 30V, I_F = 0mA		—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_O > 0V		—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_O < 0V		0.8	—	—	V
Supply voltage		V_{CC}	—			10	—	35	V
Capacitance (input−output)		C_S	—	V_S = 0 , f = 1MHz Ta = 25°C		—	1.0	2.0	pF
Resistance(input−output)		R_S	—	V_S = 500V , Ta = 25°C R.H.≤ 60%		1×10^{12}	10^{14}	—	Ω

* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

Switching Characteristics (Ta = −20~70°C , unless otherwise specified)

Characteristic		Symbol	Test Circuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time	L→H	t_{pLH}	6	I_F = 8mA V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω	—	0.15	0.5	μs
	H→L	t_{pHL}			—	0.15	0.5	
Output rise time		t_r			—	—	—	
Output fall time		t_f			—	—	—	
Common mode transient immunity at high level output		C_{MH}	7	V_{CM} = 600V, I_F = 8mA V_{CC} = 30V, Ta = 25°C	−5000	—	—	V / μs
Common mode transient immunity at low level output		C_{ML}	7	V_{CM} = 600V, I_F = 0mA V_{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

* All typical values are at Ta = 25°C