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división de estudios superiores
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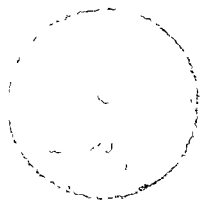
LA ELECTRONICA EN LAS COMUNICACIONES

Electrónica Básica

M. en C. Luis M. Hernández Ortega



CAPITULO I

ELECTRONICA BASICA

M. en C. Luis M. Hernández Ortega *

El objetivo del presente capítulo puede ser dividido en cuatro partes:

a. Revisar los fundamentos sobre los cuales se apoyan las aplicaciones de la electrónica a las comunicaciones.

b. Analizar en forma cualitativa las principales realizaciones de circuitos electrónicos empleados en el procesamiento de señales.

c. Familiarizar al estudiante con los sistemas integrados disponibles, con sus aplicaciones y sus limitaciones.

d. Poner en contacto al estudiante con la información proporcionada por los fabricantes y con la contenida en la literatura periódica especializada.

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INDICE

1.1 CONCEPTOS

En esta sección estudiaremos los aspectos teoricos que definen al amplificador, su modelo en función de elementos ideales de circuitos eléctricos así como un análisis de los aspectos mas relevantes de los diversos tipos de amplificadores. Hay que señalar que en esta sección no se analizarán aspectos relativos a potencia o eficiencia de los amplificadores.

1.1.1 FUNCION DEL AMPLIFICADOR

Se acostumbra definir al amplificador como un elemento que proporciona "ganancia" de voltaje o corriente; ¿Es entonces un transformador elevador un amplificador de voltaje?. Cual es entonces, la esencia de un amplificador, la respuesta es:

GANANCIA DE POTENCIA

Teniendo en mente que la función de un amplificador es incrementar un nivel de potencia pasaremos al siguiente tema.

1.1.2 EL AMPLIFICADOR COMO SISTEMA

Una concepción elemental del amplificador como sistema se muestra en la figura 1.1.1

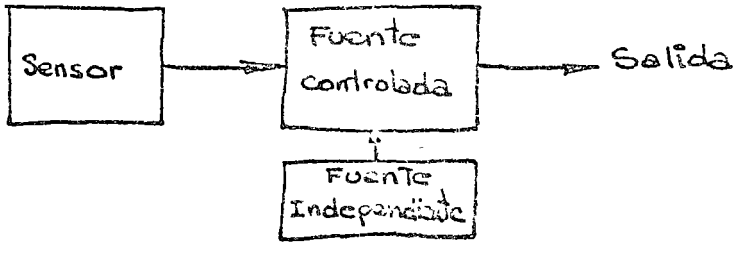


Fig. 1.1.1

Para nuestro caso, el sensor y la fuente controlada podrán ser de voltaje o corriente, siendo la fuente independiente de voltaje en la mayoría de los casos. Podemos entonces considerar cuatro tipos básicos de amplificadores.

TIPO	SENSOR	FUENTE CONTROLADA
I	Voltaje	Voltaje
II	Voltaje	Corriente
III	Corriente	Corriente
IV	Corriente	Voltaje

Para analizar un amplificador en base a la teoría de circuitos, es necesario representar tanto el sensor como las fuentes por medio de elementos conocidos en la teoría de circuitos, a esta representación se le conoce como MODELADO DEL AMPLIFICADOR.

Los elementos ideales serán:

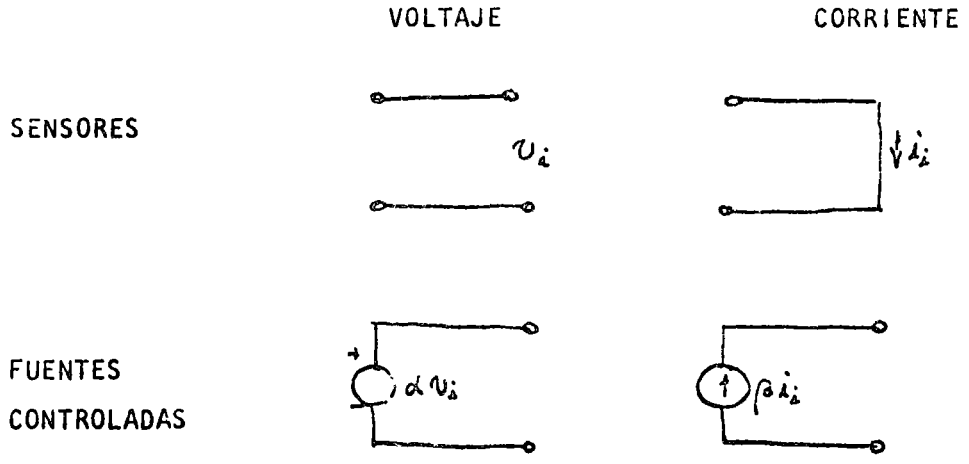


Fig. 1.1.2

Las desviaciones de la idealidad estarán representadas por elementos pasivos; por ejemplo, para frecuencias tales que las partes imaginarias de las impedancias sean despreciables, el modelo de un amplificador tipo II puede ser:

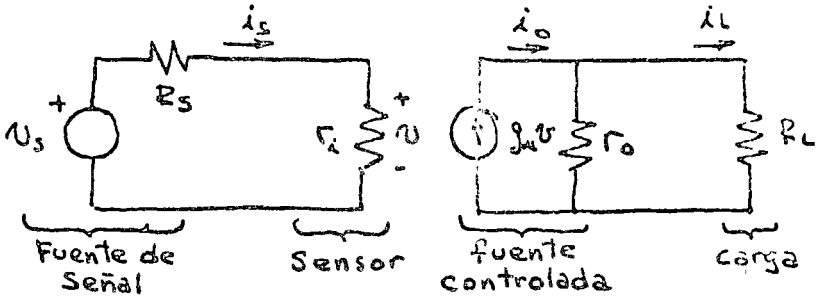


Fig 1.1.3

En este caso

$$v = \frac{r_i}{R_s + r_i} v_s \quad \therefore \text{ Si } r_i \to \infty$$

Llegamos al caso ideal

$$\underline{v = v_s}$$

además:

$$i_L = \frac{r_o}{r_o + R_L} g_m v \quad \text{Si } r_o \to \infty$$

Tendremos

$$\underline{i_L = i_o = g_m v}$$

o sea el caso ideal

de esta misma forma podemos analizar el comportamiento de un amplificador real.

1.1.3 TEOREMAS BASICOS

En esta sección formularemos algunos teoremas que facilitan grandemente el análisis de circuitos eléctricos que contienen fuentes controladas (o sea en terminos de electrónica amplificadores).

A.- OPERACIONES CON FUENTES CONTROLADAS: Es conveniente el tener en mente las diversas manipulaciones que pueden hacerse sobre una o

(varias) fuentes controladas a fin de simplificar el análisis de un cierto circuito. A fin de ejemplificar este tipo de manipulaciones consideremos el siguiente circuito.

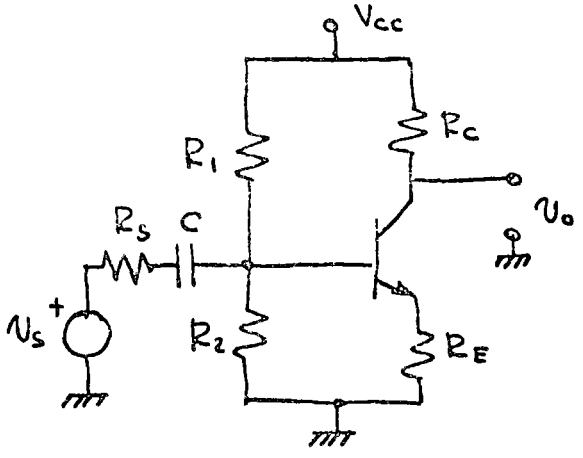
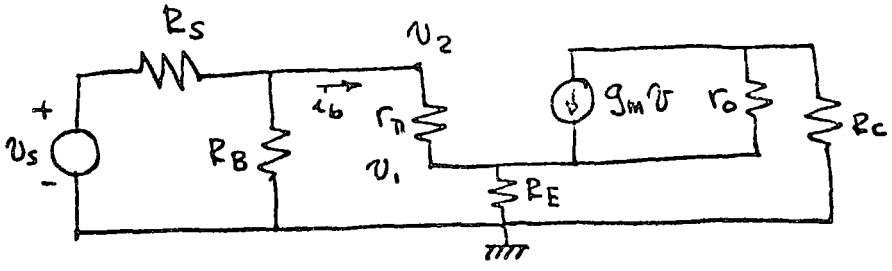


Fig. 1.1.4

El modelo de señal pequeña estará dado por:



$R_B = R_1 // R_2$, $v = v_2 - v_1$

Fig. 1.4.5

Podemos convertir la fuente controlada de corriente a una de voltaje en la forma usual.

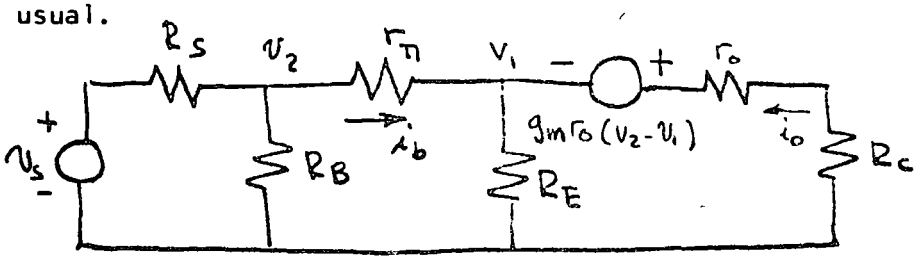


Fig. 1.4.6

Si analizamos las definiciones de las variables encontraremos las siguientes relaciones:

$$gm\ (V_1 - V_2) = \beta\, i_b$$

$$io = (\beta + 1)\ i_b$$

pero:

$$V_1 = io\, R_E$$

por tanto la definición de la fuente controlada estará dada por

$$gm\ (V_1 - V_2)\, r_o = gm\, r_o\, i_o\ R_E - gm\, r_o\ V_2$$

$$= \mu\, i_o R_E - \mu V_2$$

Pero esta última ecuación puede representarse como un circuito de la forma:

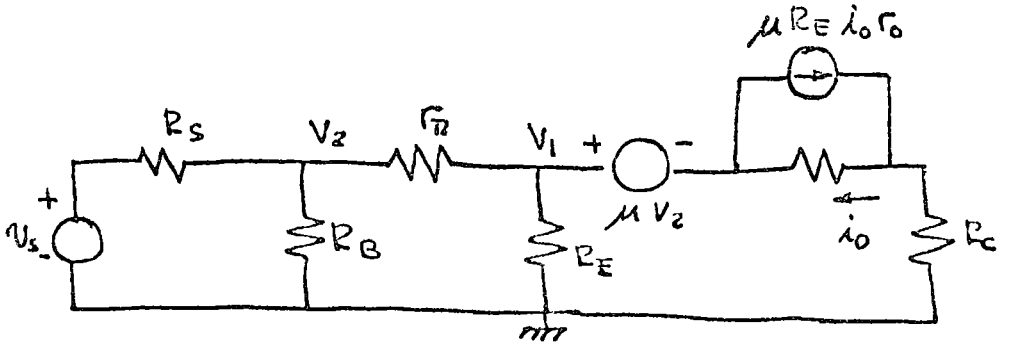


Fig. 1.4.7

En esta forma podemos reacomodar el circuito para facilitar la aplicación de ecuaciones de mallas o nodos.

Mas aún, podemos hacer uso de dos hechos:

-Si substituimos por dos fuentes de voltaje identicas una fuente de voltaje conectada a un circuito en paralelo podemos cortar la rama central tal como se muestra en la figura 1.4.8.

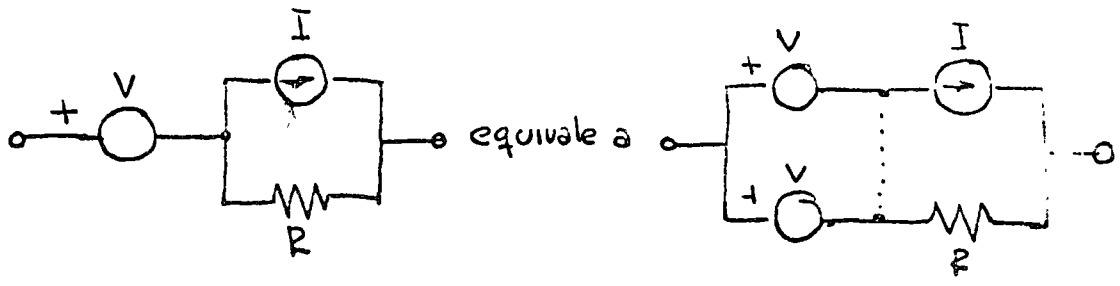


Fig. 1.4.8

- Si substituimos una fuente de corriente por dos fuentes de corriente idénticas en serie podemos conectar el nodo entre las dos fuentes a un nodo cualquiera del circuito.

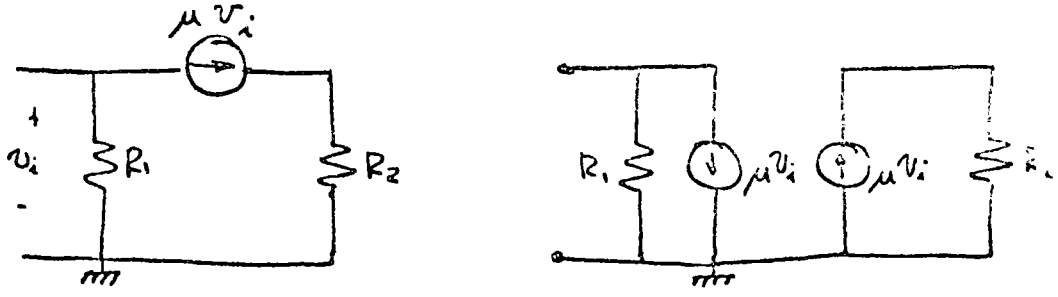


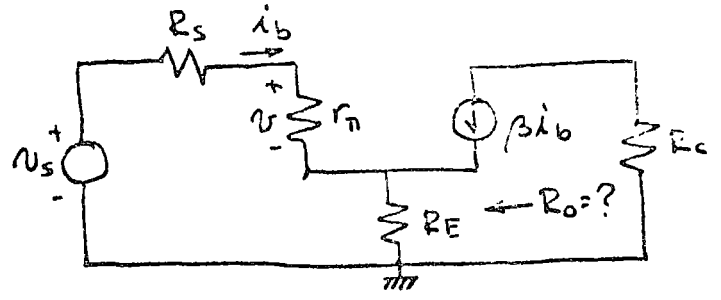
Fig. 1.4.9

Aplicando estas substituciones al circuito de la figura 1.4.7 podemos llegar a transformar substancialmente el circuito.

B.- TEOREMA DE THEVENIN PARA CIRCUITOS ACTIVOS.

Un teorema que merece especial atención, es el teorema de Thevenin, ya que no puede aplicarse directamente a un circuito que contenga fuentes controladas. Un ejemplo es el cálculo de la impedancia de salida de un amplificador con TBJ y resistencia en el emisor:

Si analizamos aplicando directamente Thevenin obtenemos



$$R_o = R_E \,//\, (R_S + r_\pi)$$

Fig. 1.4.10

lo cual es evidentemente incorrecto. Ahora bien, si reformulamos el teorema de Thevenin en forma mas general como:

- Podemos substituir un circuito entre dos puntos, por una fuente de valor igual al voltaje de circuito abierto entre dichos puntos y una resistencia en serie con dicha fuente igual al voltaje de circuito abierto, dividido por la corriente de corto circuito.

Aplicando lo anterior al circuito de la figura 1.4.10 obtenemos:

$$v_{CA} \doteq v_s \qquad \text{si } \beta \gg 1,\ r_\pi \text{ y } R_S \ll (\beta+1)R_E$$

$$i_{cc} = (\beta+1)\frac{v_s}{r_\pi + R_S}$$

por tanto

$$R_o \doteq \frac{r_\pi + R_S}{\beta+1}$$

lo cual, sí corresponde a la realidad.

Otros teoremas útiles son:

C.- TEOREMA DE LA SUBSTITUCION

Una fuente controlada puede ser substituída por una conductancia

siempre y cuando:

- La ganancia de la fuente (A) sea real

- La conductancia sea de valor A

- El circuito sea lineal

- La corriente que fluye a través de la fuente sea positiva con respecto al voltaje entre las terminales de la fuente.

Lo anterior se ilustra en la figura 1.4.11

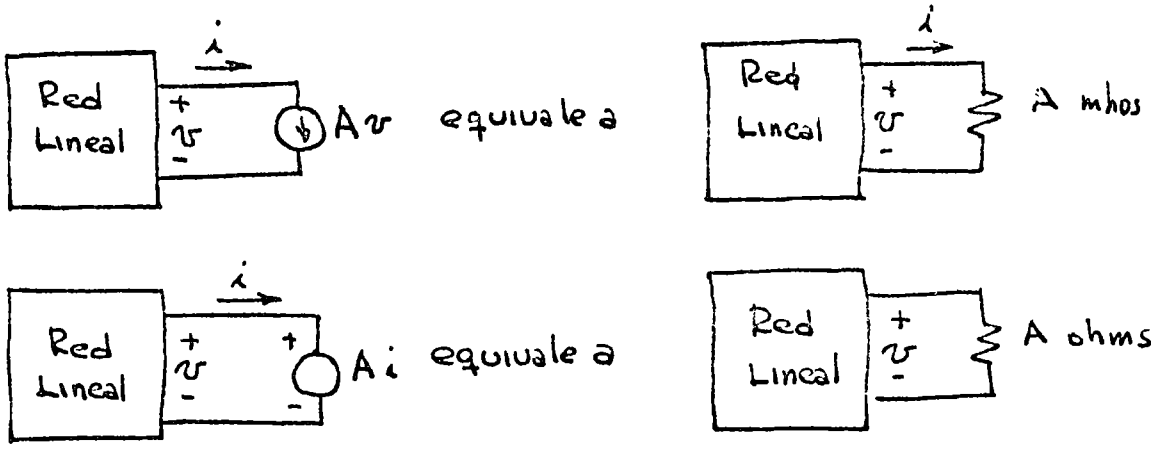


Fig. 1.4.11

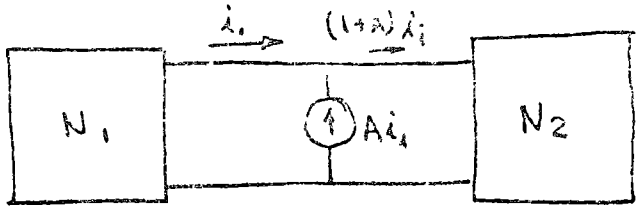
D.- TEOREMA DE LA REDUCCION

En una red como la mostrada en la figura 1.1.12a los voltajes en N_1 y N_2 permanecerán sin alterarse al remover la fuente controlada siempre y cuando:

a.- Cada impedancia en N_1 y corriente en cada fuente de corriente en N_2 se divida entre 1+A

b.- Cada impedancia en N_2 corriente en cada fuente de corriente en N_1 se multiplique por 1+A

a:-



b:-

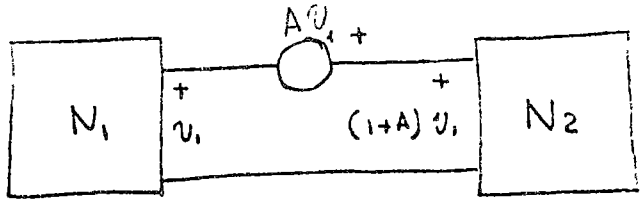


Fig. 1.1.12

El dual del teorema aplicará en la figura 1.1.12b.

1.2. El amplificador Operacional

Se denomina Amplificador Operacional a un dispositivo ideal que cumple las siguientes características:

- Ganancia de voltaje infinita ($Av \to \infty$)
- Impedancia de entrada infinito ($r_i \to \infty$)
- Impedancia de salida cero ($r_0 \to 0$)
- Ancho de banda infinito
- Excursión de voltaje de salida simétrico con respecto a tierra.
- $v_0 = 0$ Si $v_{in} = 0$
- Entrada diferencial

Un circuito que corresponde a estas especificaciones es el mostrado en la figura 1.2.1.

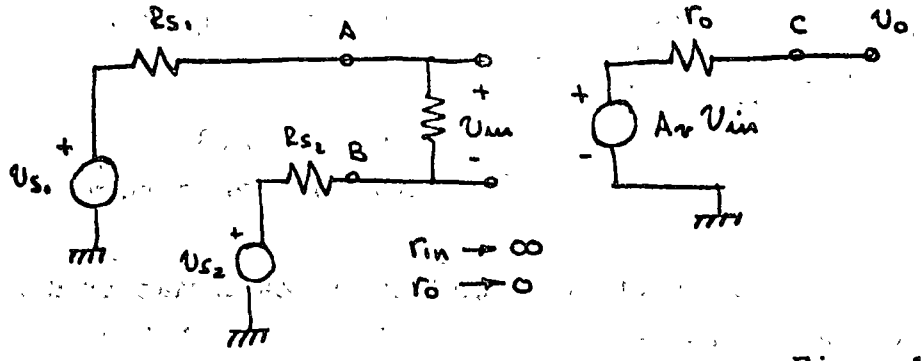


Fig. 1.2.1

Para este circuito:

$$v_{in} = v_{s1} - v_{s2}$$

$$v_o = Av\,(v_{s1} - v_{s2}) \qquad 1.2.1$$

1.2.1 Nomenclatura del Amplificador Operacional: A fin de hablar un mismo lenguaje al presentar los aspectos mas sobresalientes del amplificador operacional, estableceremos tanto la simbología como la nomenclatura adecuada. El símbolo del A.O. se muestra en la figura 1.2.2 y corresponde en sus terminales al circuito de la figura 1.2.1. El nombre que se le da a las entradas A y B (No inversora e Inversora respectivamente) se puede justificar al analizar la ecuación 1.2.1.

SIMBOLO DEL A. O.

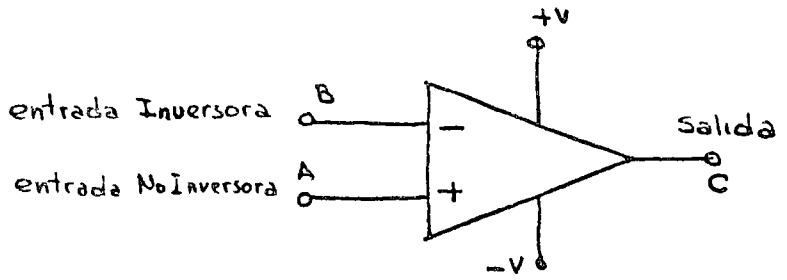


Fig. 1.2.2

Las entradas marcas +V y -V sirven para conectar el circuito a las fuentes externas de energía (polarizar el circuito); a continuación presentaremos algunas definiciones éstas se encuentran referidas a la figura 1.2.3

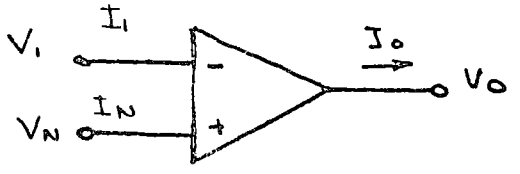
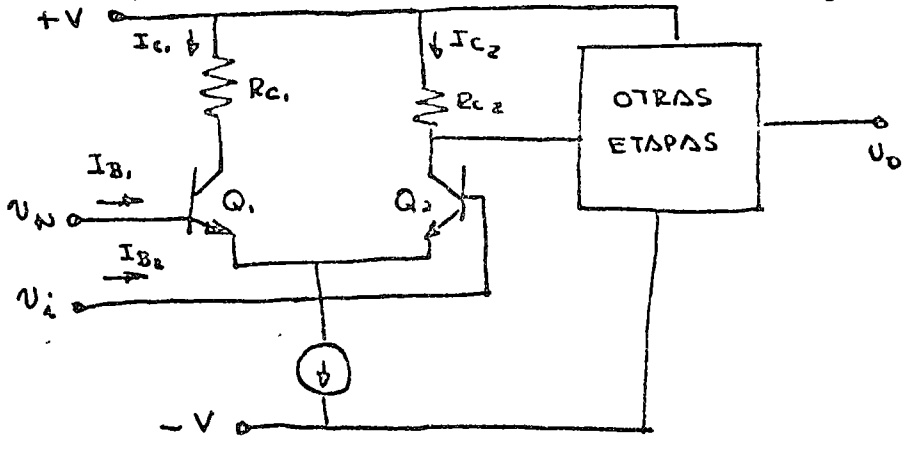


Fig. 1.2.3

CORRIENTE DE POLARIZACION $\frac{I_1 + I_n}{2}$, es la corriente necesaria para polarizar los dispositivos de entrada, en el caso mas común, un par acoplado por emisor como se muestra en la figura 1.2.4



en este caso $I_{B1} = I_1$, $I_{B2} = I_N$

Fig. 1.2.4

OFFSET DE CORRIENTE $I_I - I_N \quad v_0 = 0$

OFFSET DE VOLTAJE. Es el voltaje que debe aplicarse a la entrada $V_N - V_I$ para que $v_0 = 0$ (Este voltaje deberá ser suministrado por fuentes con iguales impedancias de salida generalmente 10 k

IMPEDANCIA DE ENTRADA $Z_{in} = \frac{Z_I + Z_n}{2}$

donde $Z_I = \frac{V_I}{I_I} \quad Y_N = 0$

$Z_N = \frac{V_N}{I_N} \quad V_I = 0$

generalmente se considera $Z_I = Z_N$

IMPEDANCIA DE SALIDA

$Z_o = \frac{V_o}{I_o} \quad V_o \doteq 0$

La razón de definir Z_o para voltajes de salida muy pequeños es con el fin de minimizar los efectos del sistema interno de protección contra exceso de corriente.

RELACION DE RECHAZO DE MODO COMUN: es el cambio en V_o debido a un cambio simultaneo en V_I y V_N con $V_I = V_N$ se denomina CMRR.

FRECUENCIA DE CORTE: Frecuencia a la cual la ganancia de voltaje es 3db menor que su valor a frecuencia cero f_{edb}

FRECUENCIA DE TRANSICION: frecuencia a la cual $A_v = 1 \quad f_r$

RAZON MAXIMA DE CAMBIO (Slew Rate): es la máxima variación en el tiempo de la señal de entrada $(\frac{dv_{in}}{dt}_{max})$ que puede seguir fielmente v_o.

FRECUENCIA MAXIMA DE SALIDA: Es una combinación de los parámetros anteriores; por una excursión simétrica del voltaje de salida es igual a: $f_{max} = \frac{\text{RAZON MAXIMA DE CAMBIO}}{2\Pi(\text{Voltaje de Saturación})}$

Cabe hacer notar que los parámetros que definen la respuesta del amplificador operacional en el dominio de la frecuencia no solo dependen del amplificador en si, sino también de los componentes pasivos incluidos externamente para compensar el amplificador (ver curvas características en el apéndice A).

DISMINUCION DE LA EXCURSION MAXIMA (Roll Off): Este fenómeno consiste en una limitación (función de la frecuencia) a la excursión máxima del voltaje de salida o sea que el voltaje de saturación disminuye con la frecuencia.

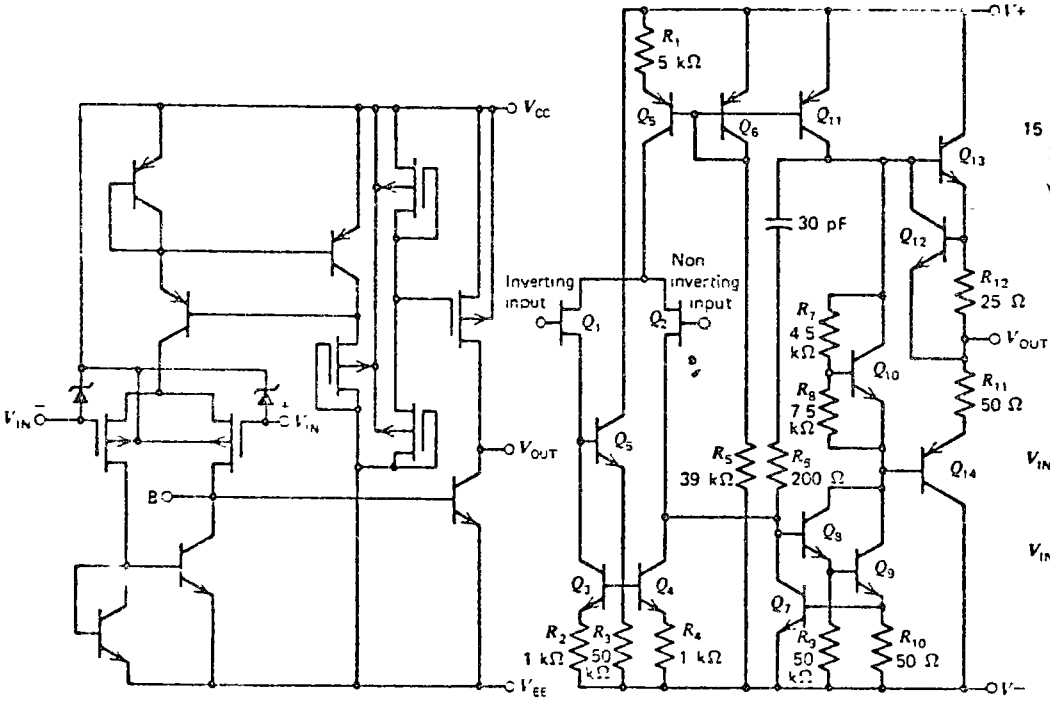
Existen otros parámetros como son limitaciones máximas, figuras de ruido, etc. (ver apéndice A) pero dejaremos su consideración para e

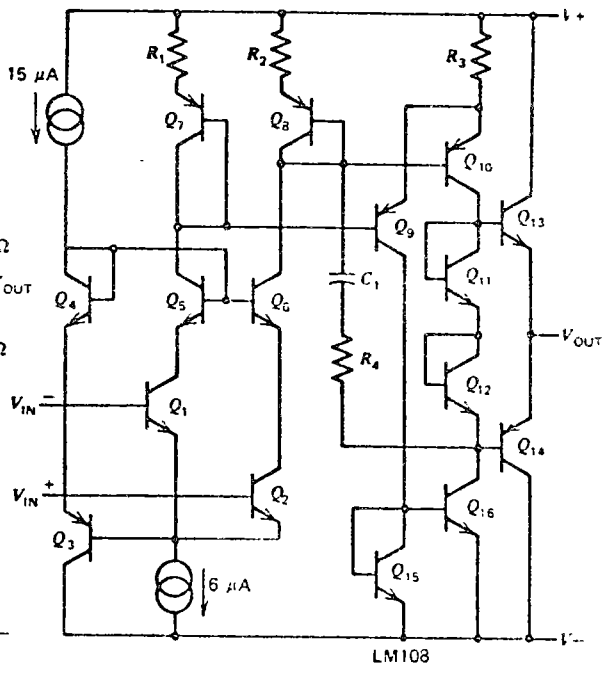
MOS FET
Siliconix L120

J FET
μA740A

Bipolars

Super Beta
LM 108/108A LM 110
LM 112
LM 216
MC 1556





L120 Schematic Diagram

L120 Specifications

Input-leakage current	50 pA
Input resistance	2×10^{-3} Ω
Slew rate	15 V μsec (typ)
CMRR	50 dB (min)

μA740A Schematic Diagram

μA740A Specifications

Input-bias current	200 pA (max)
Input-offset current	100 pA (max)
Input resistance	1 000 000 MΩ (typ)
Slew rate	6 V μsec (typ)
CMRR	80 dB (min)

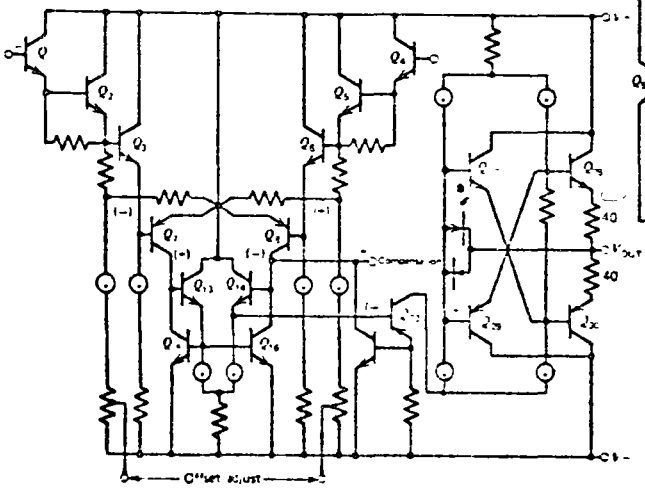
LM 108 Schematic Diagram

LM 108 Specifications

Input-bias current	2.0 nA (max)
Input-offset current	0.2 nA (max)
Input resistance	70 MΩ (typ)
Slew rate	0.3 V/μsec (typ)
CMRR	85 dB (min)

Darlington
LM 118
SE 531

Regular
4250 μA747
μA709 MC 1558
μA725 LM 101/101A
μA741 LM 107

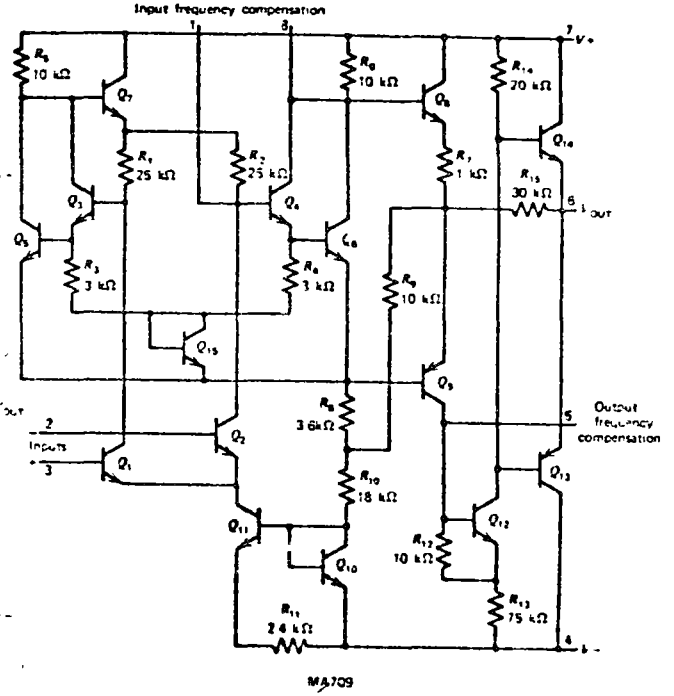


NE531 Schematic Diagram

SE531 Specifications

Input-bias current	500 nA (max)
Input-offset current	200 nA (max)
Input resistance	20 MΩ (typ)
Slew rate	30-35 V/μs (typ)
CMRR	70 dB (min)

* All values at 25°C



μA709 Schematic Diagram

μA709 Specifications

Input-bias current	500 nA (max)
Input-offset current	200 nA (max)
Input resistance	400 kΩ (typ)
Slew rate	0.25 V/μs (typ)
CMRR	70 dB (min)

momento de el estudio de aplicaciones.
En la figura 1.2.5 se presentan algunos circuitos típicos que nos muestran el estado del arte en A.O., monoliticos, en estos se pueden apreciar las relaciones que existen entre los diversos parámetros y el diseño del amplificador.

1.2.3 Aplicaciones del Amplificador Operacional.

Debido a la gran versatilidad y al bajo costo del amplificador operacional monolitico, se han implementado una gran variedad de circuitos en base a amplificadores operacionales, en el apéndice B se muestra una selección de circuitos que de ninguna manera pretende ser exhaustiva, sino mas bien, tiene el objeto de despertar inquietud respecto al enorme potencial de este circuito. En lo que resta de esta sección se analizarán algunos circuitos básicos dentro del campo de la electrónica directamente relacionado con las comunicaciones.

amplificador inversor: Esta conección se muestra en la figura 1.2.6

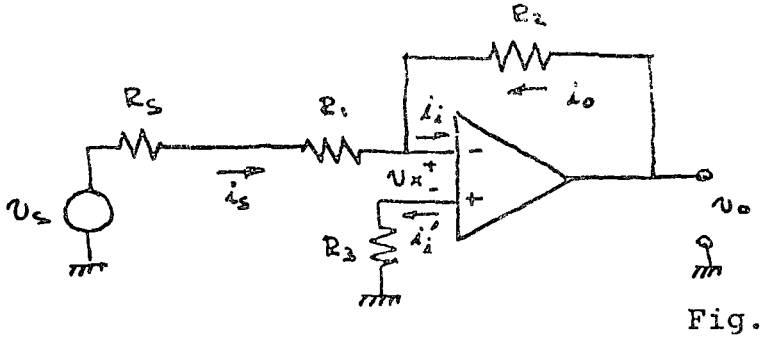


Fig. 1.2.6

considerando que si $A_v \to \infty$ $v_x \to 0$ (tierra virtual) y además que i_i i_s, i_o (ya que $z_i \to \infty$).
Podemos afirmar que:

$$i_s \doteq \frac{v_s}{R_s+R_1}$$

$$i_o \doteq \frac{v_o}{R_2}$$

Por lo tanto

$$\frac{v_o}{v_s} = A_v = \frac{R_2}{R_s+R_1}$$

Lo anterior será válido siempre y cuando:
$i_i \doteq i_i'$ (offset de corriente despreciable)

A_{vo} $\frac{R_2}{R_s+R_1}$ donde A_{vo} es la ganancia del amplificador en malla abierta a la frecuencia de operación.

$Z_i \to \infty$

$i_i R_3 \doteq 0$

$R_3 = (R_s + R_1) \,//\, R_2$ Para minimizar los efectos del offset de voltaje

Ejercicio: Demostrar que para esta conexión

$$r_{im} = R_1 + \frac{R_2}{A_{vo} + 1}$$ (considerando R_s como parte de la fuente de señal)

$$r_o = r_o \,//\, \frac{R_2}{A_{vo} + 1}$$

En algunos casos se requieren ganancias 1 e impedancias de entrada grandes, lo cual conduce a valores impracticos par R_2 por ejemplo para obtener $A_v = 100$ y r_{in} 1 M se requiere R_2 100 M para solucionar este problema se puede recurrir a un circuito como el mostrado en la figura 1 .2.7

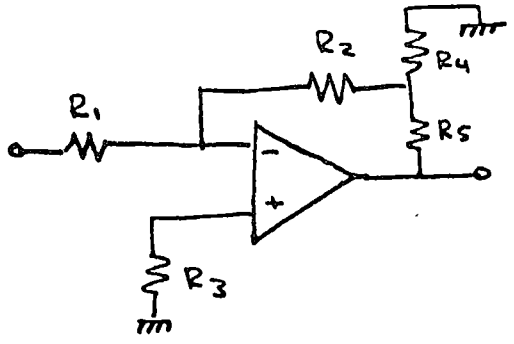


Fig. 1.2.7

R_2 R_1

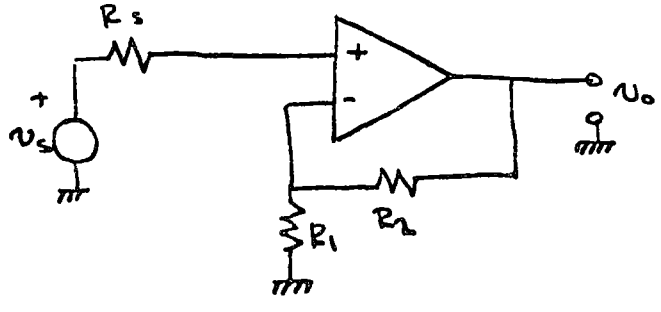
R_2 R_4, R_5

$R_3 \doteq R_1 \,//(R_2 + R_4//R_5)$

Para este circuito:

$$A_v = \frac{R_2(R_4+R_5}{R_1\ R_4}$$

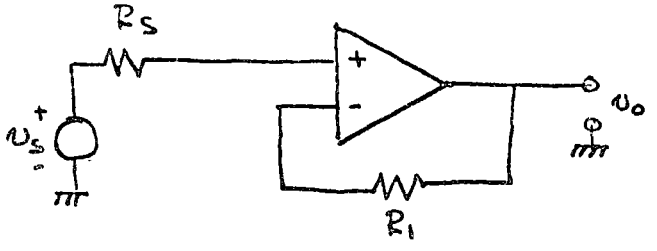
AMPLIFICADOR NO INVERSOR: En aplicaciones en las cuales no se desee la inversión de fase o se requiera alta impedancia de entrada se puede emplear el circuito mostrado en la figura 1.2.8



$R_s = R_1//R_2$ para minimizar efectos de offset de corriente.

$A_v \doteq \frac{R_1 + R_2}{R_1}$ Fig.1..

en este amplificador la resistencia de entrada es prácticamente la misma del amplificador operacional en si.
Una aplicación importante se tiene para $R_1 \to \infty$ y se conoce como seguidor de voltaje ($A_V = 1$), en este circuito (fig. 1.2.9)



$A_V = 1$
$R_1 = R_S$ para mínimo error por offset de corriente.

Fig. 1.2.9

Sus características son:

- Máxima impedancia de entrada
- Máximo ancho de banda

Sin embargo se deben tomar precauciones para no exceder los límites en el voltaje común con respecto a tierra para no caer en condición de encadenamiento por realimentación positivo (Latch up) de voltaje elemental, pero en un buen punto de partida para analizar las demandas que la aplicación impone sobre las características del A.O. asi como las posibles aplicaciones de este tipo de circuito.

Una combinación de ambas configuraciones nos da capacidad para sumar algebráicamente diversos voltajes en forma analógica por ejemplo el circuito mostrado en la figura 1.2.10

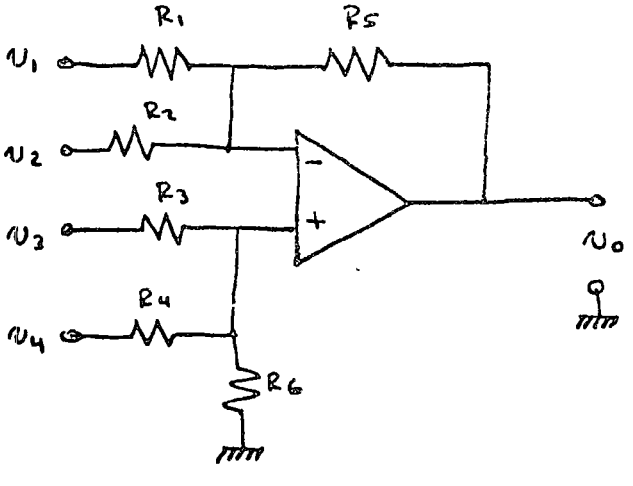


Fig. 1.2.10

en este caso

$$v_o = - v_1 \frac{R_5}{R_1} - v_2 \frac{R_5}{R_2} + v_3 \frac{R_1//R_2 + R_5}{R_1//R_2} \quad \frac{R_6//R_y}{R_6//R_y+R_3}$$

$$+ v_4 \frac{R_1//R_2 + R_5}{R_1//R_2} \quad \frac{R_c//R_3}{R_6//R_3+R_4}$$

Cabe hacer notar que las impedancias para las entradas inversoras y no inversoras son diferentes.

COMPARADOR DE VOLTAJE: En esta aplicación hacemos uso de la alta ganancia en malla abierta de un A.O., para realizar una aproximación a la característica ideal del comparador de voltaje mostrada en la figura 1.2.11, esta gráfica corresponde a un comparador

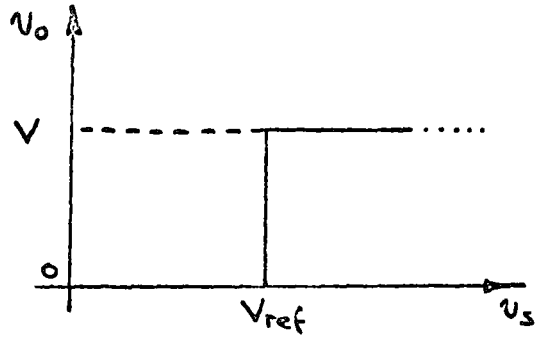
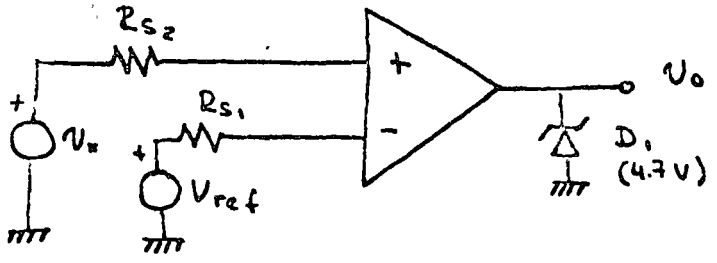


Fig 1.2.11

Una posible realización de un comparador se muestra en la figura 1.2.12 , en la cual la no linealidad se obtiene debido a la alta ganancia del A.O.



$R_{s1} = R_{s2}$

Fig. 1.2.12

La curva de transferencia de este circuito será

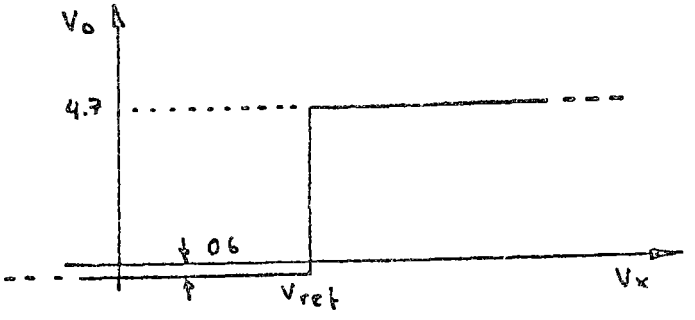


Fig 1.2.13

Nótese que el voltaje de salida está limitado mediante un diodo Zener, para evitar que no excursione entre los límites de saturación del A.O. Cabe hacer que este circuito funcionará en forma adecuada soli si el A.O. tiene limitación interna de corriente.

Aunque en el mercado existen circuitos construidos "ex-profeso" como comparadores, en muchas aplicaciones sobre todo de baja frecuencia el A.O. puede desempeñar un buen papel si observamos las siguientes reglas:

- Minimizar offset de voltaje y de corriente y tiempo de respuesta.
- Proporcionar una sobre excitación al comandar el comparador.
- Escoger un A.O. sin compensación interna de frecuencia.
- Reducir la capacitancia parásita, tanto en D_1 como entre terminales.

Es evidente que el material presentado no es exhaustivo en lo que se refiere a la presentación de las potencialidades del A.O. como amplificador, sugerimos consultar el Apéndice B donde se comentan aplicaciones de otro tipo de A.O., asi como las referencias especialmente los editados por Burr y Brown y Harris Semiconductors.

1.3 Osciladores

1.3.1 Fundamentos teóricos: La base para el análisis sencillo de osciladores construidos en base a amplificadores operacionales se encuentra en la teoria de sistemas realimentados. Para el caso de sistemas electrónicos convencionales un modelo ideal sería como el mostrado en la figura 1.3.1

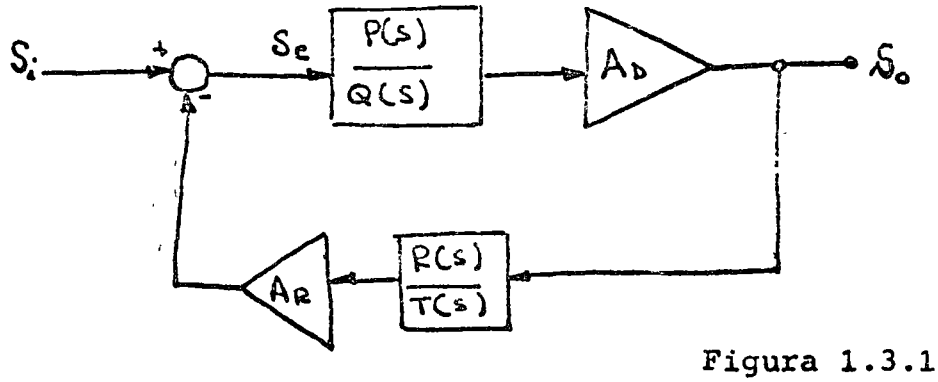


Figura 1.3.1

En este modelo:

P(s), Q(s), R(s) y T(s) son polinomios en S (s=jw) A_D u A_R son amplificadores ideales unilaterales si A_R 0 tendremos realimentación negativa, si A_R 0 tendremos realimentación positiva.

La expresión que relaciona Si (s) y So(s) estará dada por:

$$\frac{S_o(s)}{S_i(s)} = \frac{A_D \frac{P(s)}{Q(s)}}{1 + A_R A_D \frac{P(s)}{Q(s)} \frac{R(s)}{T(s)}} \qquad \text{ec. 1.3.1}$$

Debemos estar conscientes que el sistema caracterizado por la ecuación 1.3.1 es una representación idealizada de un amplificador real, no el amplificador o sistema electrónico que tenemos entre manos, el cual carecerá de alguno de los elementos mostrados en la figura - 1.3.1 y estará integrado por bloques que no corresponderán a la descripción ideal de los mismos, sin embargo la representación idealizada nos ayudará a establecer criterios sencillos para el diseño, asi como a visualizar racionalmente los efectos que sobre la respuesta prevista tendrán las desviaciones de la idealidad de los elementos constituyentes del sistema.

Osciladores: Una forma intuitiva de considerar un oscilador nos - llevaría a pensarlo como un sistema que tiene como salida una señal

senoidal estable en amplitud y en frecuencia, y cuya entrada es nula. Es evidente que dicho sistema es irrealizable, sin embargo, si consideramos el denominador de la ecuación 1.3.1 podemos observar - que si:

$$A_R A_D \frac{P(s)\ R(s)}{Q(s)\ T(s)} = -1 \qquad \text{ec. 1.3.2}$$

entonces $\dfrac{S_o(s)}{S_i(s)} \to \infty$

Como s = jw lo anterior solo se cumplirá para ciertos valores de w, que mediante una selección adecuada pueden ser reducidos a uno solo. Lo señalado en la ecuación 1.3.2 se denomina criterio de - - - Barkhausen para osciladores.

Antes de proceder al análisis de circuitos electrónicos que cumplan con este criterio pasaremos a plantear algunos problemas de orden práctico inherentes a la implementación del sistema:

a) Es imposible mantener en forma estable un sistema que cumpla con la ecuación 1.3.2 en forma exacta, esto se ilustra en la figura 1.3.2 mediante la representación del lugar geométrico de las raíces (root Locus)

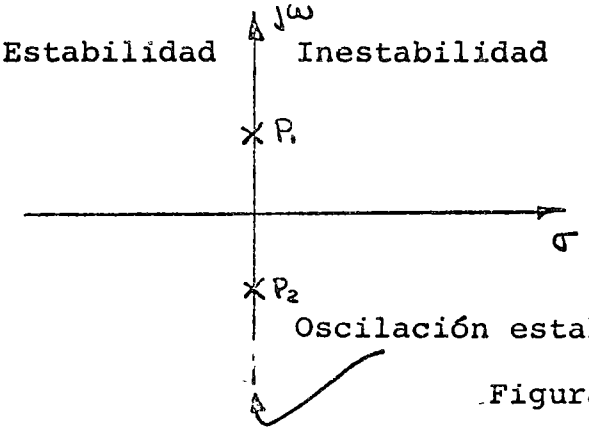


Figura 1.3.2

P_1 y P_2 muestran la localización de los polos del sistema (valores que satisfacen el criterio de Barkhausen) para oscilación estable, debido a que tanto , como jw dependen de parámetros del sistema (resistencia, capacitancia, ganancia, etc.) y éstos se ven afectados por condiciones ambientales, es prácticamente imposible el mantenerlos con =0 lo cual a su vez llevará a nuestro sistema a no oscilar o a hacerlo en forma destructiva. La solución mas comúnmente empleada es sitúar los polos con $\sigma > 0$ e introducir en el circuito(normal-

mente está presente) una no-linealidad que limite (sature). La amplitud de la señal de salida; lo difícil será el hacerlo sin que se introduzca distorsión apreciable en la señal de salida.

b) Dado que el mecanismo de arranque del oscilador será la presencia de señales generadas internamente en los dispositivos (ruido), la naturaleza de las funciones de S debe ser tal que proporcione buena selectividad para reducir la distorsión armónica total, lo anterior se ilustra en la figura 1.3.3

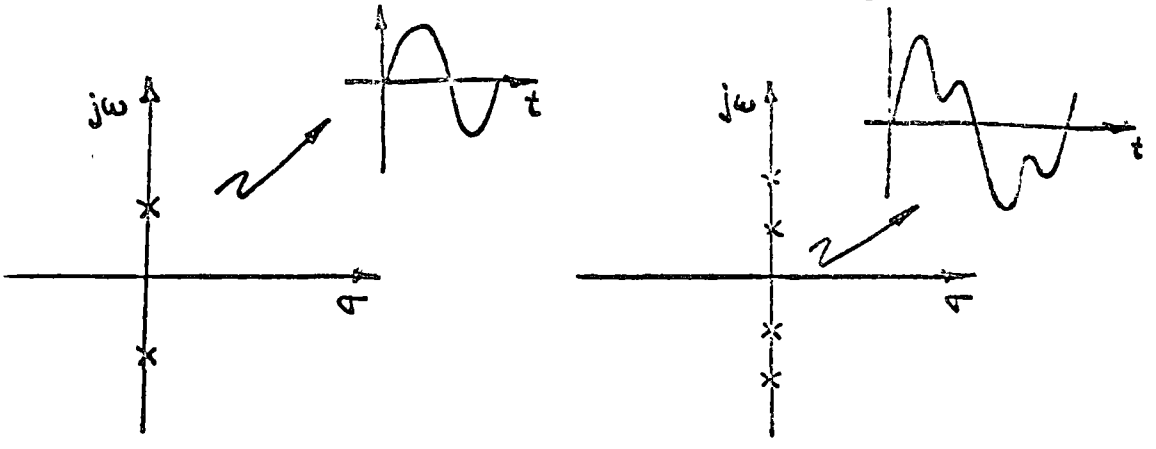


Figura 1.3.3

c) Deberá buscarse una máxima estabilidad en los componentes que fijan tanto la amplitud como la frecuencia de oscilación.

1.3.2 Aplicaciones: En esta sección analizaremos los pasos seguidos para llegar a la realización práctica de un oscilador construido en base a un amplificador Operacional. Comenzaremos por analizar un circuito denominado oscilador por puente de Wien, el cual se muestra en la figura 1.3.4. Nuestro primer objetivo será el determinar el valor de A necesario para que el circuito oscile

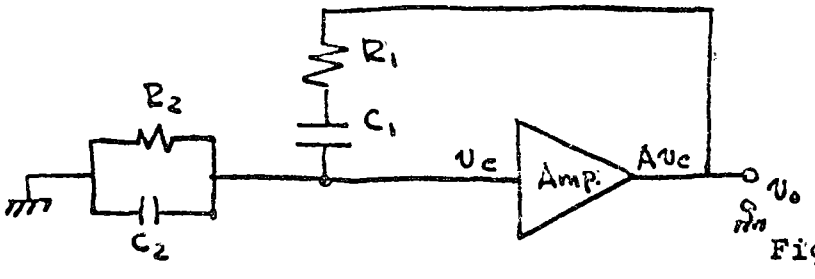


Figura 1.3.4

Suponiendo el amplificador ideal:

$$v_o = A_{ve}$$

$$v_e = v_0 \frac{Z_2}{Z_1 + Z_2} \quad \text{donde:}$$

$$Z_1 = R_1 + \frac{1}{jwc_1}$$

$$Z_2 = \frac{R_2 \frac{1}{jwc_2}}{R_2 + \frac{1}{jwc_2}} = \frac{R_2}{jwR_2C_2 + 1}$$

Si $R_1 = R_2 = R$ y $C_1 = C_2 = C$

$$v_e = v_o \frac{R}{(jwRC + 1)\left(R + \frac{1}{jwc} + \frac{R}{jwRC+1}\right)}$$

$$= v_o \frac{R}{jwR^2C + R + \frac{jwrC+1}{jwC} + R}$$

$$= v_o \frac{1}{R+2 + j\left(wRC - \frac{1}{wc}\right)}$$

Analizando el circuito como un sistema realimentado obtenemos lo mostrado en la figura 1.3.5

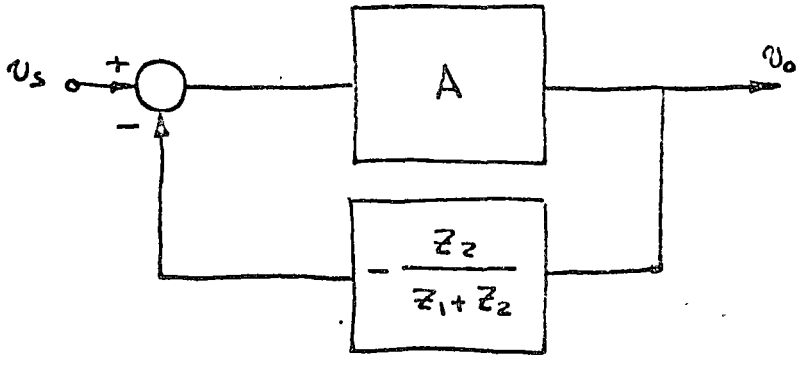


Figura 1.3.5

De acuerdo con el criterio de Barkhausen tendremos oscilación cuando:

$$-\frac{AZ_2}{Z_1+Z_2} = -1$$

O sea cuando

$$A\frac{R}{1 + jwRC} = R + \frac{1}{jwc} + \frac{R}{1+jwRC}$$

Suponiendo $1 + jwRC \neq 0$

$$AR = R(1 + jwRC) + \frac{1+jwRC}{jwC} + R$$

$$= 3R + jwR^2C - \frac{j}{wc}$$

igualando partes reales e imaginarias

para la parte Real $AR = 3R$

$$A = 3$$

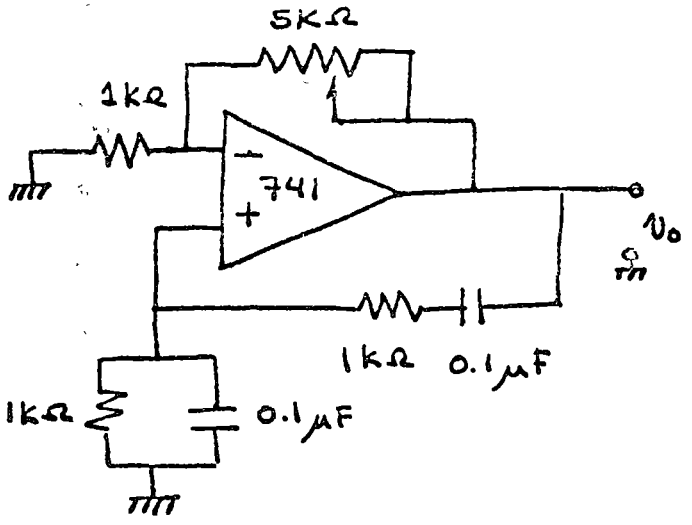
para la parte imaginaria

$$0 = wR^2C - \frac{1}{wC}$$

$$w^2R^2C^2 = 1$$

$$W = \frac{1}{RC} \qquad f = \frac{1}{2\Pi RC}$$

La realización de este oscilador es muy sencilla y se muestra en l la figura 1.3.6



$f = 1.6KH_z$

Figura 1.3.6

El potenciómetro deberá ajustarse para obtener máxima pureza de la señal.

Un problema de este circuito es la necesidad de efectuar ajustes en el potenciómetro, para evitar el problema se puede substituir la resistencia variable por una combinación de datos y resistencias como la mostrada en la figura 1.3.7, en este circuito, el valor de la resistencia entre los puntos A y B variará dependiendo del voltaje N_{AB} tal como se muestra en la gráfica

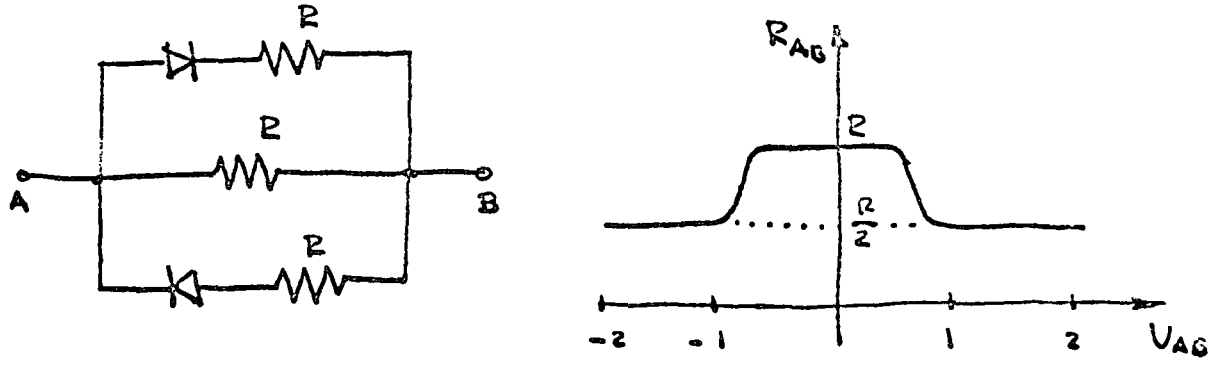


Figura 1.3.7

Podemos inclusive alterar los puntos en los cuales cambia el valor de la resistencia y por tanto controlar la amplitud del Voltaje de Salida.

Otra manera de limitar la amplitud de salida y hacer más estable el oscilador es mediante un JFET conectado como resistencia variable tal como se muestra en la figura 1.3.8

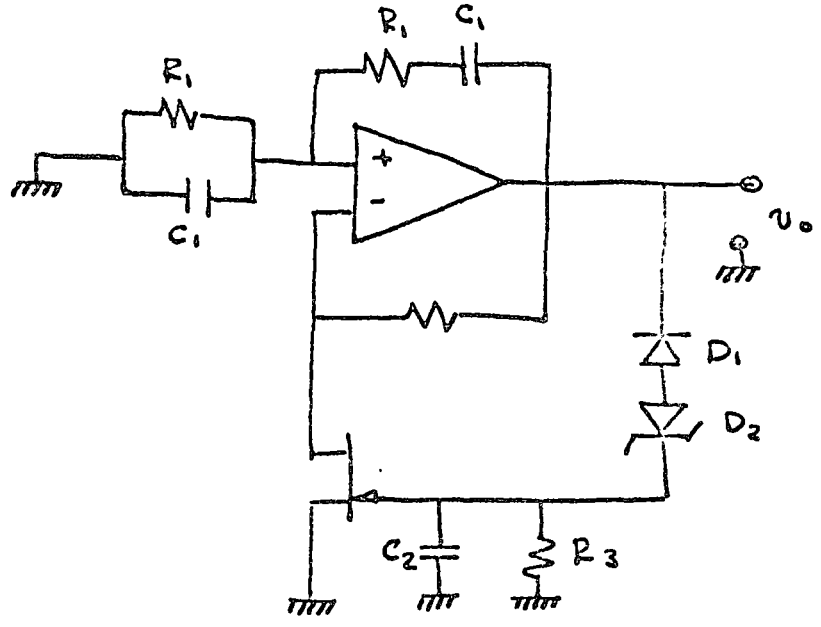


Figura 1.3.8

1.4 Filtros Activos.

1.4.1 Introducción: La teoría de los filtros activos también se apoya en la teoría de sistemas, mas aún, es la misma teoría mediante la cual se estudia el comportamiento en el dominio de la frecuencia de circuitos R-L-C, no es por tanto, nada "nuevo" dentro del campo técnico. La novedad del filtro activo se basa en los siguientes hechos:

a) Se dispone de buenas aproximaciones al Amplificador ideal a muy bajo costo.
b) Es difícil trabajar con inductores a bajas frecuencias.
c) Es más barato trabajar resistencias y capacitores que con inductores en circuitos integrados híbridos.
d) Los filtros pasivos de"alto orden" producen en general gran atenuación de la señal.

En resumen: Mediante el empleo de Amplificadores, resistencias y capacitores se pueden implementar redes selectivas que en ciertos casos son mas económicas y flexibles que los filtros tradicionales.

A continuación presentaremos los principales tipos de redes selectivas implementada mediante algún tipo de red activa. Esta presentación tiene el fin de ilustrar los principios básicos de la sintetización de filtros mediante elementos activos. Para un análisis mas exhaustivo referimos al lector a las referencias incluidas al final de la sección.

1.4.2 Filtros Paso Bajas: Un filtro activo paso bajas presenta la siguiente característica

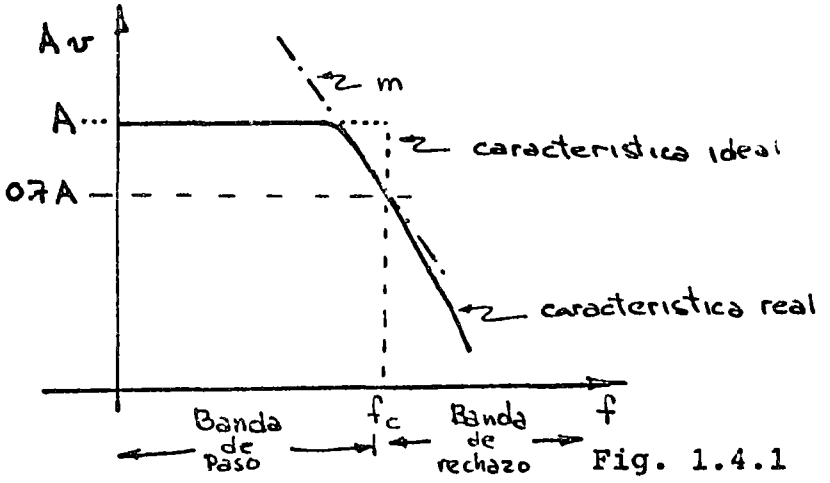


Fig. 1.4.1

La característica mostrada en la figura 1.4.1 puede aproximarse

mediante una función de segundo orden de la forma:

$$H(s) = \frac{A}{a_2 s^2 + a_1 S + 1} \qquad \text{ec. 1.4.1}$$

Una realización de esta función (Debida a Sallen y Key) se muestra en la figura 1.4.2

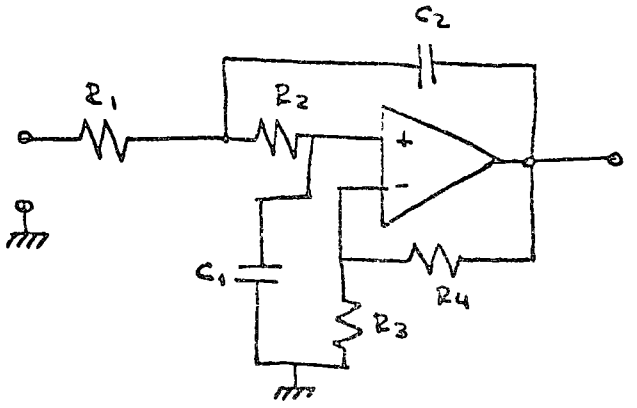


Fig. 1.4.2

Los parámetros de la ecuación 1.4.1 correspondientes al circuitc mostrado en la figura 1.4.2 son:

$$A = 1 + \frac{R_4}{R_3} \qquad a_2 = R_1 R_2 C_1 C_2$$

$$a = \frac{R_2 R_3 C_1 + R_1 R_3 C_1 - R_1 R_4 C}{R_3}$$

Dependiendo de la posición de los polos del sistema en el plano complejo podemos detener diferentes tipos de respuesta en el dominio de la frecuencia; por ejemplo una caracteristica de Bando de paso plana se obtiene si los polos estan en un circulo en el semplano izquierdo (Filtro Butterworth) cuya característica se muestra para n=2 y n = 4

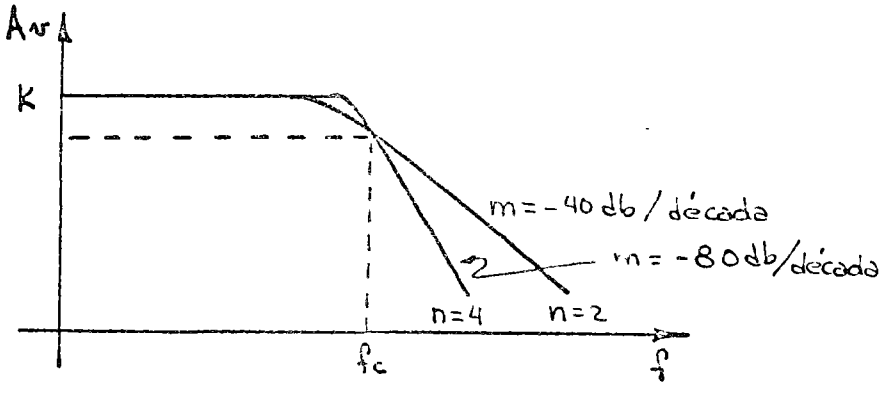
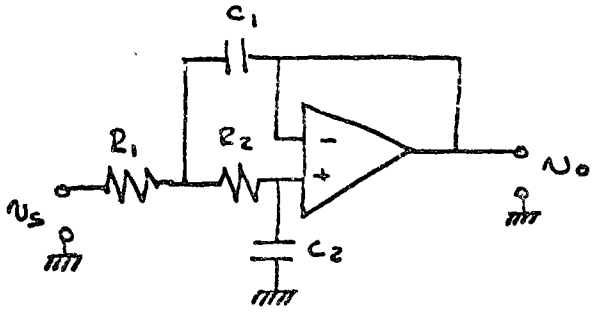


Fig. 1.4.3

$$H(jw) = \frac{K}{1 + (\frac{W}{wc})^{2n}}$$

Ejemplos de Gráficas empleadas para la obtención de los valores correspondientes a R_1, R_2, R_3, C_1 y C_2 se encuentran en el apéndice - (gráficas tomadas del libro "Manual of Active Filter Design" por J. L. Hilburn y D.E. Johnson Ed. Mc.Graw Hill).

Otra realización de una característica Maximamente plana es la mostrada en la figura 1.4.4



$A_V = 1$ en la banda de paso.

Fig. 1.4.4

Para este circuito:

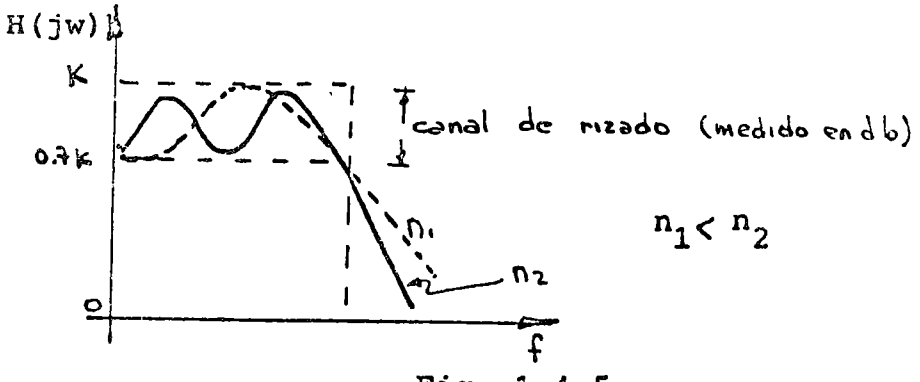
$$C_1 = \frac{R_1 + R_2}{2 R_1 R_2 w_c}$$

$$C_2 = \frac{2}{(R_1 + R_2) w_c}$$

R_1 y R_2 se escogerán en función de las características del amplificador operacional.

Otra característica común en filtros es la de Chebyshev, que presenta mejores características de corte. (M mayor que en el tipo - - Buttherworth) pero a costa de tener una banda de paso con rizado. La gráfica de este tipo de filtro se muestra en la figura 1.4.5

$$H(jw) = \frac{k}{1 + \varepsilon^2 C_n^2 \frac{w}{w_c}}$$



$n_1 < n_2$

Fig. 1.4.5

donde ε es una constante relacionada con el rizado y C_n es un polinomio de Chbyshev de primera clase y orden n (ver ejemplo de curvas pa

ra diseño en el apéndice C). Finalmente, un filtro cuya variación de fase es lineal con la frecuencia puede obtenerse si en la figura 1.4.4 hacemos:

$$C_1 = \frac{R_1 + R_2}{3\, R_1 R_2 w_c} \qquad C_2 = \frac{3}{(R_1 + R_2) w_c}$$

En el apéndice C se presentan familias para calcular los valores de los elementos en función de los parámetros del circuito.

1.4.3 Filtro paso Altas: La característica de éste se muestra en la figura 1.4.7

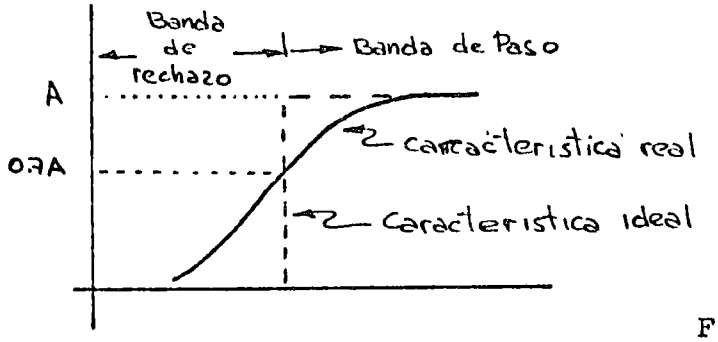


Fig. 1.4.7

también en este tipo de filtros tendremos los casos de respuesta - Butterworth, Chbyschev y fase lineal siendo las configuraciones las duales de la sección 1.4.2.

La función de transferencia estará dada por (caso de segundo orden).

$$H(s) = \frac{As^2}{s^{2+a_1 s+a_o}}$$

La realización de Sallen y Key es:

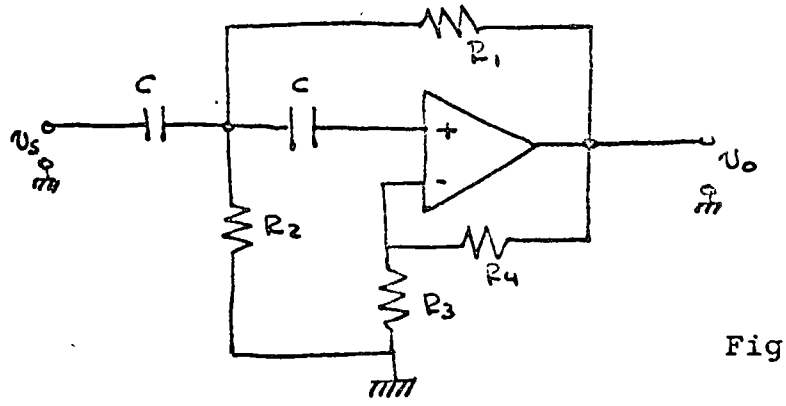


Fig. 1.4.8

Para la realización de la figura 1.4.8

$$A = 1 + \frac{R_4}{R_2}$$

$$a_1 = \frac{2}{R_2 C} - \frac{R_4}{R_1 R_3 C}$$

$$b = \frac{1}{R_1 R_2 C^2}$$

En el apéndice C se muestran las fórmulas para el cálculo de los elementos asi como ejemplos de las gráficas auxiliares mencionadas en la sección 1.4.2.

Otra realización de la característica Butterworth se muestra en la figura 1.4.9

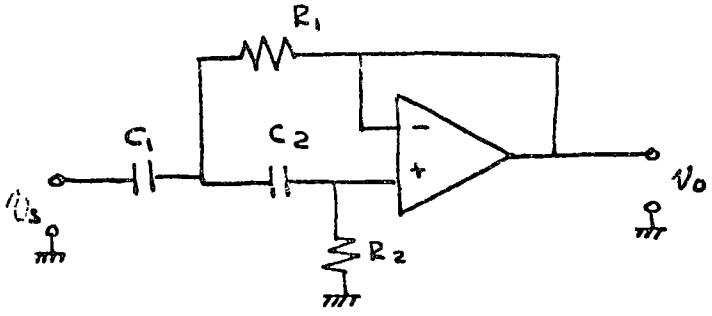


Fig. 1.4.9

Este circuito funcionará también para el caso de respuesta de cambio de fase lineal con las mismas fórmulas que corresponden a la figura 1.4.4.

1.4.4 Filtros Pasa Banda: Este tipo de circuitos permiten el paso de señales comprendidas entre dos frecuencias dadas, tal como se muestra en la figura 1.4.10. Existen esencialmente dos técnicas para la realización de estos filtros, dependiendo del ancho de la banda de paso.

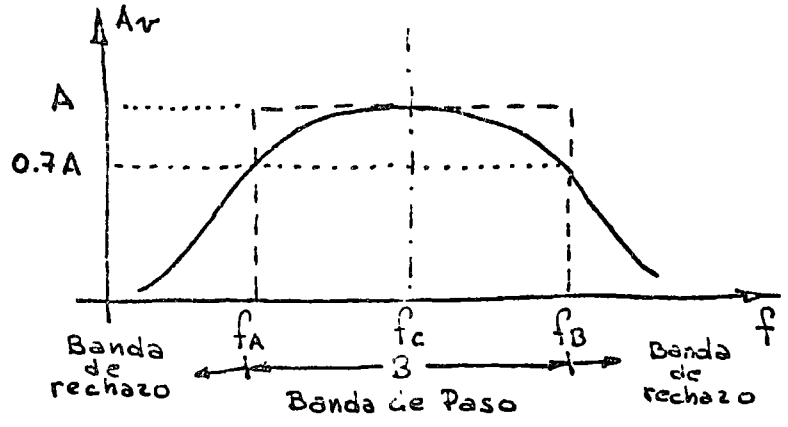


Fig. 1.4.10

Si $B = f_E - f_A$ es grande podemos conectar en cascada dos filtros en la forma mostrada en la figura 1.4.10.

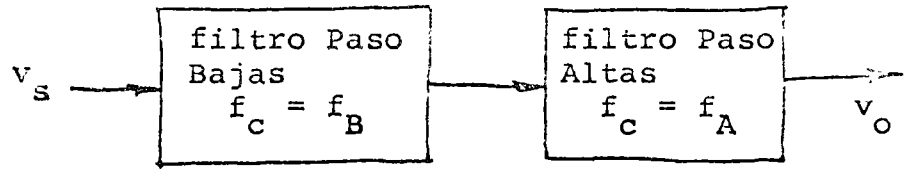


Fig. 1.4.11

Si B es pequeño, la solución será un circuito de tipo resonante centrado en f_c. Una aproximación de segundo orden para este caso estaría dada por:

$$H(s) = \frac{ks}{s^2+Bs+w_c^2}$$

Para este caso $A = \frac{k}{B}$

$Q = \frac{w_c}{B}$ (Q factor de merito que indica la selectividad del filtro)

La realización de esta función, propuesta por Kerwin y Huelsman se muestra en la figura 1.4.12, esta realización es adecuada para $Q < 4$.

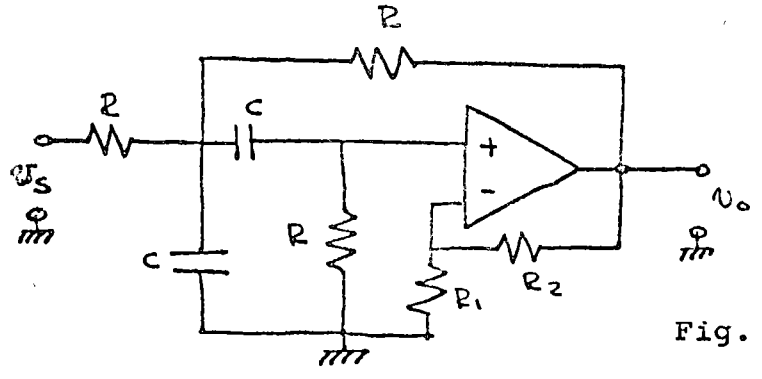


Fig. 1.4.12

$$K = \frac{A}{RC} \qquad \omega_c^2 = \frac{2}{R^2C^2}$$

$$B = \frac{4-A}{RC} \qquad A = 1 + \frac{R^3}{R_2}$$

Para obtener filtros con $Q > 5$ podemos recurrir a un circuito de múltiple realimentación como el mostrado en la figura 1.4.13

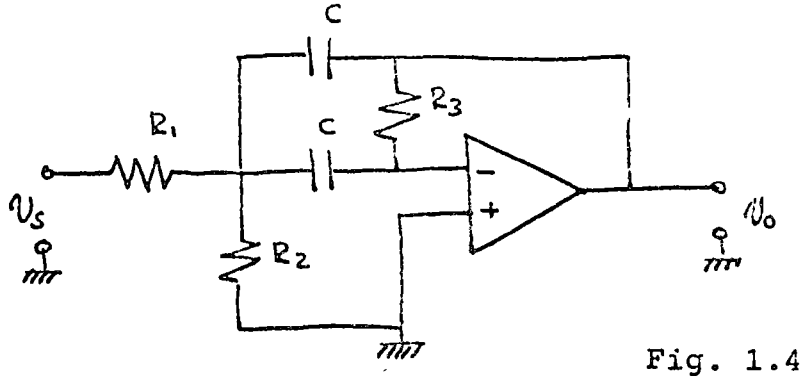


Fig. 1.4.13

En este circuito existirá un defasamiento de 180°entre v_s y v_o debido a la conexión inversora del A.O. los parámetros del circuito están dados por:

$$K = -\frac{1}{R_1 C} \qquad B = \frac{2}{R_3 C}$$

$$\omega_c^2 = \frac{1}{R_3 C^2}\left(\frac{1}{R_1} + \frac{}{R_2}\right)$$

Existe una gran variedad de realizaciones aparte de las presentadas como son filtros de variable de estado de realimentación positiva, bicuadráticos etc. Sin embargo aunque no han sido presentados en este curso, el diseñador interesado puede referirse a la literatura especializada para encontrar la teoría adecuada a estas y otras aplicaciones de redes RC en conjunción con A.O.

Finalmente, en el apéndice B hemos incluido otros circuitos y sus correspondientes fórmulas de diseño, sugerimos estudien y traten de realizar algunos de estos circuitos a fin de ganar familiaridad con nuevas configuraciones y con las limitaciones que éstas imponen sobre los elementos activos empleados.

1.5 Circuitos Digitales.

Existen aplicaciones en las cuales por necedidad o conveniencia el ingeniero en comunicaciones tiene que tomar en cuenta algún procedimiento de señales digitales en su sistema; es nuestra intención en esta parte del capítulo, el señalar las principales características tanto de las familias como de algunos elementos de dichas familias que son de especial importancia en los sistemas de comunicaciones.

1.5.1 COMPARACION DE FAMILIAS LOGICAS:

A.- Puntos de Comparación. Existe una infinidad de datos si tomamos en cuenta los de cada uno de los integrantes de una cierta familia lógica, sin embargo existen algunos que son especialmente relevantes al diseño global del sistema cuyo diseño se esté considerando.

Los parámetros de comparación mas aceptados son:

a.- Consumo de potencia: Dado lo extensivo que puede ser un sistema digital, es muy importante el consumo de potencia de cada uno de los elementos que lo integran, ya que afectará grandemente el diseño de otros subsistemas, por ejemplo, fuente de poder, Bastidor e incluso el local en que se instale el equipo.

b.- Fanout: Nos indica cuantos elementos lógicos pueden conectarse a la salida de cada uno de dichos elementos. Esto es si un elemento tiene Fanout de 10, se podrán conectar 10 elementos de la misma familia a su salida.

c.- Margen de Ruido: Es una medida de la inmunidad de los miembros de la familia a señales erpureas, este parámetro puede ser de capital importancia en ambientes electricamente ruidosos electricamente hablando.

d.- Velocidad y :Retraso de propagación: Son dos parametros intimamente relacionados que nos dan idea de la rapidez con

que cambia el estado lógico a la salida de un elemento, con — respecto a la variación en su salida.

Otros elementos de juicio que pueden ayudar a seleccionar la familia lógica adecuada pueden ser:

- disponibilidad en el mercado
- variedad de elementos
- Densidad de elementos individuales por "paquete"
- Compatibilidad con las fuentes de poder disponibles en el sistema
- Rango de operación con respecto a variaciones ambientales
- Secillez de manejo etc...

B.- Familias Lógicas

Las familias mas comunes son:

TTL	Lógica	Transistor-transitor
ECL	Lógica	Acoplado por Emisor
CMOS	Lógica	MOS Complemetaria
DTL	Lógica	Transistor-diodo
RTL	Lógica	Resistencia-transistor
HTL	Lógica	De Alto Nivel

De estas familias las mas empleadas son las tres primeras. - Cabe hacer notar que existe gran variedad de elementos provenientes de la tecnológica MOS (metal oxido semiconductor), pero dado que su uso es especilizado, en circuitos de alta densidad (L.S.I.), como son memorias, microprocesadores etc., no — los analizaremos como "familia lógica".

C.- Comparación entre familias lógicas

T T L

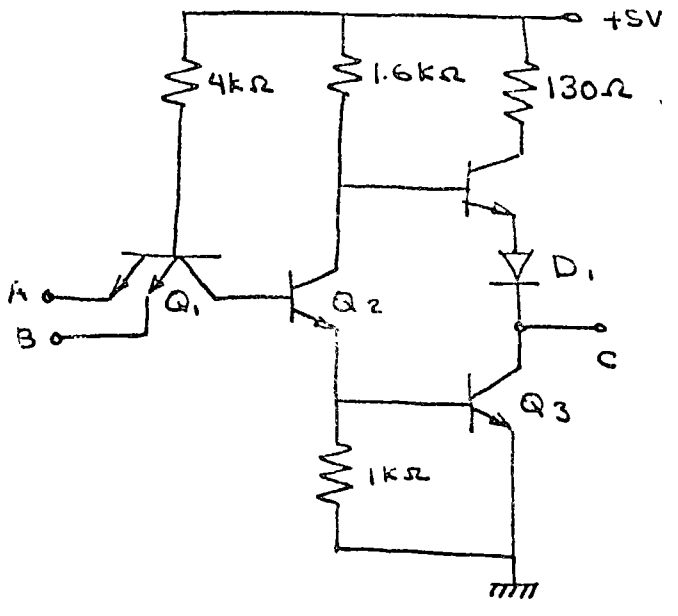
Circuito básico	-	AND
Fanout tipico	-	10

Polarización	-	5 V ± 10%
Margen de ruido	-	Bueno I V
Costo	-	Bajo
Disponibilidad	-	Amplia

En lo que respecta a la velocidad y consumo de potencia, tenemos que diferenciar entre "subfamilias" T T L

		Consumo por compuerta	retraso por compuerta	Frecuencia maxima de operación
T T L	Standar	12mW	10 nS	35 MHz
T T L	Alta Velocidad	22mW	6 nS	50 MHz
T T L	Schottky	19mW	3 nS	125 MHz
T T L	baja potencia	1mW	33 nS	3 MHz
T T L	Schottky baja potencia	2mW	9 nS	45 MHz

El circuito de una compuerta NAND TTL Standar se muestra en la figura - 1.5.1



$C = \overline{A \cdot B}$

Fig. 1.5.1

CMOS

Circuito básico NAND ó NOR

Fanout típico	50	
Polarización	3 a 18V	
Margen de ruido	muy bueno	30 a 45% de la polarización
Costo	mediano	
Disponibilidad	pequeña	
Consumo por compuerta	0.01 mW estático 1 mW 1 MHz	
Retrazo por compuerta	70 nS	
Frecuencia máxima de Operación	5 MHz	

El circuito típico de un inversor CMOS se muestra en la figura 1.5.2

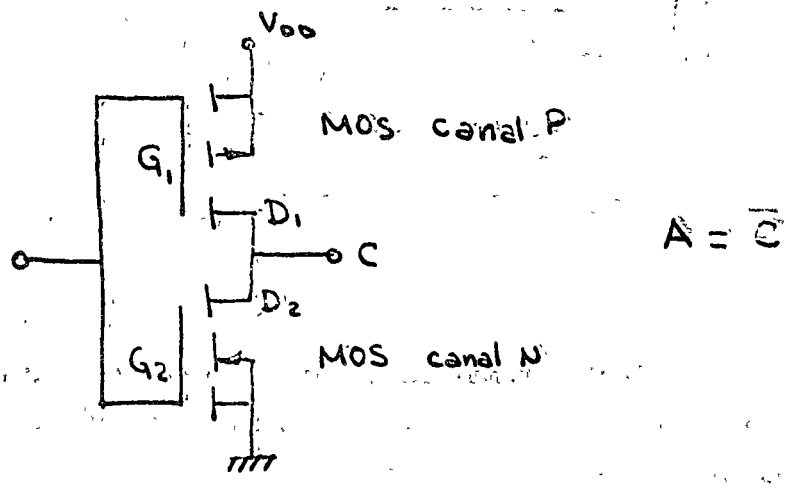


Figura 1.5.2

E C L

Circuito básico	OR y NOR
Fanout típico	25 (10 en las de mas alta velocidad)
Polarización	5.2 V ± 10%
Margen de ruido	pobre 0.5V
Costo	Alto
Disponibilidad	Casi nula
Consumo por compuerta	22 a 60 mW mas la carga
Retraso por compuerta	4 a 1 nSeg
Frecuencia máxima de operación	70 a 400 MHz

El circuito típico de una compuerta OR y NOR se muestra en la figura — 1.5.3

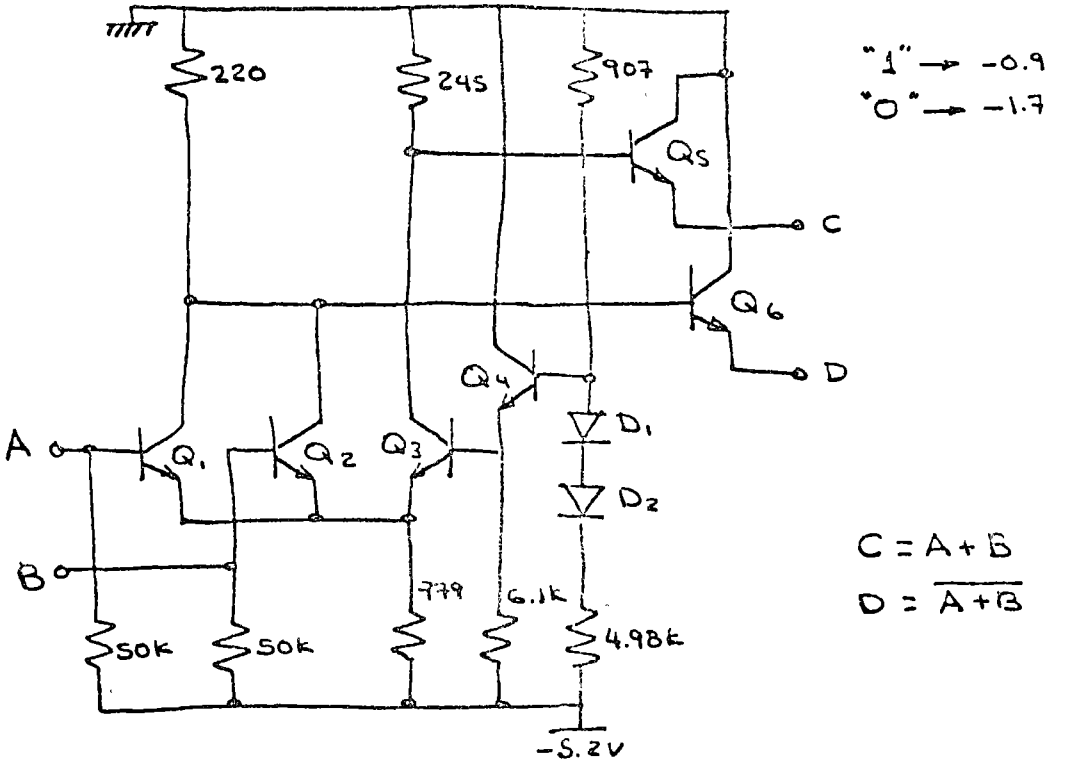


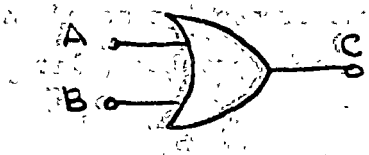
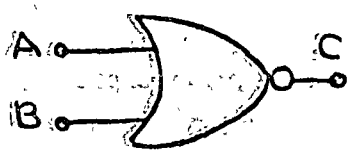
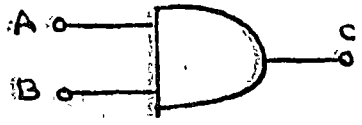
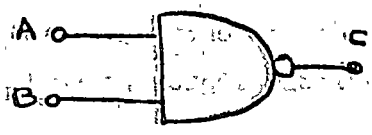
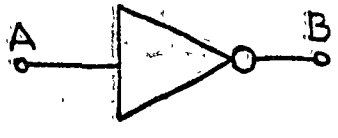
Fig. 1.5.3

Las restantes familias lógicas son de popularidad decreciente c excepto HTL cuya alta inmunidad al ruido (≈ 5 V) la hace muy deseable en circuitos industriales de control.

1.5.2 DEFINICION DE LOS ELEMENTOS LOGICOS.

A continuación presentamos un resumen de las definiciones de los elementos mas empleados en comunicaciones

A.- COMPUERTAS

SIMBOLO	TABLA DE VERDAD (A B C)	NOMBRE Y FUNCION
	0 0 0 0 1 1 1 0 1 1 1 1	OR (o lógico) C = A + B
	0 0 1 0 1 0 1 0 0 1 1 0	NOR (o lógico negado) $C = \overline{A + B}$
	0 0 0 0 1 0 1 0 0 1 1 1	AND (y lógico) C = A • B
	0 0 1 0 1 1 1 0 1 1 1 0	NAND (y lógico negado) $C = \overline{A \cdot B}$
	0 0 0 0 1 1 1 0 1 1 1 0	Exclusive OR (o lógico exclusivo) $C = (A+B) \cdot \overline{AB}$ $= A \oplus B$
	0 1 1 0	INVERSOR $B = \overline{A}$

Teorema de Morgan: Un teorema que es especialmente útil para substituir compuertas AND por OR y viceversa es el teorema de Morgan, el cual para dos variables indica que

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

6.- Circuitos Biestables son elementos cuya salida no depende únicamente del estado actual de las variables de entrada, sino también del estado anterior del circuito, o sea que en cierta forma tienen "memoria", a continuación presentamos las tablas de verdad de los biestables (Flip-Flops) mas usuales.

a.- Biestable J-K Flanco positivo (preset y clear)

P	C	CLK	J	K	Q	integrado típic
L	H	X	X	X	H	7470
H	L	X	X	X	L	
L	L	X	X	X	inestable	
H	H	↓	L	L	Q_o	
H	H	↑	H	L	H	
H	H	↑	L	H	L	
H	H	↑	H	H	Toggle (cambia de estado con CLK)	
H	H	L	X	X	Q_o	

X indica indiferencia al estado lógico presente en esa entrada

↑ indica cambio en la transición 0 → 1 de la variable lógica presente en la terminal

H equivale a "1"

L equivale a "0"

b.- Biestable J-K Maestro-Esclavo (preset)

P	CIK	J	K	Q	integrado típico
L	X	X	X	H	
H	⊓	L	L	Q_o	74 L 71
H	⊓	H	L	H	
H	⊓	L	H	L	
H	⊓	H	H	Toggle	

indica que J y K deben permanecer constantes durante el período alto de la variable, y que la salida cambiará con el flanco de caida de 1 a 0 de dicha variable

c.- Biestables RS Maestro esclavo (prest y clear)

P	C	ClK	S	R	Q	integrado típico
L	H	X	X	X	H	
H	L	X	X	X	L	74 L 71
L	L	X	X	X	inestable	
H	H	⊓	L	L	Q_o	
H	H	⊓	H	L	H	
H	H	⊓	L	H	L	
H	H	⊓	H	H	indeterminada	

d.- Biestable tipo D flanco positivo (preset y clear)

P	C	CIK	D	Q	integrado típico
L	H	X	X	H	
H	L	X	X	L	74 74
L	L	X	X	inestable	
H	H	↑	H	H	
H	H	↑	L	L	
H	H	L	X	Q_o	

Existen otros tipos de circuitos biestales, sin embargo su operación es similar a los descritos anteriormente.

C.- Registros de corrimiento

Un registro de corrimientos es una serie encadenada de biestales - - - (JK, RS ó D) tal que un nivel lógico presentado a la entrada de registro es transferido de un biestable a otro de acuerdo a las variaciones del reloj tal como se muest a en la figura 1.5.4

Diagrama de tiempos(simplificado) de un Registro de Corrimiento

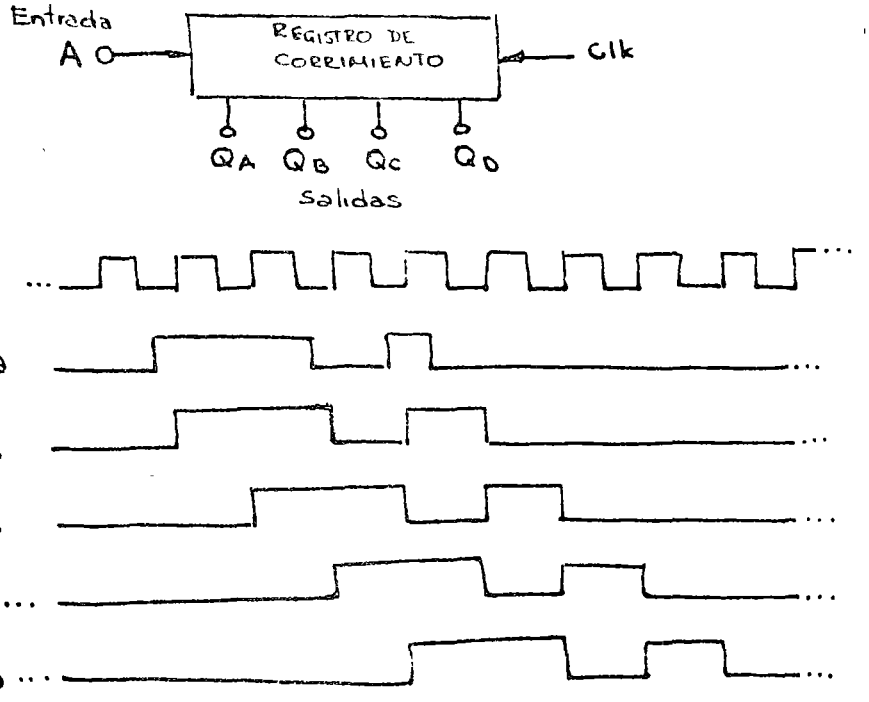
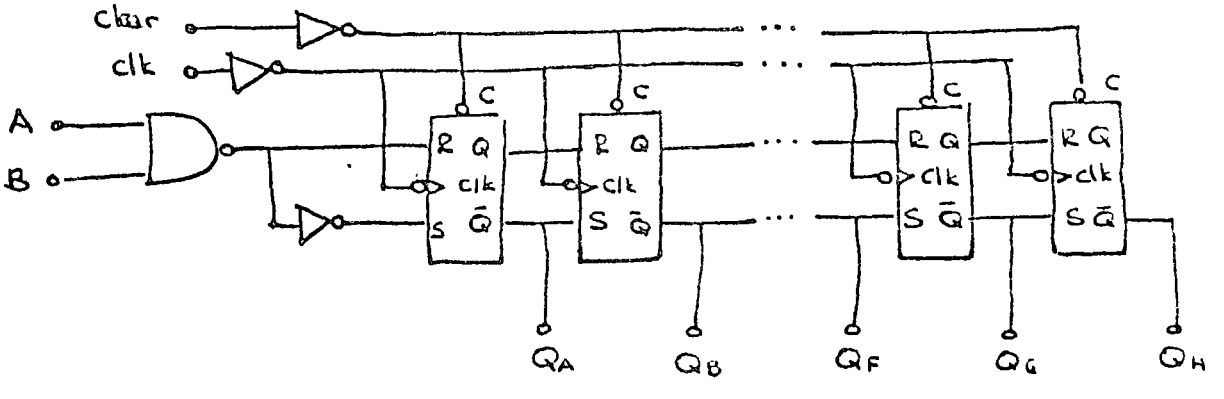


Fig 1.5.4

Implementación de un registro de corrimiento(74164)



$\diamond$ indica que la entrada sera activada en la transicion 1→0 del nivel lógico correspondiente

La aplicacion de registros de corrimiento como el mostrado, va desde transformaciones Serie → Paralelo de palabras digitales, hasta memorias de acceso seriado de 16 Kbits realizadas en tecnologia MOS.

1.6 CONVERTIDORES

1.6.1 OPERACION ELEMENTAL DE UN SISTEMA ELECTRONICO

El concepto general de un sistema electrónico corresponde al diagrama de bloques que se muestra en la figura 1.6.1.

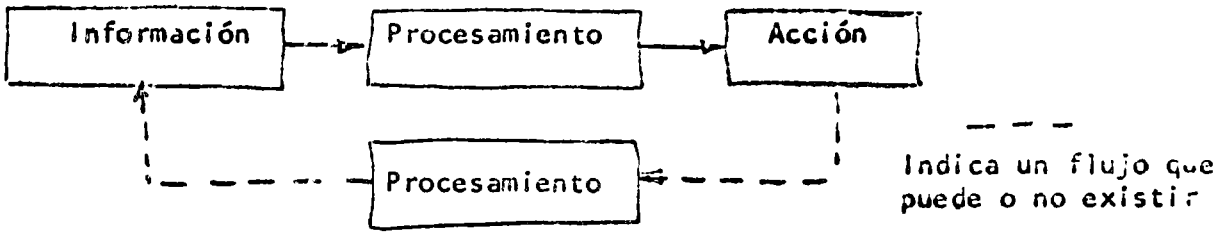


Figura 1.6.1.

En este diagrama se presenta la siguiente idea: El mundo físico nos proporciona la información necesaria para poder decidir el curso de acción mas adecuado, esta acción puede o no generar modificaciones a la información original, en algunos casos (sistema retroalimentado) esta modificación a la información original deberá tomarse en cuenta para modificar el curso de acción. Lo anterior puede aclararse mediante un ejemplo.

Ejemplo 1.6.1. Si se desea un sistema que permita conocer la altura a la cual se encuentra un avión, podemos obtener la información de altura a partir de la presión atmosférica absoluta, hacer que esta presión varie la resistividad de un cierto solido, detectar este cambio transformándolo a un voltaje mediante un puente de wheatstone, convertir este voltaje a corriente y finalmente darle significado físico mediante un galvanometro y una escala convenientemente graduada;

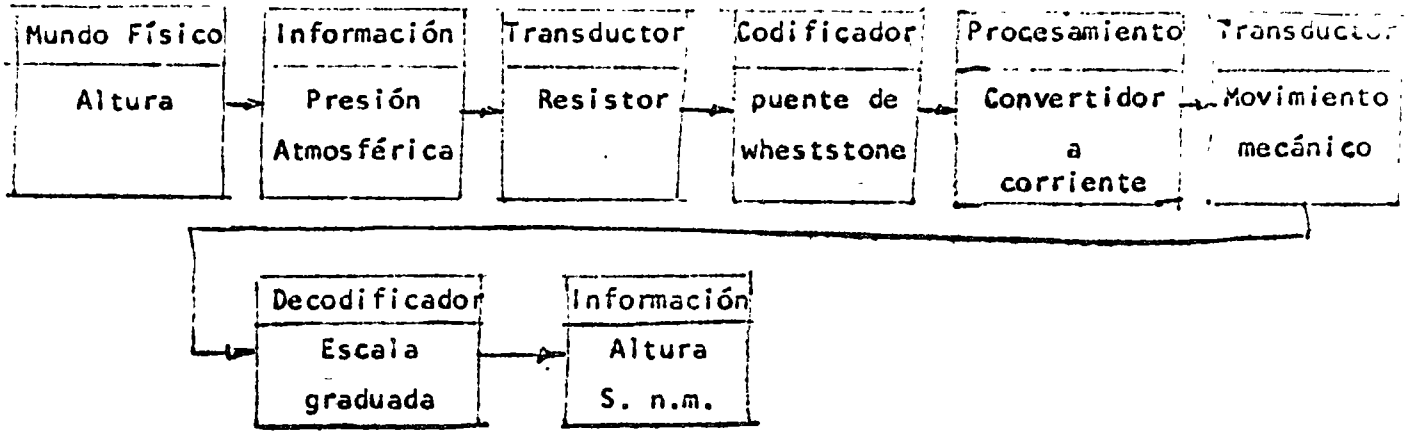


Figura 1.6.2

Podemos dividir el sistema en tres grandes bloques

1- Captación de la información y codificación de ésta en la variación de un parámetro eléctrico.

2- Procesamiento del parametro eléctrico y transformaciones de éste a otros parametros.

3- Decodificación de la información en forma útil al usuario (o al sistema dependiente del sistema en cuestión).

Nos interesa a nosotros la codificación y las transformaciones que esta codificación experimenta como parte de la operación del sistema.

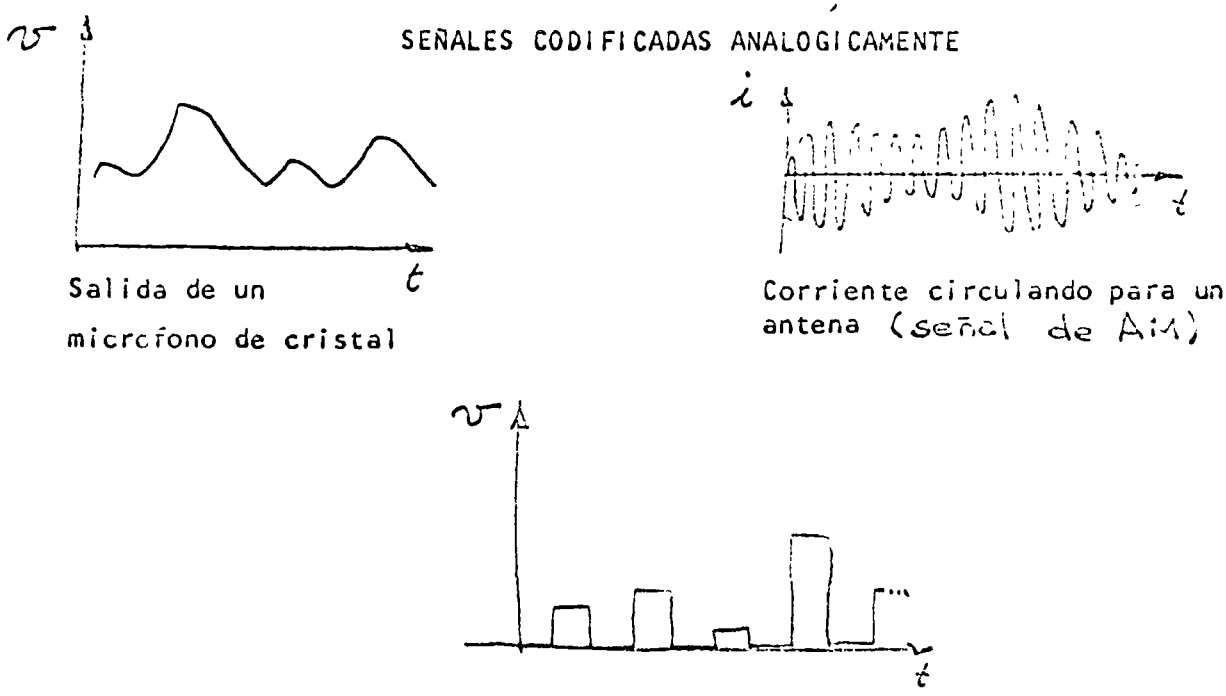
1.6.2- CODIFICACION DE INFORMACION EN SEÑALES ELECTRICAS

Nos centraremos en el estudio de las alternativas que existen para codificar una cierta información, obtenida mediante un transductor adecuado, en una señal eléctrica, de modo tal, que su procesamiento posterior sea lo mas eficiente posible.

Se presentan a primera vista tres alternativas (1):

1- Codificar la señal mediante la variación de la magnitud del parametro electrico (carga, corriente o voltaje), por ejemplo la señal de AM (amplitud modulada) empleada en radiodifusoras; a esta forma de

codificación se le denomina Analógica, hay que hacer énfasis en que la información está contenida en la magnitud del parametro eléctrico como se muestra en la figura 1.6.3



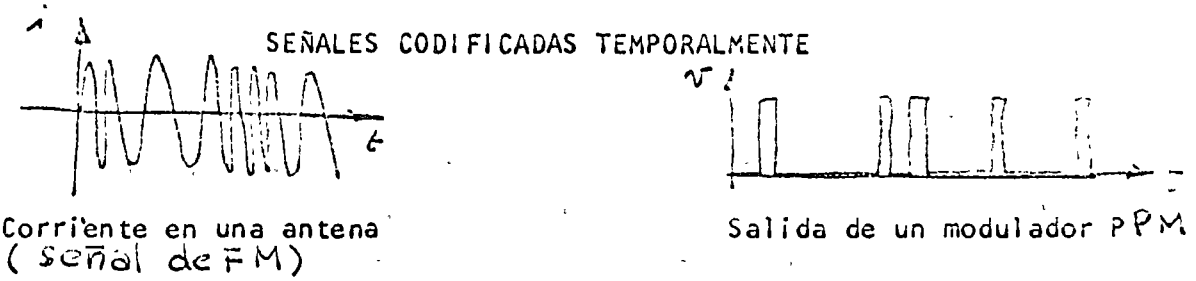
Salida de un micrófono de cristal

Corriente circulando para una antena (señal de AM)

Salida de un detector de video CCD (Charge conpled devices)

Figura 1.6.3

2- Codificar en la relación temporal existente entre dos características cualquiera de la señal eléctrica; por ejemplo: Frecuencia de la señal, Ancho de un pulso, posición de un pulso etc. Es evidente que en este tipo de codificación, al no intervenir la magnitud de la variable, es menos sensible al efecto aditivo del ruido.



Corriente en una antena (señal de FM)

Salida de un modulador PPM

Figura 1.6.4

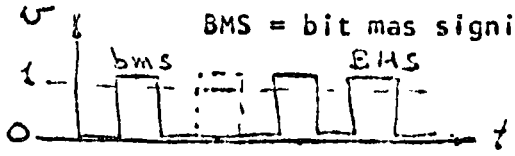
3- Codificar la señal digitalmente o sea asignándole un número, ya sea este mediante el número de veces que una cierta señal discreta se encuentre presente en un intervalo de tiempo dado, o directamente como una cifra (generalmente expresada en forma binaria) ya sea esta en forma serie (n dígitos en una línea) o en paralelo (n líneas); este tipo de codificación es la que posee mayor inmunidad al ruido, siempre y cuando su amplitud no sea comparable a la señal deseada; más aún, este tipo de codificación es suceptible de ser procesada a fin de añadir sedundancia con el fin de poder recuperar información perdida en proceso de transmisión

SEÑALES CODIFICADAS DIGITALMENTE

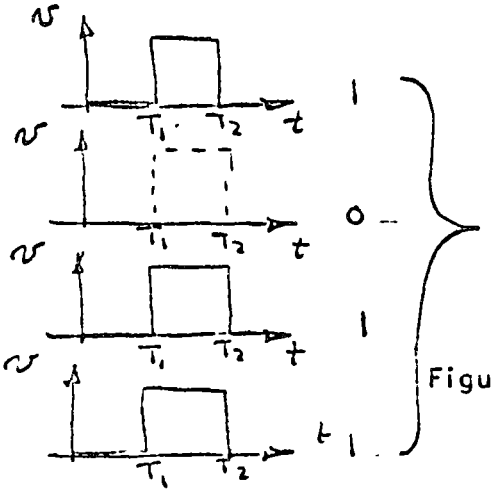
Salida de un contador geiger

bms = bit menos significativo

BMS = bit mas significativo



palabra digital serie de cuatro bits



palabra digital paralela de cuatro bits

Figura 1.6.5.

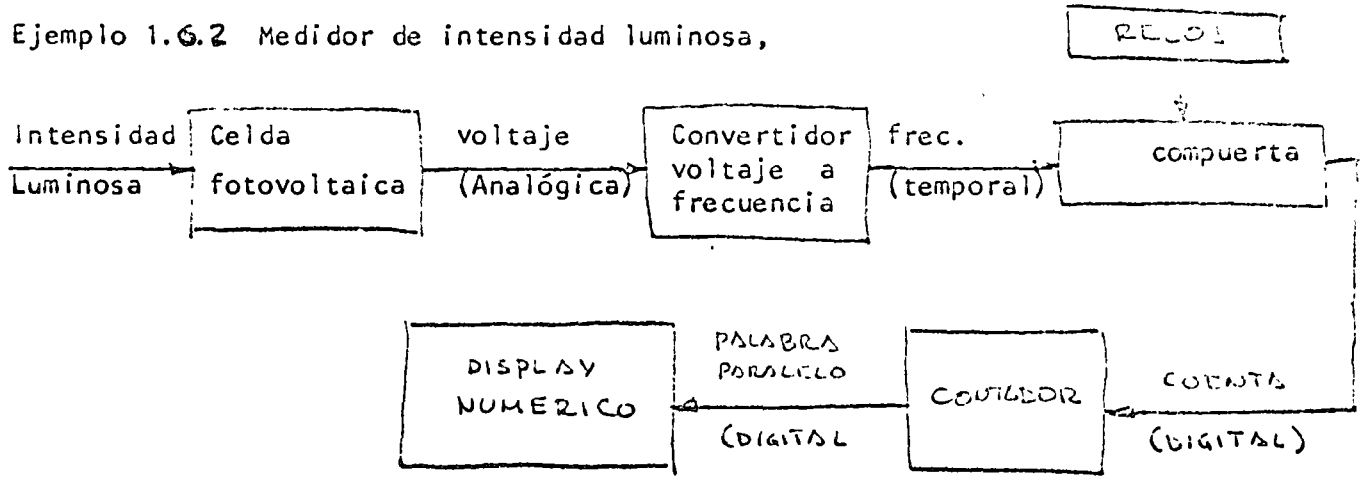
1.6

1.6.3 CONVERTIDORES DE TIPO DE CODIFICACION

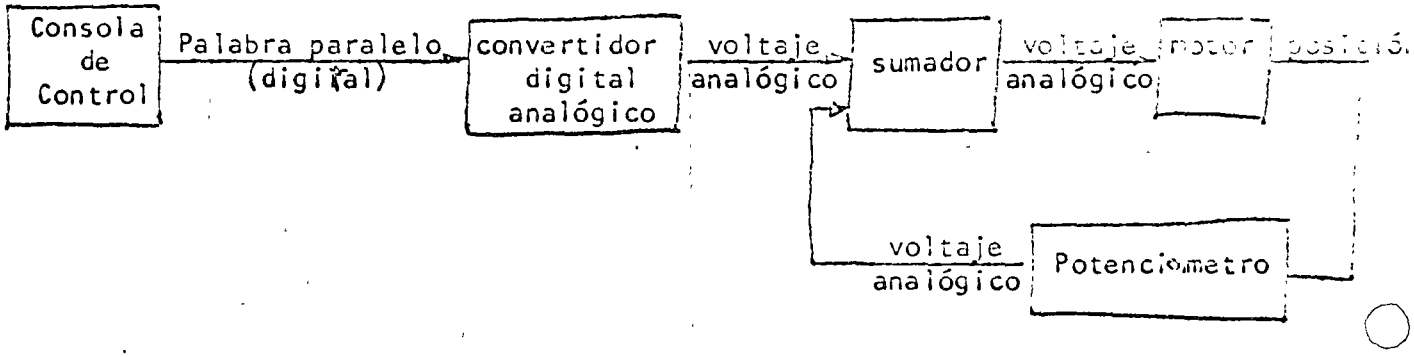
Al plantear un sistema electrónico desde el punto de vista de la adquisición, procesamiento y presentación o utilización de la información acerca de un cierto fenomeno físico, nos encontramos entre la necesidad de incluir varios tipos de codificación; por ejemplo, para adquirir información la codificación

analógica es la mas ususal (debido a que la mayor parte de los transductores codifican la variable física en forma analógica (2,3), sin embargo para procesamientos que involucran una extensa manipulación de la información, la codificación digital es la solución mas adecuada. A continuación se presentar ejemplos en el cual se muestran los cambios de codificación que una información sufre al pasar por un cierto sistema electrónico de medición y uno de control.

Ejemplo 1.6.2 Medidor de intensidad luminosa,



Ejemplo 1.6.3 Control digital de Posición Angular (4)



En este ejmplo el sumador puede ser digital y el potenciametro substituirse por una rueda codificada, realizando en este caso la conversión digital analógica antes del servo motor.

1.6.4 SISTEMAS CONVERTIDORES DE TIPO DE CODIFICACION

En la sección 1.6.3 se pone de manifiesto la necesidad de realizar conversiones de tipo de codificación en la mayoría de los sistemas electrónicos, en este capítulo analizaremos los tipos mas usuales de convertidores de codificación, sin tomar en cuenta los convertidores que trabajan en un mismo tipo o dominio de codificación por ejemplo:

Corriente a voltaje
Palabra serie a palabra paralelo
Carga a voltaje
etc.

A.- CONVERTIDORES ANALOGICO TEMPORAL

Para analizar este tipo de convertidores partiremos de una codificación analógica común: Magnitud del voltaje entre dos puntos; los sistemas más sencillos serían:

A.1 CONVERTIDOR VOLTAJE A FRECUENCIA

Este sistema conocido también como VCO ("Voltaje Controlled Oscilator") generará una forma de onda cuya frecuencia está relacionada linealmente con el voltaje que aparece en su puesto de entrada; una configuración empleada a menudo para lograr este propósito se muestra en la figura 1.6.6

CONVERTIDOR VOLTAJE A FRECUENCIA

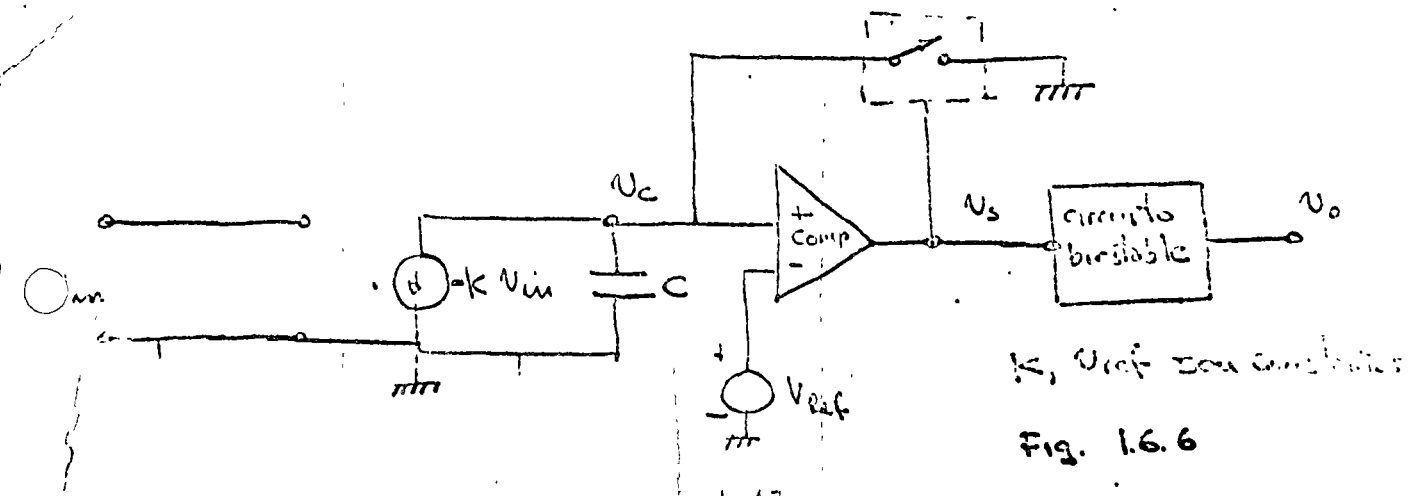


Fig. 1.6.6

Las formas de onda para $V_{in} = V_{in}(t)$ se muestran a continuación

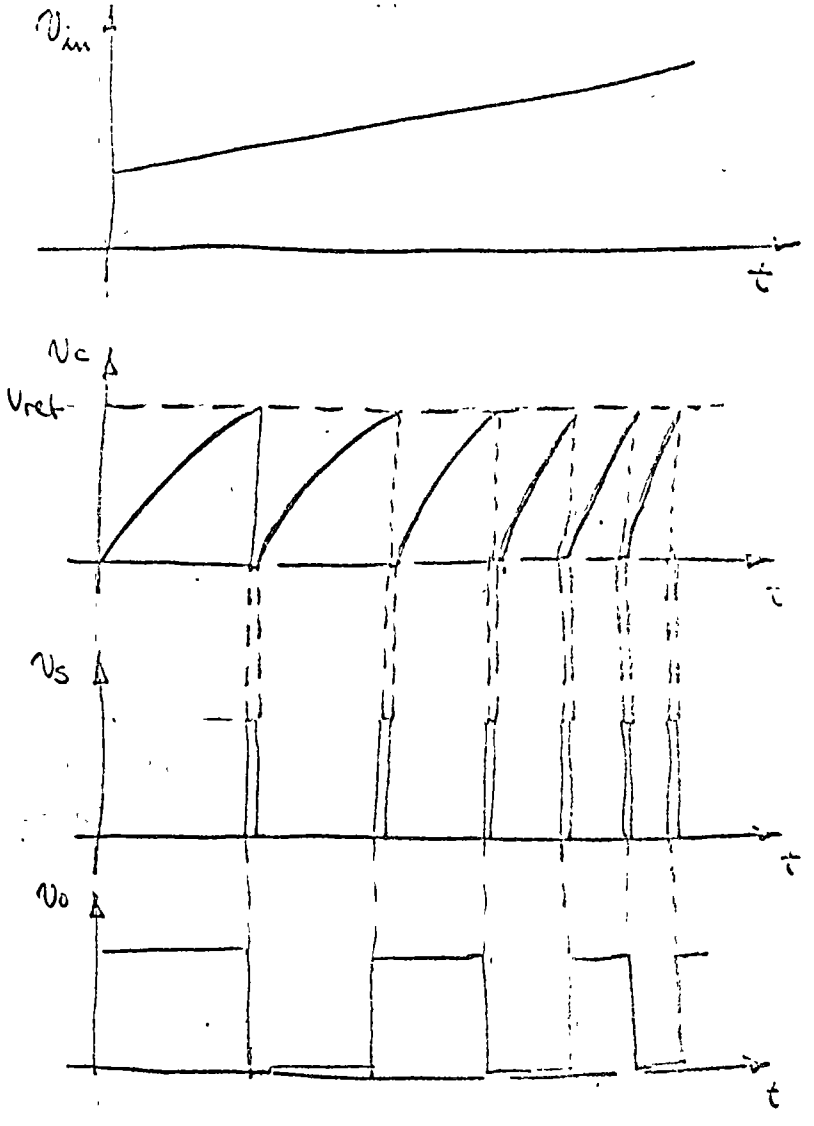


Figura 1.6.7

El circuíto mostrado en la figura, es muy sencillo de analizar desde el punto de vista intuitivo, sin embargo es difícil de implementar debido al interruptor, una realización práctica se encuentra en el circuíto generador de funciones 566 (5)el cual emplea dos fuentes de corriente

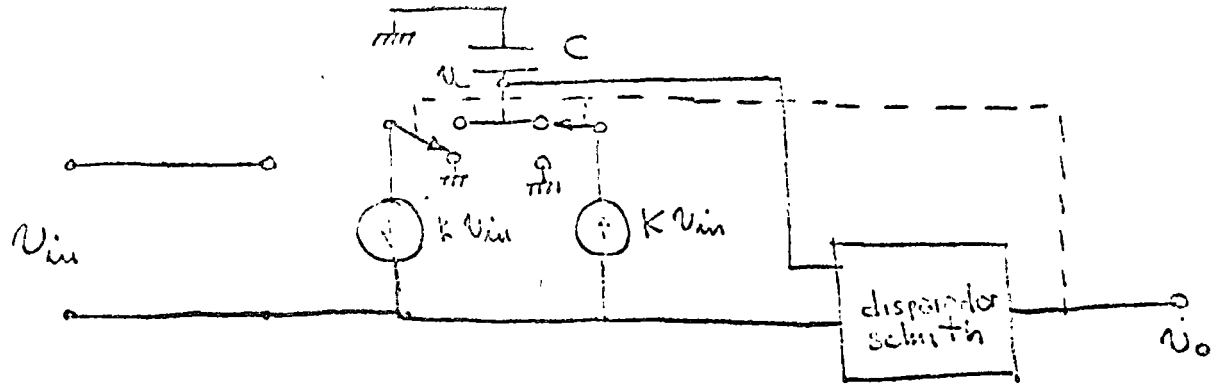


Figura 1.6.8

En este caso V_c será una onda triangular y no un diente de sierra. Cabe hacer notar que en este caso el problema relacionado con las grandes corrientes, que debe manejar el interruptor debido a la carga reactiva, se eliminan al descargar el capacitar mediante una fuente de corriente y no corto circuitando éste. En la figura 1.6.9 se muestran características típicas correspondientes a este circuíto (5).

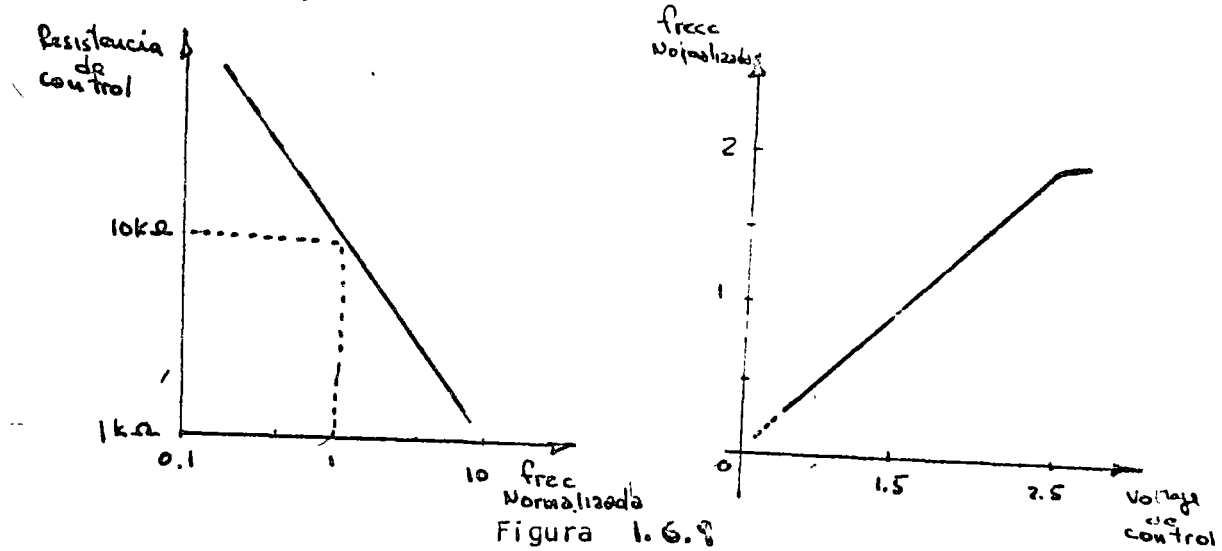


Figura 1.6.9

A.2 CONVERTIDOR VOLTAJE - ANCHO DE PULSO

El objeto de este circuíto es trasladar la información contenida en la magnitud de un cierto voltaje al ancho de un cierto pulso de voltaje o corriente, de amplitud constante. En su forma mas elemental este convertidor deberá constar de los siguientes sistemas:

a- Un sistema que nos permita tomar muestras de la señal analógica y mantenerlas (independientes de las variaciones de la señal analógica)

hasta terminar el proceso de conversión.

b- Un generador de rampa que nos relacione amplitudes de voltaje y tiempo en forma lineal.

c- Un comparador que determine el instante en el cual la rampa de referencia y la entrada analógica son iguales, para generar la onda de salida y controlan el sistema.

A continuación se muestra en la figura 1.6.10 la forma de realizar un circuíto de este tipo.

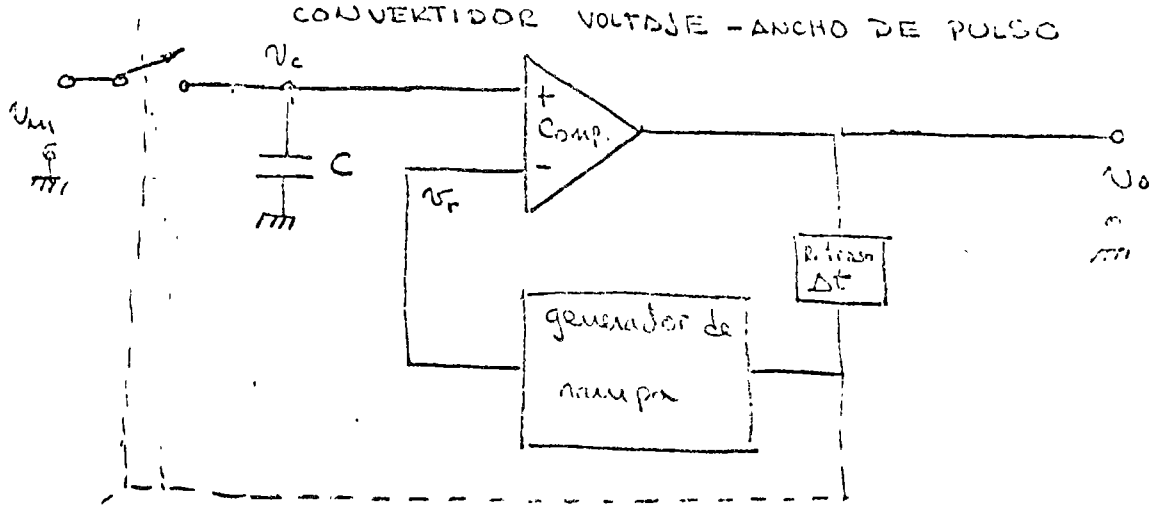
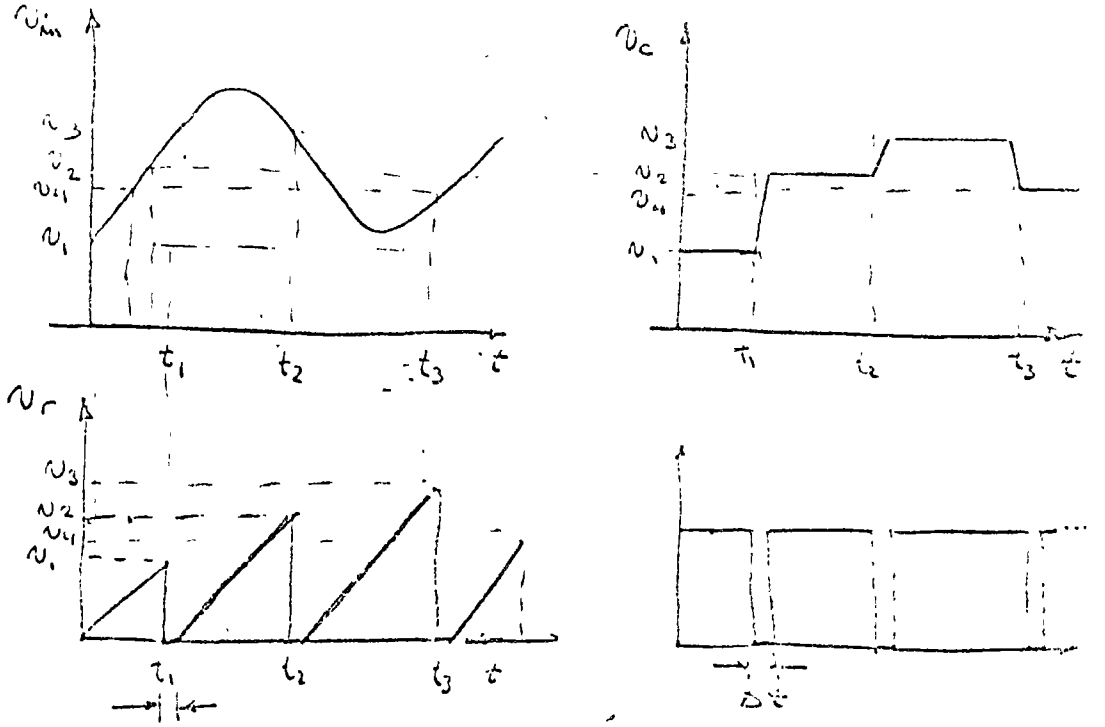


FIGURA 1.6.10



Este tipo de convertidor puede también realizarse generando una rampa variable (función de V_{in}) y una referencia fija, posteriormente analizaremos este circuito como parte de convertidores mas complejos.

Cabe hacer notar que en el proceso de conversión analógica temporal existe siempre una frecuencia máxima de V_{in} para un sistema convertidor dado esto es obvio en el sistema mostrado en la figura 1.6.10, en el cual, debido a la presencia del muestreador, cualquier variación (información) que se presente cuando el interruptor S está abierto (condición de mantenimiento) será ignorada.

B.- CONVERTIDORES TEMPORAL - DIGITAL

La operación de este tipo de convertidores es quizá la mas directa ya que en esencia involucra únicamente la cuantización de un cierto intervalo de tiempo o de el número de eventos que ocurren en un intervalo dado de tiempo. Tomemos por ejemplo la medición digital de la velocidad angular de un motor de combustión interna del cual conocemos los siguientes hechos:

a- Existen pulsos de alto voltaje que ocurren en el final del ciclo de compresión de cada pistón.

b- El ciclo de compresión ocurre en cada pistón a la mitad de la frecuencia correspondiente a la velocidad angular del motor (ciclo de cuatro tiempos)

c- Se requiere contar con información acerca del funcionamiento del motor cada segundo, en forma numérica.

Podemos entonces afirmar que un sensor de voltaje colocado en la línea de alto voltaje del distribuidor a la bujía contendrá información relativa a la velocidad angular del motor codificada en forma temporal, por tanto bastara un convertidor de codificación para obtener la información en la forma deseada, un sistema que realiza este propósito se encuentra en la figura 1.6.11

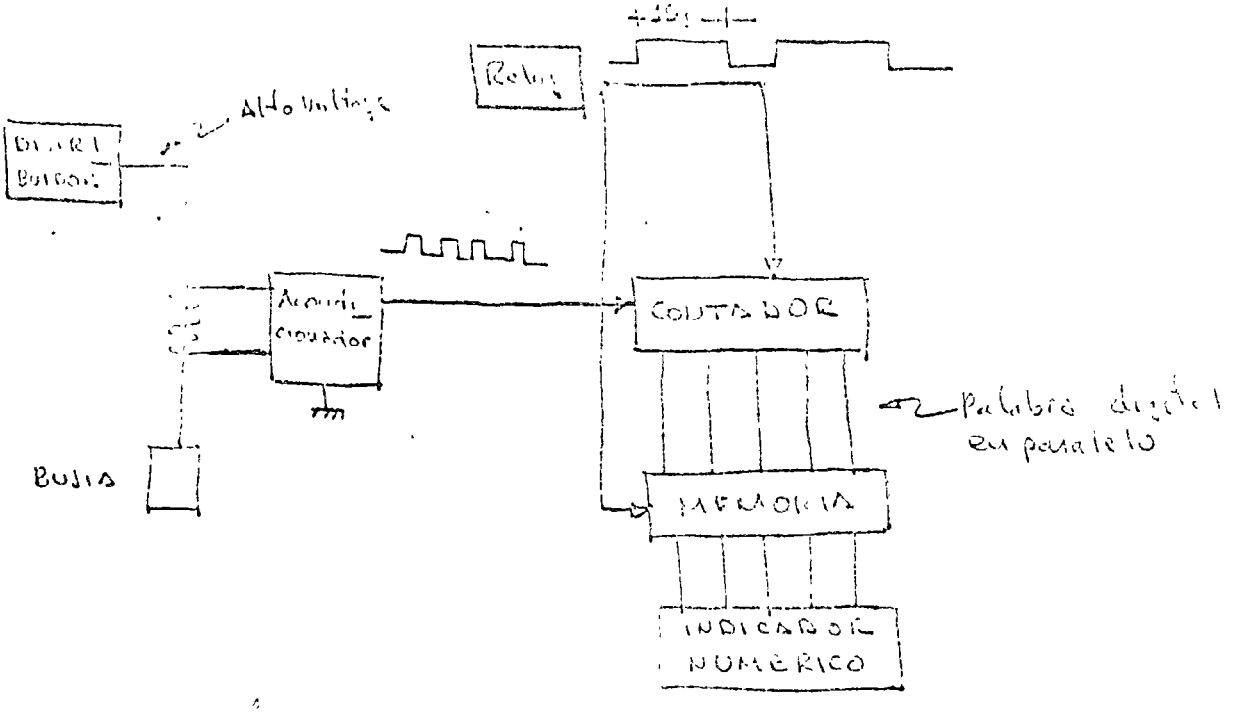


Figura 1.6.11

La función del reloj (generador de pulsos de 1 seg. de duración) es la de inicializar el contador a ceros al principio de cada ciclo y habilitar la memoria para cambiar los datos contenidos en ella al final de cada ciclo. La memoria presentará al indicador el resultado de la conversión efectuada en el ciclo anterior, decodificada numéricamente en la forma adecuada.

Si invertimos las entradas del reloj y la señal codificada temporalmente podemos contar con un convertidor de modulación por ancho de pulso a señal digital, haciendo que el contador cuantifique el número de pulsos de reloj que llegan al contador durante el penodo "alto" del pulso que contiene la información.

c.-

CONVERTIDORES DIGITAL - ANALOGICO

El propósito de un convertidor digital analógico es el de generar una corriente o un voltaje proporcional a una palabra digital generalmente alimentada en paralelo al convertidor. Un diagrama de bloques muy simplificado de un convertidor de este tipo de muestra en la figura 1.12 La función de los interruptores S_1, S_2.... S_n es conectar al sumador analógico $\sum$ la i-esima referencia si el i-esimo dígito binario es 1 lógico (este 1 "lógico" corresponde a un voltaje predeterminado en el

sistema) permanecer abierto, si el i-esimo dígito binario es 0; en el ejemplo mostrado la palabra digital es 1011 siendo el dígito (bit) más significativo (BMS) el de la extrema izquiera y el bit menos significativo (bms) el de la extrema derecha; en este caso el voltaje analógico resultante será igual a:

$$v_o = V_{ref}\left(\frac{1}{2}(1) + \frac{1}{4}(0) + \frac{1}{8}(1) + \frac{1}{16}(1)\right)$$

$$v_o = V_{ref}\left(\frac{11}{16}\right)$$

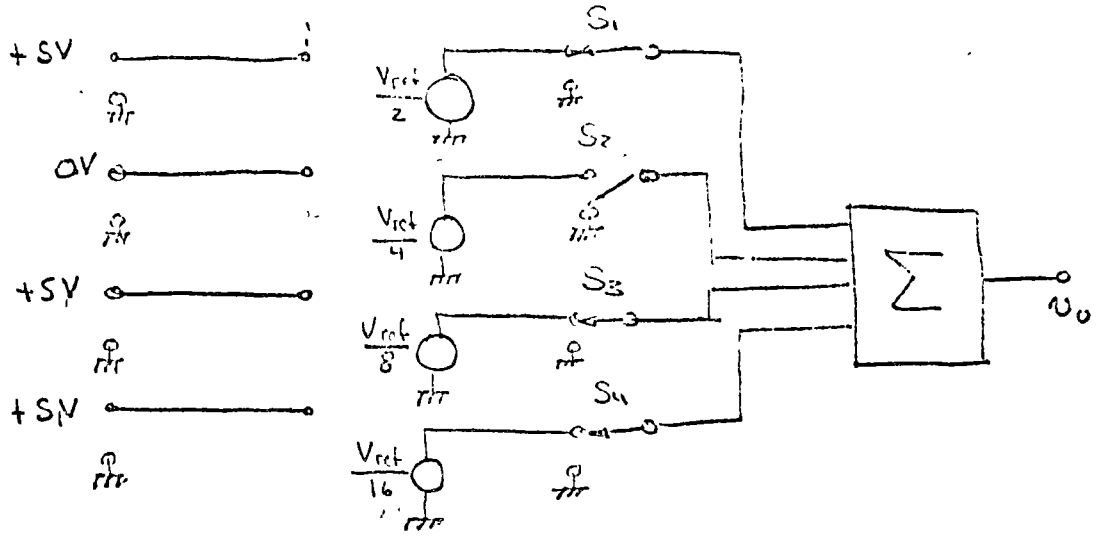


Figura 1.6.12

A continuación iremos detallando los circuítos prácticos para realizar las funciones de interruptor y de referencias pesadas de acuerdo al código empleado en la palabra dígital (en este artículo nos centraremos en el caso de codificación binaria).

C.1 INTERRUPTORES ELECTRONICOS

El realizar la función de un interruptor controlado por algún parametro externo en forma no electromecánica (por ejemplo relevadores) es un problema difícil para el cual existe un gran número de soluciones(ó). En términos generales podemos pensar en dos grandes categorías en función de la señal eléctrica a controlar en:

Interruptores de corriente

Interruptores de voltaje

de acuerdo a la posición del interruptor con respecto a la carga en:

Interruptores en serie

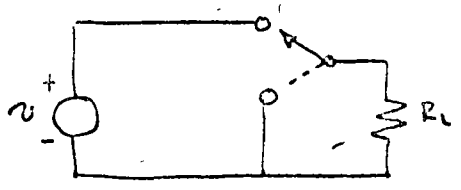
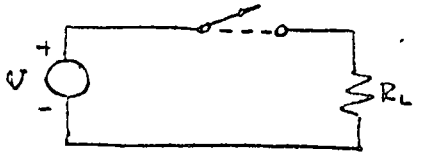
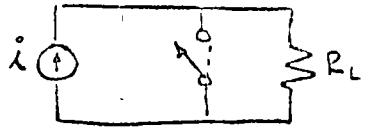
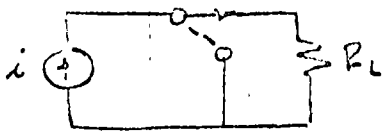
Interruptores en paralelo

Interruptores compuestos serie-paralelo

En cada caso hay también que considerar el grado de aislamiento eléctrico que existe entre los puestos de entrada, salida y control. En la figura 1.6.13 se muestran algunos ejemplos a fin de ayudar a aclarar los conceptos expuestos anteriormente.

EJEMPLOS DE TIPOS DE INTERRUPTORES

Figura 1.6.13

D I A G R A M A	DESCRIPCION	REALIZACION
	Interruptor de voltaje y corriente Tipo serie paralelo	Transistor bipolar entre límites de corte y saturación. (poco aislamiento en general).
	Interruptor de corriente Tipo serie	Transistor MOS (buen aislamiento entre puerto de control y otros puertos).
	Interruptor de voltaje Tipo paralelo	Fotodiodo y fototransistor. buen aislamiento entre el puerto de control y otros puertos)
	Interruptor de corriente tipo serie-paralelo	Por diferencia realizado con transistores bipolares

C.2 REFERENCIAS DE VOLTAJE O CORRIENTE.

En esta parte del presente artículo no se incluyen los circuítos electrónicos empleados para larealización de referencias estables de voltaje o corriente, sino la forma de obtener una serie de voltajes o corrientes pesadas de acuerdo a un cierto código sin tener que recurrir mas que a una sola referencia general, si el lector se encuentra interesado en este tema puede consultar la referencia7 . A primera vista, la forma mas sencilla de obtener un juego de valores de voltaje en base a una sola referencia se muestra en la figura en este circuíto se muestra una combinación de resistencias y amplificadores operacionales (8) que realizan la función requerida.

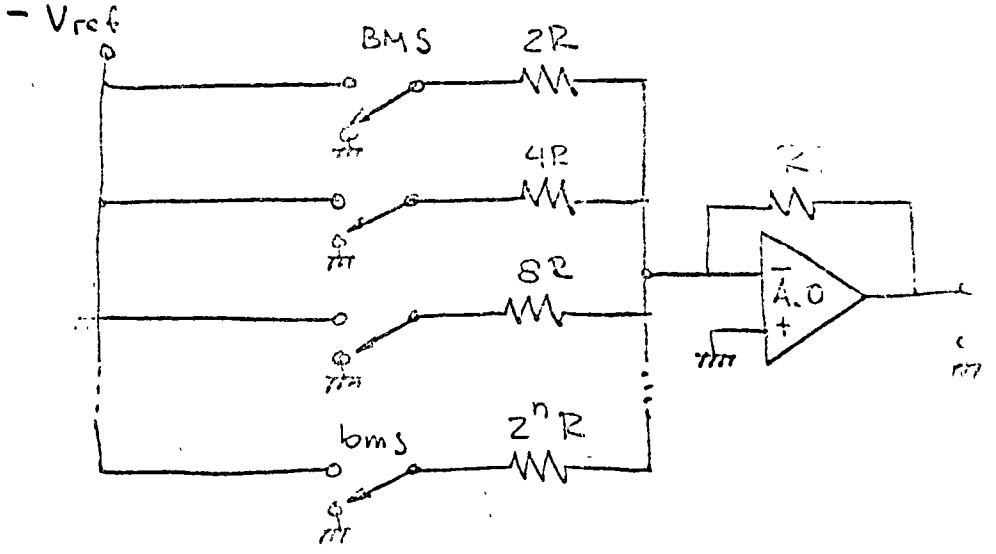


Figura 1.6.14

Este tipo de convertidor tendrá una salida para una palabra digital de bits b_1, b_2, b_3.... bn ($b_1 \rightarrow$ BMS, $b_n \rightarrow$ bms) dada por:

$$V_o = Vref \left(b_1 \frac{1}{2} + b_2 \frac{1}{4} + \cdots + b_n \frac{1}{2^n}\right)$$

correspondiente a la salida dada por el convertidor de la figura 2.3.1. El principal inconveniente que presenta este tipo de codificadores es el de requerir resistencias de presición en un amplio rango de valores, por ejemplo, para el caso de un convertidor con entrada de 10 bits (n= 10) existe una diferencia de tres órdenes de magnitud entre R y 2^nR, esto presenta graves problemas al tomar en cuenta variaciones de temperatura y restricciones tecnológicas para su realización integrada, ya sea esta en forma monolítica o hibrida (9) Un arreglo que soluciona el problema de dispersión de

valores resistivos se basa en la red escalera que se muestra en la figura 1.6.15 (a) denominada Red R-2R

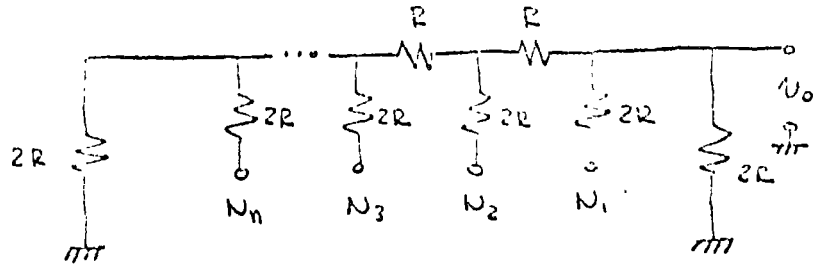


Figura 1.6.15

En este arreglo los nodos N_1, N_2 ... N_n se encuentran conectados al potencial de referencia o a tierra (potencial cero) dependiendo del valor del bit asignado a dicho nodo o sea que

$$\text{Si } b_i = 0 \quad V_{Ni} = 0$$

$$\text{Si } b_i = 1 \quad V_{Ni} = \text{Vref}$$

La operación de esta red se puede visualizar fácilmente mediante un ejemplo:

Supongamos que en la red mostrada en la figura 1.6.15 $b_1 = 1$, b_2, b_3 ... $b_n = 0$, o sea la palabra digital 1000 ... 0, tal como se muestra en la figura 1.6.16

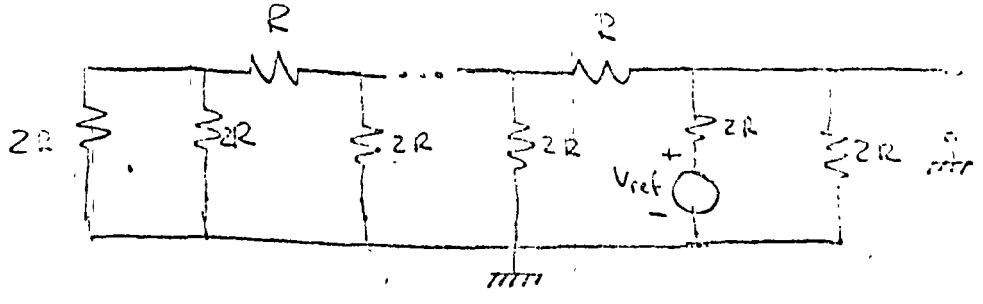


Figura 1.6.16

el circuito puede reducirse al mostrado en la figura 1.6.17 donde fácilmente puede verse que $V_o = \frac{1}{3} V_{ref}$

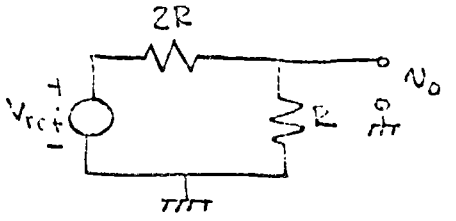


Figura 1.6.17

Si ahora la palabra digital cambia a 0.00 ... 0, el circuito equivalente al de la figura 1.6.15 para estas condiciones queda como el mostrado en la figura 1.6.18

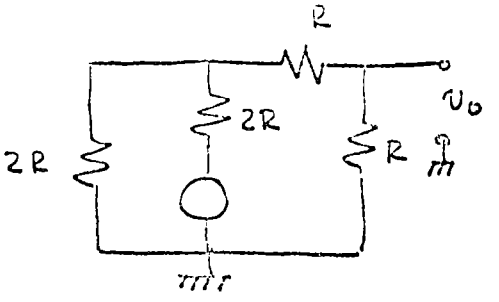


Figura 1.6.18

Para este caso la salida $V_o = \frac{1}{6} V_{ref}$. Podemos continuar en forma similar el análisis obteniendo para el caso general la siguiente expresión

$$V_o = \frac{2}{3} \left(\frac{1}{2} b_1 + \frac{1}{4} b_2 + \ldots + \frac{1}{2^n} b_n \right) V_{ref}$$

Generalmente a la salida se coloca un amplificador operacional a fin de impedir que las variaciones en el circuito externo afecten a la red decodificadora.

Existen una gran variedad adicional de circuitos que realizan este tipo de función (8, 12 ,) sin embargo la descripción de estos está mas allá de los límites dados por el enfoque del presente artículo. Finalmente en la figura 1.6.19, se muestra un circuito convertidor Digital - Analógico completo, en este caso la escalera R-2R ha sido modificada ligeramente a fin de proporcionar una mas facil realización.

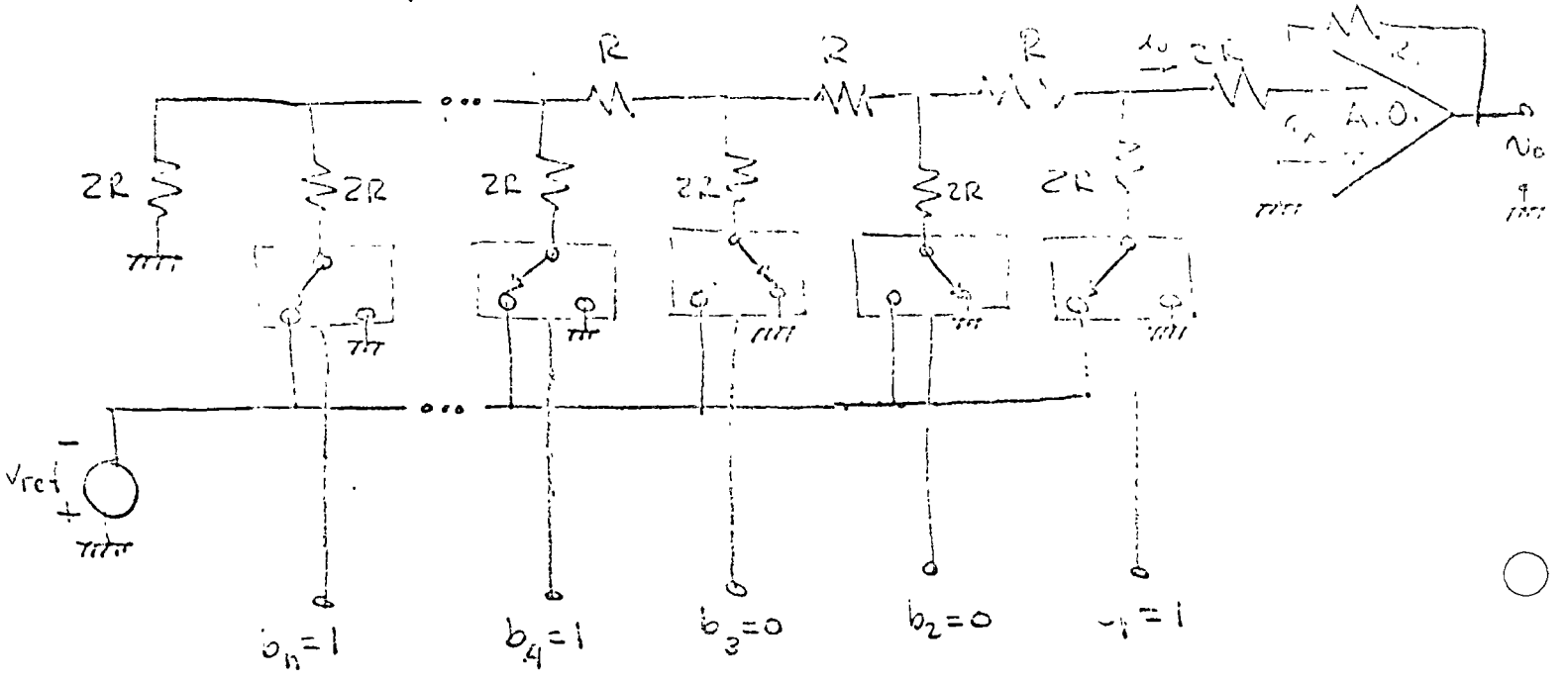


Figura 1.6.19

En este ejemplo:

$$V_o = V_{Ref} \frac{R}{3R} \left(\frac{1}{2} b_1 + \frac{1}{4} b_2 + \ldots \frac{1}{2^n} b_n \right)$$

El análisis de la red decodificadora no se altera ya que para un amplificador operacional $V_x \doteq 0$; hay que hacer notar que la escalera decodificadora no proporciona estrictamente un voltaje, sino una corriente $\dot{\lambda}_o$ dada por

$$\dot{\lambda}_o = \frac{V_{ref}}{3R} \left(\frac{1}{2} b_1 + \frac{1}{4} b_2 + \ldots \frac{1}{2^n} b_n \right)$$

que es convertida a voltaje mediante la combinación de R_F y del amplificador operacional.

D.- CONVERTIDORES ANALOGICO-DIGITALES

El proceso de cuantificar la magnitud de una señal eléctrica (generalmente un voltaje) puede ser realizado en dos formas, una directa o sea sin ningún otro tipo de conversión intermedio, y otra indirecta, pasando de la codificación analógica a la temporal y de la temporal a la digital, en esta sección centraremos nuestro enfoque en la conversión directa, ya que los sistemas mas usuales de conversión indirecta, como son los de pendiente simple o doble etc. son combinaciones de los sistemas vistos en las seccion-s .A y B (4)

D.1 CONVERTIDOR ANALOGICO-DIGITAL EN PARALELO

Al atacar el problema de la conversión Analógico-Digital en forma directa, la primera idea que se presenta es la de conectar el voltaje cuyo valor numérico se desea conocer a un número M de comparadores, cada uno de ellos conectado a su vez a un voltaje de referencia V_i tal que $V_{i-1} + \frac{V_R}{M} = V_i = V_{i+1} - \frac{V_R}{M}$ donde $V_R\left(1+\frac{1}{M}\right)$ es el rango máximo de entrada, $i = 0, 1, 2 \ldots M$ y $V_0 = 0$ un sistema de este tipo se muestra en la figura 1.6.20

CONVERTIDOR ANALOGICO DIGITAL EN PARALELO

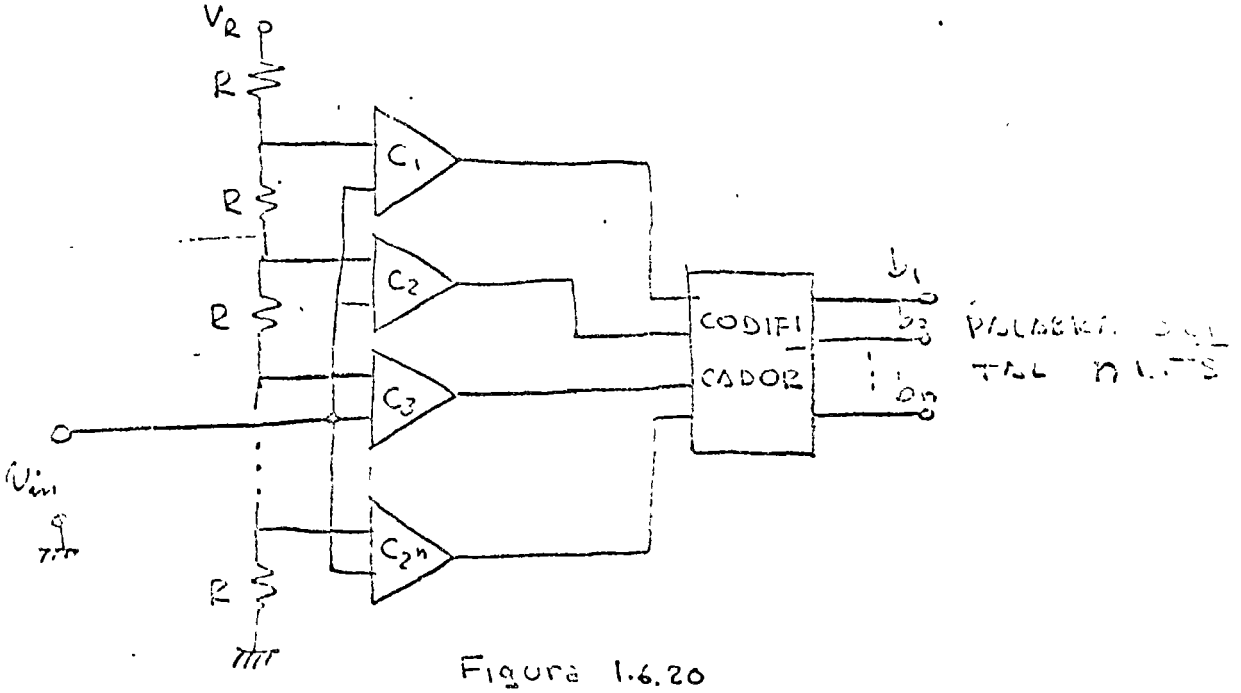


Figura 1.6.20

Algunos aspectos importantes concernientes a la operación del circuito son los siguientes:

a- Este es el tipo de convertidor mas rápido que existe, ya que se encuentra limitado únicamente por la velocidad de respuesta de los comparadores y por el retraso causado por el arreglo de circuitos lógicos que constituyen el codificador.

b- La salida digital es válida permanentemente, siendo su variación en el tiempo prácticamente la misma que la variación de

c- El número de comparadores así como la complejidad en la obtención práctica de los potenciales de referencia crece como 2^n donde n es el número de dígitos que se desean a la salida (se trata del caso binario), lo cual hace que este tipo de convertidor sea poco usado cuando $n > 4$.

En resumen, excepto en casos en los cuales la resolución del convertidor sea de pequeña importancia y se requiera una gran velocidad de conversión, este sistema es de poco interés práctico.

D.2 CONVERTIDORES ANALOGICO-DIGITAL EN SERIE

Este tipo de convertidores es el mas empleado en la actualidad, ya que el compromiso planteado entre costo, velocidad de operación y complejidad de realización conduce en casi todos los casos al empleo de esta solución. Actualmente la tecnología ofrece una gran variedad de convertidores de este tipo, incluso algunos emplean procesadores para el control del proceso de conversión. En este artículo presentaremos tres tipos de convertidores en serie, que representan diferentes tendencias en el diseño y diferentes características de operación; estos tres tipos de convertidores tienen sin embargo una característica en común: forman un sistema de malla cerrada (retroalimentado) con un convertidor Digital-Analógico en la malla de realimentación. A continuación presentaremos los principios de operación de cada uno de estos tres tipos:

a- Convertidor Analógico-Digital serie elemental: Este circuito basa su operación en la generación de una referencia variable en el tiempo, esta variación consiste en un incremento, descreto, periódico de la forma mostrada en la figura 1.6.21

VOLTAJE DE REFERENCIA PARA UN CONVERTIDOR ELEMENTAL
ANALOGICO DIGITAL MODO SERIE

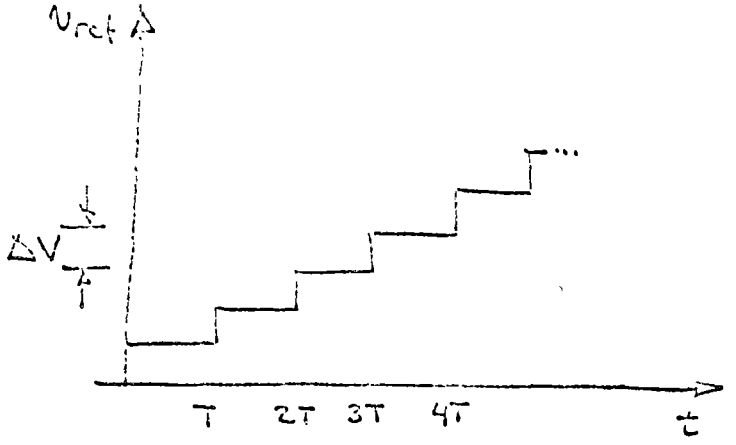


Figura 1.6.21

En la figura: $\Delta V = \frac{V_R}{2^n}$ donde V_R es el rango máximo del convertidor.

Una forma práctica de generar a un costo razonable y con una precisión adecuada la forma de onda mostrada en la figura 1.6.21 es mediante un contador binario y un convertidor Digital-Analógico, tal como se muestra en el sistema de la figura 1.6.22; este circuito es semejante en su operación al mostrado en la figura 1.6.10

CONVERTIDOR ELEMENTAL ANALOGICO-DIGITAL
MODO SERIE

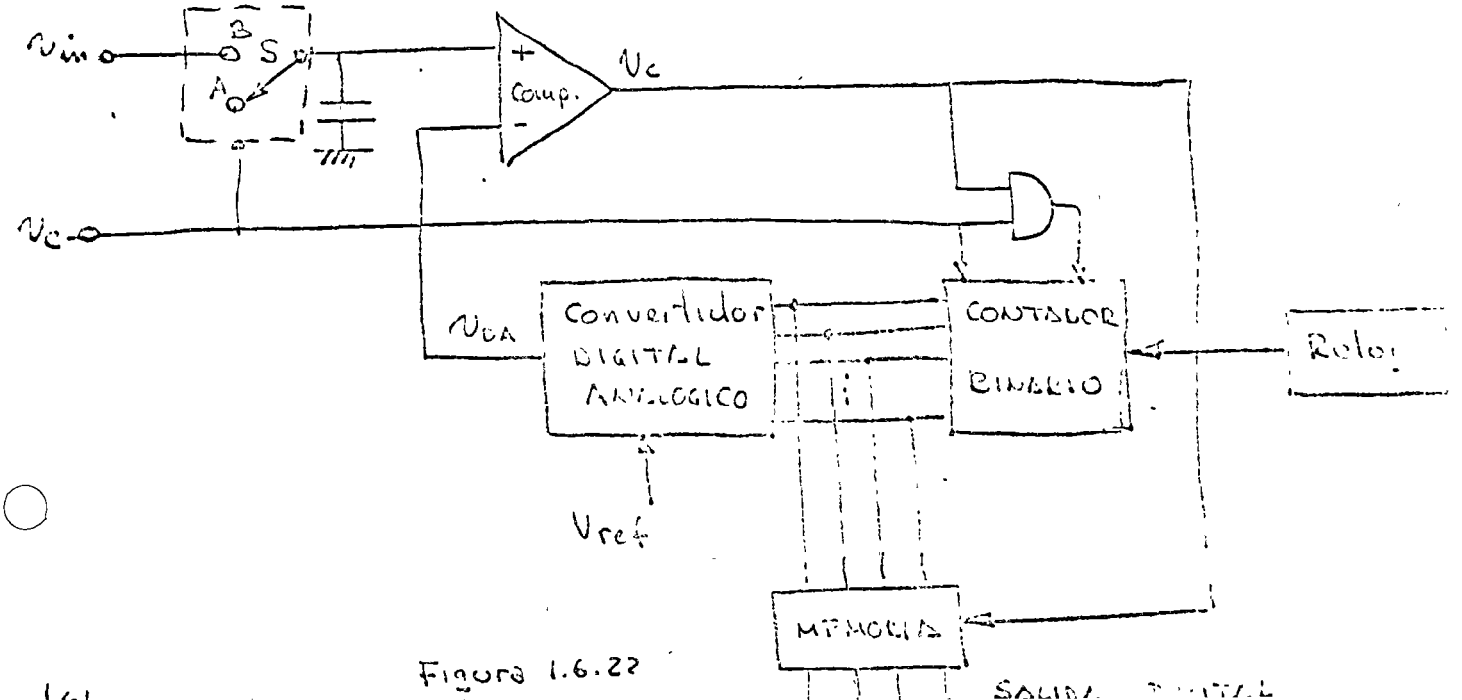


Figura 1.6.22

- El contador se habilita si V_c = "1" y V_e = "1"
- La Memoria cambia su contenido si V_c = "0"
- El interruptor S en A si V_e = "1", en B si V_e = "0"
- El contador se forza a cero en todas las salidas si V_e = "0"

La operación del convertidor será la siguiente:

- Inicialmente $V_e = V_c$ = "1", esto implica que la entrada (+) del comparador está a V_{in} y la entrada(-) a cero.

- Para t=0 se forza V_e = "1", por tanto el contador comienza a aceptar los pulsos de reloj, y por tanto V_{DA} se incrementa.

- M pulsos de reloj después $(M \leq 2^n)$ $V_{DA} \geq V_{in}(t=0)$ lo cual hace que V_c = "0", por tanto, la memoria toma el nuevo valor.

- Hacemos V_e = "0" con lo que el muestrador toma un nuevo valor y se forza $V_{DA} = 0$

Podemos destacar que en lo que se refiere a rapidez, este es un convertidor sumamente lento, ya que en el peor de los casos el tiempo de conversión ($V_{in} = V_{ref}$) será igual a 2^n ciclos de reloj, por otra parte, el tiempo de conversión es variable y requiere de un muestrador como apoyo para realizar la conversión, sin embargo su construcción es muy simple, y si las variaciones de la variable V_{in}, no son demasiado rápidas se pueden obtener grandes resoluciones, limitadas únicamente por la capacidad del convertidor Digital-Analógico.

CONVERTIDOR SEGUIDOR: Una variante del convertidor modo serie, se muestra en la figura 1.6.23 (11)

CONVERTIDOR ANALOGICO-DIGITAL
MODO SEGUIDOR

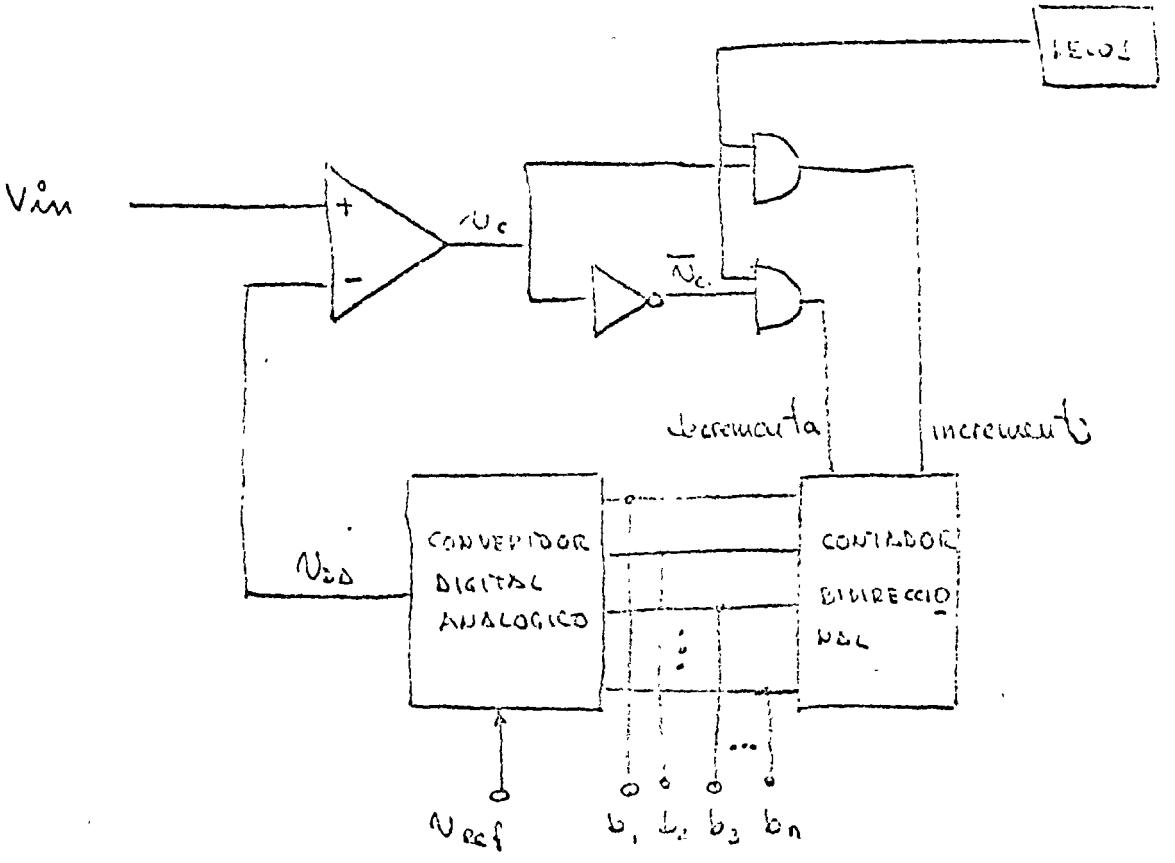


figura 1.6.23

El funcionamiento del circuito es como sigue

Si $V_{in} > V_{DA}$ V_c= "1" por tanto el reloj incrementa el contador
Si $V_{in} < V_{DA}$ V_c= "0" por tanto el reloj decrementa el contador

Este convertidor tiene dos modos de operación bien definidos:

a- Si $|V_{in} - V_{DA}| > KV_{ref}\frac{1}{2^n}$ (k es una constante que nos da el rango máximo del convertidor) el convertidor se comporta similarmente al que opera en modo serie)

b- Si $|V_{in} - V_{DA}| \leq KV_{ref}\frac{1}{2^n}$ la salida digital es siempre válida (sin tomar en cuenta el b.m.s.) y por tanto presenta exteriormente las mismas características que el convertidor modo paralelo.

Una vez que el convertidor se encuentra operando en el modo b se mantendrá en el siempre y cuando la rapidez de cambio no sea mayor que la máxima del voltaje V_{DA} fijada principalmente por el reloj del sistema, en otras palabras el sistema tiene un cierto "slew rate" similar al de un amplificador operacional. O sea, que para cuantizar señales tales que $\frac{dV_{in}}{dt} \leq \frac{KV_{ref}}{2^n T}$ podemos emplear este convertidor para tener la sencillez de un convertidor serie combinada con las ventajas de un convertidor paralelo (disponibilidad inmediata de la señal digital, operación asincrona y ausencia de un muestreador)

CONVERTIDOR ANALOGICO-DIGITAL POR APROXIMACIONES SUCESIVAS:
En si, este tipo de convertidor, pertenece a una categoría de sistemas que requiere una cierta lógica para su funcionamiento; la lógica de este sistema es suficientemente simple como para poderse implementar mediante lógica alambrada ("Hard ware") pero sienta los principios de operación de convertidores cuya eficiencia depende del algoritmo implementado, que con el advenimiento de los microprocesadores puede ser tan complejo como se requiera.

El algoritmo de la aproximación sucesiva se muestra a continuación en la figura 1.6.24

ALGORITMO DE LA APROXIMACION SUCESIVA

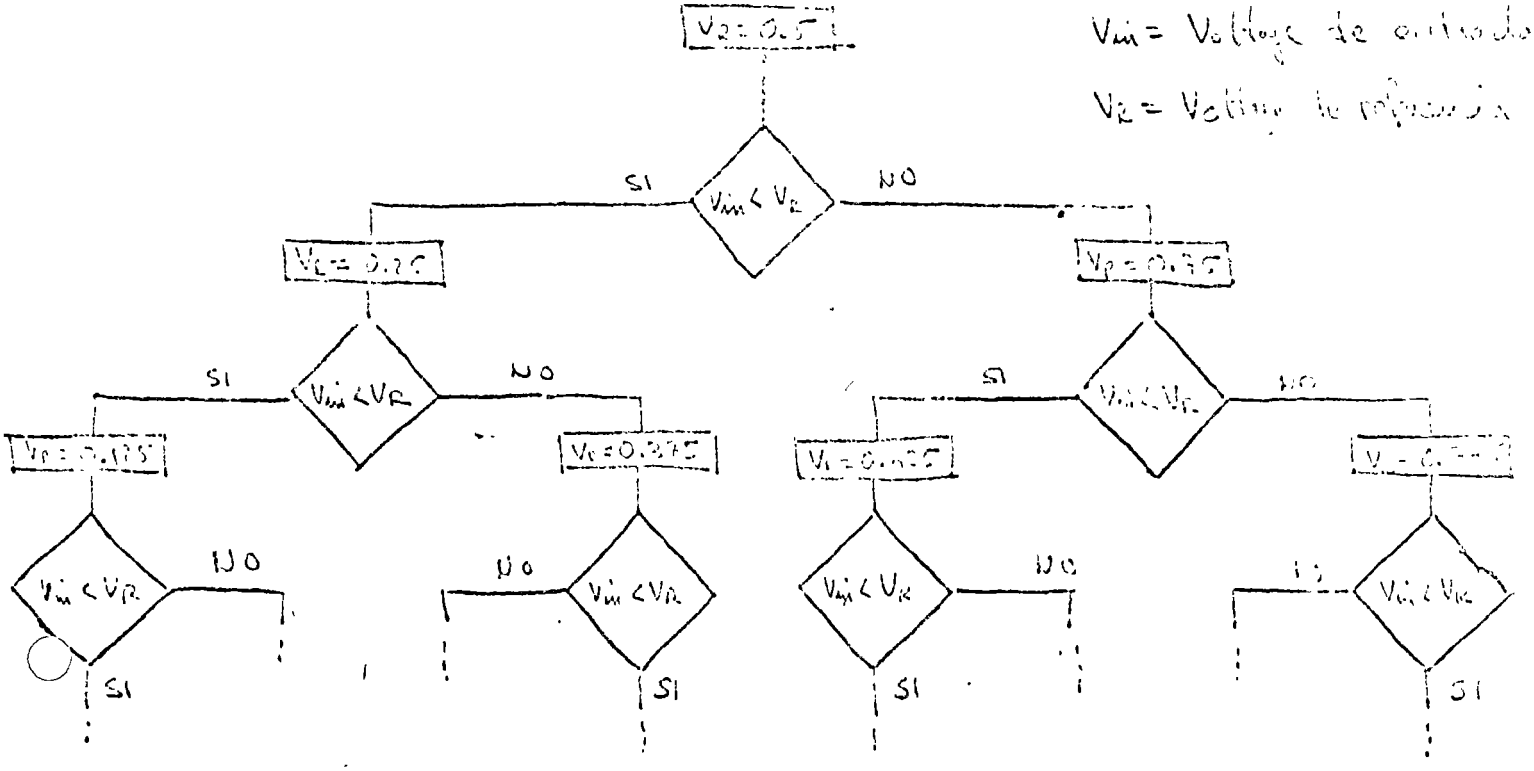


figura 1.6.24

Supongamos que la referencia variable se quiere realizar mediante un convertidor Digital-Analógico, el diagrama resultante quedaría para un convertidor de 4 volts como se muestra en la figura 1.6.25 ; en esta figura se pueden observar las siguientes características de operación:

- Para modificar la referencia en cualquier caso, basta con cambiar un bit
- Del resultado de la comparación se elimina o el bit añadido en el paso anterior o se añade uno a la palabra digital.

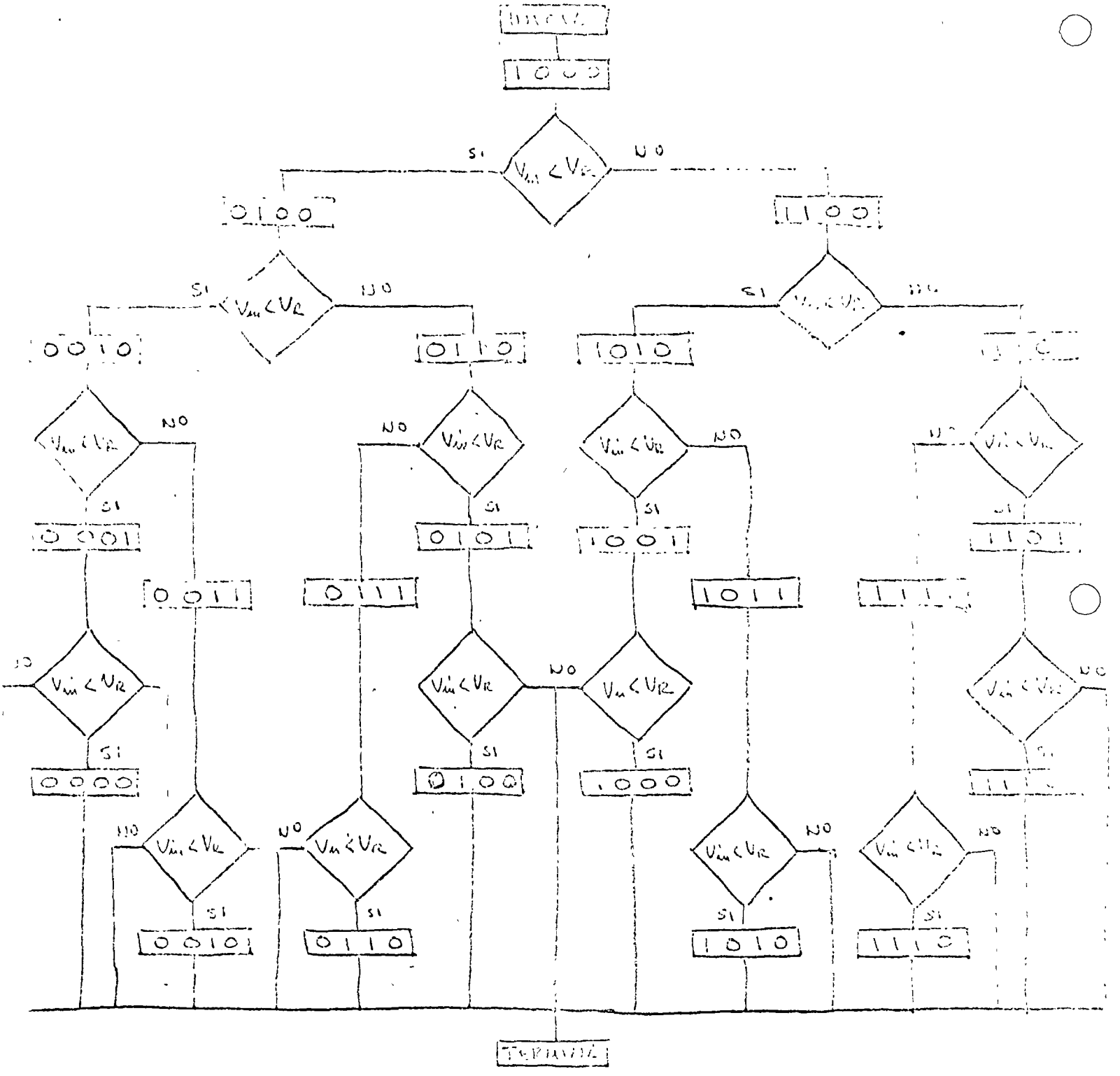

1 0 0 0
SI
NO
0 1 0 0
1 1 0 0
0 0 1 0
0 1 1 0
1 0 1 0
0 0 0 1
0 1 0 1
1 0 0 1
1 1 0 1
0 0 1 1
0 1 1 1
1 0 1 1
0 0 0 0
0 1 0 0
1 0 0 0
0 0 1 0
0 1 1 0
1 0 1 0
1 1 1 0

figura 1.6.25

Aunque aparentemente difícil de realizar, el sistema puede ser facilmente convertido en base a registros de corrimiento y biestables (10); en la figura 1.6.26 se muestra un circuito que realiza el algoritmo indicado en la figura 1.6.26

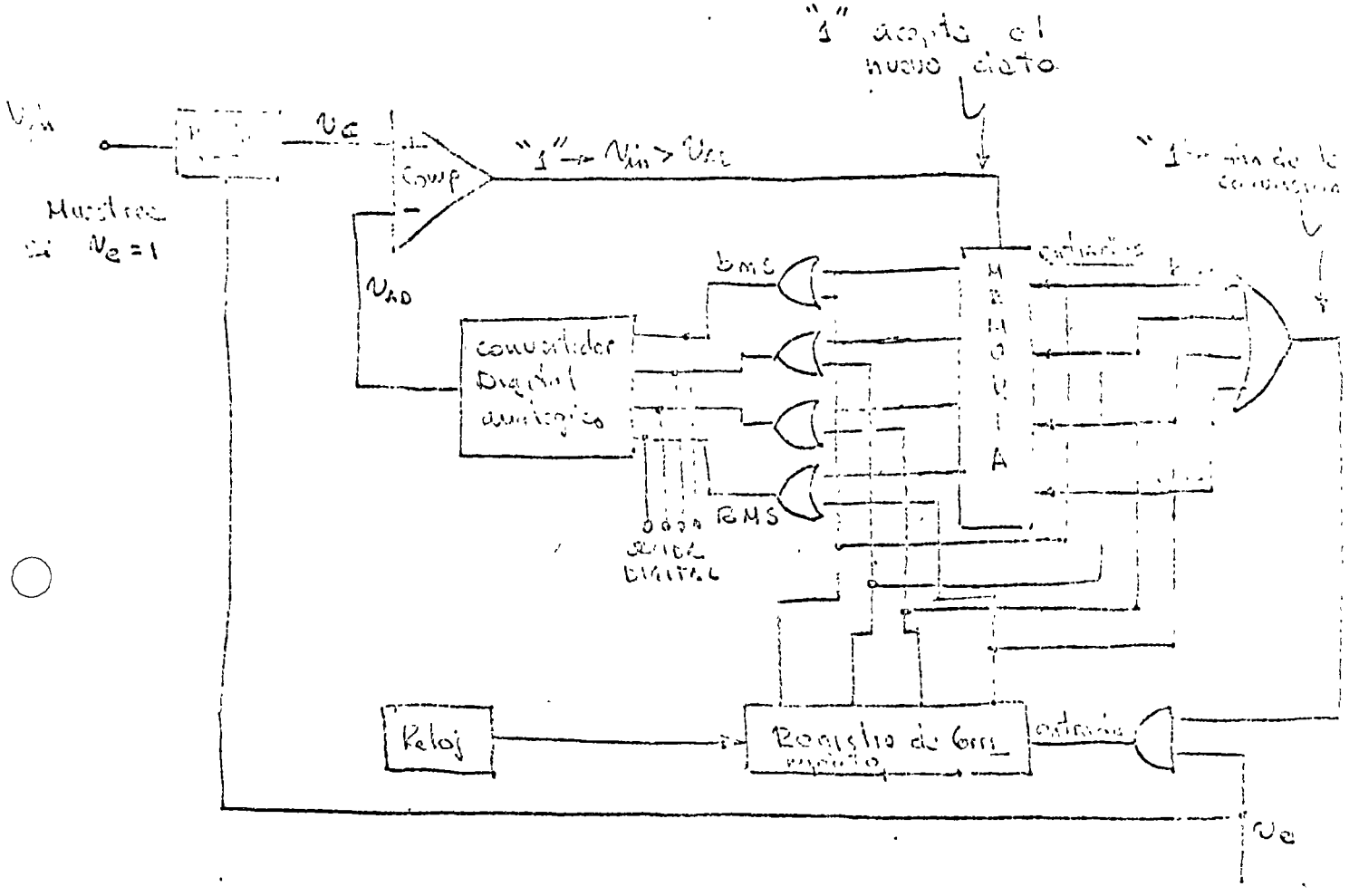


figura 1.6.26

En la operación de este sistema hay que tener en cuenta lo siguiente:

- El ciclo de conversión es siempre constante igual a n ciclos de reloj
- La salida Digital será válida unicamente cuando la señal de fin de conversión se encuentre en el estado "1"

TABLAS COMPARATIVAS DE CARACTERISTICAS DE AMPLIFICADORES OPERACIONALES TANTO COMERCIALES COMO MILITARES

Comparison of popular integrated circuit operational amplifier parameters

Device	*Maximum input-offset current* (n/A) (*at* 25°C)	*Maximum input-offset voltage* (mV) (*at* 25°C)	*Typical slew rate* (V/μsec)	*Typical unity gain bandwidth* (MHz)	*Maximum input-offset voltage drift* (μV/°C)
LM101A	20	2	0.5	1	15
μA741	500	5	0 5	1	15
LM108A	0 4	0 5	0.1	0 5	5
μA725A	40	0 5	0 005	0.05	1
μA740	0.01	20	6.0	1	5[a]
SN62088	0.3	0.075	25.0	3	0 6
HA2900	0.1	0 060	2.5	3	0 6
4250	5	4	0.16	0 25	

[a] Typical

Comparison of commercial-grade devices

Device	*Offset*[a] *voltage* (mV)	*Bias*[a] *current* (nA)	*Slew*[b] *rate* (V/μsec)	*Bandwidth*[b] (MHz)	*Supply*[a] *current* (mA)
LM310	7.5	7.0	40	20	5.5
LM302	15	30	20	10	5.5
MC1456	10	30	2.5	1	1.5
μA715C	7.5	1500	20	10	10
LM308	7.5	7.0	0.3	1	0.8
LM308A	0.5	7.0	0.3	1	0.8
LM301A	7.5	250	0 6	1	3.0
μA741C	6 0	500	0.6	1	3.0

[a] Maximum at 25°C.
[b] Typical at 25°C.

Comparing performance of military grade integrated circuit operational amplifiers in the voltage-follower connection

Device	*Offset*[a] *voltage* (mV)	*Bias*[a] *current* (nA)	*Slew*[b] *rate* (V/μsec)	*Bandwidth*[b] (MHz)	*Supply*[c] *current* (mA)
LM110	6.0	10	40	20	5 5
LM102	7.5	100	10	10	5 5
MC1556	6 0	30	2.5	1	1 5
μA715	7.5	4000	20	10	7 0
LM108	3.0	3	0.3	1	0 6
LM108A	1.0	3	0.3	1	0 6
LM101A	3.0	100	0 6	1	3 0
μA741	6.0	1500	0.6	1	3.0

[a] Maximum for $-55°C \leq T_A \leq 125°C$.
[b] Maximum at 25°C.
[c] Typical at 25°C.

DESCRIPTION

The LM101A and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

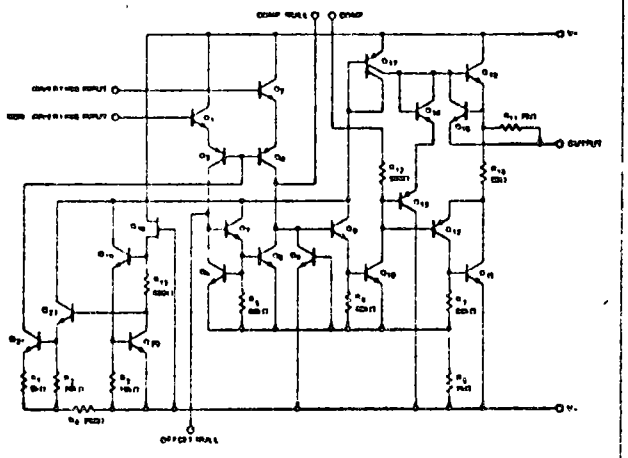
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	LM101A	±22V
	LM301A	±18V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM101A	-55°C to 125°C
	LM301A	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES

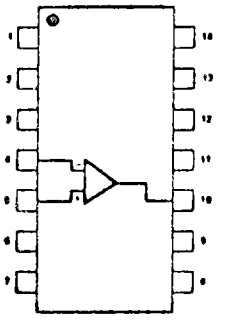
1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101A and 100°C for the LM301A. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

A & F PACKAGE (Top View)

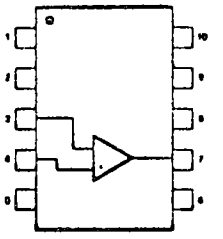


1. NC
2. NC
3. Freq Comp /Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq Comp.
13. NC
14. NC

ORDER PART NOS

LM101AD/LM301AD LM101AN-14/LM301AN-14

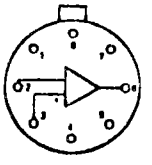
G PACKAGE



1. NC
2. Bal/Comp
3. Input
4. Input
5. V^-
6. Bal
7. Output
8. V^+
9. Comp
10. NC

ORDER PART NOS.
LM101AF/LM301AF

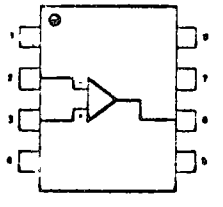
T PACKAGE



1. Freq Comp/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
LM101AH/LM301AH

V PACKAGE



1. Freq Comp /Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO.
LM301AN

LM101A

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$, $\pm 5V \leq V_S \leq \pm 20V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		0 7	2 0	mV
Input Offset Current	$T_A = 25°C$		1.5	10	nA
Input Bias Current	$T_A = 25°C$		30	75	nA
Input Resistance*	$T_A = 25°C$	1.5	4		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1 8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3 0	15	µV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$		0 01 0 02	0 1 0 2	nA/°C nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB

LM301A

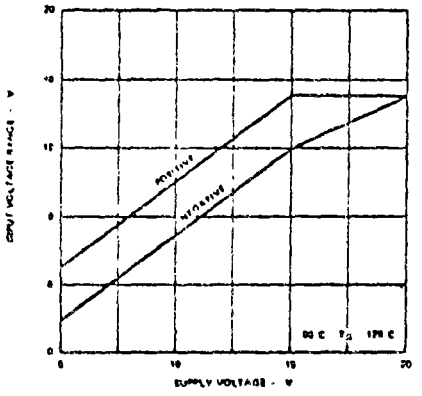
ELECTRICAL CHARACTERISTICS ($0°C \leq T_A < 70°C$, $\pm 5V, \leq V_S \leq \pm 15V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2.0	7 5	mV
Input Offset Current	$T_A = 25°C$		3	50.	nA
Input Bias Current	$T_A = 25°C$		70	250	nA
Input Resistance	$T_A = 25°C$	0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1 8	3 0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$; $R_L \geq 2k\Omega$	25	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	µV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0 01 0.02	0 3 0.6	µA/°C µA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		dB

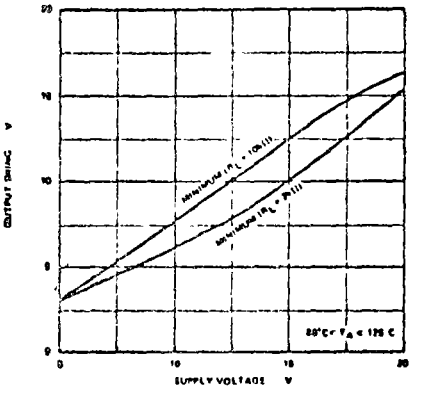
TYPICAL CHARACTERISTIC CURVES

LM101A

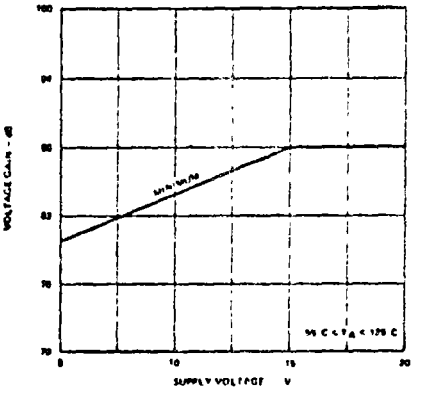
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

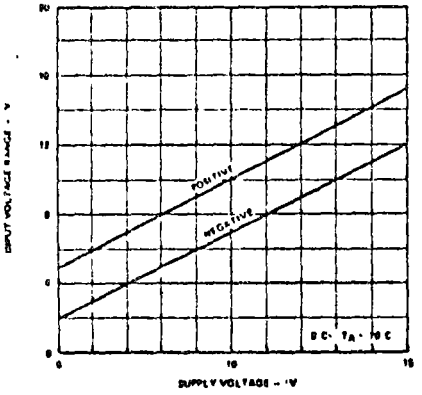


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

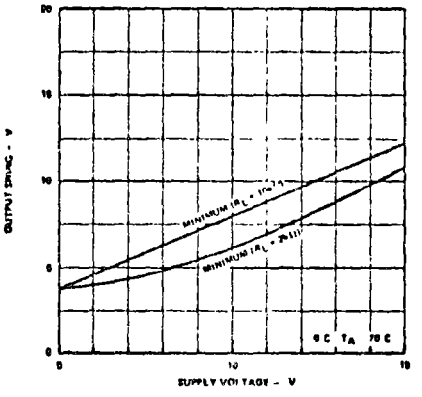


LM301A

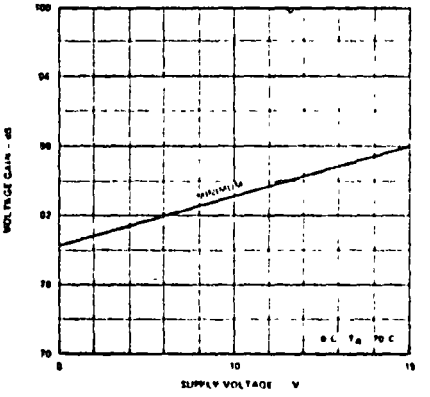
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

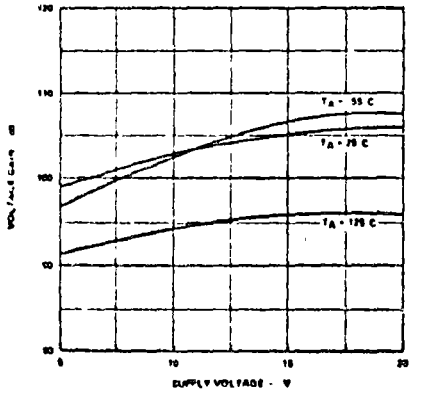


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

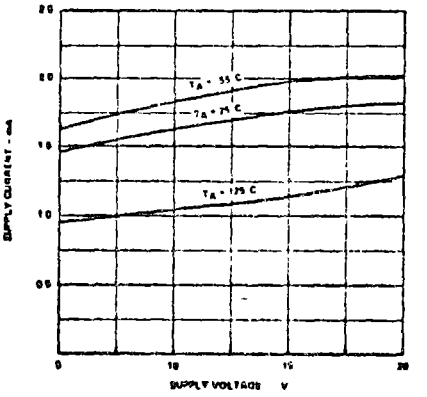


LM101A

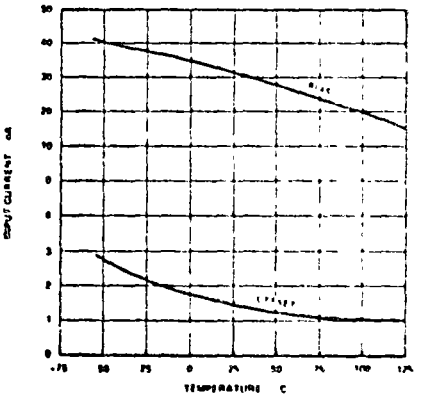
VOLTAGE GAIN



SUPPLY CURRENT



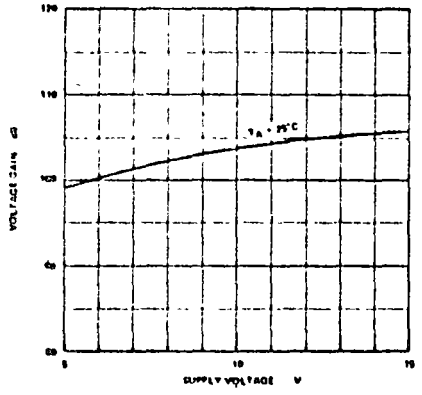
INPUT CURRENT



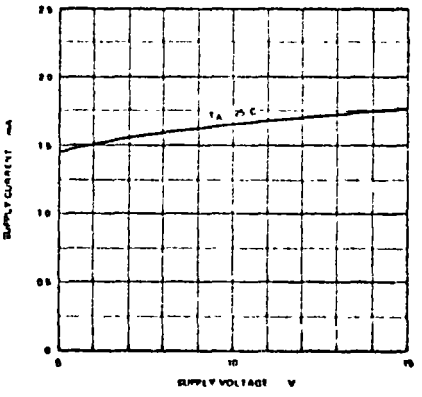
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM301A

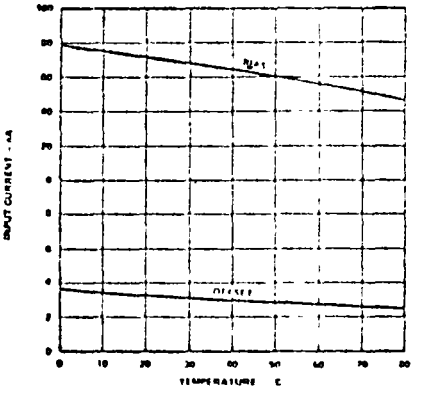
VOLTAGE GAIN



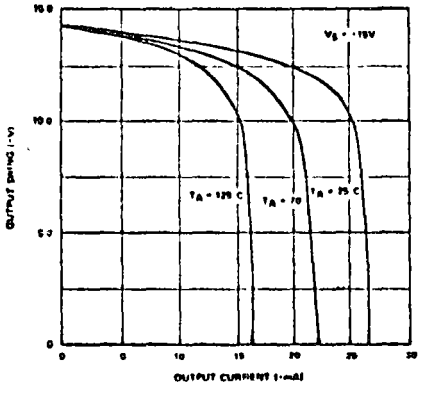
SUPPLY CURRENT



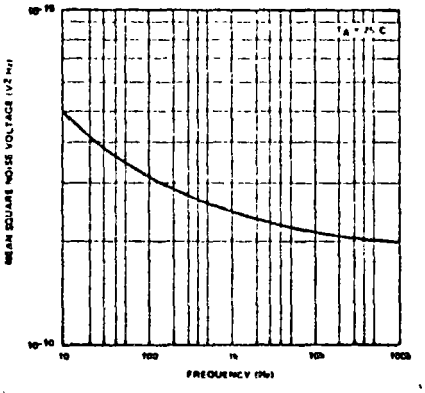
INPUT CURRENT



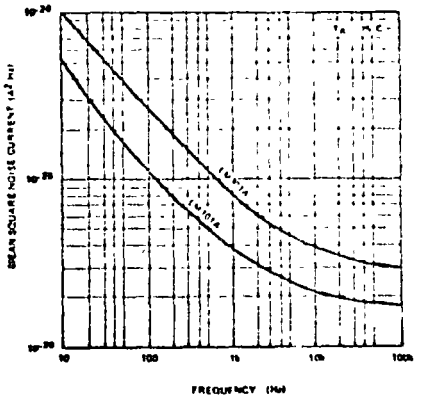
CURRENT LIMITING



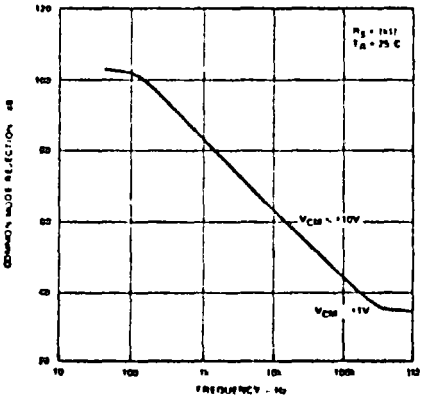
INPUT NOISE VOLTAGE



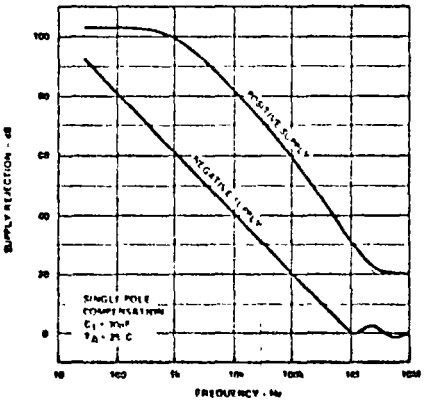
INPUT NOISE CURRENT



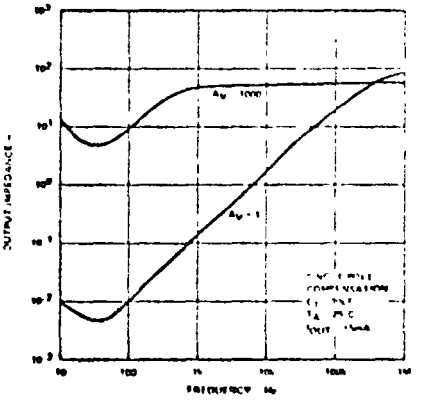
COMMON MODE REJECTION



POWER SUPPLY REJECTION



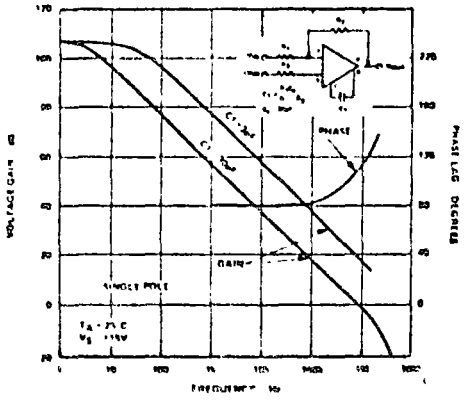
CLOSED LOOP OUTPUT IMPEDANCE



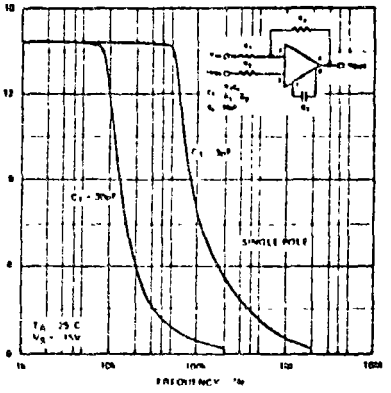
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

SINGLE POLE COMPENSATION

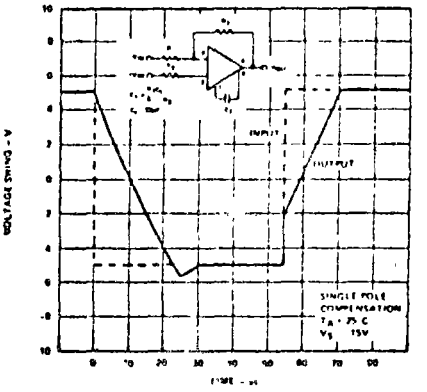
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

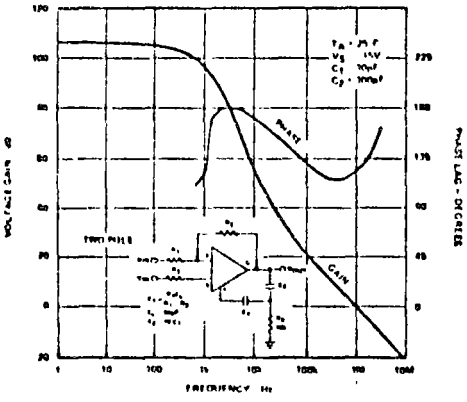


VOLTAGE FOLLOWER PULSE RESPONSE

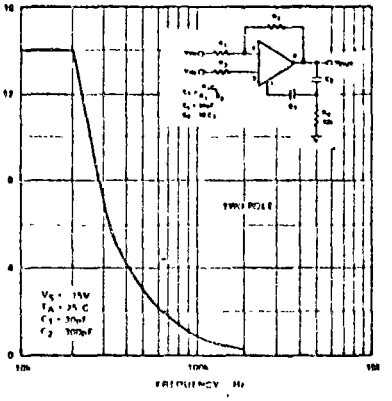


TWO POLE COMPENSATION

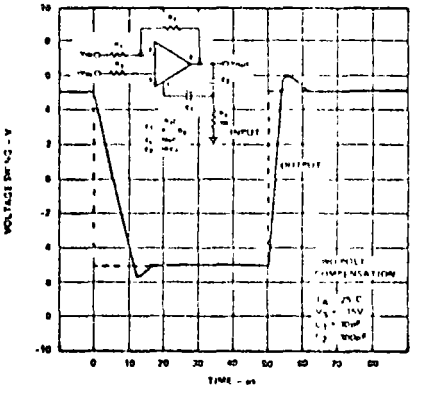
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

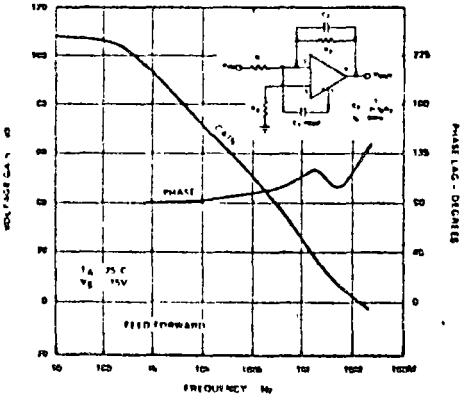


VOLTAGE FOLLOWER PULSE RESPONSE

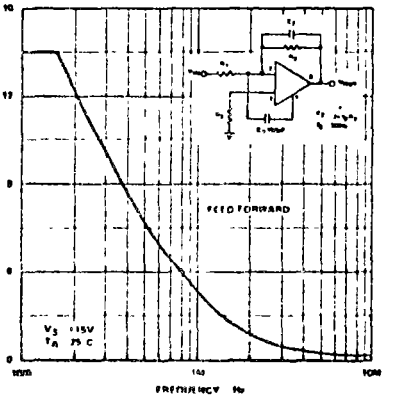


FEED FORWARD COMPENSATION

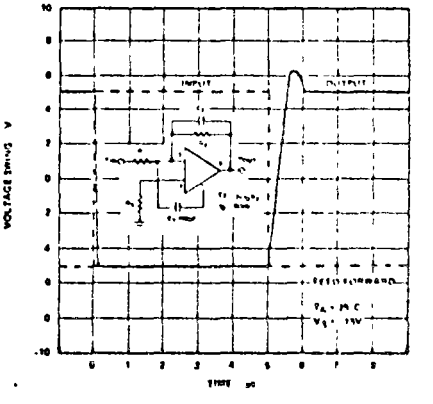
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

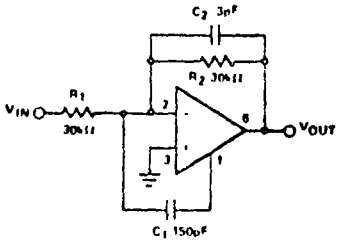


INVERTER PULSE RESPONSE



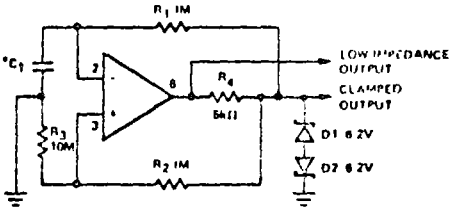
TYPICAL APPLICATIONS (Pin numbers shown refer to T or V package only)

FAST SUMMING AMPLIFIER



Power Bandwidth 250kHz
Small Signal Bandwidth. 3.5MHz
Slew Rate· 10V/μs

LOW FREQUENCY SQUARE WAVE GENERATOR



*Adjust C_1 for frequency

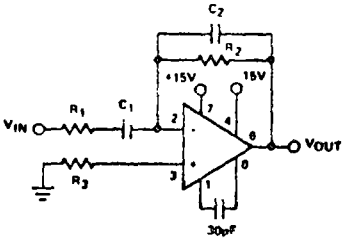
PRACTICAL DIFFERENTIATOR

$$f_c = \frac{1}{2\pi R_2 C_1}$$

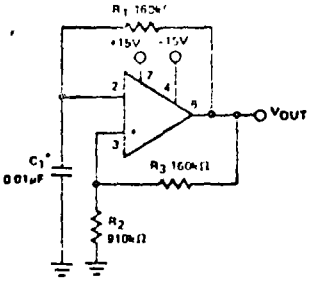
$$f_n = \frac{1}{2\pi R_1 C_1}$$

$$= \frac{1}{2\pi R_2 C_2}$$

$f_c < f_n < f_{unity\ gain}$

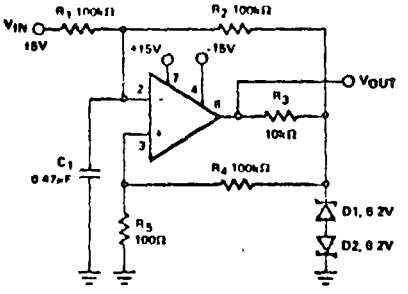


FREE-RUNNING MULTIVIBRATOR

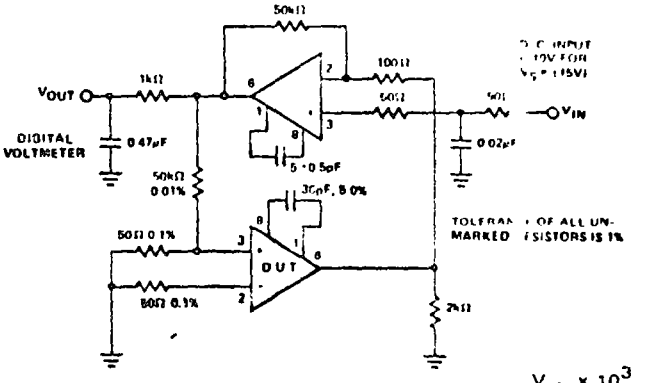


*Chosen for oscillation at 100Hz

PULSE WIDTH MODULATOR

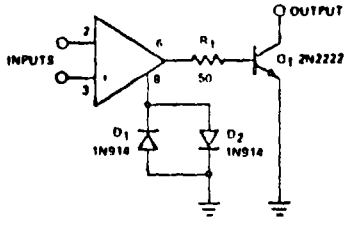


GAIN TEST CIRCUIT

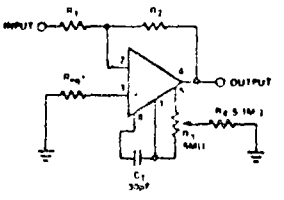


$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}}$$

VOLTAGE COMPARATOR FOR DRIVING RTL LOGIC OR HIGH CURRENT DRIVER

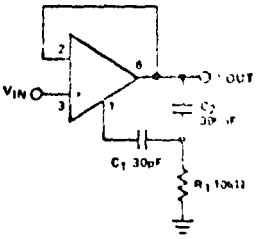


INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

FAST VOLTAGE FOLLOWER



Power Bandwidth 15kHz
Slew Rate. 1V/μs

DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains D.C. performance equal to the best general purpose types while providing far superior large signal A.C. performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier can be compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- 35V/μsec SLEW RATE AT UNITY GAIN
- PIN FOR PIN REPLACEMENT FOR μA709, μA748 OR LM101
- COMPENSATED WITH A SINGLE CAPACITOR
- SAME LOW DRIFT OFFSET NULL CIRCUITRY AS μA741
- SMALL SIGNAL BANDWIDTH 1 MHz
- LARGE SIGNAL BANDWIDTH 500KHz
- TRUE OP AMP D.C. CHARACTERISTICS MAKE THE 531 THE IDEAL ANSWER TO ALL SLEW RATE LIMITED OPERATIONAL AMPLIFIER APPLICATIONS.

NOTES

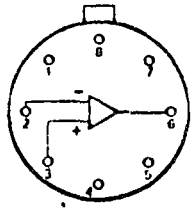
1. Rating applies for case temperatures to 125 °C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	300mW
Differential Input Voltage	±15V
Common Mode Input Voltage (Note 2)	±15V
Voltage Between Offset Null and V^-	±0.5V
Operating Temperature Range	
NE531	0°C to +70°C
SE531	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

PIN CONFIGURATION

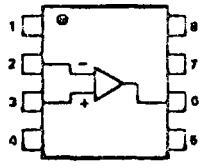
T PACKAGE
(Top View)



1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp

ORDER PART NOS.
SE531T/NE531T

V PACKAGE

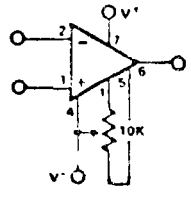


1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp

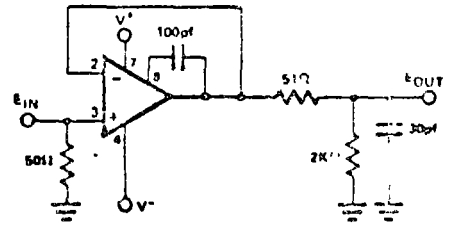
ORDER PART NO. NE531V

TEST CIRCUITS

OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



GENERAL ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C Unless Otherwise Specified)

NE531

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	6	mV
Input Offset Current			50	200	nA
Input Bias Current			0.4	1.5	μA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	20,000	60,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Full Power Bandwidth			500		KHz
Settling Time 1%	A_V = +1, V_{IN} = ±10V		1.5		μsec
Settling Time .01%	A_V = +1, V_{IN} = ±10V		2.5		μsec
Large Signal Overshoot	A_V = +1, V_{IN} = ±10V		2		%
Small Signal Overshoot	A_V = +1, V_{IN} = 400mV		5		%
Small Signal Risetime	A_V = +1, V_{IN} = 400mV		300		nsec
The Following Apply for					
0°C ≤ T_A ≤ +70°C					
Input Offset Voltage	$R_S \leq 10K\Omega$			7.5	mV
Input Offset Current	T_A = +70°C			200	nA
	T_A = 0°C			300	nA
Input Bias Current	T_A = +70°C			1.5	μA
	T_A = 0°C			2.0	μA
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	15,000			
Output Voltage Swing	$R_L \geq 2K\Omega$	±10	±13		Volt
Slew Rate	A_V = 100		35		V/μs
	A_V = 10		35		V/μs
	A_V = 1 (non inverting)		30		V/μs
	A_V = 1 (inverting)		35		V/μs
Supply Current	T_A = +70°C		4.5	5.5	mA

SE531

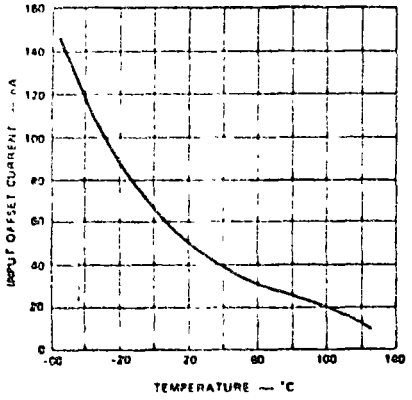
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			300	500	nA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, V_{OUT} = ±10V	50,000	100,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Full Power Bandwidth			500		KHz
Settling Time 1%	A_V = +1, V_{IN} = ±10V		1.5		μsec
Settling Time .01%	A_V = +1, V_{IN} = ±10V		2.5		μsec
Large Signal Overshoot	A_V = +1, V_{IN} = ±10V		2		%
Small Signal Risetime	A_V = +1, V_{IN} = 400mV		300		nsec
Small Signal Overshoot	A_V = +1, V_{IN} = 400mV		5		%
Slew Rate	A_V = 100		35		V/μs
	A_V = 10		35		V/μs
	A_V = 1 (non inverting)		30		V/μs
	A_V = 1 (inverting)		35		V/μs
The following apply for					
-55°C ≤ T_A ≤ +125°C					
Input Offset Voltage	$R_S \leq 10K\Omega$			6	mV
Input Offset Current	T_A = +125°C			200	nA
	T_A = -55°C			500	nA
Input Bias Current	T_A = +125°C			500	nA
	T_A = -55°C			1.5	μA
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	μV/V
Large Signal Voltage Gain	R_L = 2KΩ, V_{OUT} = ±10V	25,000			
Output Voltage Swing	R_L = 2KΩ	±10	±13		V
Supply Current	T_A = +175°C		4.5	5.5	mA

NOTES

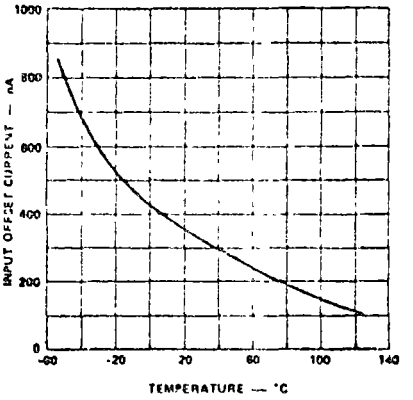
All AC parametric testing is performed using the conditions of the transient response test circuit, page 1.

TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise noted)

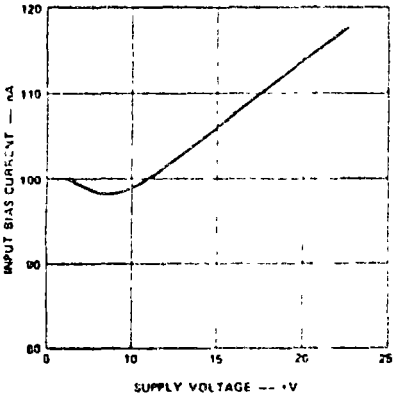
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



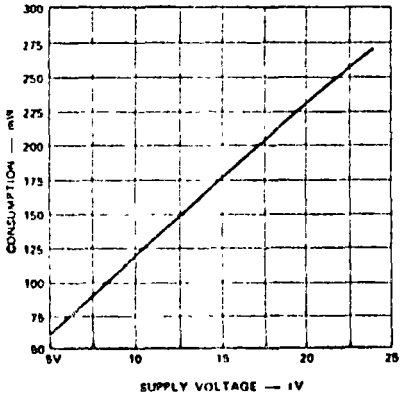
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



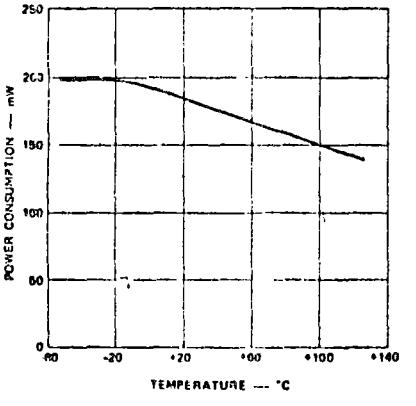
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



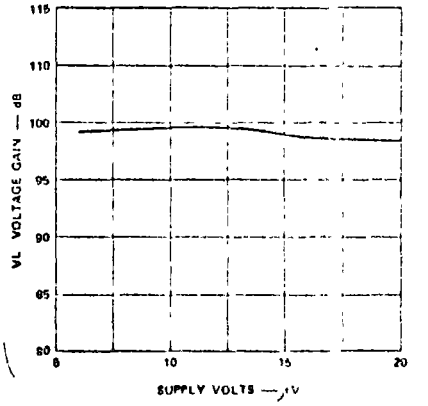
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



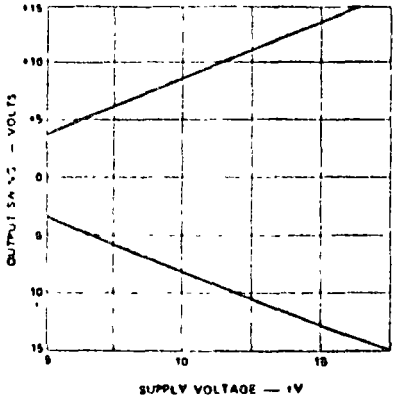
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



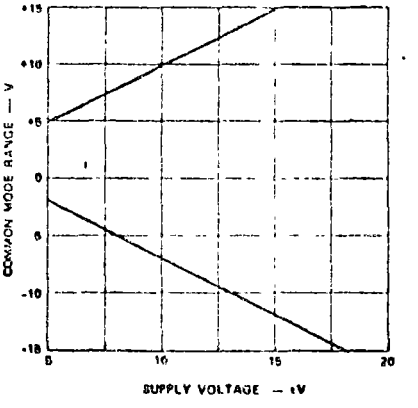
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



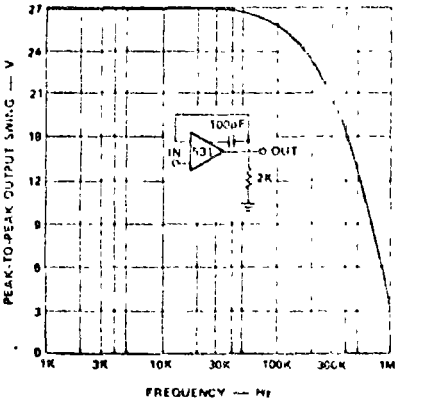
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

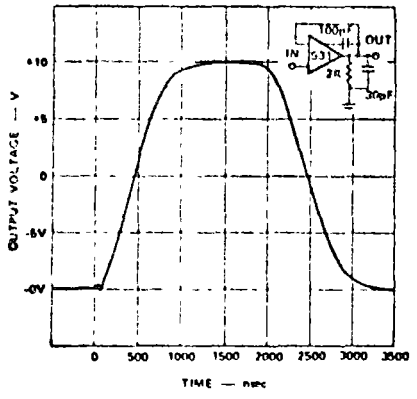


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

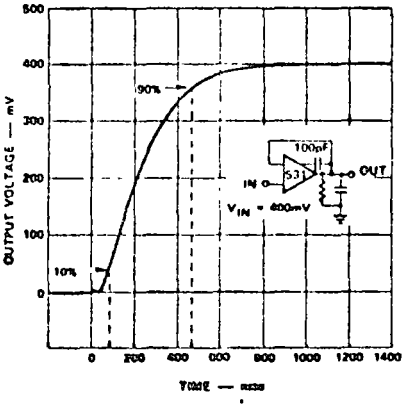


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

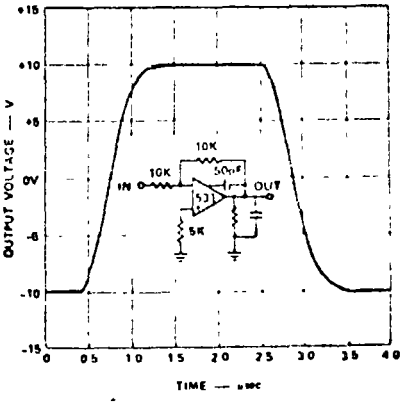
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



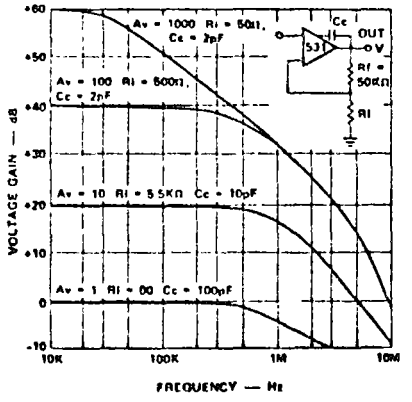
VOLTAGE FOLLOWER TRANSIENT RESPONSE



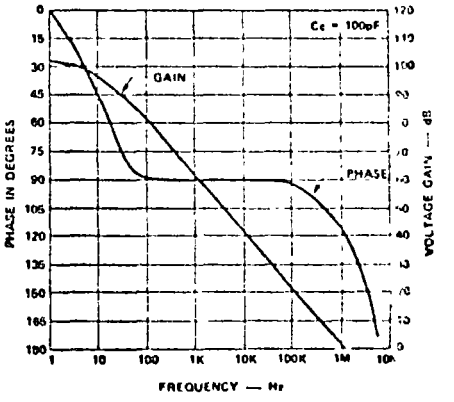
UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE



CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

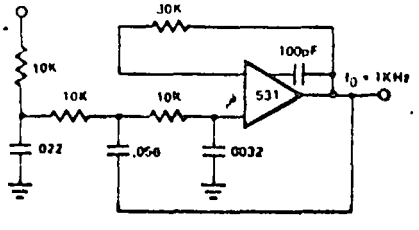


OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

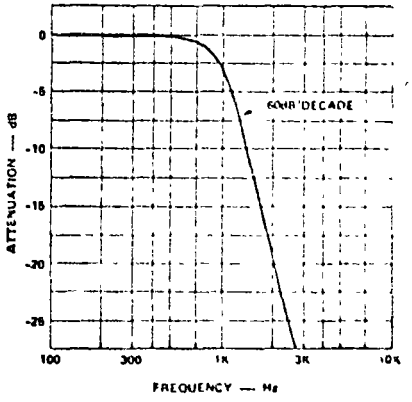


TYPICAL APPLICATIONS

3 POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



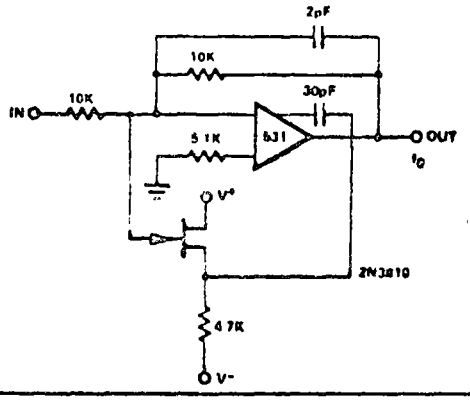
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER

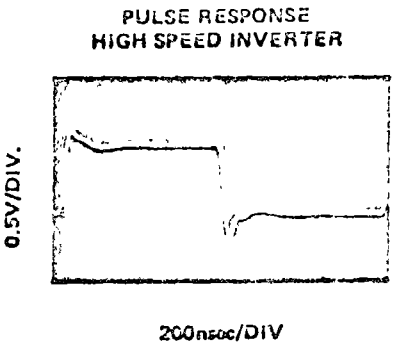


*Reference — EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

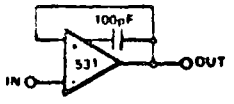
TYPICAL APPLICATIONS (Cont'd.)

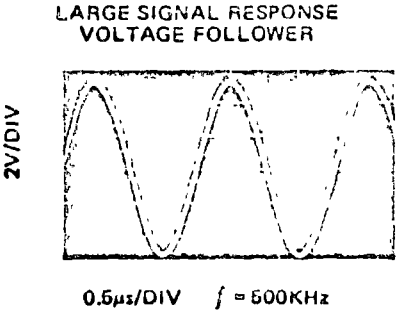
HIGH SPEED INVERTER (10MHz Bandwidth)





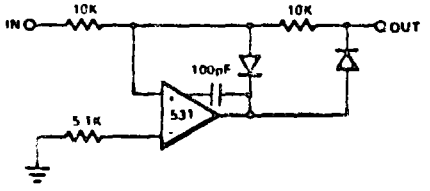
FAST SETTLING VOLTAGE FOLLOWER



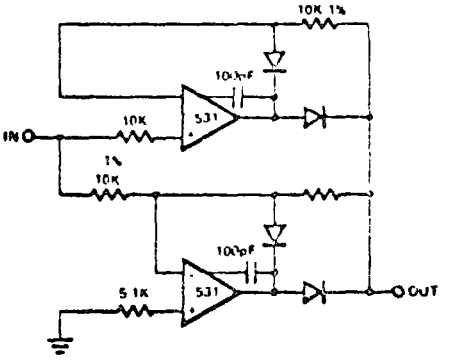


PRECISION RECTIFIERS

(a) HALF WAVE

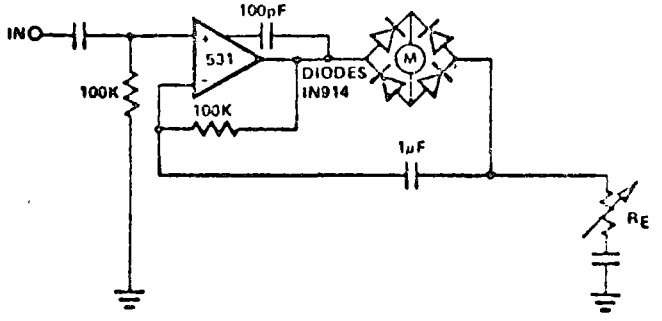


(b) FULL WAVE

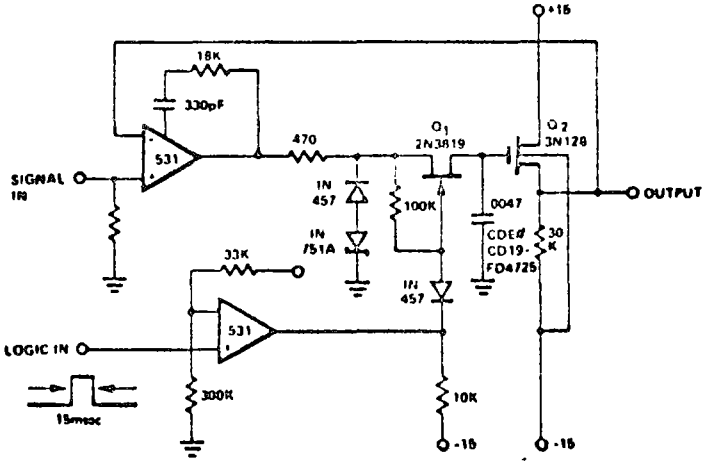


TYPICAL APPLICATIONS (Cont'd.)

AC MILLIVOLTMETER



SAMPLE AND HOLD



DESCRIPTION

The 533 is a high performance operational amplifier specifically designed for applications requiring low power consumption or reduced supply voltage. The 533 features single capacitor compensation, input and output protection and is pin compatible with the μA709, μA748, and LM101.

FEATURES

- LESS THAN 100μW POWER DISSIPATION
- LOW INPUT OFFSET VOLTAGE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH COMMON MODE AND POWER SUPPLY REJECTION RATIOS
- EXCELLENT TEMPERATURE STABILITY
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±13V
Differential Input Voltage		±5V
Input Voltage		$\pm V_S$
Operating Temperature Range	SE533	-55°C to +125°C
	NE533	0°C to 70°C
Lead Temperature (Solder, 60 sec)		300°C
Output Short Circuit Duration (Note 1)		Indefinite

1. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PULSE RESPONSE TEST CIRCUIT

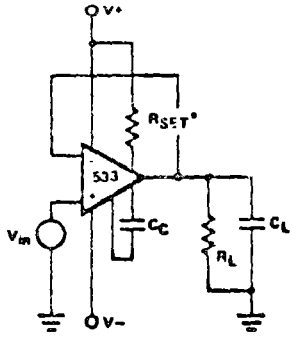
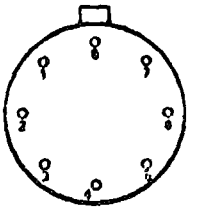


FIGURE 1

PIN CONFIGURATION

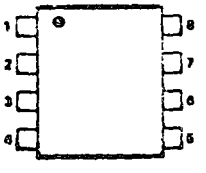
T PACKAGE
(Top View)



1. Compensation
2. Inverting Input
3. Noninverting Input
4. V^-
5. Compensation
6. Output
7. V^+
8. R_{SET}

ORDER PART NOS.
SE533T/NE533T

V PACKAGE
(Top View)



1. Compensation
2. Inverting Input
3. Noninverting Input
4. V^-
5. Compensation
6. Output
7. V^+
8. R_{SET}

ORDER PART NOS.
SE533V/NE533V

NOTE

R_{SET} establishes internal biasing of the amplifier to allow for a wide range of supply voltages. Recommended values of R_{SET} are 3.9mΩ at V_s = ±3V or 15mΩ at V_s = ±15V. Consult graphs for intermediate values.

ELECTRICAL CHARACTERISTICS (NOTE 1)

PARAMETER	CONDITIONS	NE533			SE533			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_S = ±3V, and ±15, R_S = 100KΩ			3				mV
Input Offset Voltage	V_S = ±3V, and ±15V, R_S=100K, T_A=25°C		1	2		0.5		mV
Input Bias Current	V_S = ±3V, and ±15V			30			3.0	nA
Input Bias Current	V_S = ±3V, and ±15V, T_A = 25°C		5	10		2	10	nA
Input Offset Current	V_S = ±3V, and ±15V			10			10	nA
Input Offset Current	V_S = ±3V, and ±15V, T_A = 25°C		1	5		0.5	5	nA
Input Resistance	V_S = ±3V, and ±15V	15			15			mΩ
Input Resistance	V_S = ±3V, and ±15V, T_A = 25°C	30	60		30	60		mΩ
Input Voltage Range	V_S = ±3V	±1.50			±1.50			V
Input Voltage Range	V_S = ±15V	±10			±10			V
Large Signal Voltage Gain	V_S = ±3V, R_L ≥ 20kΩ, V_{out} = ±1.0V	10			10			V/mV
Large Signal Voltage Gain	V_S = ±3V, R_L ≥ 20kΩ, V_{out} = ±1.0V, T_A = 25°C	12	15		16	20		V/mV
Large Signal Voltage Gain	V_S = ±15V, R_L ≥ 50kΩ, V_{out} = ±10V	25			25			V/mV
Large Signal Voltage Gain	V_S = ±15V, R_L ≥ 50kΩ, V_{out} = ±10V, T_A = 25°C	40	60		50	70		V/mV
Output Short Circuit Current	V_S = ±3V, ±15V, T_A = 25°C		6			6		mA
Common Mode Rejection Ratio	V_S = ±3V, R_S ≤ 100kΩ	74			80			dB
Common Mode Rejection Ratio	V_S = ±3V, R_S ≤ 100kΩ, T_A = 25°C	84	105		90	100		dB
Common Mode Rejection Ratio	V_S = ±15V, R_S ≤ 100kΩ	84			80			dB
Common Mode Rejection Ratio	V_S = ±15V, R_S ≤ 100kΩ, T_A = 25°C	90	110		100	120		dB
Power Supply Rejection Ratio	V_S = ±3V to ±15V, R_S ≤ 100kΩ			100			50	μV/V
Power Supply Rejection Ratio	V_S = ±3V to ±15V, R_S ≤ 100kΩ, T_A=25°C T_A = 25°C		20	50		10	25	μV/V
Supply Current	V_S = ±3V V_O = 0V			20			1	μA
Supply Current	V_S = ±15V V_O = 0V			50			30	μA
Power Dissipation	V_S = ±3V V_O = 0V			120			1.6	mW
Power Dissipation	V_S = ±15V V_O = 0V			1.5			0.9	mW

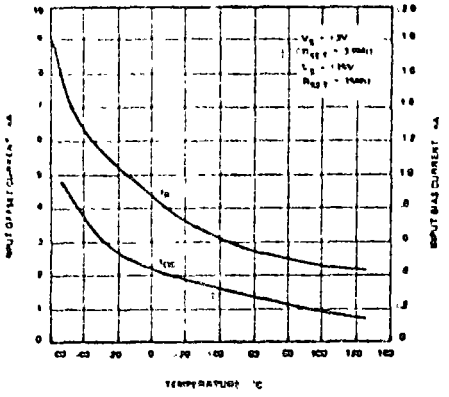
TRANSIENT RESPONSE (See Figure 1)

Rise Time	V_S = ±3V, R_L = 20k, C_L = 100pF		2			2		[illegible]
Overshoot	V_{in} = 10mV, C_C = 0.05μf		10			10		%
Slew Rate	T_A = 25°C		5			5		V/μsec
Rise Time	V_S = ±15V, R_L = 50k, C_C = 100pF		1			1		μsec
Overshoot	V_{in} = 20V, C_C = 0.05μf		10			10		%
Slew Rate	T_A = 25°C		30			30		V/μsec

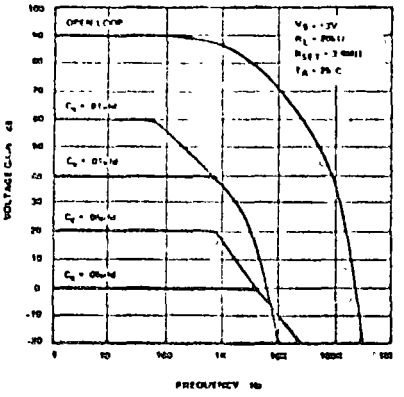
NOTE 1. Specifications apply for the full temperature range unless otherwise stated. For V_S = ±3V R_{set} = 3.9mΩ, for V_S = ±15V R_{set} = 1mΩ

TYPICAL CHARACTERISTIC CURVES

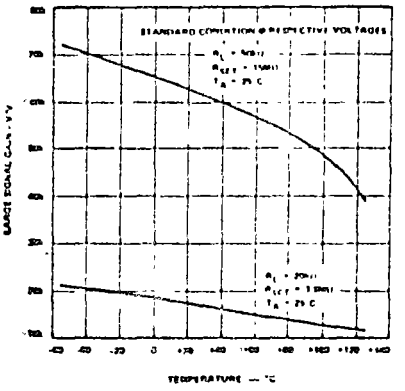
INPUT BIAS AND OFFSET CURRENTS AS FUNCTIONS OF AMBIENT TEMPERATURE



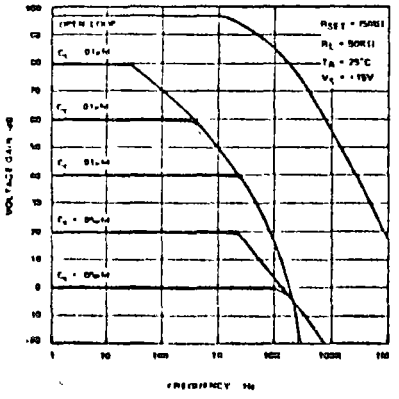
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



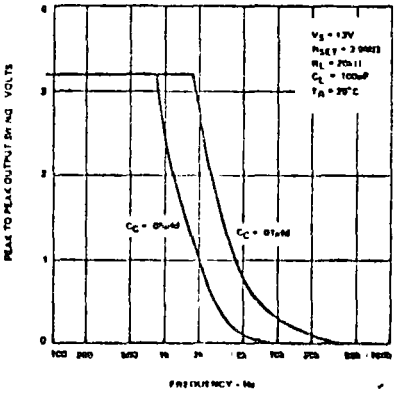
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



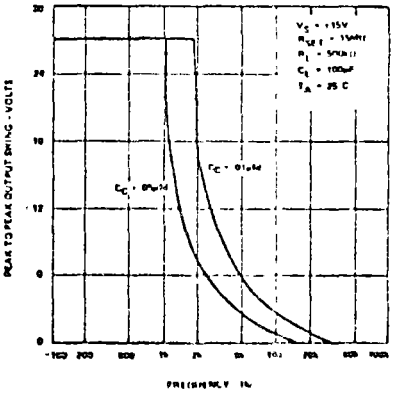
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



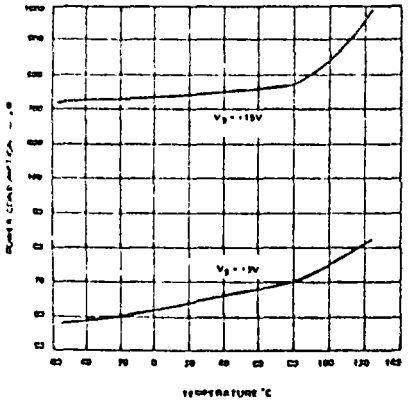
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



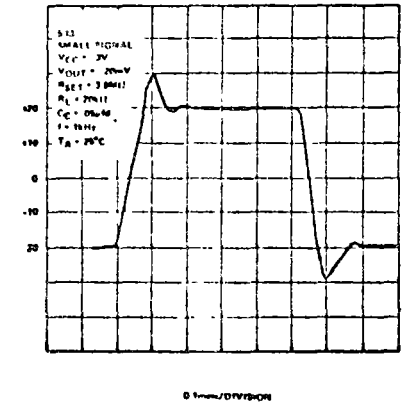
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



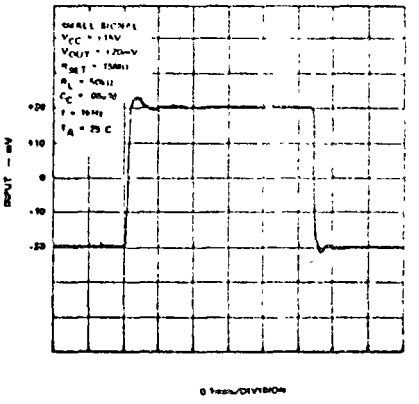
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



SMALL SIGNAL UNITY GAIN TRANSIENT RESPONSE

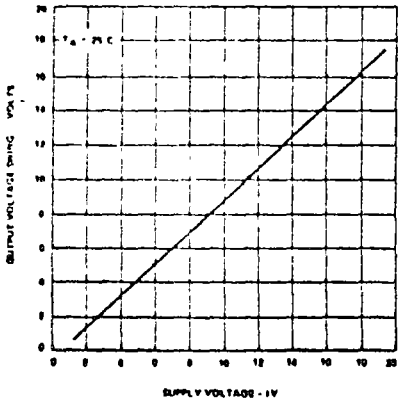


SMALL SIGNAL UNIT GAIN TRANSIENT RESPONSE

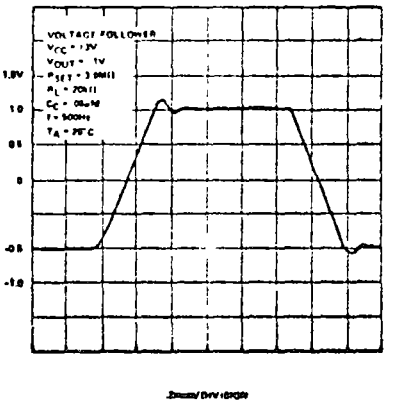


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

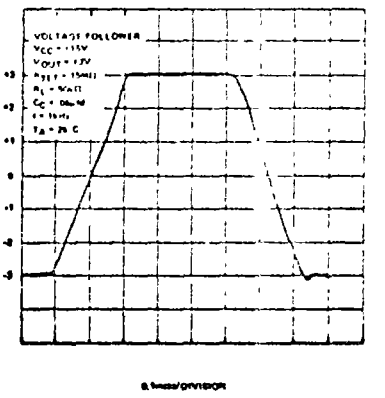
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



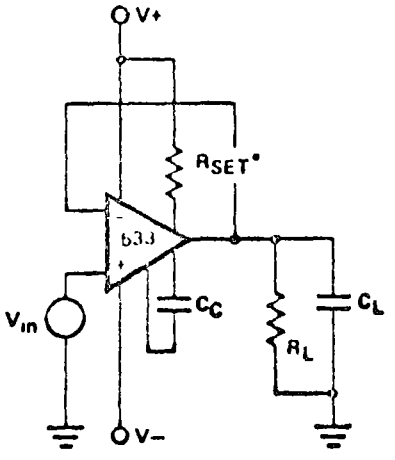
UNITY GAIN VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



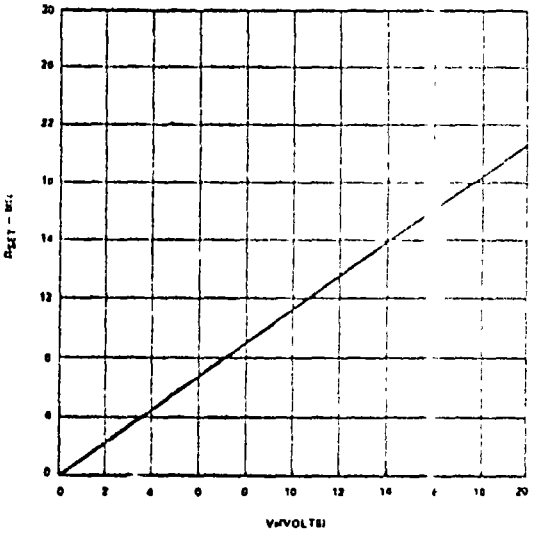
UNITY GAIN VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



TYPICAL APPLICATIONS



RECOMMENDED VALUES OF R_{SET} FOR INTERMEDIATE SUPPLY VOLTAGES



DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing a FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

- 5pA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- 1 MHz UNITY GAIN BANDWIDTH

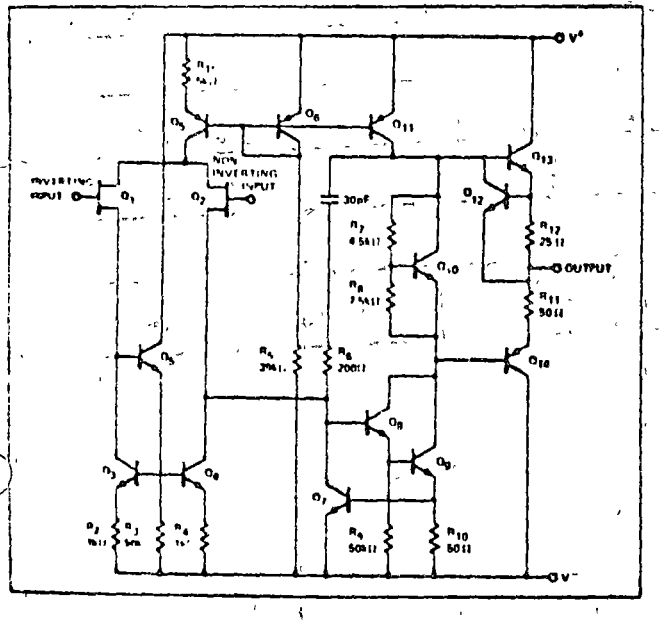
ABSOLUTE MAXIMUM RATING

Supply Voltage		±22V
Differential Input Voltage Range		±30V
Common Mode Input Voltage Range		$\pm V_s$
Power Dissipation (Note 1)		500mW
Operating Temperature Range	SU536T	−55°C to +85°C
	NE536T	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Solder, 60 sec)		300°C
Output Short Circuit Duration (Note 2)		Indefinite

NOTES

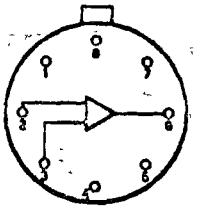
1. Rating applies for case temperatures to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75 °C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT



PIN CONFIGURATION

T PACKAGE
(Top View)

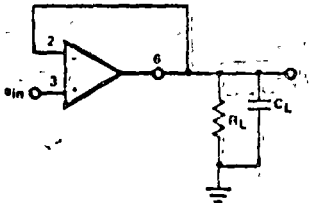


1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V⁻
5. Offset Null
6. Output
7. V⁺
8. NC

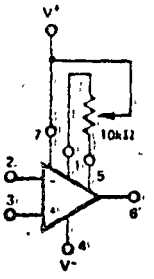
ORDER PART NOS. SE536T/NE536T

TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT



OFFSET NULL CIRCUIT



ELECTRICAL CHARACTERISTICS (SU536: $\pm 6V \leq V_S \leq \pm 20V$, NE536. $V_S = \pm 15V$ unless otherwise noted.)

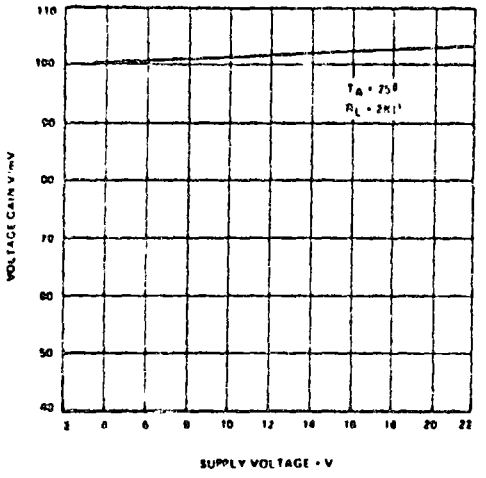
PARAMETER	TEST CONDITIONS	SU536			NE536			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISITICS								
Large Signal Voltage Gain @ +25°C	$V_S = \pm 15$ V, $V_{OUT} = \pm 10V$	50	100		50	100		V/mV
Over Temperature Range	$R_L > 2k\Omega$	50	100		25	100		V/mV
Input Offset Voltage @ +25°C			7.5	20		30	90	mV
Over Temperature Range			7.5	30		30		mV
vs Temperature (drift)			20			30		µV/°C
vs Common Mode Voltage (C M R R)	$V_{IN} = \pm 10V$, $R_S < 10k\Omega$	70	80		64	80		dB
vs Power Supply (P S R R)	Note 1, $R_S < 10k\Omega$		50	150		100	300	µV/V
Input Current @ +25 C			5	30		30	100	pA
Over Temperature Range	Either Input		250	3000				pA
vs Temperature (drift)		Typ Doubles Every 10°C						
Input Offset Current @ +25°C			5			5		pA
Over Temperature (drift)								
Input Impedance								
Differential Resistance	$T_A = +25°C$		10^{14}			10^{14}		Ω
Differential Capacitance	$T_A = +25°C$		6			6		pF
Input Noise (0.1Hz – 100kHz)								
Voltage Noise			20			20		µVrms
Common Mode Voltage Range	$V_S = \pm 15V$	±10	±11		±10	±11		V
OUTPUT CHARACTERISTICS								
Output Current	$V_S = \pm 15V$	5			5			mA
Open Loop Output Impedance			100			100		Ω
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 2k\Omega$	±10	±12		±10	±10		V
	$V_S = \pm 15V$, $R_L \geq 10k\Omega$	±12	±13		±12	±13		V
Short Circuit Current	$V_S = \pm 15V$, $T_A = +25°C$		17			17		mA
FREQUENCY AND TRANSIENT RESPONSE								
Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = +25°C$, A = 100		1			1		MHz
Unity Gain Frequency	$V_S = \pm 15V$, $T_A = +25°C$		1			1		MHz
Full Power Bandwidth	$V_S = \pm 15V$, $T_A = +25°V$		100			100		kHz
Slew Rate								
Inverter	$V_S = \pm 15V$, $T_A = +25°C$, A = -1		6			6		V/µs
Follower	$V_S = \pm 15V$, $T_A = +25°C$, A = +1		6			6		V/µs
POWER SUPPLY REQUIREMENT								
Power Supply Range		±6		±20	±6		±18	V
Quiescent Supply Current	$V_S = \pm 20V$, $V_{OUT} = 0V$, $T_A = +25°C$		4.5	5.5				mA
	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$					6.0	8.0	mA
Quiescent Power Dissipation	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$		180			180		mW

Parameters are tested over temperature range unless otherwise noted.

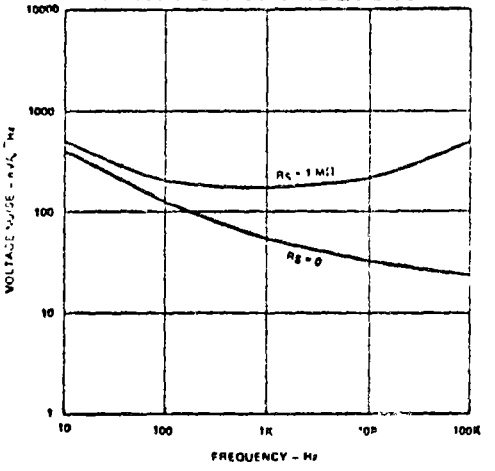
NOTE 1 SU536 $V_S = \pm 6V$ to $\pm 20V$
NE536 $V_S = \pm 6V$ to $\pm 15V$

TYPICAL CHARACTERISTIC CURVES

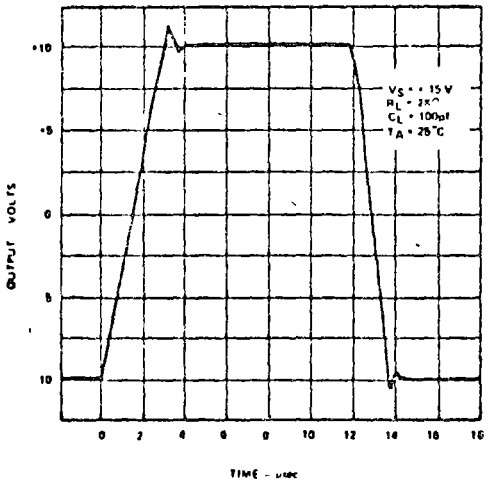
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



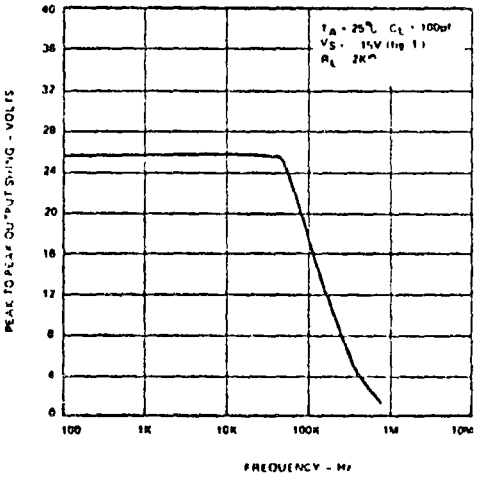
INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



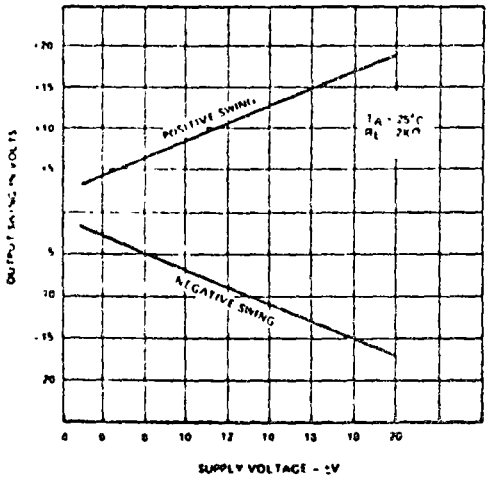
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



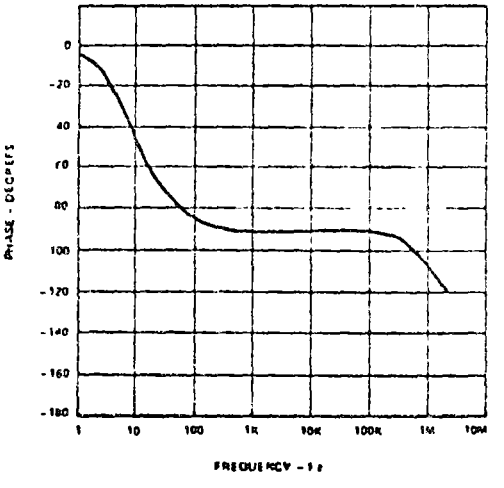
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

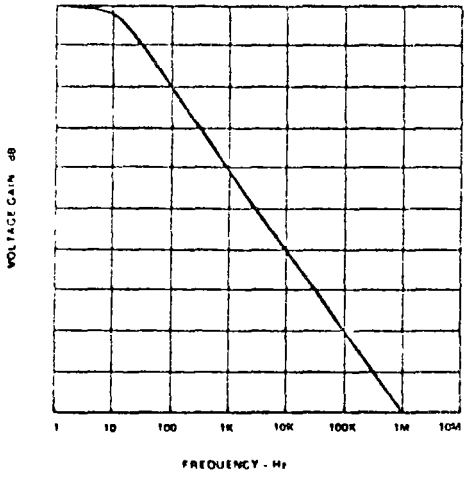


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

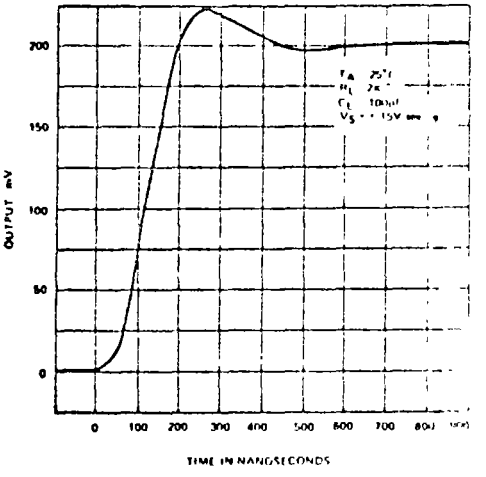


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

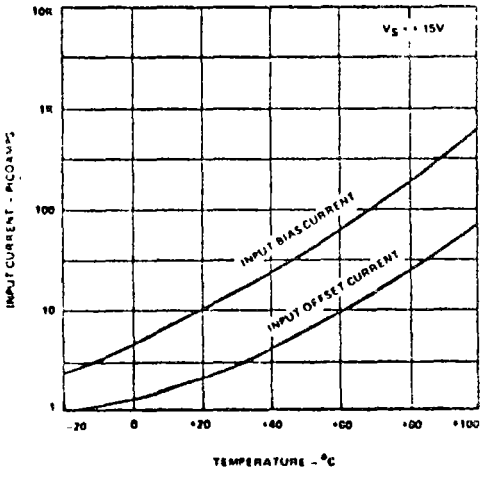
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



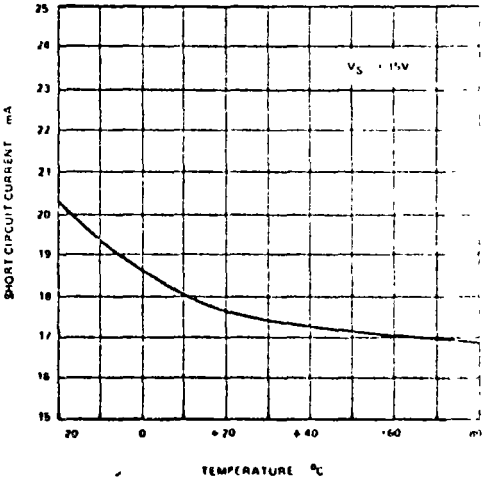
VOLTAGE FOLLOWER TRANSIENT RESPONSE



INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SIGNETICS

HIGH PERFORMANCE OPERATIONAL AMPLIFIER | μA741

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

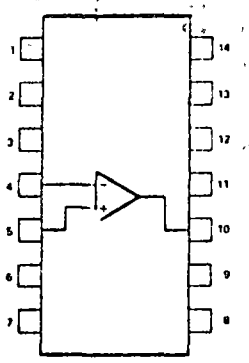
ABSOLUTE MAXIMUM RATINGS

	μA741C	μA741
Supply Voltage	±18V	±22V
Internal Power Dissipation (Note 1)	500mW	500mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Voltage between Offset Null and V⁻	±0.5V	±0.5V
Operating Temperature Range	0°C to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Solder, 60 sec)	300°C	300°C
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite

Notes
1. Rating applies for case temperatures to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATIONS

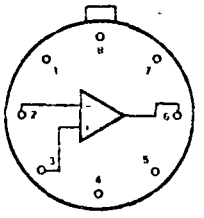
A PACKAGE
(Top View)



1. NC
2. NC
3. Offset Null
4. Inv. Input
5. Non-Inv. Input
6. V⁻
7. NC
8. NC
9. Offset Null
10. Output
11. V⁺
12. NC
13. NC
14. NC

ORDER PART NO. μA741CA

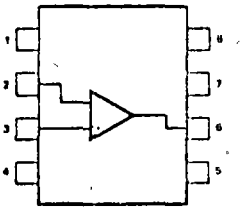
T PACKAGE



1. Offset Null
2. Inverting Input
3. Non-Inverting Input
4. V⁻
5. Offset Null
6. Output
7. V⁺
8. NC

ORDER PART NOS. μA741T/μA741CT

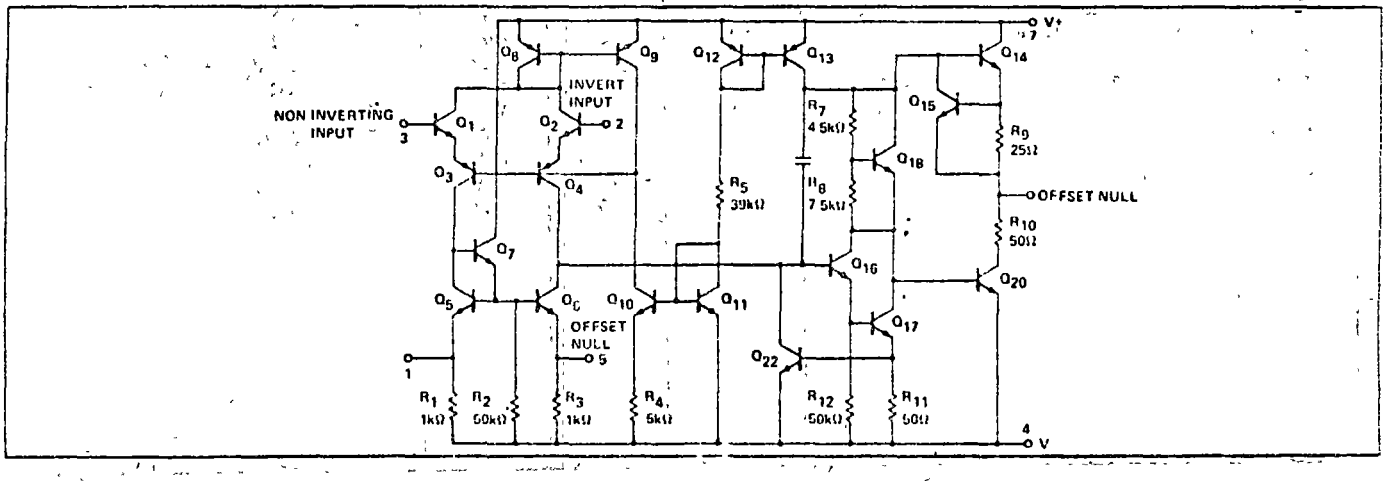
V PACKAGE



1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V⁻
5. Offset Null
6. Output
7. V⁺
8. NC

ORDER PART NO. μA741CV

EQUIVALENT CIRCUIT

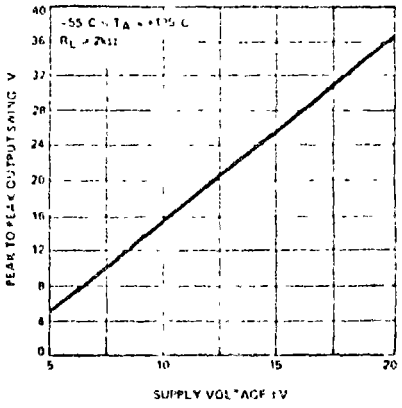


ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

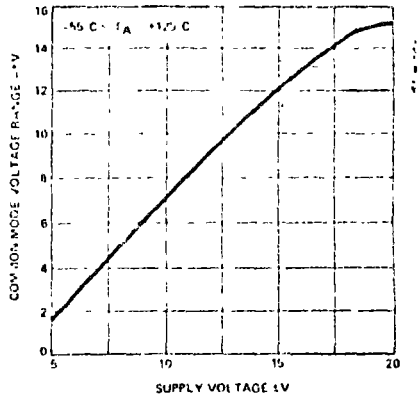
PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
μA741C					
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		20	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	20,000	200,000			$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Output Resistance		75		Ω	
Output Short-Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					V_{in} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Offset Voltage			7.5	mV	
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large Signal Voltage Gain	15,000				$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±10	±13		V	$R_L \geq 2k\Omega$
μA741					
Input Offset Voltage		1.0	5.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		10	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Large Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Resistance		75		Ω	
Output Short Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					V_{in} = 20mV, R_L = 2kΩ, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Input Offset Voltage		1.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		7.0	200	nA	T_A = +125°C
		20	500	nA	T_A = −55°C
Input Bias Current		0.03	0.5	μA	T_A = +125°C
		0.3	1.5	μA	T_A = −55°C
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	25,000				$R_L \geq 2k\Omega$, V_{out} = ±10V
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Supply Current		1.5	2.5	mA	T_A = +125°C
		2.0	3.3	mA	T_A = −55°C
Power Consumption		45	75	mW	T_A = +125°C
		45	100	mW	T_A = −55°C

TYPICAL CHARACTERISTIC CURVES

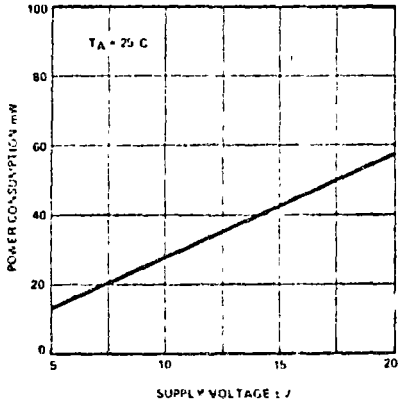
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



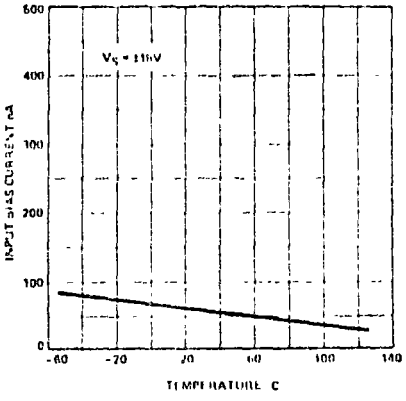
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



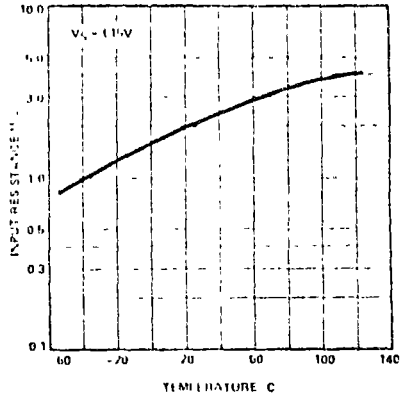
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



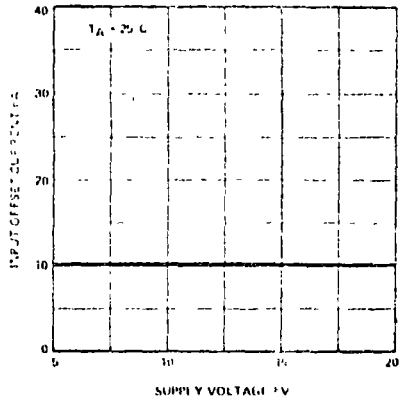
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



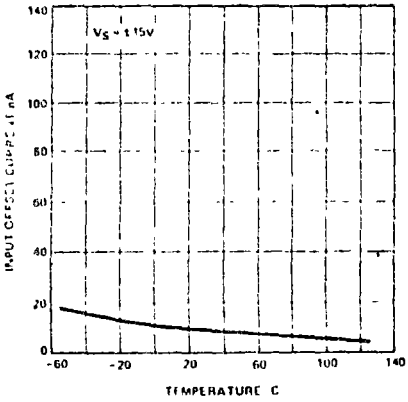
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



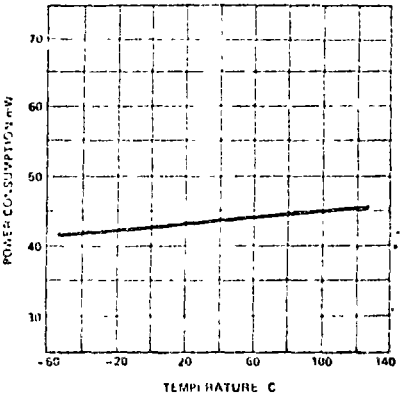
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



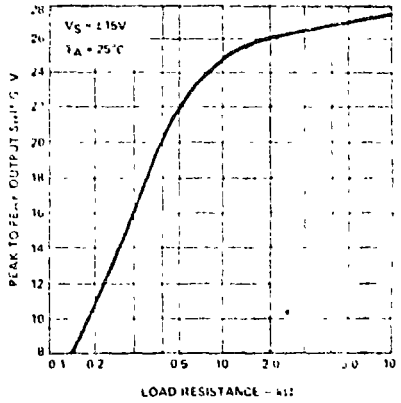
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

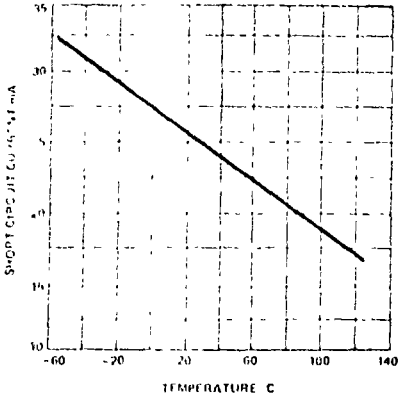


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

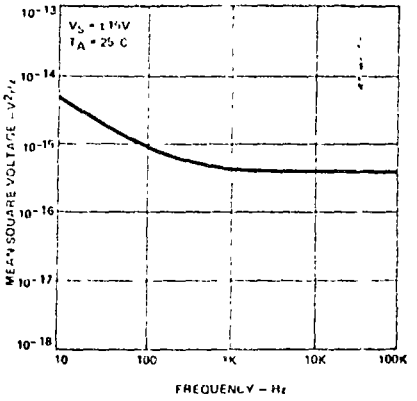


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

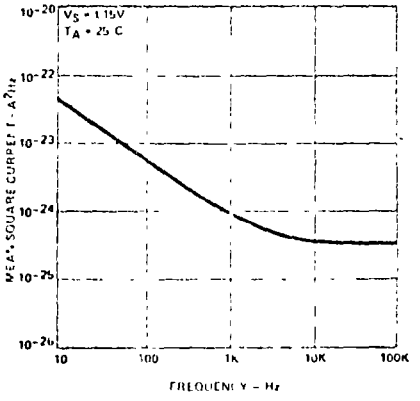
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



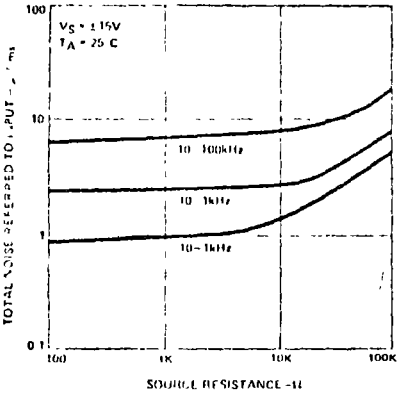
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



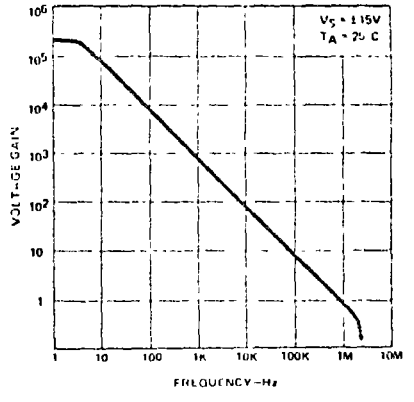
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



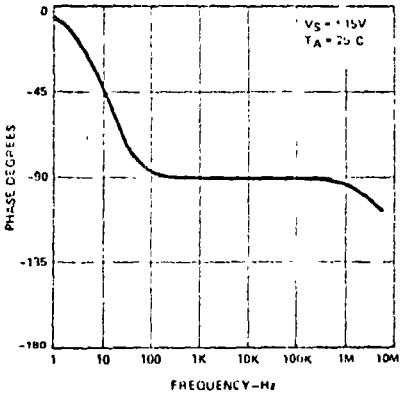
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



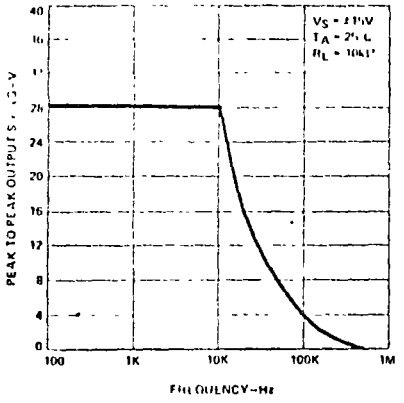
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



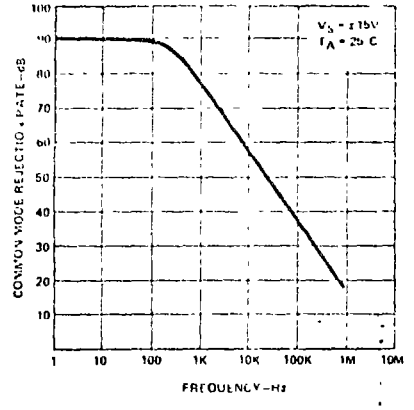
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



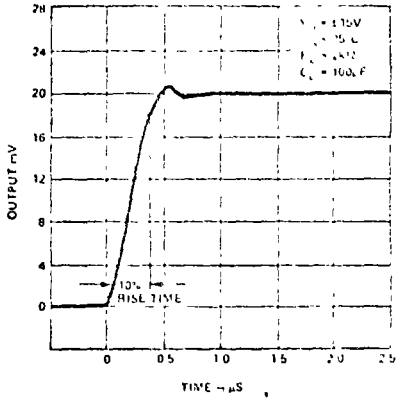
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



Algunos aspectos elementales del amplificador operacional

Eduardo Cristo Alvarez
Luis M. Hernández Ortega

1. INTRODUCCION

Con el termino amplificador operacional, se designe en un principio a aquellos dispositivos que se ajustan lo mejor posible a un cierto concepto ideal que se puede definir como un amplificador que cumple los siguientes requisitos:

— Impedancia de entrada infinita
— impedancia de salida nula
— Ganancia diferencial de voltaje infinita
— Ganancia común de voltaje nula.

Aunque antes su empleo se limitó al campo de las computadoras analógicas, es en la actualidad uno de los bloques más utiles con que cuenta el diseñador de sistemas electrónicos analogicos; se puede decir que el amplificador operacional surge en 1947, con el trabajo de Ragazzini (ref 1).

El objeto del presente articulo no es señalar algunas aplicaciones del amplificador operacional pues son tantas que se requieren textos completos para listar algunas de ellas (refs 2 y 3), más bien se trata de presentar las principales caracteristicas de los diferentes tipos de amplificadores operacionales que existen actualmente en el mercado; explicar el porque (cualitativamente) de sus limitaciones y, por ultimo, presentar el panorama que se abre ante el diseñador de sistemas debido a la inclusión de macromodelos de amplificadores operacionales como parte de los simuladores digitales de circuitos electrónicos.

Actualmente, no todos los amplificadores operacionales se ajustan al modelo ideal presentado al principio de este articulo, ya que existen en el mercado circuitos cuya transconductancia es variable, por ejemplo el CA3060 de RCA (ref 4), cuyo modelo se muestra en la fig 1.1-b y el LM3900 (ref 5) de National Semiconductors, que podria definirse como un amplificador diferencial de corriente, comúnmente denominado amplificador operacional de Norton (fig 1.1-c).

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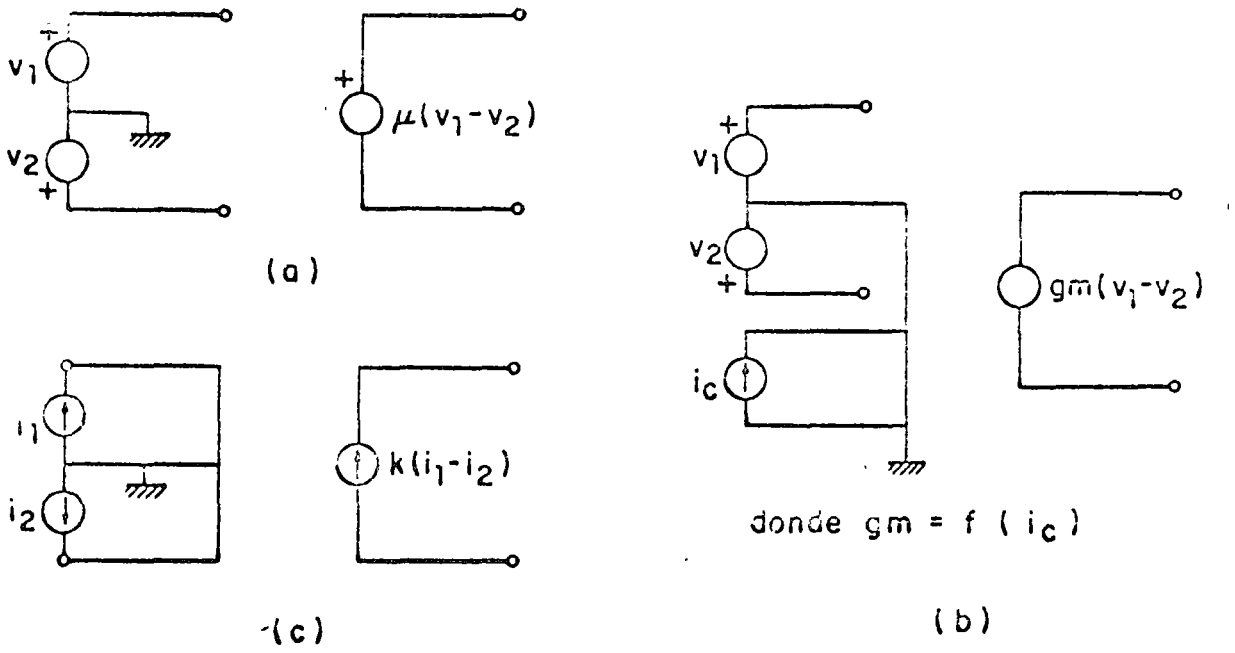


Fig. 1.1

2. CONFIGURACIONES TIPICAS SIMPLIFICADAS

2.1 Etapa de entrada

Se centrará la atención en la etapa de entrada, ya que en ella residen las caracteristicas que distinguen entre si los diversos tipos de amplificadores operacionales.

2.1.1 Amplificador operacional de voltaje

El circuito que tradicionalmente se emplea para llevar a la práctica este tipo de amplificador es el par acoplado por emisor, polarizado mediante una fuente de corriente, realizada por medio de un espejo de corriente. En la fig 2 1 se muestra esta etapa; Q_1 y Q_2 constituyen el par acoplado por emisor y Q_3 y Q_4 (conectado como doido), la fuente de corriente.

Una de las limitaciones de esta configuración es que, para su correcto funcionamiento, requiere que los transistores que integran el par acoplado por emisor posean iguales caracteristicas (ocurre algo similar con el par de transistores que componen la fuente de corriente); si se realiza el circuito en forma monolitica, se puede obtener dicha igualdad de caracteristicas: por otra parte, si se analiza la polarización mediante fuente de corriente, se verá que esta depende de relaciones adimensionales de resistencias, lo cual facilita fijar los puntos de operación de los transistores dentro de limites aceptables de variación (ref 6).

Esta configuración de entrada es fácilmente modificable, para satisfacer especificaciones más estrictas, por ejemplo: para altas impedancias de entrada, Q_1 y Q_2 pueden ser sustituidas por conexiones tipo Darlington o mediante Darlington hibrido con entrada por JFET, con lo cual se pueden obtener impedancias de entrada del orden de 10^{12} ohmios; si el problema es la respuesta en el dominio de la frecuencia, Q_1 y Q_2 pueden sustituirse por un cascodo, etc.

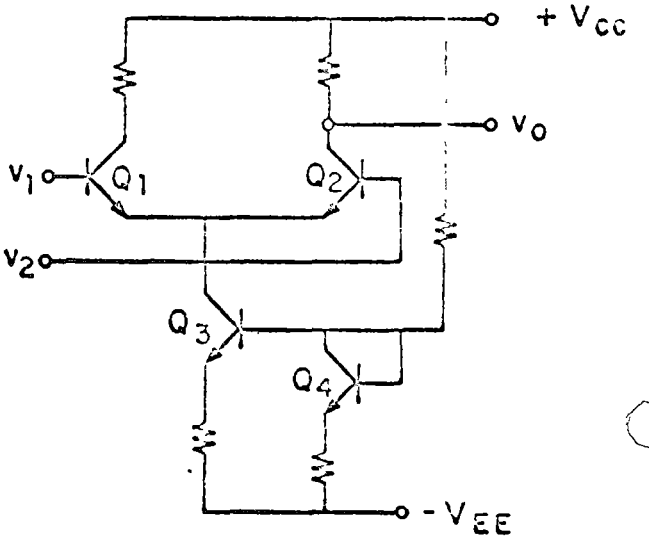


Fig 2.1

2.1.2 Amplificador operacional de transconductancia

Este tipo de amplificador operacional basa su funcionamiento en la caracteristica de dependencia lineal de la transconductancia de pequeña señal en un TBJ con la corriente de colector (ref 7), o sea que se puede cambiar la transconductancia equivalente del par diferencial variando externamente su corriente de polarización; la solución más comúnmente empleada se muestra en la fig 2.2, donde si se considera la ganancia de corriente (β) del transistor Q_1 muy grande, la corriente que fluya por Q_1 y Q_2 será esencialmente ic/2. Un análisis más detallado puede encontrarse en el Manual de aplicación del CA3060 (ref 4).

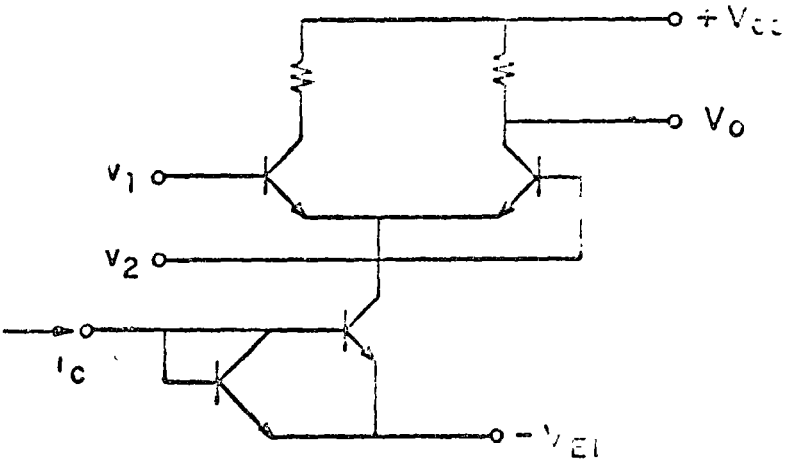


Fig 2.2

2.1.3 Amplificador operacional de Norton

En este tipo de amplificador operacional se pretende emplear una señal diferencial de corriente para controlar la salida del dispositivo. Una configuración empleada para satisfacer este propósito usa el concepto de "espejo de corriente" y se muestra en la fig 2.3.

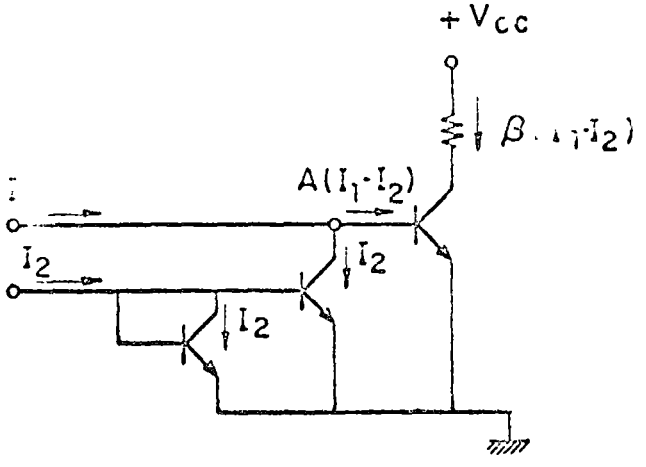


Fig 2.3

Se puede apreciar que la comparacion de corrientes se efectúa en el nodo A, donde la corriente I_1 se resta a la corriente I_2; esta es una de las principales limitaciones del dispositivo, ya que forzosamente $I_2 > I_1$; nuevamente se remite al lector interesado en profundizar en este tipo de amplificadores a las notas de aplicación del fabricante, en este caso National Semiconductors (ref 5) en el capitulo referente al LM3900.

2.2 Etapa intermedia

Hay aspectos sumamente importantes dentro del diseño de amplificadores operacionales; como el de convertir la salida diferencial del par acoplado por emisor a salida común.

Obviamente existe la solución trivial consistente en tomar la salida entre alguno de los colectores del par y el nodo de referencia, esta solucion adolece del defecto de reducir la ganancia a la mitad, lo cual es un grave problema en un circuito con el que se desean obtener altos niveles de ganancia. El problema puede resolverse mediante una configuración denominada amplificador polarizado por diodos (ref 7), que se muestra en la fig 2.4.

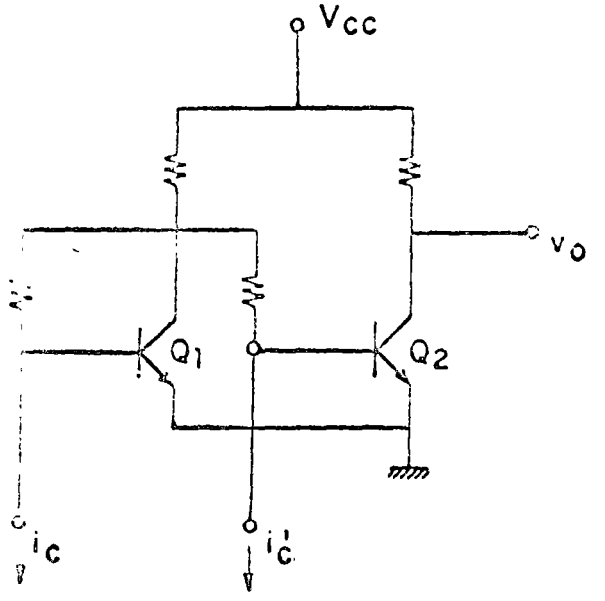


Fig 2.4

Si en esta configuración se sustituyen las fuentes i_c e i'_c por los colectores de Q_1 y Q_2 de la fig 2.1, se pueden obtener salidas comunes a partir de etapas con salida diferencial de corriente. Analizando el amplificador se llega a:

$$V_0 = 2\,\beta\,R_1\,i_{c_1}$$

además, como $Vce_1 \doteq Vcc_2 = \dfrac{2\,Vcc}{\beta} + Vbe + \dfrac{R_1\,I_c}{2}$, evidentemente los puntos de operación no dependerán de los parámetros de los dispositivos activos empleados, esto estabiliza al dispositivo con respecto a variaciones de dichos parámetros de fabricación. Es claro que existen muchas otras configuraciones que proporcionan ganancia de voltaje; sin embargo, estas son ampliamente conocidas y no requieren de una nueva presentación; cabe mencionar en este punto que existen también configuraciones como la celda de Gilbert (ref 8), cuyo principal objetivo es la ganancia de corriente; dicha configuración se muestra en la fig 2.5.

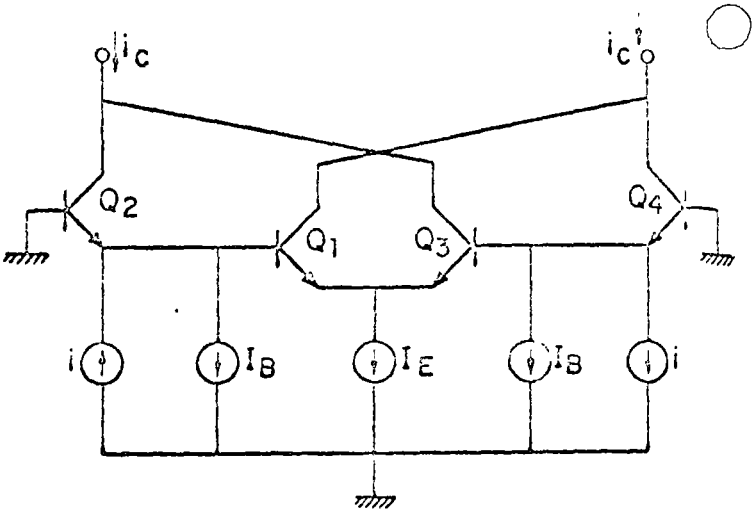


Fig 2.5

Un análisis del circuito (ref 9) muestra que

$$A_i = 1 + \frac{I_E}{2I_B}$$

O sea que la ganancia de la celda puede escogerse seleccionando la relación $\dfrac{I_E}{I_B}$ en forma adecuada; más aún, excepto en la polarización de las fuentes de corriente, no se emplean resistencias, lo cual simplifica el diseño en forma monolítica (ref 6).

2.3 Etapa de salida

Esta es la etapa que constituye el acoplamiento con los demás circuitos del sistema; sus características dependen, por tanto, de las del modelo teórico que se desee emplear. En caso de amplificadores operacionales convencionales, esta etapa consta de algún arreglo en tipo AB; un problema interesante de diseño en estos circuitos son las redes de cambio de nivel de $D.C.$ necesarias para garantizar que habrá 0 voltios a la salida para 0 voltios a la entrada. Lo anterior se consigue, generalmente, como se muestra en la fig 2.6 en forma simplificada. En este circuito, que esencialmente es un emisor seguidor, la polarización del transistor Q_1 se logra mediante la fuente de corriente Q_2, Q_3. Dado que la impedancia que presenta dicha fuente de corriente es mucho mayor que la resistencia R, no habrá atenuación de señal, pero sí una caída de voltaje proporcional a la corriente de operación I_{EQ}.

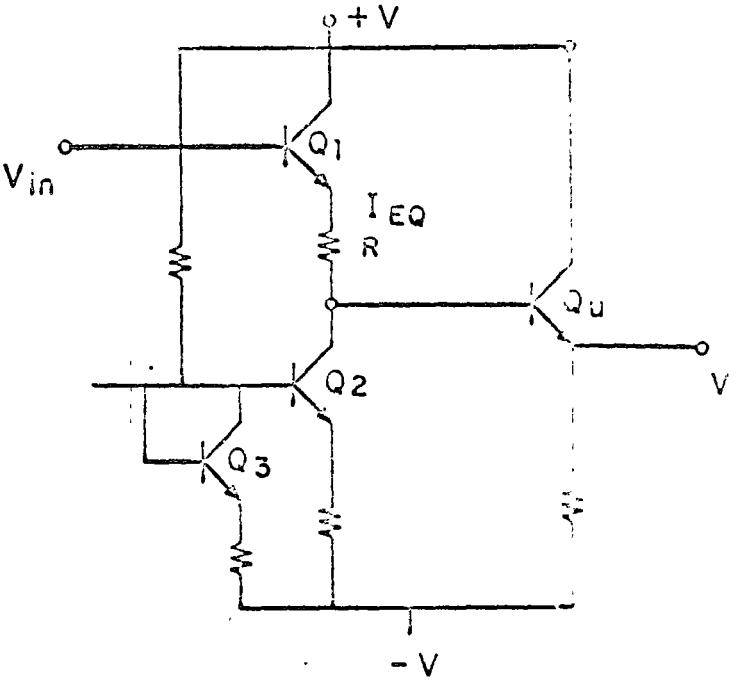


Fig 2.6

En tal caso, el transistor Q_4 es la etapa de potencia (clase A) con característica de baja impedancia de salida. Hasta aquí se han mostrado, en forma simplificada, algunas de las etapas que integran un amplificador operacional, teniendo en mente fundamentalmente motivar al estudio más profundo y sobre todo a su aplicación.

3. DESVIACIONES DEL MODELO IDEAL

En esta sección se presentan las principales desviaciones que tiene el amplificador operacional con respecto a un modelo ideal. Es evidente que también en este caso existe la necesidad de un estudio más profundo y del análisis de la configuración específica en cuestión para descubrir la raíz de las limitaciones; sin embargo, esto cada vez es más sencillo, debido a la presencia de simuladores y lo será aún más en lo futuro, cuando la principal preocupación respecto a estas no idealidades será caracterizarlas adecuadamente para cuantificar los parámetros de los modelos implantados en dichos simuladores.

A continuación se hace un análisis somero de las siguientes no idealidades de segundo orden

1. Slew rate
2. Offset
3. Tiempo de transición
4. Ancho de banda
5. Ruido

3.1 Slew rate

Si se excita un amplificador operacional con una función escalón $K\,u(t)$ de varios voltios y tiempo de subida lo bastante rápido (del orden de pico-segundos), se aprecia que la respuesta del amplificador no "sigue" a la entrada inmediatamente (ref 9). Esto es, la derivada del voltaje de salida con respecto al tiempo, es finita.

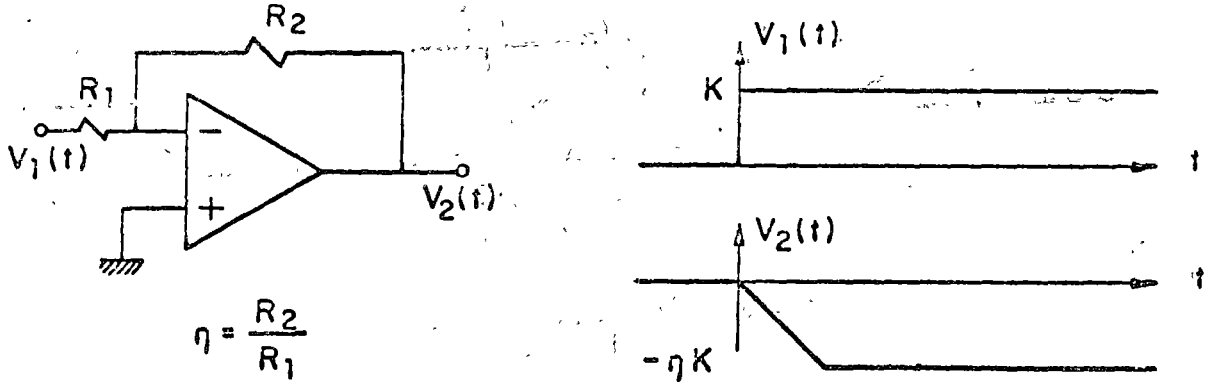


Fig 3.1

De acuerdo con la definición anterior

$$\frac{dV_2(t)}{dt} = \text{Slew rate}$$

$$\frac{dV_2(t)}{dt} = \infty \longrightarrow \text{Ideal}$$

$$\frac{dV_2(t)}{dt} \longrightarrow \text{entre 0.5 } V/\mu s \text{ y 2000 } V/\mu s \longrightarrow \text{Real}$$

Dividiendo al amplificador operacional en 3 etapas, exactamente como se planteó su estructura, se tiene

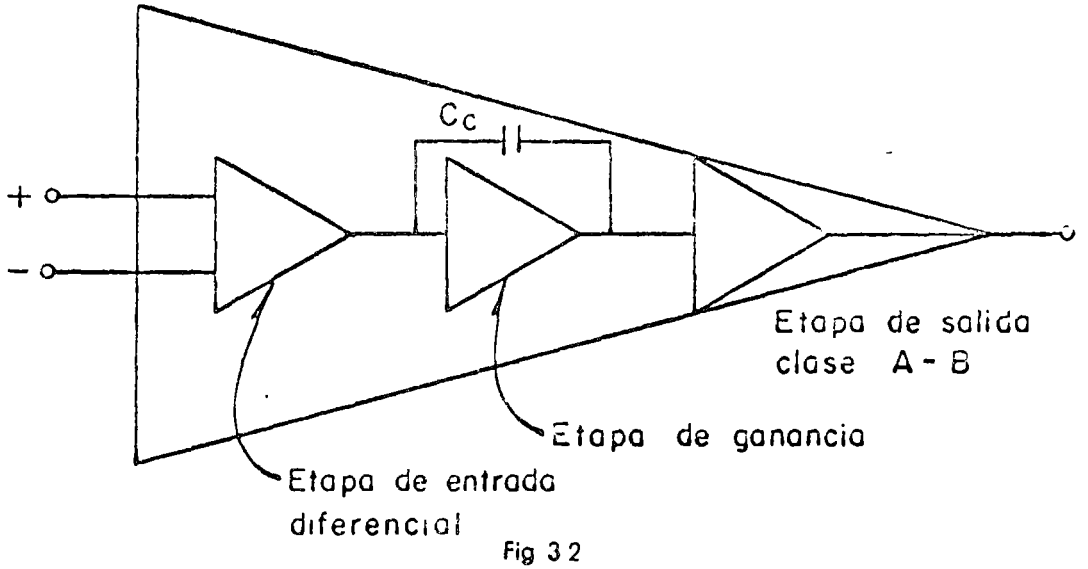


Fig 3.2

Para evitar que el amplificador operacional oscile la etapa de ganancia debe estar fuertemente compensada (ref 2); esto se logra aprovechando el efecto Miller, el cual puede verse como un efecto integrativo (ref 2). Debido al condensador C_c de compensación, son despreciables las capacitancias parásitas de esta etapa de ganancia, de la etapa de entrada diferencial, y de la etapa de salida clase AB, comparadas con la capacitancia C_c de compensación cuyo valor aparente es mucho mayor debido al antes mencionado efecto Miller.

Suponiendo nuevamente que se excita el amplificador operacional con una función escalón, y asumiendo que la etapa de salida clase AB reproduce fielmente la señal inyectada por la etapa intermedia de ganancia del amplificador operacional, se tiene

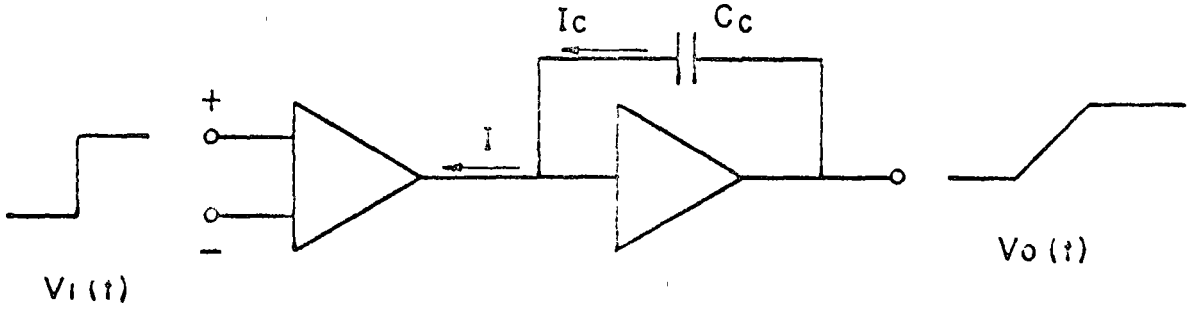


Fig. 3.3. Modelo para determinar el Slew rate asumiendo condiciones iniciales = 0. Esto es, C_c descargado

$$\frac{dV_o(t)}{dt} = \frac{I_c}{C_c}$$

$I_c = I$ debido a que la impedancia de entrada de la etapa de ganancia es bastante mayor que la impedancia de salida de la etapa de entrada diferencial

$$\frac{dV_o(t)}{dt} = \frac{I}{C_c}$$

Esto es, conociendo el valor del condensador de compensación de la etapa de ganancia C_c y el valor de la corriente entre las etapas de ganancia y de entrada, I, es posible determinar el Slew rate de un amplificador operacional.

Para verificar este resultado, se analizará el caso del μA 741, el cual tiene

$C_c = 30\ pf$ típico; $I = 15\ \mu A$ típicamente.

$$\text{Slew rate} = \frac{dV_o(t)}{dt} = \frac{15 \times 10^{-6}}{30 \times 10^{-12}} = 0.5\ V/\mu s.$$

3.2 Offset de voltaje a la entrada

Se denomina así al voltaje diferencial que es necesario aplicar para lograr que el voltaje de salida sea de cero voltios. La especificación típica para el offset de voltaje dada por el fabricante está referida a cero voltios de entrada en modo común, y para valores nominales de fuente de poder. El valor ideal de offset de voltaje es cero voltios; el valor real gira alrededor de cero voltios, siendo generalmente de $\pm$ 2 mv.

Para instrumentación, donde se requiere medición de bajos niveles de corriente directa, un error de voltaje como el correspondiente al offset opacaría completamente el nivel a medir.

A continuación se estudia el problema que trae consigo el offset de voltaje en un integrador simple como el mostrado en la fig 3.4.

Supóngase que $V_1(t) = 0$; esto implicaría que el voltaje de salida $V_2(t) = 0$, pero analizando la ec 3.2.1 se tiene

$$V_2(t) = V_{of} + \frac{1}{RC}\int_o^t V_{of}\ dt$$

$$V_1(t) = 0$$

Estas ecuaciones implican que el voltaje de salida $V_2(t)$ tendrá un valor inicial en $t = 0$, correspondiente al voltaje de offset y a partir de ese instante empezará a integrar V_{of} hasta llegar a un límite $\pm V_s$ correspondiente al voltaje de saturación de salida del amplificador operacional (fig 3.5).

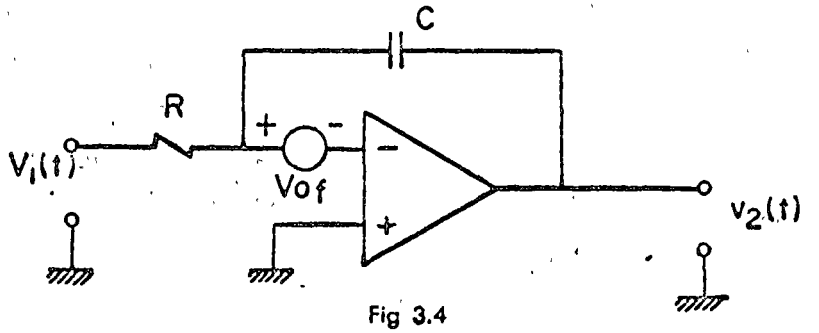


Fig 3.4

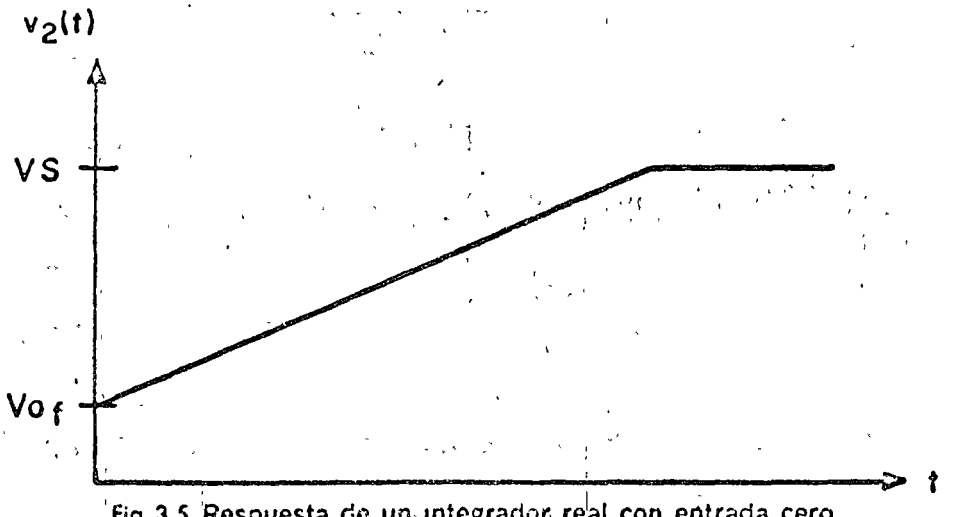


Fig 3.5 Respuesta de un integrador real con entrada cero

3.3 Tiempo de transicion

Es el tiempo que tarda la respuesta de un amplificador operacional en mantenerse entre 0.1 y 0.01 por ciento de su valor final. En muchas aplicaciones del amplificador operacional, dicho parámetro es muy importante.

El tiempo de transicion puede dividirse en dos periodos distintos: el primero esta limitado por el Slew rate del amplificador y es el tiempo en el cual el voltaje de salida cambia de su valor original a la vecindad de un nuevo valor. La segunda parte es el tiempo de asentamiento, o sea el periodo en que el voltaje de salida alcanza un valor razonablemente cercano (0.1 o 0.01 por ciento) a su valor final.

Los valores relacionados con el tiempo de transicion son dados por el fabricante con el amplificador montado en ganancia unitaria no inversora, como se muestra en la fig 3.6.

3.4 Ancho de banda con ganancia unitaria

Dentro de la region lineal del amplificador operacional, la ganancia de voltaje diferencial decrece cuando la frecuencia se incrementa. Junto con el margen de fase, el ancho de banda con ganancia unitaria es la forma más común (ref 4) de especificar la respuesta en frecuencia de un amplificador operacional.

Un análisis de la fig 3.7 muestra que la frecuencia f_t a la cual la ganancia es unitaria viene dada por

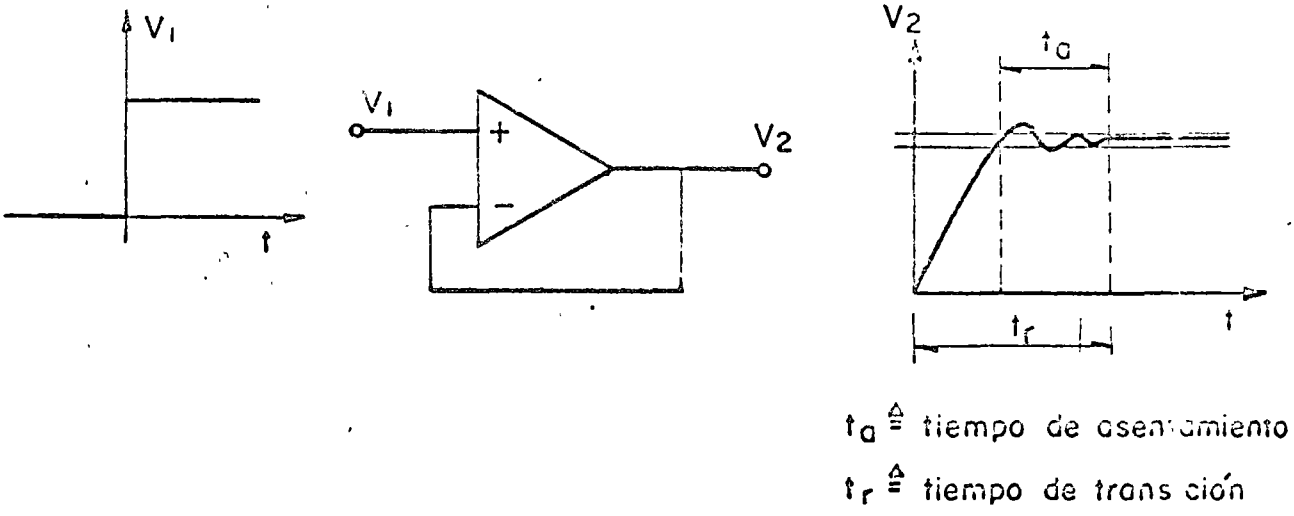


Fig 3.6 tiempo de transición

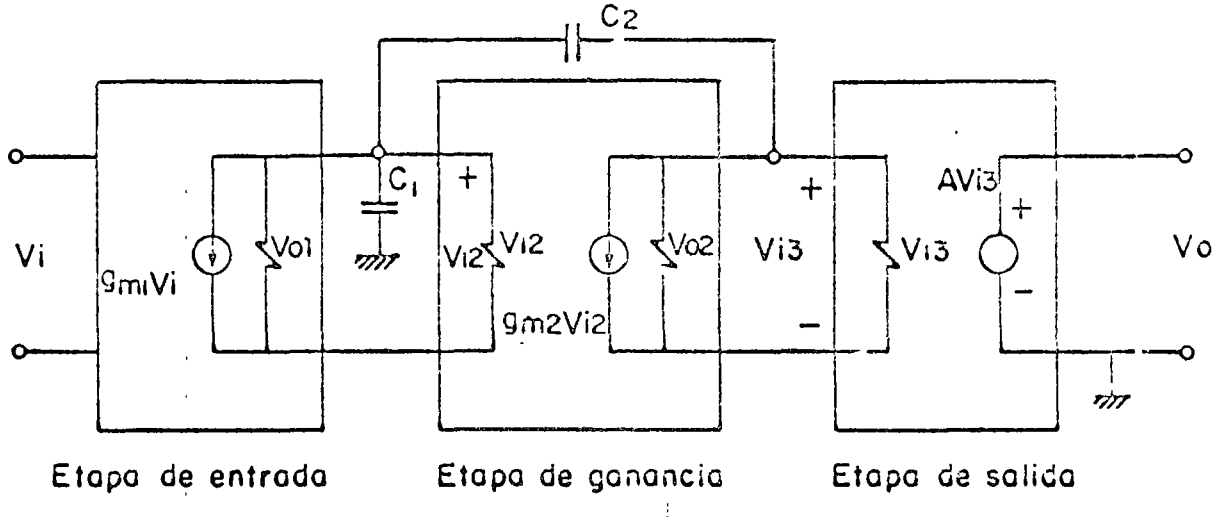


Fig. 3.7. Modelo para calcular frecuencia de corte

$$W_c = \frac{Gm_1\ A}{C_2}$$

considerando únicamente C_2

$$W_c = \frac{Gm_1\ Gm_2}{C_1}\ (r_{o2}\ //\ r_{i3})A$$

considerando únicamente C_1

Asumiendo que

$$(r_{o1}\ //\ r_{i2}) \gg \frac{1}{W_c\ C_1}$$

$$(r_{o1}\ //\ r_{i2}) \gg \frac{1}{C_2\ Gm_2\ (r_{o2}\ //\ r_{i3})\ W_c}$$

lo cual se satisface en cualquier tipo de amplificador operacional.

La tecnología actual en la fabricación de circuitos integrados es capaz de producir transistores NPN (ref 10) con una frecuencia de transición f_t del orden de 600-800 MHz; Por otra parte, los transistores PNP producidos con la misma tecnología, tienen una frecuencia de transición f_t del orden de 2·5 MHz, lo cual es una muy seria limitación para lograr un ancho de banda en amplificadores operacionales más allá de 1 MHz.

3.5 Ruido

Por ruido se entiende aquellas corrientes o voltajes que se generan dentro de los mismos dispositivos (transistores, resistencias, etc) que constituyen el circuito electrónico; la naturaleza del fenómeno es estocástica (ref 13), por tanto, en lo que respecta a su estudio se prefiere analizar el valor medio cuadratico de este tipo de señal, ya que entonces se pueden hacer comparaciones en términos de niveles de potencia Independientemente de la clasificación que se haga del ruido con base en sus caracteristicas, desde el punto de vista probabilistico, puede clasificarse de acuerdo con la naturaleza fisica del fenómeno en:

1 Ruido térmico: Causado por la agitación molecular hasta una frecuencia de 10^{11} Hz; depende linealmente de la temperatura absoluta.

2 Ruido discreto: Es causado por el flujo de portadores de carga (electrones, iones o huecos) a través de una región carente de estos cuando se presentan las siguientes condiciones:

— El flujo de los portadores es un fenómeno cuántico y aleatorio

— El tiempo de tránsito de los portadores a través de la región vacia, es mucho menor que el periodo de variación de las señales externas aplicadas al dispositivo

— La probabilidad de que un portador atraviese la región vacia es independiente de lo que ocurra con otros portadores.

Este tipo de ruido se presenta en junturas PN polarizadas en inversa y depende del valor medio de la corriente que circula por el dispositivo, siempre y cuando la frecuencia de análisis sea menor que la decima parte del inverso del periodo del tiempo de tránsito del portador a través de la región vacia.

3. Ruido de parpadeo: Está asociado con un flujo de corriente directa a través del dispositivo y tiene una densidad espectral de la forma

$$K\ \frac{I^a}{f^b}$$

4. Ruido de ráfaga: Se debe principalmente a la existencia de niveles de trampa en la región prohibida, depende de $1 + f^2$.

5. Ruido de avalancha: Causado por los mecanismos de ruptura de una juntura PN en inversa; este ruido está asociado con las siguientes caracteristicas:

— Flujo de C.D.
— Amplitud mucho mayor que el ruido discreto
— Distribución de amplitudes no gaussianas.

De los 5 tipos de ruido mencionados solo los dos primeros son predecibles teóricamente con cierta exactitud; los otros deberán medirse experimentalmente en el laboratorio.

Como auxiliar de diseño, los fabricantes de amplificadores operacionales generalmente proporcionan graficas de nivel de ruido di o di^2 contra frecuencia. Tomando en cuenta que el amplificador operacional es un filtro paso bajas, se puede estimar una frecuencia central, determinar el valor de di^2 obteniendo asi fuentes equivalentes que puedan considerarse como existentes a la entrada del modelo del amplificador operacional, y asi calcular la magnitud de este componente indeseable a la salida.

4. MODELOS DE AMPLIFICADORES OPERACIONALES

Los simuladores digitales de circuitos electrónicos han tenido gran aceptación entre los ingenieros diseñadores de circuitos. Su uso se ha extendido grandemente hasta el diseño de subsistemas de circuitos integrados y al diseño en gran escala. Desafortunadamente, el propósito fundamental de estos simuladores no era el de cubrir estas áreas, ya que un simulador digital realiza, en forma iterativa, el analisis de un circuito (ref 12), y como cada iteracion requiere de un analisis completo de circuito, el tiempo de computación (por el cual se paga, y en algunos casos resulta caro) requerido para el analisis de un subsistema con circuitos integrados, seria prohibitivo y poco eficiente.

4.1 MODELOS ELEMENTALES

Considérese el modelo mostrado en la fig 4.1, el cual representa en su forma mas elemental un amplificador operacional de voltaje, por ejemplo el μA 741.

R_r = Escogida arbitrariamente = $1K$
R_{in} = Resistencia de entrada
R_o = Resistencia de salida
A_v = Ganancia en malla abierta para C.D.
f_t = Ancho de banda con ganancia unitaria

$$C_r = \frac{A_v}{2\Pi R_r f_t}$$

Como es evidente, en un modelo tan elemental los parametros internos del amplificador operacional no intervienen directamente. En este caso, el problema consiste en tratar al amplificador operacional como una red de dos puertos para poder obtener la mayor información posible, por ejemplo: R_{in}, R_o, A_v, f_t.

Con el modelo mostrado en la fig 4.1 y la información obtenida se alimenta a un programa de computadora, simulador de circuitos electrónicos, el cual nos dará como respuesta un diagrama de polos y ceros, un diagrama de Bode en magnitud y fase y el ancho de banda con ganancia unitaria; no es posible obtener más información, ya que los parámetros internos del amplificador no van incluidos en el modelo.

Evidentemente la falla estriba en el modelo y no en el simulador, mas si lo que se pretende es ver el amplificador operacional como un elemento de circuito, seria necesario caracterizarlo de manera más completa.

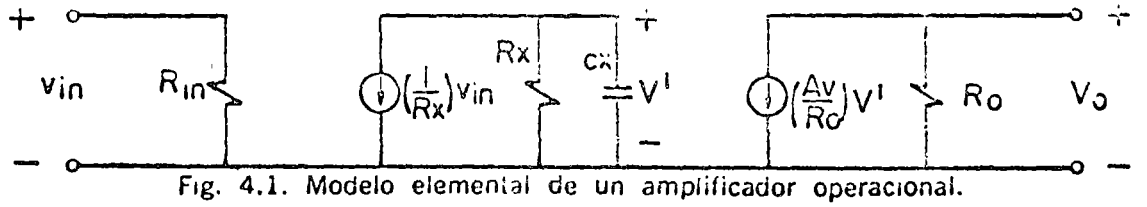


Fig. 4.1. Modelo elemental de un amplificador operacional.

4 2 MACROMODELOS

El objetivo del macromodelo es obtener un modelo lo mas real posible de un circuito integrado o una fraccion de el, a fin de reducir significativamente la complejidad del circuito, para poder simularlo en menor tiempo, y a menor costo para utilizarlo en circuitos integrados a gran escala o en subsistemas con circuitos integrados.

Un macromodelo del amplificador operacional ICL 8741 se muestra en la fig 4 2 (ref 11). Dicho macromodelo en comparacion con el circuito real del ICL 8741 representa una reducción considerable de nodos y ramas y además una aproximación bastante buena de los parametros de mayor interés, por ejemplo caracteristicas de entrada y salida, ganancias en modo comun y en modo diferencial, respuesta en frecuencia, offset de voltaje y corriente, polarización, Slew rate, excursión de voltaje a la salida y limitación de corriente a la salida por cortocircuito. Además, el macromodelo tiene la ventaja de que reduce aproximadamente 80 uniones PN a únicamente 8 uniones PN para una más rápida convergencia en el proceso iterativo.

El circuito de la fig 4.2 que representa el macromodelo cumple con la estructura basica de un amplificador operacional, esto es, etapa de entrada, etapa intermedia de ganancia y etapa de salida.

La etapa de entrada consiste en dos transistores ideales Q_1 y Q_2 asociados con fuentes de corriente y elementos pasivos. Reproduce las linealidades y no linealidades necesarias para representar las caracteristicas en modo común y en modo diferencial del amplificador operacional. El capacitor C_c se usa para introducir efectos de segundo orden en el Slew rate y el capacitor C_1 en el cambio de fase, al aumentar la frecuencia.

La ganancia de voltaje en modo común y en modo diferencial del amplificador operacional viene dada por los elementos de la etápa intermedia de ganancia, G_{cm}, G_a, R_2, G_b, y R_{o2}.

La etapa de salida provee de la resistencia apropiada tanto de *A.C.* como de *D.C.*, D_1, D_2, R_o, G_c, simulan el efecto de máxima corriente de salida en cortocircuito. Los elementos D_3, V_c, D_4, V_e, son circuitos recortadores para limitar la máxima excursión de voltaje a la salida.

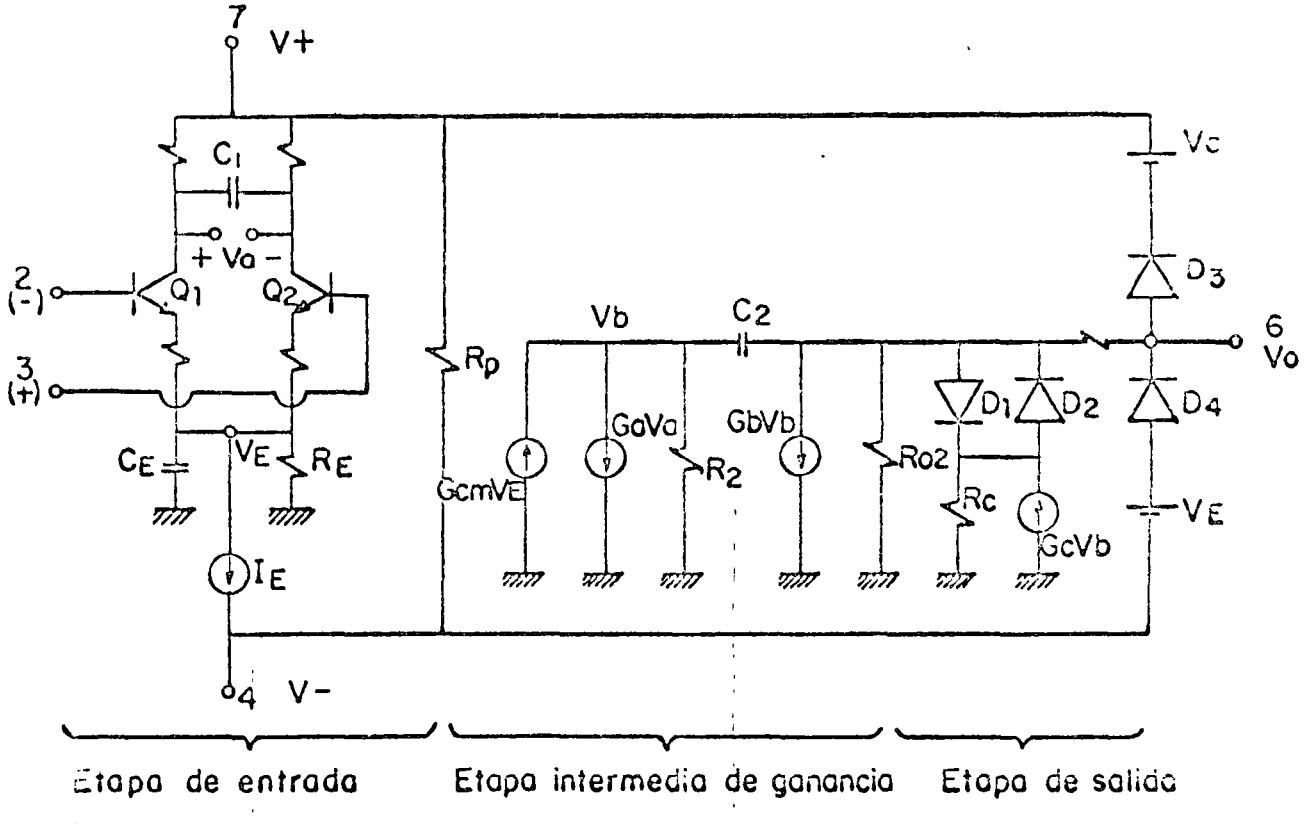


Fig 4.2 Macromodelo del amplificador operacional ICL 8741.

AN APPLICATIONS GUIDE FOR OPERATIONAL AMPLIFIERS

INTRODUCTION

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost—in quantity—would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has provided circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase locking.

The availability of the low cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity gain buffer to relatively complex generator and wave shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical: amplifier parameters will be discussed as they affect circuit performance and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, waveshapers and generators, and power supplies. The [illegible] amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown, however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

THE INVERTING AMPLIFIER

The basic operational amplifier circuit is shown in Figure 1. This circuit gives closed loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed loop bandwidth is equal to the unity gain frequency divided by one plus the closed loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

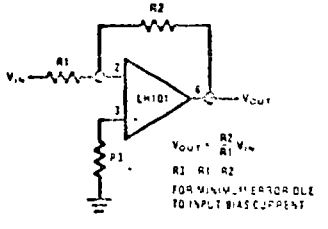


FIGURE 1 Inverting Amplifier

Offset voltage at the input of an operational amplifier is composed of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, but [illegible] bution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB. While it requires 30 pF in the non inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non inverting unity gain connection. The compensation trade off for a particular connection is stability versus bandwidth: larger values of [illegible] capacitor yield greater stability and lower bandwidth and vice versa.

The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

THE NON INVERTING AMPLIFIER

Figure 2 shows a high input impedance non inverting circuit. This circuit gives a closed loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed loop 3 dB bandwidth equal to the amplifier unity gain frequency divided by the closed loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain (Open loop gain/Closed loop gain). In DC coupled applications input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

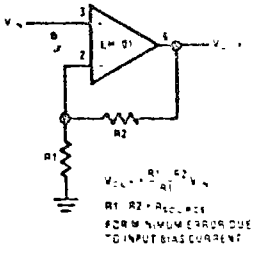


FIGURE 2 Non Inverting Amplifier

THE UNITY GAIN BUFFER

The unity gain buffer is shown in Figure 3. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open loop gain or to the common mode rejection, whichever is less.

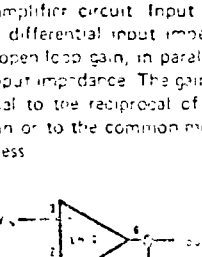
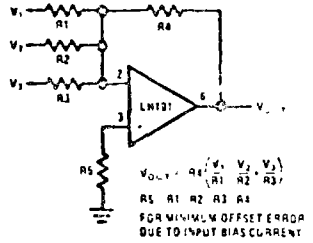


FIGURE 3 Unity Gain Buffer

t impedance is a misl[illegible]ng concept in a DC
lled unity gain buffer. Bias current for the
lifier will be supplied by the source resistance
will cause an error at the amplifier input due
is voltage drop across the source resistance
e this is the case a low bias current amplifier
as the LH102[6] should be chosen as a unity
buffer when working from high source resis
es. Bias current compensation techniques are
ussed in Reference 5

cautions to be observed in applying this c
are three: the amplifier must be compensated
unity gain operation, the output swing of the
lifier may be limited by the amplifier common
le range, and some amplifiers exhibit a latch up
le when the amplifier common mode range is
eeded. The LH101 may be used in this circuit
none of these problems or, for faster opera-
, the LM102 may be chosen.



URE 4 Summing Amplifier

MMING AMPLIFIER

summing amplifier, a special case of the in
ing amplifier, is shown in Figure 4. The circuit
s an inverted output which is equal to the
ghted algebraic sum of all three inputs. The
of any input of this circuit is equal to the
o of the appropriate input resistor to the feed
k resistor, R4. Amplifier bandwidth may be
culated as in the inverting amplifier shown in
ure 1 by assuming the input resistor to be the
allel combination of R1, R2, and R3. Applica
cautions are the same as for the inverting
olifier. If an uncompensated amplifier is used
mpensation is calculated on the basis of this
dwidth as is discussed in the section describing
simple inverting amplifier.

advantage of this circuit is that there is no
raction between inputs and operations such as
ding and weighted averaging are simply
easily.

E DIFFERENCE AMPLIFIER

difference amplifier is the complement of the
ming amplifier and allows the subtraction of
voltages or, as a special case, the cancellation
unwanted common to both inputs. It is shown

is shown in Figure 5 and is useful as a computational amplifier, in making a different al to single-ended conversion or in rejecting a common mode signal.

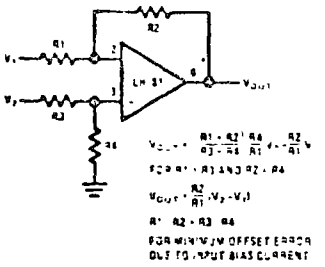


FIGURE 5 Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal. Inverting input impedance is the same as for the inverting amplifier of Figure 1 and the non inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

DIFFERENTIATOR

The differentiator is shown in Figure 6 and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R2C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.

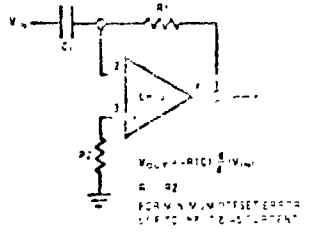


FIGURE 6 Differentiator

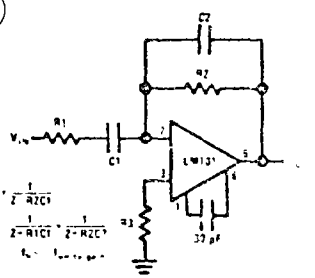


FIGURE 7 Practical Differentiator

A practical differentiator is shown in Figure 7. Here both the stability and noise problems are corrected by addition of two additional components R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll off in the feedback network and R1C1 form a 6 dB per octave roll off network in the input network for a total high frequency roll off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in Figure 8 for clarity.

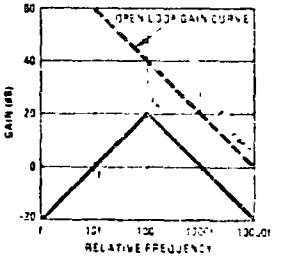


FIGURE 8 Differentiator Frequency Response

INTEGRATOR

The integrator is shown in Figure 9 and performs the mathematical operation of integration. This

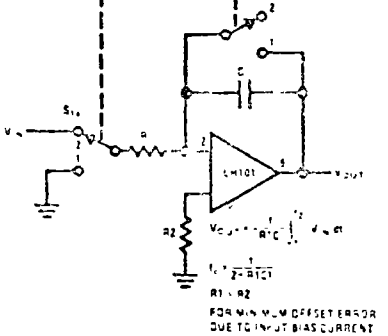


FIGURE 9 Integrator

circuit is essentially a low pass filter with a frequency response decreasing at 6 dB per octave. An amplitude frequency plot is shown in Figure 10.

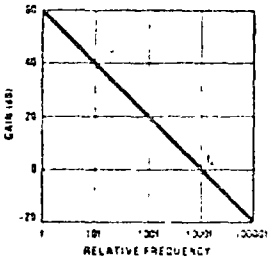


FIGURE 10 Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1 the amplifier is connected in unity gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity gain operation and R2 must equal R1 for minimum error due to bias current.

SIMPLE LOW PASS FILTER

The simple low-pass filter is shown in Figure 11. This circuit has a 6 dB per octave roll off after a closed loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c however, the time domain response is that of a single RC rather than an integral.

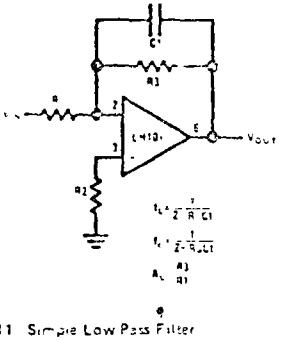


FIGURE 11 Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity gain or an internally compensated amplifier can be used.

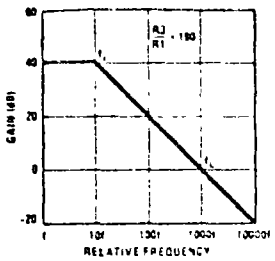


FIGURE 12 Low Pass Filter Response

A gain frequency plot of circuit response is shown in Figure 12 to illustrate the difference between this circuit and the true integrator.

THE CURRENT-TO-VOLTAGE CONVERTER

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current to voltage transducer is shown in Figure 13. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this

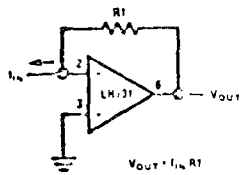


FIGURE 13 Current to Voltage Converter

circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity gain operation. Various techniques for bias current compensation are contained in Reference 5.

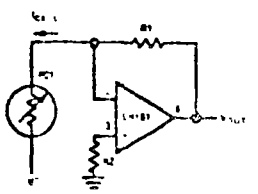


FIGURE 14 Amplifier for Photoconductive Cell

PHOTOCELL AMPLIFIERS

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in Figures 14, 15, and 16 respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current to voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage: zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

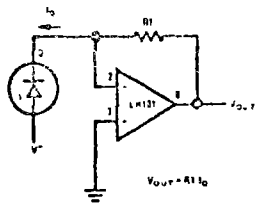


FIGURE 15 Photodiode Amplifier

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.

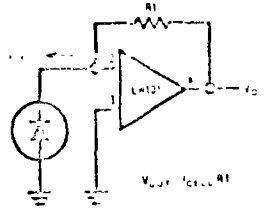


FIGURE 16 Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is effective in the case of photovoltaic cells or of photodiodes. It is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

PRECISION CURRENT SOURCE

The precision current source is shown in Figures 17 and 18. The configurations shown will sink or source conventional current respectively.

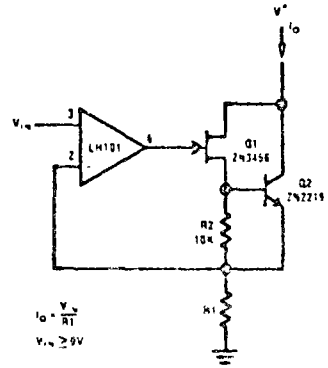


FIGURE 17 Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in Figures 17 and 18 use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET bipolar combination in cases

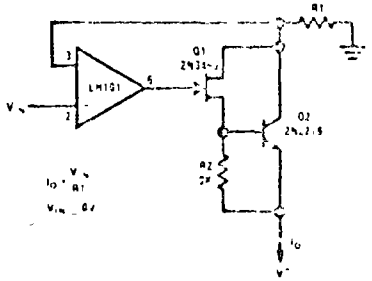


FIGURE 18 Precision Current Source

where the output current is high... rent of the Darlington input would ... significant error.

The amplifiers used must be compensated for unity gain and additional compensation may be required depending on load reactance and external transistor parameters.

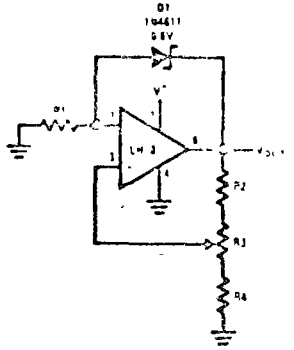


FIGURE 19a Positive Voltage Reference

ADJUSTABLE VOLTAGE REFERENCES

Adjustable voltage reference circuits are shown in Figures 19 and 20. The two circuits shown have different areas of applicability. The basic difference between the two is that Figure 19 illustrates a voltage source which provides a voltage greater than the reference diode while Figure 20 illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

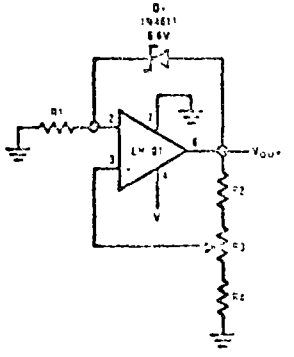


FIGURE 19b Negative Voltage Reference

High precision extended to ... applications of the circuit of Figure 19 require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener TC. Since I_Z is not a function of V^+, reference TC will be ... dependent of V^+.

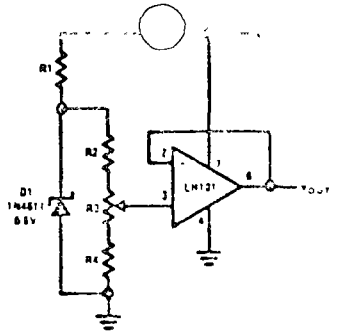


FIGURE 20a. Positive Voltage Reference

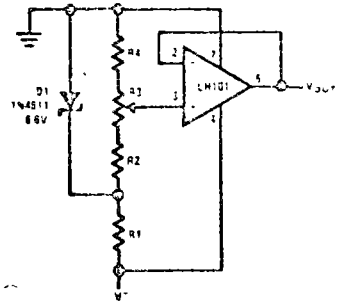


FIGURE 20b. Negative Voltage Reference

The circuit of Figure 20 is suited for high precision extended temperature service if V^- is reasonably constant since I_Z is dependent on V^-. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity gain operation or if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply. This requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with the single power supply since the common mode range includes V^- with the addition of 2 volts of V^-.

THE RESET STABILIZED AMPLIFIER

The reset stabilized amplifier is a form of chopper stabilized amplifier and is shown in Figure 21. As shown, the amplifier is connected [illegible]

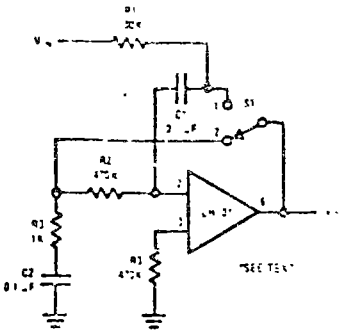


FIGURE 21. Reset Stabilized Amplifier

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current. The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance. S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from $(V_{OS} + I_{b\,\text{max}}R2)$ to $V_{IN} + I_{b\,\text{max}}R2$ as S_1 is changed from position 2 to position 1. Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves to reduce the offset at the amplifier output if the amplifier must drive maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to load current. Source resistance. The time spent in position 2 should be long with respect to the charging time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and the compensation does not [illegible]

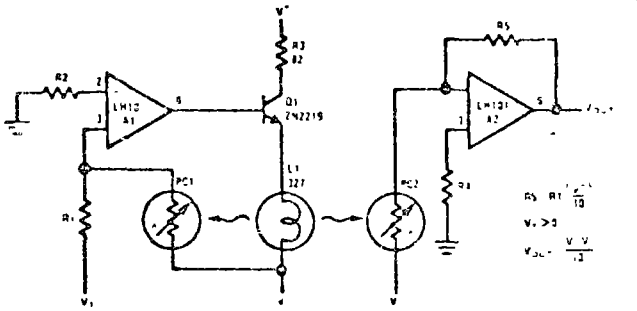


FIGURE 22. Analog Multiplier

THE ANALOG MULTIPLIER

A simple embodiment of the analog multiplier is shown in Figure 22. This circuit circumvents many of the problems associated with the log antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1. When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminates PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen [illegible] the product of R1 and V^-, the [illegible] simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in rush current when first turning on the lamp, L1.

THE FULL WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in Figure 23 is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full wave rectifier, and deletion of C1 provides an absolute value generator.

The [illegible] may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a [illegible] unity gain inverter, with input resistor, R1, and feedback resistor, R3, giving a positive going output.

For positive inputs, A1 operates as [illegible] fier connected to the A2 summing point through resistor R3. Amplifier A1 then [illegible] unity gain inverter with input [illegible]

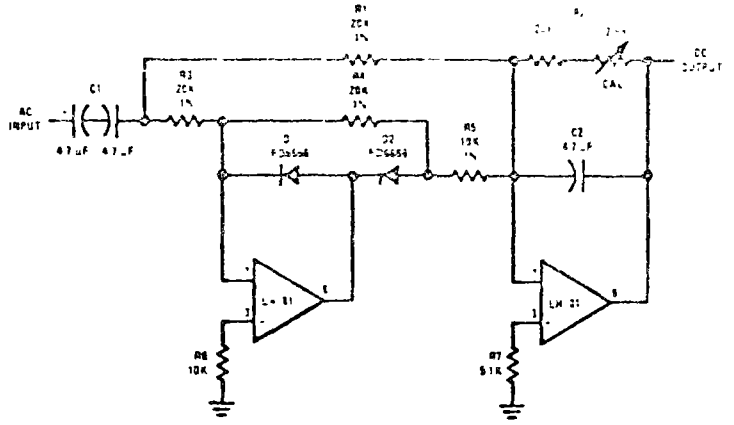


FIGURE 23 Full Wave Rectifier and Averaging Filter

feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

The amplifiers chosen must be compensated for unity gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

SINE WAVE OSCILLATOR

A stabilized sine wave oscillator is shown in Figure 24. This circuit provides high

of the circuit is that the [illegible] gain. Filament lamp amplitude regulator is [illegible] along with its [illegible] and [illegible] problems.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency. To stabilize the frequency of oscillation, and to reduce harmonic distortion

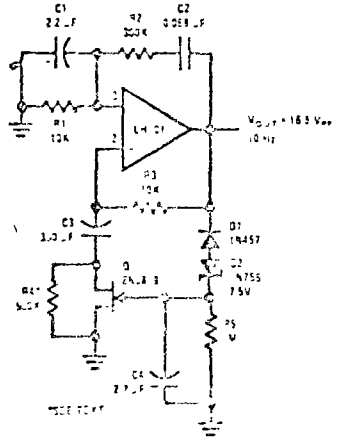


FIGURE 24 Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and/or D2 to conduct, charging C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general-purpose oscillator.

TRIANGLE-WAVE GENERATOR

A constant amplitude triangular-wave generator is shown in Figure 25. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

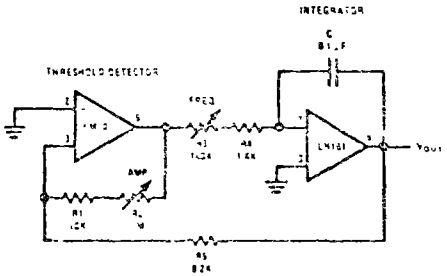


FIGURE 25 Triangular Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysteresis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When it does, the circuit saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R5 and R1, causing a current I^+ to flow. The integrator then generates a negative going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in Figure 26.

The integrator should be compensated for unity gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

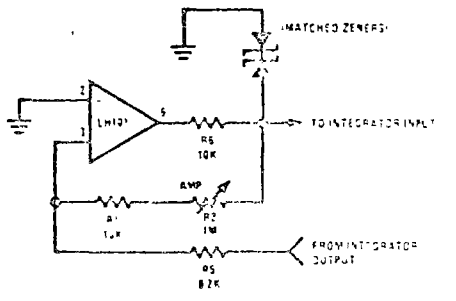


FIGURE 26 Threshold Detector with Regulated Output

TRACKING REGULATED POWER SUPPLY

A tracking regulated power supply is shown in Figure 27. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition only one voltage reference and a minimum number of passive components are required.

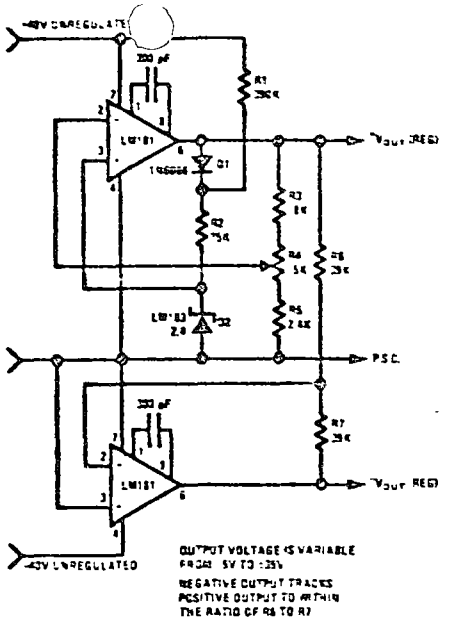


FIGURE 27. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start up current from the unregulated positive supply. After start up, the low amplifier output impedance reduces reference current variations due to the current through R1.

The negative regulator is simply a unity gain inverter with input resistor, R6, and feedback resistor, R7.

The amplifiers must be compensated for unity gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

PROGRAMMABLE BENCH POWER SUPPLY

The complete power supply shown in Figure 28 is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.

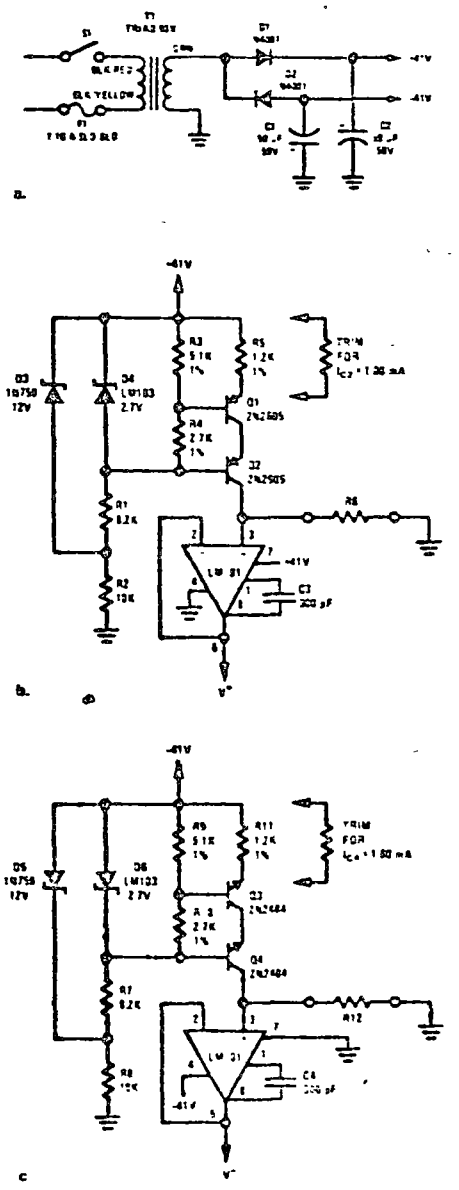


FIGURE 28. Low Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from -38V to 0V with respect to ground. Since LH101 amplifiers are used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

CONCLUSIONS

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

APPENDIX I
DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance. The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large amplitude step function applied to the input.

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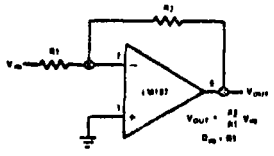
4. A Palimpsest on the Electronic Analog Art. H. M. Paynter, Editor. Published by George A. Philbrick Researches, Inc., Boston, Mass.
5. Drift Compensation Techniques for Integrated D.C. Amplifiers. R. J. Widlar, EDN, June 10, 1968.
6. A Fast Integrated Voltage Follower With Low Input Current. R. J. Widlar, Microelectronics, Vol. 1 No. 7, June 1968.

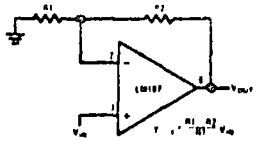
Robert C Dobkin
February 1970

op amp circuit collection

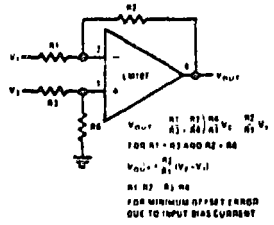
section 1 — basic circuits



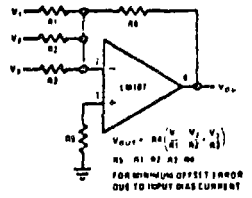
Inverting Amplifier



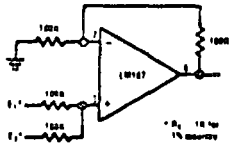
Non Inverting Amplifier



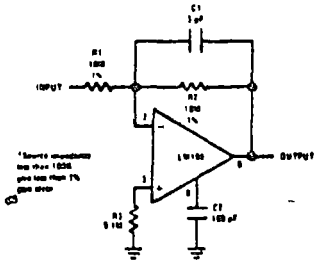
Difference Amplifier



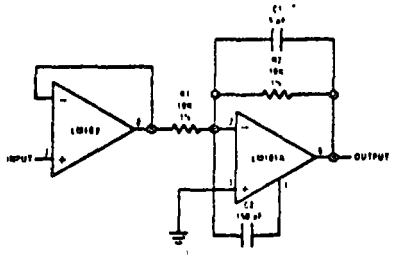
Inverting Summing Amplifier



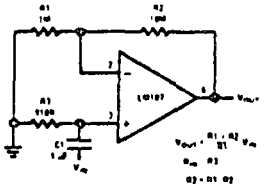
Non Inverting Summing Amplifier



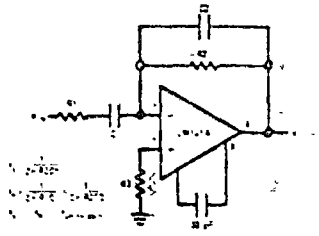
Inverting Amplifier with High Input Impedance



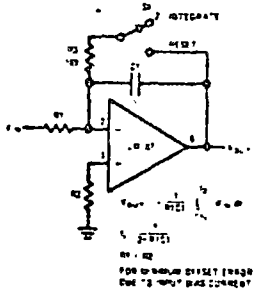
Fast Inverting Amplifier With High Input Impedance



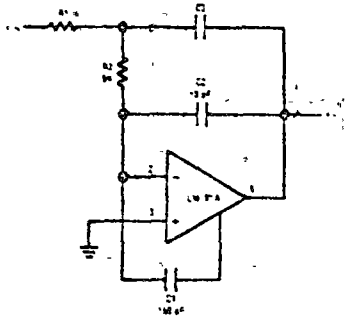
Non Inverting AC Amplifier



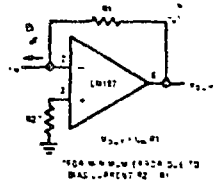
Practical Differentiator



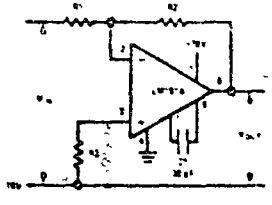
Integrator



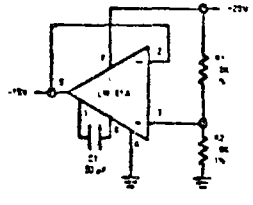
Fast Integrator



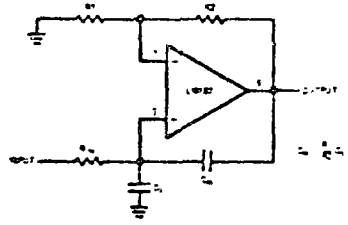
Current to Voltage Converter



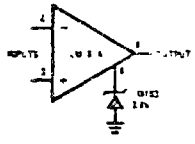
Circuit for Operating the LM107 without a Negative Supply



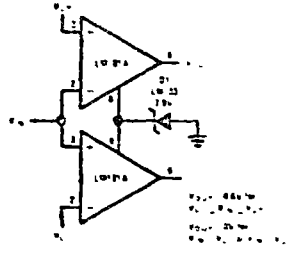
Circuit for Generating the Second Positive Voltage



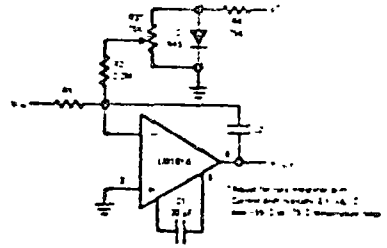
Neutralizing Input Capacitance to Optimize Response Time



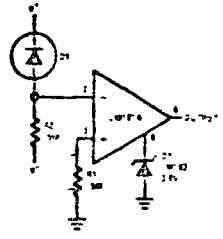
Voltage Comparator for Driving DTL or TTL Integrated Circuits



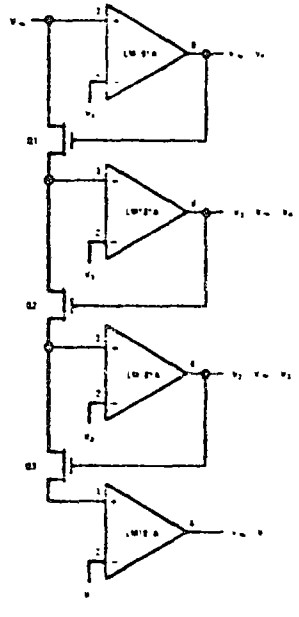
Double Ended Limit Detector



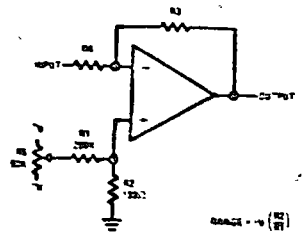
Integrator with Bias Current Compensation



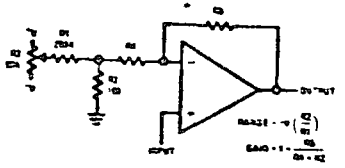
Threshold Detector for Photodiodes



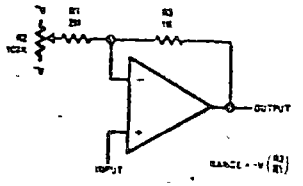
Multiple Aperture Window Discriminator



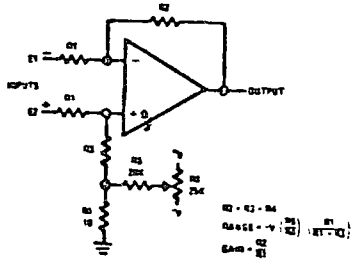
Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element



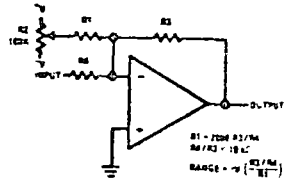
Offset Voltage Adjustment for Non-Inverting Amplifiers



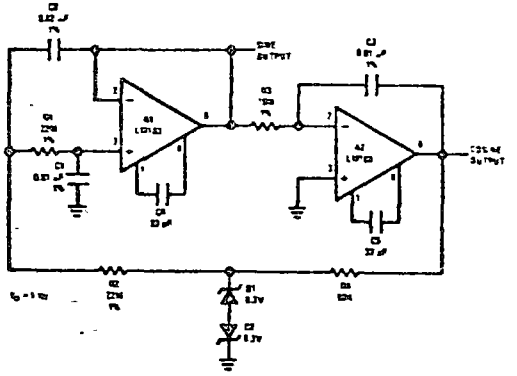
Offset Voltage Adjustment for Voltage Followers



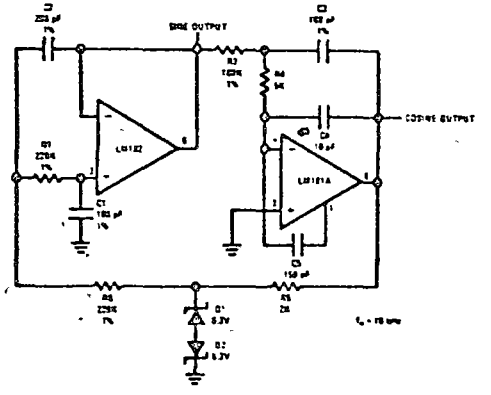
Offset Voltage Adjustment for Differential Amplifiers



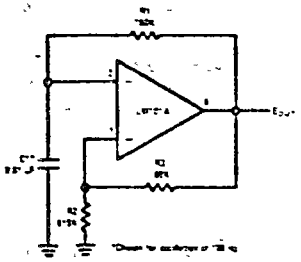
Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less



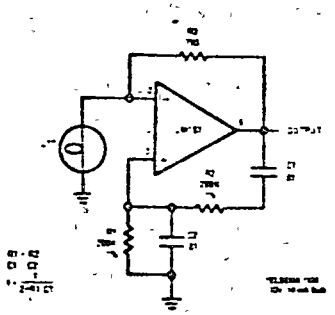
Low Frequency Sine Wave Generator with Quadrature Output



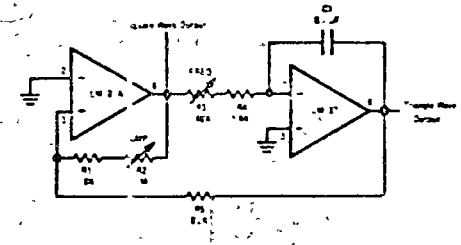
High Frequency Sine Wave Generator with Quadrature Output



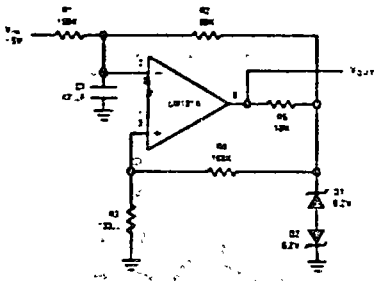
Free-Running Multivibrator



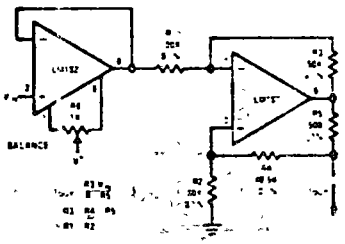
Wein Bridge Sine Wave Oscillator



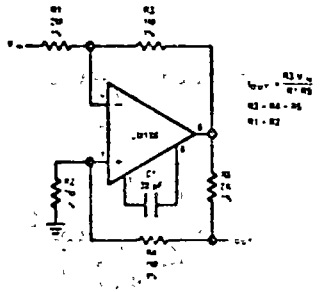
Function Generator



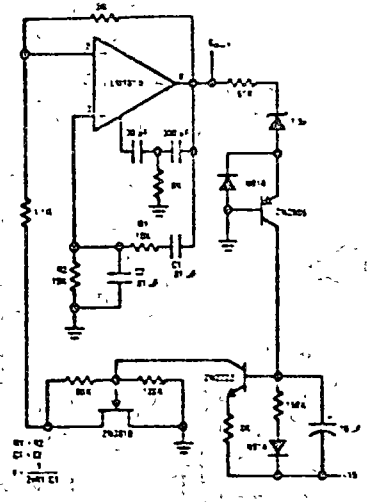
Pulse Width Modulator



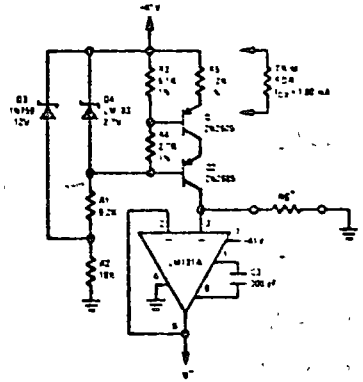
Bilateral Current Source

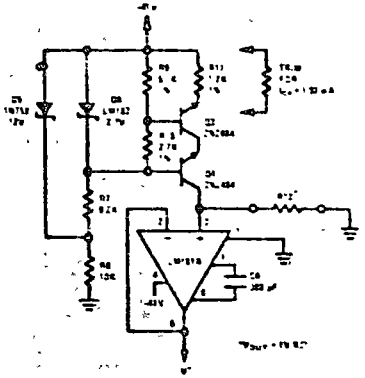


Bilateral Current Source

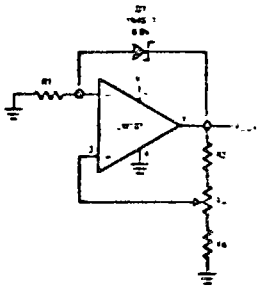


Wein Bridge Oscillator with FET Amplitude Stabilization

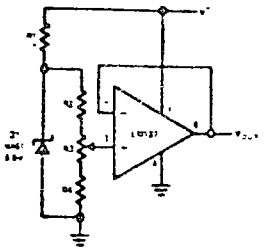




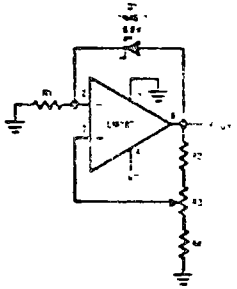
Low Power Supply for Integrated Circuit Testing



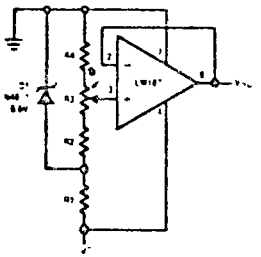
Positive Voltage Reference



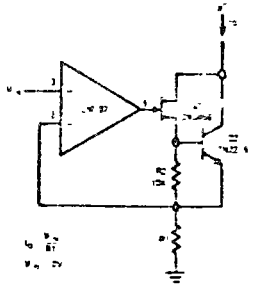
Positive Voltage Reference



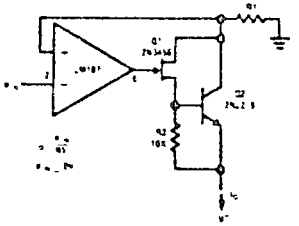
Negative Voltage Reference



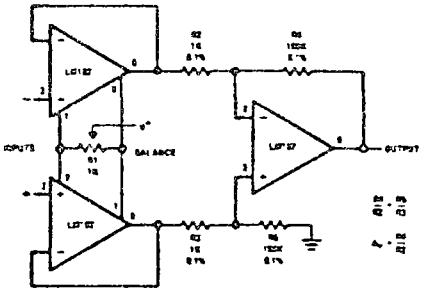
Negative Voltage Reference



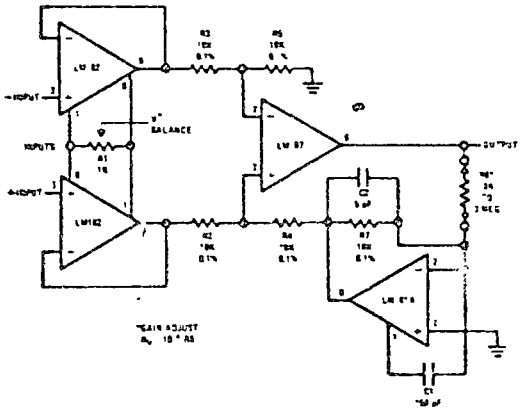
Precision Current Sink



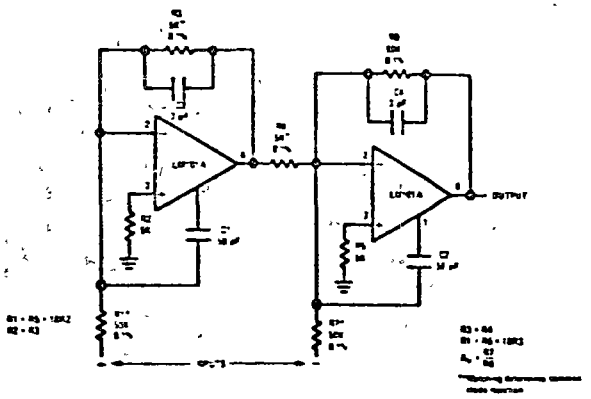
Precision Current Source



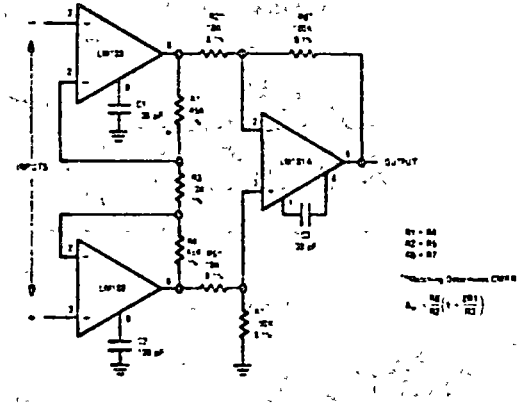
Differential Input Instrumentation Amplifier



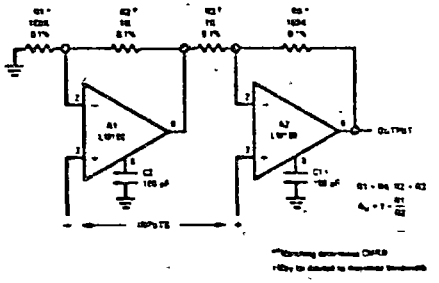
Variable Gain, Differential Input Instrumentation Amplifier



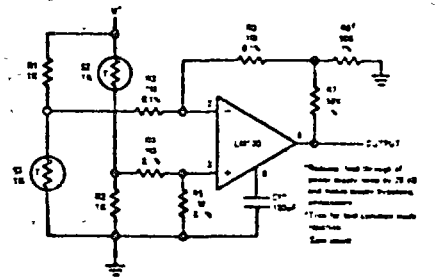
Instrumentation Amplifier with ±100 Volt Common Mode Range



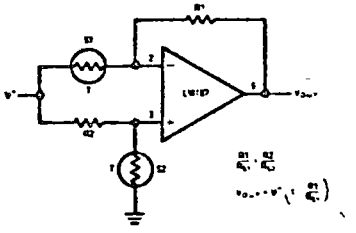
Differential Input Instrumentation Amplifier with High Common Mode Rejection



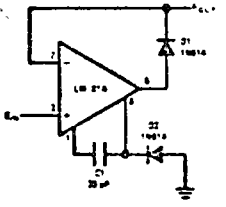
High Input Impedance Instrumentation Amplifier



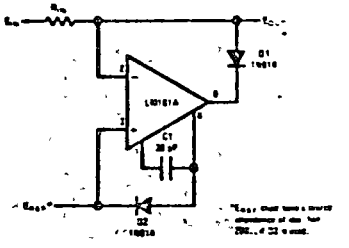
Bridge Amplifier with Low Noise Compensation



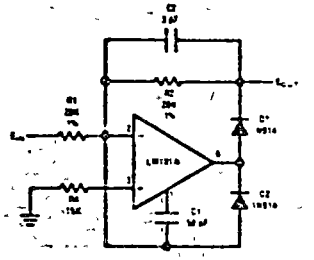
Bridge Amplifier



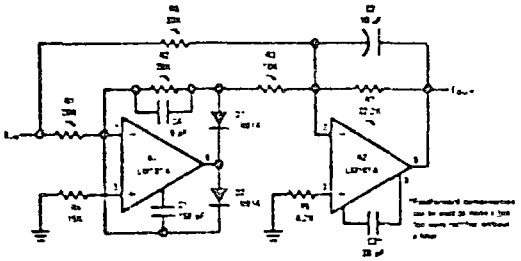
Precision Diode



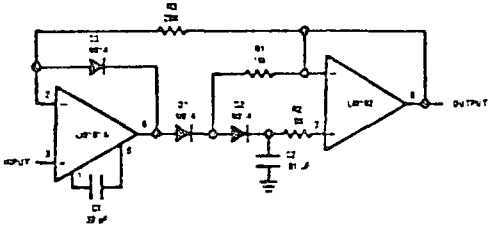
Precision Clamp



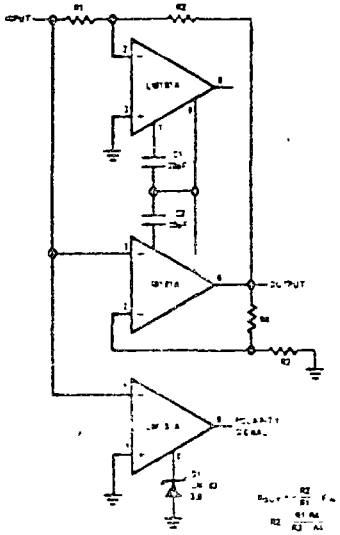
Fast Half Wave Rectifier



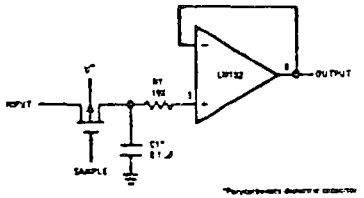
Precision AC to DC Converter



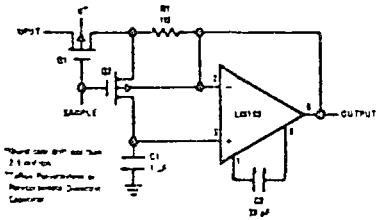
Low Drift Peak Detector



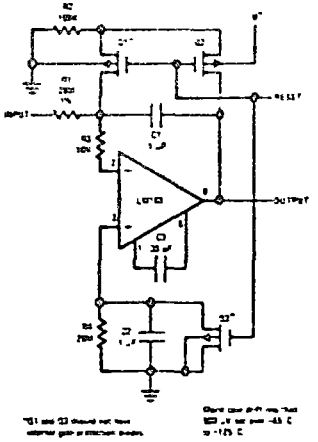
Absolute Value Amplifier with Polarity Detector



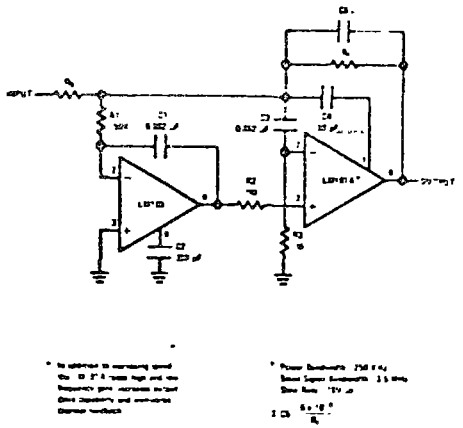
Sample and Hold



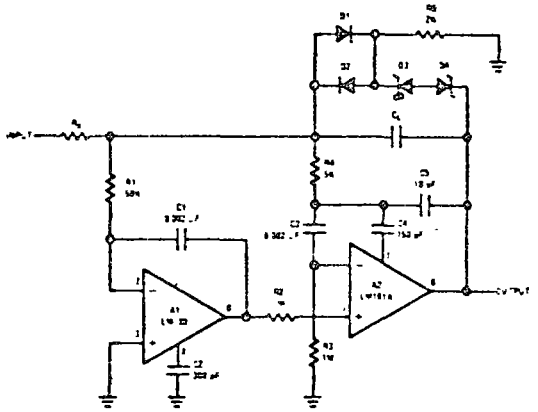
Sample and Hold



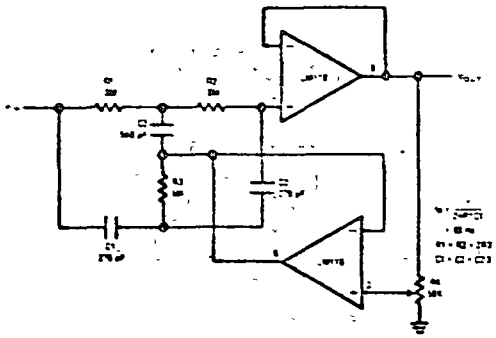
Low Drift Integrator



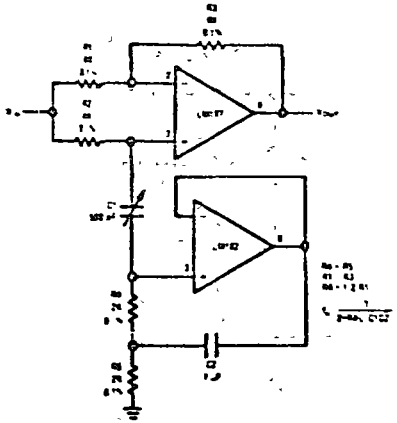
Fast† Summing Amplifier with Low Input Current



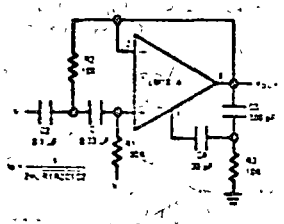
Fast Integrator with Low Input Current



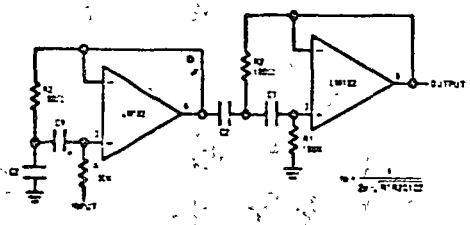
Adjustable Q Notch Filter



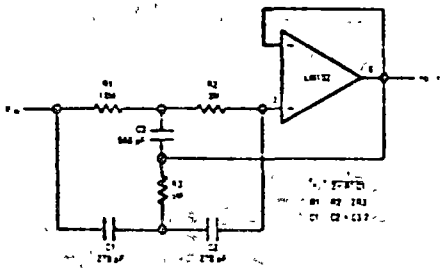
Easily Tuned Notch Filter



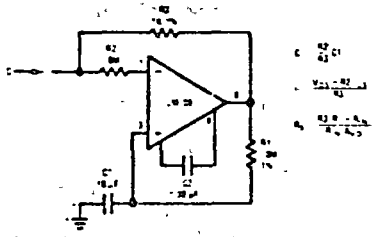
Tuned Circuit



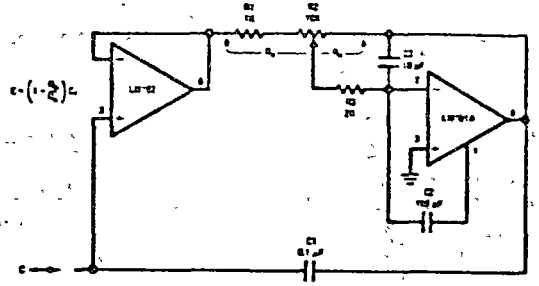
Two-Stage Tuned Circuit



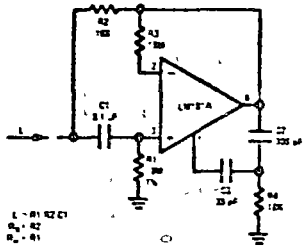
High Q Notch Filter



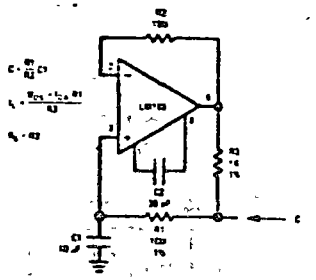
Negative Capacitance Multiplier



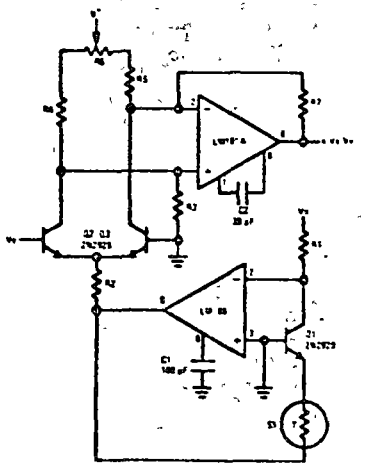
Variable Capacitance Multiplier



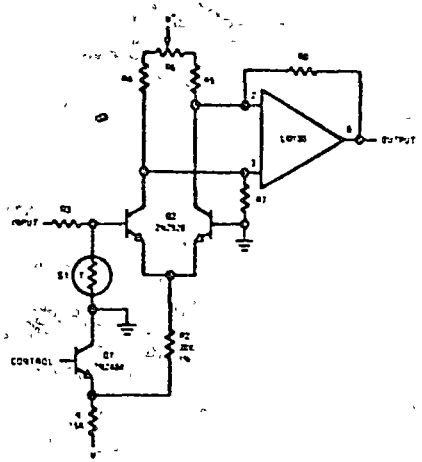
Simulated Inductor



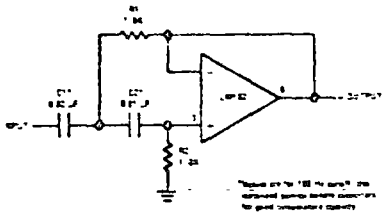
Capacitance Multiplier



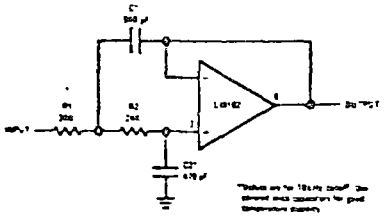
Two Quadrant Multiplier



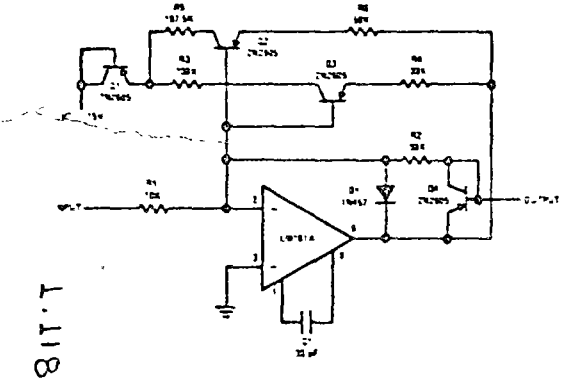
Voltage Controlled Gain Circuit



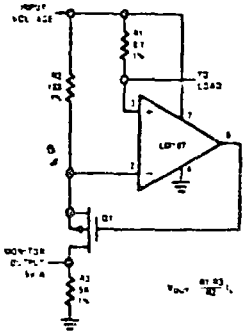
High Pass Active Filter



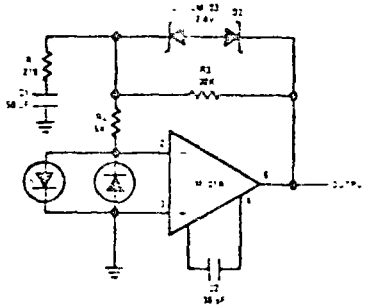
Low Pass Active Filter



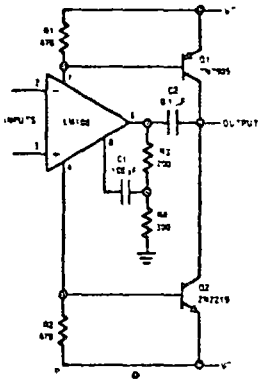
Nonlinear Operational Amplifier with
Temperature Compensated Breakpoints



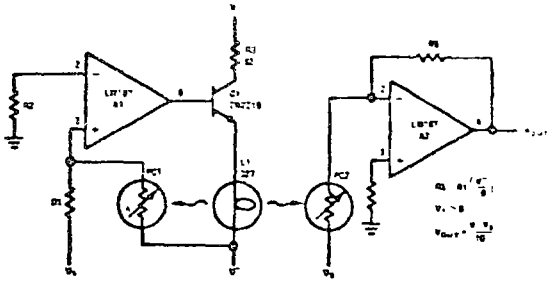
Current Monitor



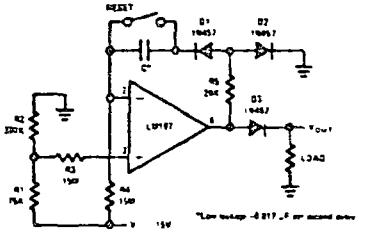
Saturating Servo Preamplifier with
Rate Feedback



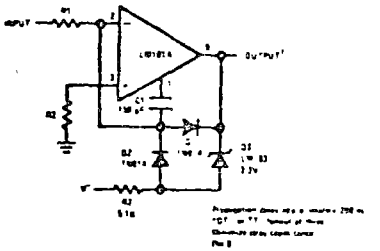
Power Booster



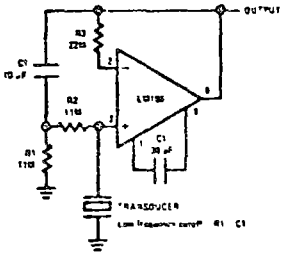
Analog Multiplier



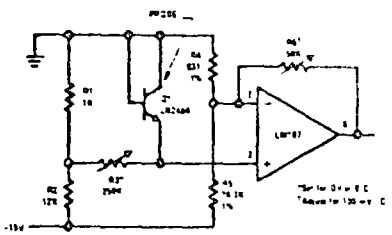
Long Interval Timer



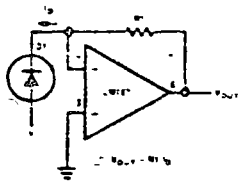
Fast Zero Crossing Detector



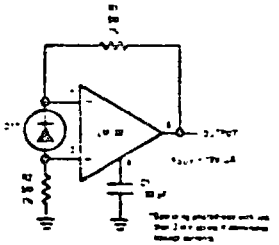
Amplifier for Piezoelectric Transducer



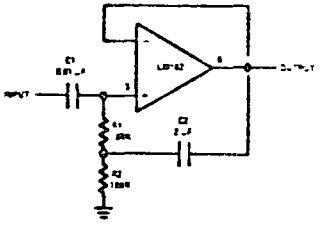
Temperature Probe



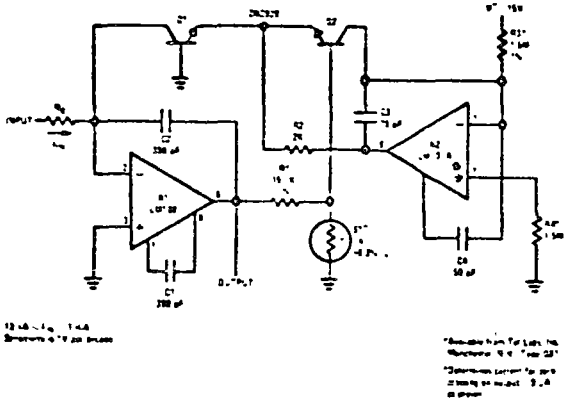
Photodiode Amplifier



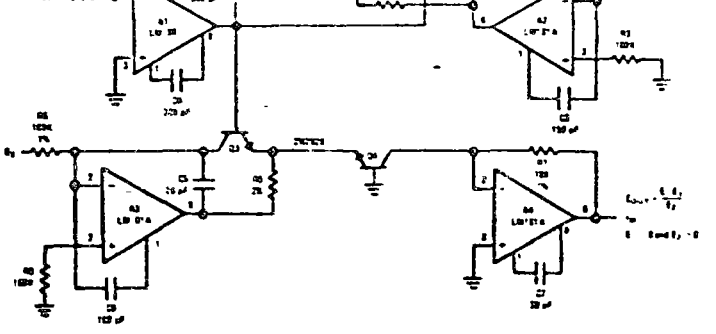
Photodiode Amplifier



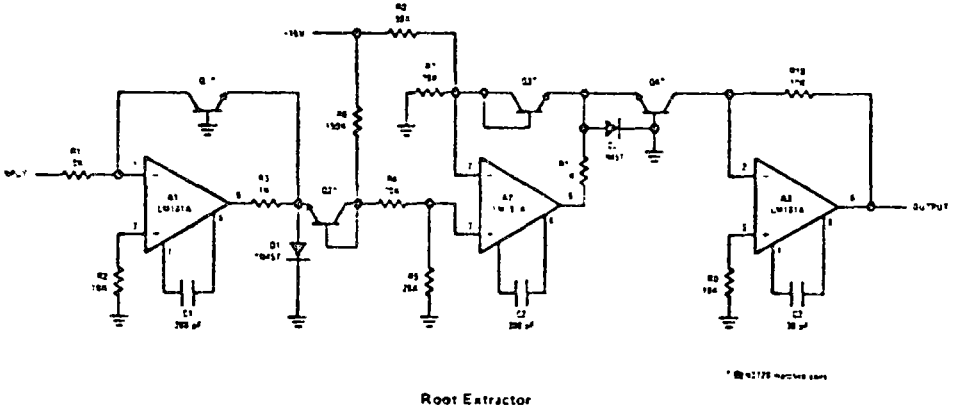
High Input Impedance AC Follower



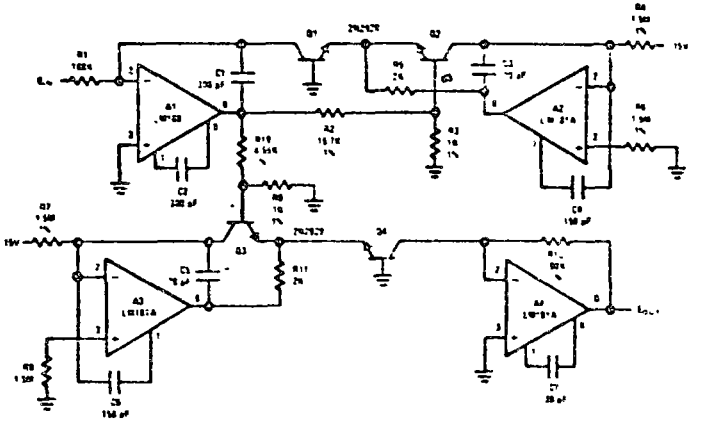
Temperature Compensated Logrithmic Converter



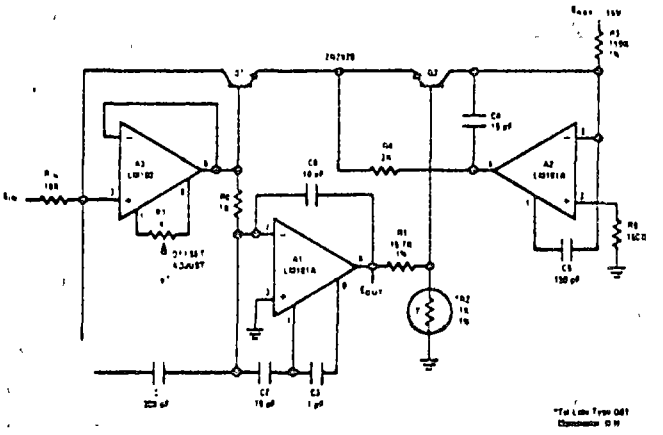
Multiplier/Divider



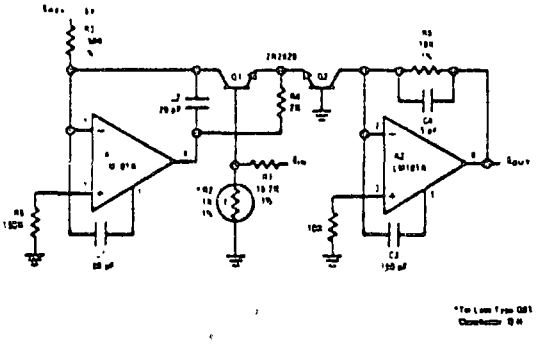
Root Extractor



Cube Generator



Fast Log Generator



Anti-log Generator

THE LM3900—A NEW CURRENT-DIFFERENCING QUAD OF ± INPUT AMPLIFIERS

1.0 AN INTRODUCTION TO THE NEW "NORTON" AMPLIFIER

The LM3900 represents a departure from conventional amplifier designs. Instead of using a standard transistor differential amplifier at the input, the non-inverting input function has been achieved by making use of a "current-mirror" to "mirror" the non-inverting input current about ground and then to extract this current from that which is entering the inverting input terminal. Whereas the conventional op amp differences input voltages, this amplifier differences input currents and therefore the name 'Norton Amp' has been used to indicate this new type of operation. Many biasing advantages are realized when operating with only a single power supply voltage. The fact that currents can be passed between the input terminals allows some unusual applications. If external, large valued input resistors are used (to convert from input voltages to input currents) most of the standard op amp applications can be realized.

Many industrial electronic control systems are designed that operate off of only a single power supply voltage. The conventional integrated-circuit operational amplifier (IC op amp) is typically designed for split power supplies ($\pm$ 15 V_{DC}) and suffers from a poor output voltage swing and a rather large minimum common-mode input voltage range (approximately + 2 V_{DC}) when used in a single power supply application. In addition, some of the performance characteristics of these op amps could be sacrificed—especially in favor of reduced costs.

To meet the needs of the designers of low-cost, single-power-supply control systems, a new internally compensated amplifier has been designed that operates over a power supply voltage range of +4 V_{DC} to 36 V_{DC} with small changes in performance characteristics and provides an output peak-to-peak voltage swing that is only 1V less than the magnitude of the power supply voltage. Four of these amplifiers have been fabricated on a single chip and are provided in the standard 14-pin dual-in-line package.

The cost, application and performance advantages of this new quad amplifier will guarantee it a place in many single power supply electronic systems. Many of the "housekeeping" applications which are now handled by standard IC op amps can also be handled by this "Norton" amplifier operating off the existing $\pm$ 15 V_{DC} power supplies.

1.1 Basic Gain Stage

The gain stage is basically a single common-emitter amplifier. By making use of current source loads a large voltage gain has been achieved which is very constant over temperature changes. The output voltage has a large dynamic range, from essentially ground to one V_{BE} less than the power supply voltage. The output stage is biased class A for small signals but converts to class B to increase the load current which can be "absorbed" by the amplifier under large signal conditions. Power supply current drain is essentially independent of the power supply voltage and ripple on the supply line is also rejected. A very small input biasing current allows high impedance feedback elements to be used and even lower "effective" input biasing currents can be realized by using one of the amplifiers to supply essentially all of the bias currents for the other amplifiers by making use of the 'matching' which exists between the 4 amplifiers which are on the same IC chip (see Figure 84).

The simplest inverting amplifier is the common-emitter stage. If a current source is used in place of a load resistor, a large open-loop gain can be obtained even at low power-supply voltages. This basic stage (Figure 1) is used for the amplifier.

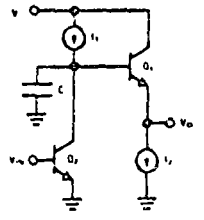


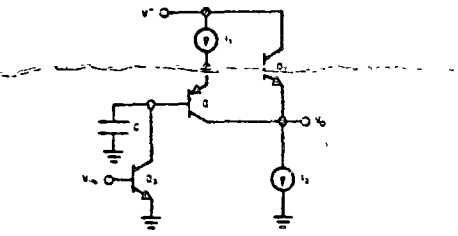
FIGURE 1. Basic Gain Stage

All of the voltage gain is provided by the gain transistor, Q_2, and an output emitter-follower transistor, Q_1, serves to isolate the load impedance from the high impedance that exists at the collector of the gain transistor, Q_2. Closed-loop stability is guaranteed by an on-chip capacitor C-3 pF, which provides the single dominant open-loop pole. The output emitter-follower is biased for class-A operation by the current source I_2.

This basic stage can provide an adequate open-loop voltage gain (70 dB) and has the desired

rge output voltage swing capability A disvantage of this circuit is that the DC input urrent, I_{IN}, is large as it is essentially equal the maximum output current, I_{OUT}, divided β^2 For example for an output current apability of 10 mA the input current would be least 1 μA (assuming $\beta^2 = 10^4$) It would be esirable to further reduce this by adding an dditional transistor to achieve an overall β^3 eduction Unfortunately if a transistor is dded at the output (by making Q_1 a Darlingn pair) the peak-to-peak output voltage swing ould be somewhat reduced and if Q_2 were ade a Darlington pair the DC input voltage vel would be undesirably doubled

o overcome these problems, a lateral PNP ansistor has been added as shown in Figre 2 This connection neither reduces the utput voltage swing nor raises the DC input oltage but does provide the additional gain at was needed to reduce the input current



IGURE 2 Adding a PNP Transistor to the Basic Gain Stage

otice that the collector of this PNP transistor, Q_1 is connected directly to the output terminal his "bootstraps" the output impedance of Q_1 nd therefore reduces the loading at the highmpedance collector of the gain transistor, Q_3

addition, the collector-base junction of the NP transistor becomes forward biased under a rge-signal negative output voltage swing conion The design of this device has allowed to convert to a vertical PNP transistor durg this operating mode which causes the outut to change from the class A bias to a class output stage This allows the amplifier to nk more current than that provided by the urrent source I_2 (1 3 mA) under large signal onditions

2 Obtaining a Non inverting Input Function

he circuit of Figure 2 has only the invertg input A general purpose amplifier requires o input terminals to obtain both an inverting nd a non-inverting input In conventional p amp designs an external differential amplifier rovides these required inputs The output voltage then depends upon the difference (or error) between the two input voltages An input common-mode voltage range specification exists and, basically, input voltages are compared

For circuit simplicity and ease of application in single power supply systems a non-inverting input can be provided by adding a standard IC "current-mirror" circuit directly across the inverting input terminal, as shown in Figure 3

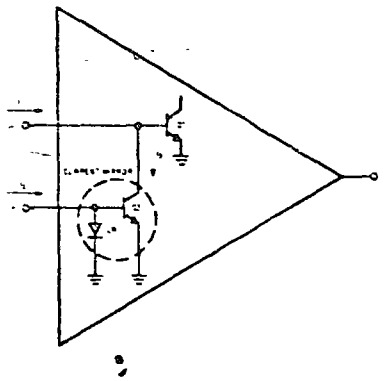


FIGURE 3. Adding a Current Mirror to Achieve a P oninverting Input

This operates in the current mode as now input currents are compared or differenced (this can be thought of as a Norton differential amplifier) There is essentially no input common-mode voltage range directly at the input terminals (as both inputs will bias at one diode drop above ground) but if the input voltages are converted to currents (by use of input resistors), there is then no limit to the common-mode input voltage range This is especially useful in high-voltage comparator applications By making use of the input resistors to convert input voltages to input currents, all of the standard op amp applications can be realized Many additional applications are easily achieved especially when operating with only a single power supply voltage This results from the built-in voltage biasing that exists at both inputs (each input biases at ~ V_{BE}) and additional resistors are not required to provide a suitable common-mode input DC biasing voltage level Further, input summing can be performed at the relatively low impedance level of the input diode of the current-mirror circuit

1 3 The Complete Single supply Amplifier

The circuit schematic for a single amplifier stage is shown in Figure 4a) Due to the circuit simplicity four complete amplifiers can be fabricated on a single chip One common biasing circuit is used for all of the individual amplifiers

A new symbol for this "Norton" amplifier is shown in Figure 4b) This is recommended to avoid using the standard op amp symbol as the basic operation is different The current source symbol between the inputs implies this new current-mode of operation In addition it

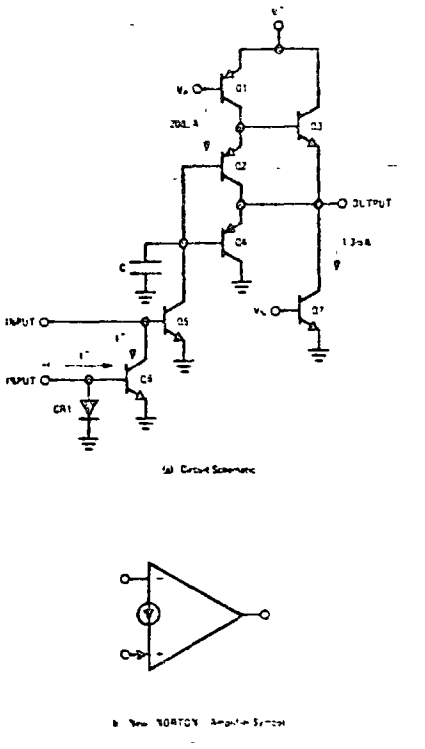


FIGURE 4. The Amplifier Stage

signifies that current is removed from the (-) input terminal Also the current arrow on the (+) input lead is used to indicate that this functions as a current input The use of this symbol is helpful in understanding the operation of the application circuits and also in doing additional design work with the LM3900

The bias reference for the PNP current source V_p which biases Q_1, is designed to cause the upper current source (200 μA) to change with temperature to give first order compensation for the β variations of the NPN output transistor Q_3 The bias reference for the NPN "pull-down" current sink V_n (which biases Q_7) is designed to stabilize this current (1 3 mA) to reduce the variation when the temperature is changed This provides a more constant pull-down capability for the amplifier over the temperature range The transistor Q_4 provides the class B action which exists under large signal operating conditions

The performance characteristics of each amplifier stage are summarized below

Power-supply voltage range	4 to 36 V_{DC} or ±2 to ±18 V_{DC}
Bias current drain per amplifier stage	1 3 mA_{DC}
Open loop	
Voltage gain (R_L = 10k)	70 dB
Unity-gain frequency	2 5 MHz
Phase margin	50 degrees
Input resistance	1 MΩ
Output resistance	8 kΩ
Output voltage swing	(V_{cc} - 1) V_{DC}
Input bias current	30 nA_{DC}
Slew rate	0 5V/μs

As the bias currents are all derived from diode forward voltage drops there is only a small change in bias current magnitude as the power-supply voltage is varied The open-loop gain changes only slightly over the complete power supply voltage range and is essentially independent of temperature changes The open-loop frequency response is compared with the "741" op amp in Figure 5 The higher unity-gain crossover frequency is seen to provide an additional 10 dB of gain for all frequencies greater than 1 kHz

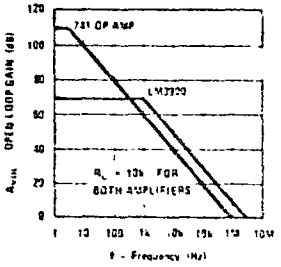


FIGURE 5. Open-loop Gain Characteristics

The complete schematic diagram of the LM3900 is shown in Figure 6 The one resistor R_5, establishes the power consumption of the circuit as it controls the conduction of transistor Q_{28} The emitter current of Q_{28} is used to bias the NPN output class-A biasing current sources and the collector current of Q_{28} is the reference for the PNP current source of each amplifier

The biasing circuit is initially started by Q_{20} Q_{30} and CR_5 After start-up is achieved Q_{30} goes OFF and the current flow through the reference diodes CR_5 CR_6 and CR_8 is dependent only on $V_{BE}/(R_6 - R_7)$ This guarantees that the power supply current drain is essentially independent of the magnitude of the power supply voltage

The input clamp for negative voltages is provided by the multi-emitter NPN transistor Q_{21}

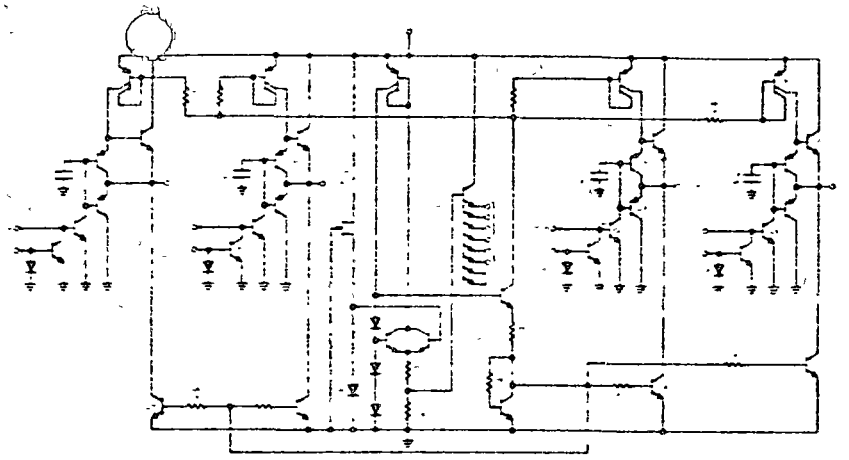


FIGURE 6. Schematic Diagram of the LM3900

One of the emitters of this transistor goes to each of the input terminals. The reference voltage for the base of Q_{21} is produced by R_6 and R_7 and is approximately V_{BE}.

2.0 INTRODUCTION TO APPLICATIONS OF THE LM3900

Like the standard IC op amp the LM3900 has a wide range of applications. A new approach must be taken to design circuits with this 'Norton' amplifier and the object of this note is to present a variety of useful circuits to indicate how conventional and unique new applications can be designed—especially when operating with only a single power supply voltage.

To understand the operation of the LM3900 we will compare it with the more familiar standard IC op amp. When operating on a single power supply voltage, the minimum input common-mode voltage range of a standard op amp limits the smallest value of voltage which can be applied to both inputs and still have the amplifier respond to a differential input signal. In addition the output voltage will not swing completely from ground to the power supply voltage. The output voltage depends upon the difference between the input voltages and a bias current must be supplied to both inputs. A simplified diagram of a standard IC op amp operating from a single power supply is shown in Figure 7. The (+) and (-) inputs go only to current sources and therefore are free to be biased or operated at any voltage values which are within the input common-mode voltage range. The current sources at the input terminals I_B^+ and I_B^- represent the bias currents which must be supplied to both of the input transistors of the op amp (base currents). The output circuit is modeled as an active voltage source which depends upon the open-loop gain of the amplifier A_v and the difference which exists between the input voltages $(V^+ - V^-)$.

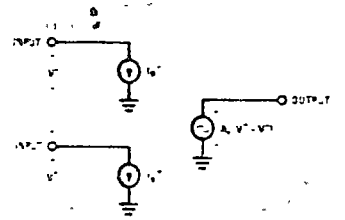


FIGURE 7. An Equivalent Circuit of a Standard IC Op Amp

An equivalent circuit for the 'Norton' amplifier is shown in Figure 8. The (+) and (-) inputs are both clamped by diodes to force them to be one-diode drop above ground—always! They are not free to move and the input common-mode voltage range directly at these input terminals is very small—a few hundred mV centered about 0.5 V_{DC}. This is why external voltages must be first converted to currents (using resistors) before being applied to the inputs—and is the basis for the current-mode (or Norton) type of operation. With external input resistors—there is *no limit* to the input common-mode voltage range. The diode shown across the (-) input actually exists as a diode in the circuit and the diode across the (-) input is used to model the base-emitter junction of the transistor which exists at this input.

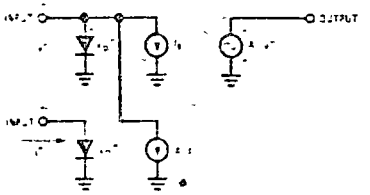


FIGURE 8. An Equivalent Circuit of the "Norton" Amplifier

Only the (-) input must be supplied with a DC biasing current I_B. The (+) input couples only to the (-) input and then to extract from this (-) input terminal the same current (A_i the mirror gain is approximately equal to 1) which is entered (by the external circuitry) into the (-) input terminal. This operation is described as a "current-mirror" as the current entering the (+) input is 'mirrored' or "reflected" about ground and is then extracted from the (-) input. There is a maximum or near saturation value of current which the "mirror" at the (-) input can handle. This is listed on the data sheet as maximum mirror current and ranges from approximately 6 mA at 25°C to 3.5 mA at 70°C.

This fact that the (+) input current modulates or effects the (-) input current causes this amplifier to pass currents between the input terminals and is the basis for many new application circuits—especially when operating with only a single power supply voltage.

The output is modeled as an active voltage source which also depends upon the open-loop voltage gain A_v, but only the (-) input voltage V^- (not the differential input voltage). Finally the output voltage of the LM3900 can swing from essentially ground (~90 mV) to within one V_{BE} of the power supply voltage.

As an example of the use of the equivalent circuit of the LM3900, the AC coupled inverting amplifier of Figure 9a will be analyzed. Figure 9b shows the complete equivalent circuit which, for convenience can be separated into a biasing equivalent circuit (Figure 10) and an AC equivalent circuit (Figure 11). From the biasing model of Figure 10 we find the output quiescent voltage V_O is

$$V_O = V_D^- + (I_B + I^+)\,R_2 \qquad (1)$$

and

$$I^+ = \frac{V^+ - V_D^+}{R_3} \qquad (2)$$

where

$$V_D^+ \cong V_D^- \cong 0.5\,V_{DC}$$

I_B = INPUT bias current (30 nA)

and

V^+ = Power supply voltage

If (2) is substituted into (1)

$$V_O = V_D^- + \left(I_B + \frac{V^+ - V_D^+}{R_3}\right) R_2 \qquad (3)$$

which is an exact expression for V_O.

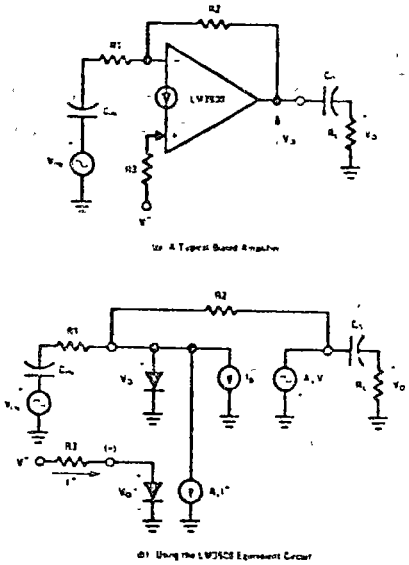


FIGURE 9. Applying the LM3900 Equivalent Circuit

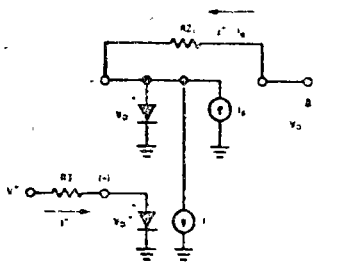


FIGURE 10. Biasing Equivalent Circuit

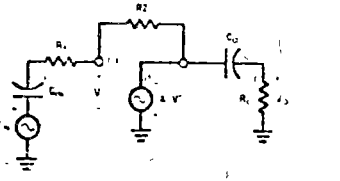


FIGURE 11. AC Equivalent Circuit

as the second term usually dominates ($V_O >>$ V_B^- and $V^+ >> V_B$ and $V^+ >> V_D$) we can simplify (3) to provide a more useful design relationship

$$V_O \cong \frac{R_2}{R_3} V^+ . \quad (4)$$

Using (4) if $R_3 = 2R_2$ we find

$$V_O \cong \frac{R_2}{2R_2} V^+ = \frac{V^+}{2} . \quad (5)$$

which shows that the output is easily biased to one-half of the power supply voltage by using V^+ as a biasing reference at the (+) input

The AC equivalent circuit of Figure 11 is the same as that which would result if a standard IC op amp were used with the (+) input grounded. The closed-loop voltage gain $A_{V_{CL}}$ is given by

$$A_{V_{CL}} \cong \frac{V_O}{V_{IN}} \cong - \frac{R_2}{R_1} \quad (6)$$

(if A_V (open-loop) $> \frac{R_2}{R_1}$)

The design procedure for an AC coupled inverting amplifier using the LM3900 is therefore to first select R_1 C_{IN} R_2 and C_O as with a standard IC op amp and then to simply add $R_3 = 2R_2$ as a final biasing consideration. Other biasing techniques are presented in the following sections of this note. For the switching circuit applications the biasing model of Figure 10 is adequate to predict circuit operation.

Although the LM3900 has four independent amplifiers, the use of the label "LM3900" will be shortened to simply "LM3900" for the application drawings contained in this note.

3.0 DESIGNING AC AMPLIFIERS

The LM3900 readily lends itself to use as an AC amplifier because the output can be biased to any desired DC level within the range of the output voltage swing and the AC gain is independent of the biasing network. In addition, the single power supply requirement makes the LM3900 attractive for any low frequency gain application. For lowest noise performance, the (-) input should be grounded (Figure 9a) and the output will then bias at $+V_{BE}$. Although the LM3900 is not suitable as an ultra low noise tape pre-amp it is useful in most other applications. The restriction to only shunt feedback causes a small input impedance. Transducers which can be loaded can operate with this low input impedance. The noise degradation which would result from the use of a large input resistor limits its usefulness where low noise and high input impedance are both required.

3.1 Single Power Suply Biasing

The LM3900 can be biased in several different ways. The circuit in Figure 12 is a standard inverting AC amplifier which has been biased

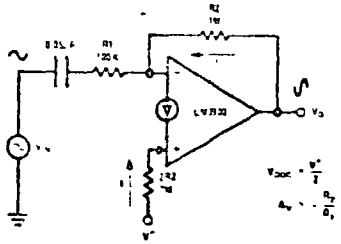


FIGURE 12. Inverting AC Amplifier Using Single-supply Biasing

from the same power supply which is used to operate the amplifier. (The design of this amplifier has been presented in the previous section.) Notice that if AC ripple voltages are present on the V^+ power supply line they will couple to the output with a 'gain' of 1/2. To eliminate this, one source of ripple filtered voltage can be provided and then used for many amplifiers. This is shown in the next section.

3.2 A Non-inverting Amplifier

The amplifier in Figure 13 shows both a non-inverting AC amplifier and a second method for DC biasing. Once again the AC gain of the amplifier is set by the ratio of feedback resistor to input resistor. The small signal impedance of the diode at the (+) input should be added to the value of R_1 when calculating gain, as shown in Figure 13

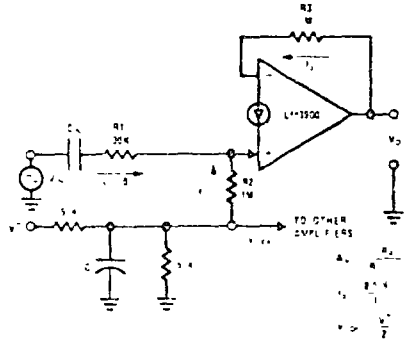


FIGURE 13. Non-inverting AC Amplifier Using Voltage Reference Biasing

By making $R_2 = R_3$ V_{ODC} will be equal to the reference voltage which is applied to the resistor R_2. The filtered $V^+/2$ reference shown can also be used for other amplifiers.

3.3 "N V_{BE}" Biasing

A third technique of output DC biasing is best described as the N V_{BE} method. This technique is shown in Figure 14 and is most useful with inverting AC amplifier applications. The

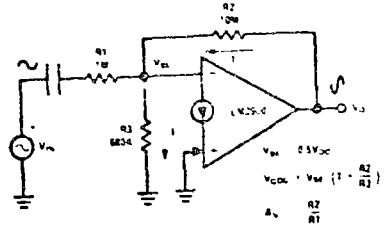


FIGURE 14. Inverting AC Amplifier Using N V_{BE} Biasing

input bias voltage (V_{BE}) at the inverting input establishes a current through resistor R_3 to ground. This current must come from the output of the amplifier. Therefore V_O must rise to a level which will cause this current to flow through R_2. The bias voltage, V_O may be calculated from the ratio of R_2 to R_3 as follows

$$V_{ODC} = V_{BE}\left(1 + \frac{R_2}{R_3}\right)$$

When NV_{BE} biasing is employed values for resistors R_1 and R_2 are first established and then resistor R_3 is added to provide the desired DC output voltage.

For a design example (Figure 14), a Z in = 1M and $A_V \cong 10$ are required.

Select R_1 = 1M

Calculate $R_2 \cong A_V R_1$ = 10M

To bias the output voltage at 7.5 V_{DC}, R_3 is found as

$$R_3 = \frac{R_2}{\frac{V_O}{V_{BE}} - 1} = \frac{10M}{\frac{7.5}{0.5} - 1}$$

or

$$R_3 \cong 680\,k\Omega .$$

3.4 Biasing Using a Negative Supply

If a negative power supply is available the circuit of Figure 15 can be used. The DC biasing current, I, is established by the negative supply voltage via R_3 and provides a very stable output quiescent point for the amplifier.

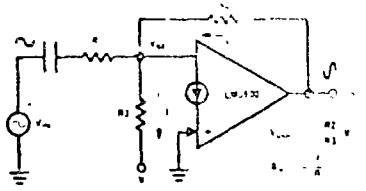


FIGURE 15. Negative Supply Biasing

3.5 Obtaining High Input Impedance and High Gain

For the AC amplifiers which have been presented, a designer is able to obtain either high gain or high input impedance with very little difficulty. The application which requires both and still employs only one amplifier presents a new problem. This can be achieved by the use of a circuit similar to the one shown in Figure 16. When the A_V from the input to point A

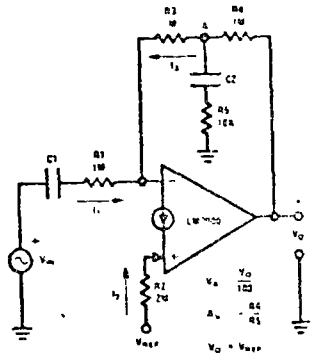


FIGURE 16. A High Z_{IN} High Gain Inverting AC Amplifier

is unity ($R_1 = R_3$) the A_V of the complete stage will be set by the voltage divider network composed of R_4, R_5 and C_2. As the value of R_5 is decreased, the A_V of the stage will approach the AC open loop limit of the amplifier. The insertion of capacitor C_2 allows the DC bias to be controlled by the series combination of R_3 and R_4 with no effect from R_5. Therefore, R_2 may be selected to obtain the desired output DC biasing level using any of the methods which have been discussed. The circuit in Figure 16 has an input impedance of 1M and a gain of 100.

3.6 An Amplifier with a DC Gain Control

A DC gain control can be added to an amplifier as shown in Figure 17. The output of the amplifier is kept from being driven to saturation as the DC gain control is varied by providing a minimum bias

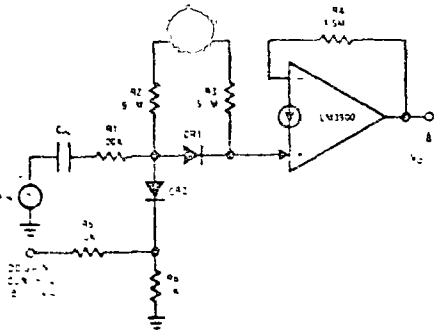


FIGURE 17. An Amplifier with a DC Gain Control

maximum gain CR_2 is OFF and both the current through R_2 and R_3 enter the (-) input and cause the output of the amplifier to bias at approximately 0.6 V*. For minimum gain CR_2 is ON and only the current through R_3 enters the (-) input to bias the output at approximately 0.3 V*. The proper output bias for large output signal accomodation is provided for the maximum gain situation. The DC gain control input ranges from $0V_{DC}$ for minimum gain to less than $10V_{DC}$ for maximum gain.

3.7 A Line-receiver Amplifier

A line-receiver amplifier is shown in Figure 18. The use of both inputs cancels out common-mode signals. The line is terminated by R_{LINE} and the larger input impedance of the amplifier will not effect this matched loading.

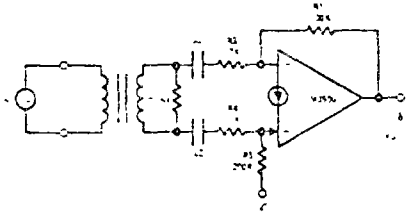


FIGURE 18. A Line receiver Amplifier

4.0 DESIGNING DC AMPLIFIERS

The design of DC amplifiers using the LM3900 tends to be more difficult than the design of AC amplifiers. These difficulties occur when designing a DC amplifier which will operate from only a single power supply voltage and yet provide an output voltage which goes to zero volts DC and also will accept input voltages of zero volts DC. To accomplish this the inputs must be biased into the linear region ($-V_{BE}$) with DC input signals of zero volts and the output must be modified if operation to actual ground (or near V_{SAT}) is required. Therefore the problem becomes one of determining what type of network is necessary to provide an output voltage (V_O) equal to zero when the input voltage (V_{IN}) is equal to zero. (See also section 10.16, adding a Differential Input Stage.)

We will start with a careful evaluation of what actually takes place at the amplifier inputs. The mirror circuit demands that the current flowing into the positive input (+) be equaled by a current flowing into the negative input (-). The difference between the current demanded and the current provided by an external source must flow in the feedback circuit. The output voltage is then forced to seek the level required to cause this amount of current to flow. If in the steady state condition $V_O = V_{IN} = 0$, the amplifier will operate in the desired manner. This condition can be established by the use of common-mode biasing at the inputs.

4.1 Using Common-mode Biasing for V_{IN} = 0 V_{DC}

Common-mode biasing is achieved by placing equal resistors between the amplifier input terminals and the supply voltage (V^+), as shown in Figure 19. When V_{IN} is set to 0 volts

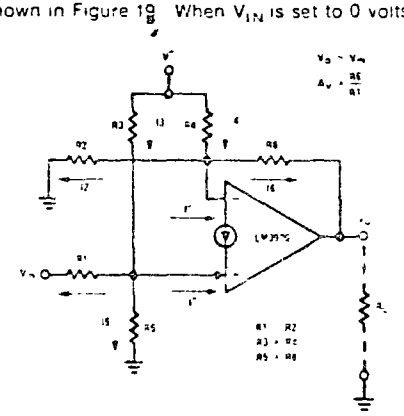


FIGURE 19. A DC Amplifier Employing Common-mode Biasing

the circuit can be modeled as shown in Figure 20 where

$$R_{EQ_1} = R_1 \parallel R_5 ,$$

$$R_{EQ_2} = R_2 \parallel R_6$$

and

$$R_3 = R_4$$

Because the current mirror demands that the two current sources be equal, this current in the two equivalent resistors must be equal as

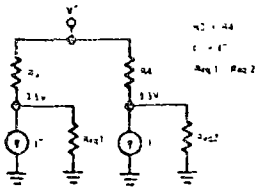


FIGURE 20. An Ideal Circuit Model of a DC Amplifier with Zero Input Voltage

If this is true, both R_2 and R_6 must have a voltage drop of 0.5 volt across them, which forces V_O to go to $V_{O\,MIN}$ (V_{SAT}).

4.2 Adding an Output Diode for V_O = 0 V_{DC}

For many applications a $V_{O\,MIN}$ of 100 mV may not be acceptable. To overcome this problem a diode can be added between the output of the amplifier and the output terminal (Figure 21).

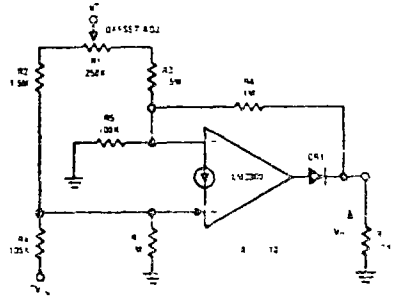


FIGURE 21. A Non-inverting DC Amplifier with Zero Volts Output for Zero Volts Input

The function of the diode is to provide a DC level shift which will allow V_O to go to ground. With a load impedance (R_L) connected, V_O becomes a function of the voltage divider formed by the series connection of R_4 and R_L.

$$\text{If } R_4 = 100\,R_L \text{ then } V_{O\,MIN} = \frac{0.5\,R_L}{101\,R_L} ,$$

$$\text{or } V_{O\,MIN} \cong 5\,mV_{DC} .$$

An offset voltage adjustment can be added as shown (R_1) to adjust V_O to $0V_{DC}$ with V_{IN} = 0 V_{DC}.

The voltage transfer functions for the circuit in Figure 21, both with and without the diode, are shown in Figure 22. While the diode greatly improves the operation around 0 volts, the voltage drop across the diode will reduce the peak output voltage swing of the stage by approximately 0.5 volt.

When using a DC amplifier similar to the one in Figure 21, the load impedance should be large enough to avoid excessively loading the amplifier. The value of R_L may be significantly reduced by replacing the diode with an NPN transistor.

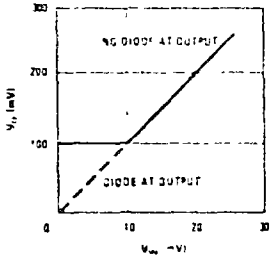


FIGURE 22. Voltage Transfer Function for a DC Amplifier with a Voltage Gain of 10

4.3 A DC Coupled Power Amplifier ($I_L \leq$ 3 Amps)

The LM3900 may be used as a power amplifier by the addition of a Darlington pair at the output. The circuit shown in Figure 23 can deliver in excess of 3 amps to the load when the transistors are properly mounted on heat sinks.

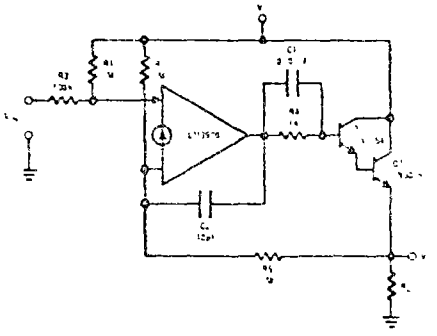


FIGURE 23. A DC Power Amplifier

4.4 Ground Referencing a Differential Voltage

The circuit in Figure 24 employs the LM3900 to ground reference a DC differential input voltage. Current I_1 is larger than current I_2 by a

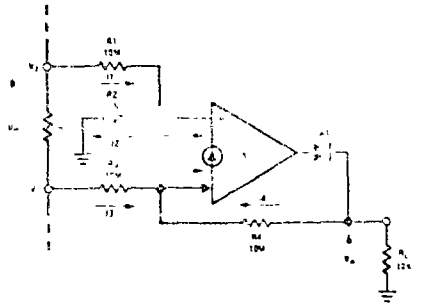


FIGURE 24. Ground Referencing a Different of Input DC Voltage

...or proportional to the differential voltage. The currents applied to Figure 24 are given

$$I_1 = \frac{V_1 + V_R - \square}{R_1}$$

$$I_2 = \square R_2$$

$$I_3 = \frac{(V_1 - \square)}{R_3}$$

$$I_4 = \frac{V_O - \square}{R_4}$$

...here
$\square \equiv V_{BE}$ at either input terminal of the LM3900

...nce the input current mirror demands that

$$I^- = I^+$$

$$I^+ = I_1 - I_2$$

$$I^- = I_3 + I_4$$

...herefore

$$I_4 = I_1 - I_2 - I_3$$

...es resulting in from the above equation

$$\frac{O - \square}{R_4} = \frac{(V_1 + V_R - \square)}{R_1} - \frac{(\square)}{R_2} - \frac{(V_1 - \square)}{R_3}$$

...d as $R_1 = R_2 = R_3 = R_4$

$$V_O = (V_1 + V_R - \square) - (\square) - V_1 + \square + \square$$

$$V_O = V_R$$

...e resistors are kept large to minimize loading ...m the 10 MΩ resistors which are shown on ...e figure an error exists at small values of V_1 ...e to the input bias current at the (-) input ...r simplicity this has been neglected in the ...uit description. Smaller R values reduce ...e percentage error or the bias current can be ...plied by an additional amplifier (see Section 10.7.1)

...r proper operation the differential input voltage must be limited to be within the output ...namic voltage range of the amplifier and the ...put voltage V_2 must be greater than 1 volt ...r example if V_2 = 1 volt, the input voltage ...n may vary over the range of 1 volt to -13 volts ...hen operating from a 15 volt supply. ...mmon-mode biasing may be added as shown ...Figure 25 to allow both V_1 and V_2 to be ...ge...ve

5 A Unity Gain Buffer Amplifier

...he buffer amplifier with a gain of one is the ...mplest DC application for the LM3900. The ...oltage applied to the input (Figure 26) will be ...eproduced at the o... however the input

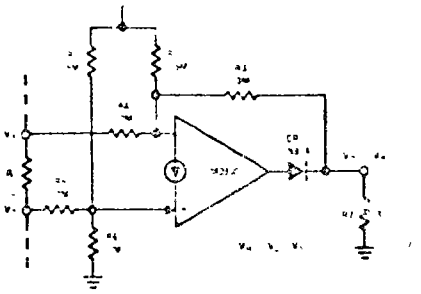


FIGURE 25 A Network to Invert and to Ground Reference a Negative DC Differential Input Voltage

voltage must be greater than one V_{BE} but less than the maximum output swing. Common-mode biasing can be added to extend V_{IN} to 0 V_{DC} if desired.

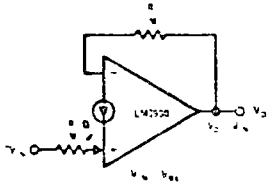


FIGURE 26 A Unity-gain DC Buffer Amplifier

5.0 DESIGNING VOLTAGE REGULATORS

Many voltage regulators can be designed which make use of the basic amplifier of the LM3900. The simplest is shown in Figure 27a where only a Zener diode and a resistor are added. The voltage at the (-) input (one $V_{BE} \cong 0.5\ V_{DC}$) appears across R and therefore a resistor value of 510Ω will cause approximately 1 mA of bias current to be drawn through the Zener. This biasing is used to reduce the noise output of the Zener as the 30 nA input current is too small for proper Zener biasing. To compensate for a positive temperature coefficient of the Zener an additional resistor can be added R_2 (Figure 27b) to introduce an arbitrary number N of effective V_{BE} drops into the expression for the output voltage. The negative temperature coefficient of these diodes will also be added to temperature compensate the DC output voltage. For a larger output current ... (Figure 27c) can be added. This ... output current of the LM3900 by the β of the added transistor. For example a β = 30 will provide a max load current of 300 mA. This added transistor also reduces the output impedance. An output frequency compensation capacitor is generally not required but may be added if desired to reduce the output impedance at high frequencies.

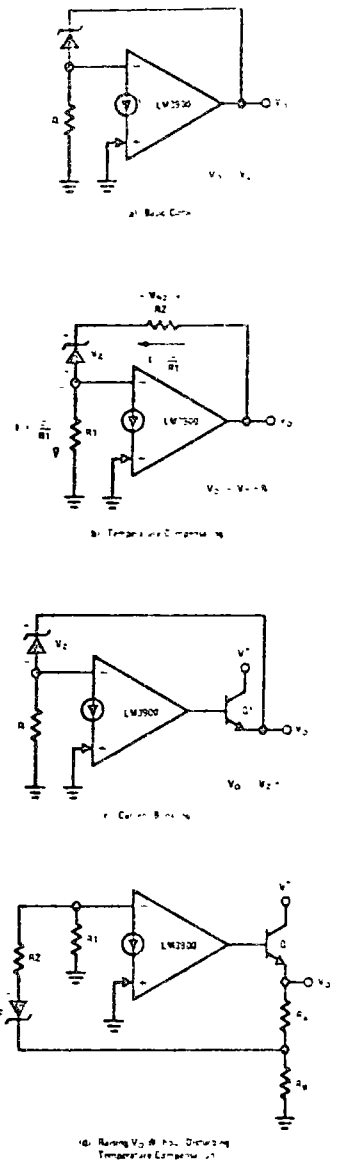


FIGURE 27 Simple Voltage Regulators

The DC output voltage can be increased and still preserve the temperature compensation of Figure 27b by adding resistors R_A and R_B as shown in Figure 27d. This can be accomplished without the added transistor Q_1. The unregulated input voltage which is applied to pin 14 of the LM3900 (and to the collector of Q_1 if used) must always exceed the regulated DC output voltage by approximately 1V when the unit is not current boosted or approximately ... when the NPN current boosting transistor is used.

5.1 Reducing the Input output Voltage

The use of an external PNP transistor will reduce the required (V_{IN} - V_{OUT}) to a few tenths of a volt. This will depend on the saturation characteristics of the external transistor at the operating current level. The circuit shown in Figure 28 uses the LM3900 to supply base drive to the PNP transistor. The resistors R_1 and R_2 are used to allow the output of the amplifier to turn OFF the PNP transistor. It is important that pin 14 of the LM3900 be tied to the $+V_{IN}$ line to allow this OFF control to properly operate. Larger voltages are permissable (if the base-emitter junction of Q_1 is prevented from entering a breakdown by a shunting diode for example), but smaller voltages will not allow the output of the amplifier to raise enough to give the OFF control.

The resistor R_3 is used to supply the required bias current for the amplifier and R_4 is again used to bias the Zener diode. Due to a larger gain a compensation capacitor C_O is required. Temperature compensation could be added as was shown in Figure 27b.

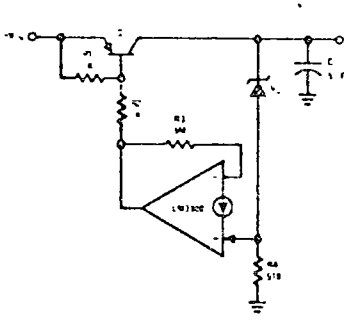


FIGURE 28 Reducing (V_{IN} – V_{OUT})

5.2 Providing High Input Voltage Protection

One of the four amplifiers can be used to regulate the supply line for the complete package (pin 14) to provide protection against large input voltage conditions and in addition, to supply current to an external load. This circuit is shown in Figure 29. The regulated output voltage is the sum of the Zener voltage CR_2 and the V_{BE} of the inverting input terminal. Again temperature compensation can be ... as in Figure 27b. The second Zener CR_1 is a low tolerance component which simply serves as a DC level shift to allow the output voltage of the amplifier to control the conduction of the external transistor Q_1. This Zener voltage should be approximately one-half of the CR_2 voltage to position the DC output voltage level of the am... approximately in the center of the d... range.

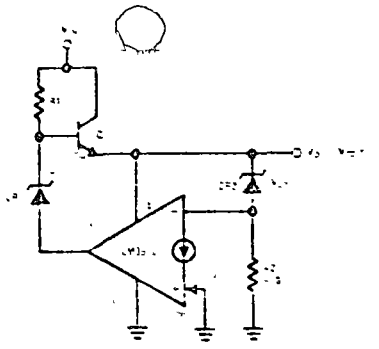


FIGURE 29 High V_{IN} Protection and Self-regulation

The base drive current for Q_1 is supplied via R_1. The maximum current through R_1 should be limited to 10 mA as

$$I_{MAX} = \frac{V_{IN(MAX)} - (V_O + V_{BE})}{R_1}$$

To increase the maximum allowed input voltage, reduce the output ripple or to reduce the (V_{IN} - V_{OUT}) requirements of this circuit the connection described in the next section is recommended.

5.3 High Input Voltage Protection and Low (V_{IN} - V_{OUT})

The circuit shown in Figure 30 basically adds one additional transistor to the circuit of Figure 29 to improve the performance. In this circuit both transistors (Q_1 and Q_2) absorb any high input voltages (and therefore need to be high voltage devices) without any increases in current (as with R_1 of Figure 29). The resistor R_1 (of Figure 30) provides a start-up current into the base of Q_2.

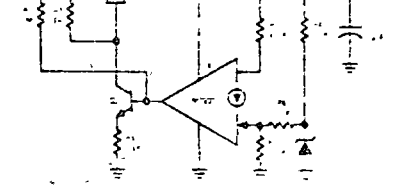


FIGURE 30 A High V_{IN} Protected Low (V_{IN} - V_{OUT}) Regulator

A new input connection is shown on this regulator (the type on Figure 29 could also be used) to control the DC output voltage. The Zener is biased via R_4 (at approximately 1 mA). The resistors R_3 and R_5 provide gain (non-inverting) to allow establishing V_O at any desired voltage larger than V_Z. Temperature compensation of either sign (±TC) can be obtained by shunting a resistor from either the (+) input to ground (to add - TC to V_O) or from the (-) input to ground (to add - TC to V_O). To understand this, notice that the resistor R, from the (+) input to ground will add -N V_{BE} to V_O where

$$N = 1 + \frac{R_3}{R}$$

and V_{BE} is the base emitter voltage of the transistor at the (+) input. This then also adds a positive temperature change at the output to provide the desired temperature correction.

The added transistor Q_2, also increases the gain (which reduces the output impedance) and if a power device is used for Q_1 large load currents (amps) can be supplied. This regulator also supplies the power to the other three amplifiers of the LM3900.

5.4 Reducing Input Voltage Dependence and Adding Short-circuit Protection

To reduce ripple feedthrough and input voltage dependence diodes can be added as shown in Figure 31 to drop-out the start circuit once

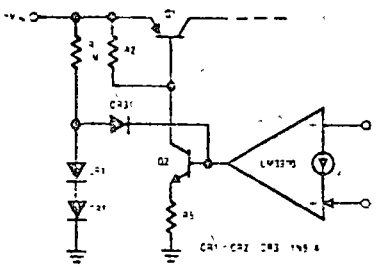


FIGURE 31 Reducing V_{IN} Dependence

start-up has been achieved. Short-circuit protection can also be added as shown in Figure 32.

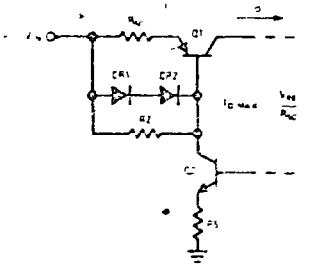


FIGURE 32 Adding Short-circuit Current Limiting

The emitter resistor of Q_2 will limit the maximum current of Q_2 to (V_O - 2 V_{BE}) / R_5.

6.0 DESIGNING RC ACTIVE FILTERS

Recent work in RC active filters has shown that the performance characteristics of multiple-amplifier filters are relatively insensitive to the tolerance of the RC components used. This makes the performance of these filters easier to control in production runs. In many cases where gain is needed in a system design it is now relatively easy to also get frequency selectivity.

The basis of active filters is a gain stage and therefore a multiple amplifier product is a valuable addition to this application area. When additional amplifiers are available, less component selection and trimming is needed as the performance of the filter is less disturbed by the tolerance and temperature drifts of the passive components.

The *passive components do control the performance* of the filter and for this reason carbon composition resistors are useful mainly for room temperature breadboarding or for final trimming of the more stable metal film or wire-wound resistors. Capacitors present more of a problem in range of values available tolerance and stability (with temperature, frequency, voltage and time). For example the disk ceramic type of capacitors are generally not suited to active filter applications due to their relatively poor performance.

The impedance level of the passive components can be scaled without (theoretically) affecting the filter characteristics. In an actual circuit if the resistor values become too small (≤10 kΩ) an excessive loading may be placed on the output of the amplifier which will reduce gain or actually exceed either the output current or the package dissipation capabilities of the amplifier. This can easily be checked by calculating (or noticing) the impedance which is presented to the output terminal of the amplifier at the highest operating frequency. A second limit sets the upper range of impedance levels; this is due to the DC bias currents (≅30 nA) and the input impedance of actual amplifiers. The solution to this problem is to reduce the impedance levels of the passive components (≤10 MΩ). In general better performance is obtained with relatively low passive component impedance levels and in filters which do not demand high gain, high Q (Q ≥ 50) and high frequency (f_o > 1 kHz) simultaneously.

A measure of the effects of changes in the values of the passive components on the filter performance has been given by sensitivity functions. These assume infinite amplifier gain and relate the percentage change in a parameter of the filter such as center frequency (f_o), Q, or gain to a percentage change in a particular passive component. Sensitivity functions which are small are desirable as 1 or 1/2

Negative sign simply means increase in the value of a passive component causes a decrease in that filter performance characteristic. As an example, if a bandpass filter listed the following sensitivity factor

$$S^{\omega_o}_{C_3} = -\frac{1}{2}$$

This states that if C_3 were to increase by 1% the center frequency, ω_o, would decrease by 0.5%. Sensitivity functions are tabulated in the reference listed at the end of this section and will therefore not be included here.

A brief look at low pass, high pass and bandpass filters will indicate how the LM3900 can be applied in these areas. A recommended text (which provided these circuits) is "Operational Amplifiers", Tobey Graeme, and Huelsman McGraw Hill 1971.

6.1 Biasing the Amplifiers

Active filters can be easily operated off of a single power supply when using these multiple single supply amplifiers. The general technique is to use the (+) input to accomplish the biasing function. The power supply voltage V^+ is used as the DC reference to bias the output voltage of each amplifier at approximately $V^+/2$. As shown in Figure 33 undesired AC components on the power supply line may have to be removed (by a filter capacitor

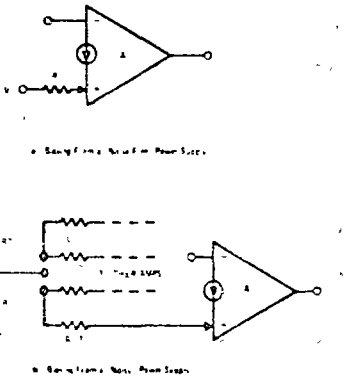


FIGURE 33 Biasing Considerations

Figure 33b) to keep the filter output free of this noise. One filtered DC reference can generally be used for all of the amplifiers as there is essentially no signal feedback to this bias point.

In the filter circuits presented here all amplifiers will be biased at $V^+/2$ to allow the maximum AC voltage swing for any given DC power supply voltage. The inputs to these filters will also be assumed at a DC level of $V^+/2$ (to those which are direct coupled).

A High Pass Active Filter

single amplifier high pass RC active filter shown in Figure 34. This circuit is easily ased using the (-) input of the LM3900. The sistor R_3 can be simply made equal to R_2 d a bias reference of V⁺/2 will establish the rput Q point at this value (V⁺/2). The input capacitively coupled (C_1) and there are erefore no further DC biasing problems.

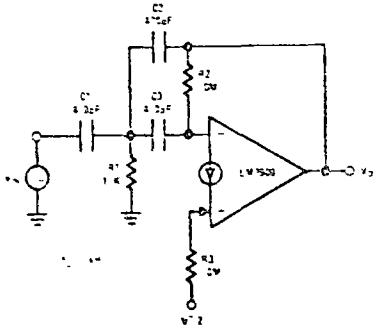


FIGURE 34 A High Pass Active Filter

he design procedure for this filter is to select e pass band gain H_0, the Q and the corner equency f_c. A Q value of 1 gives only a ght peaking near the bandedge (<2 dB) and naller Q values decrease this peaking. The ope of the skirt of this filter is 12 dB/octave r 40 dB/decade). If the gain H_0 is unity capacitors have the same value. The design ceeds as

ven H_0, Q and $\omega_c = 2\pi f_c$

find R_1, R_2, C_1, C_2, and C_3

$C_1 = C_3$ and choose a convenient starting lue

en

$$R_1 = \frac{1}{Q\,\omega_c C_1 (2H_0 + 1)} \qquad (1)$$

$$R_2 = \frac{Q}{\omega_c C_1 (2H_0 + 1)} \qquad (2)$$

d

$$C_2 = \frac{C_1}{H_0} \qquad (3)$$

a design example

quire $H_0 = 1$,

$Q = 10$

d $f_c = 1\ kHz$ ($\omega_c = 6.28 \times 10^3$ rps)

Start by selecting $C_1 = 300$ pF and then from equation (1)

$$R_1 = \frac{1}{(10)(6.28 \times 10^3)(3 \times 10^{-10})(3)}$$

$$R_1 = 17.7\ k\Omega$$

and from equation (2)

$$R_2 = \frac{10}{(6.28 \times 10^3)(3 \times 10^{-10})}$$

$$R_2 = 159\ k\Omega$$

and from equation (3)

$$C_2 = \frac{C_1}{1} = C_1$$

Now we see that the value of R_2 is quite large, but the other components look acceptable. Here is where impedance scaling comes in. We can reduce R_2 to the more convenient value of 10 MΩ which is a factor of 15.9:1. Reducing R_1 by this same scaling factor gives

$$R_{1_{NEW}} = \frac{17.7 \times 10^3}{15.9} = 11.1\ k\Omega$$

and the capacitors are similarly reduced in impedance as

$$(C_1 = C_2 = C_3)_{NEW} = (15.9)(300)\ pF$$

$$C_{1_{NEW}} = 477\ pF$$

To complete the design R_3 is made equal to R_2 (10 MΩ) and a V_{REF} of V⁺/2 is used to bias the output for large signal accomodation.

Capacitor values should be adjusted to use standard valued components by using impedance scaling as a wider range of standard resistor values is generally available.

6.3 A Low Pass Active Filter

A single amplifier low pass filter is shown in Figure 35. The resistor R_4 is used to set the

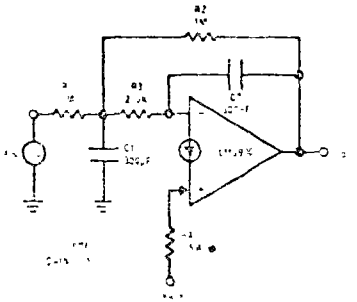


FIGURE 35 A Low Pass Active Filter

output bias level [illegible] and after the other resistors have been established.

The design procedure is as follows:

Given H_0, Q and $\omega_c = 2\pi f_c$

To find R_1, R_2, R_3, R_4, C_1 and C_2

Let C_1 be a convenient value

then

$$C_2 = KC_1 \qquad (4)$$

where K is a constant which can be used to adjust component values. For example, with $K = 1$, $C_1 = C_2$. Larger values of K can be used to reduce R_2 and R_3 at the expense of a larger value for C_2.

$$R_1 = \frac{R_2}{H_0}. \qquad (5)$$

$$R_2 = \frac{1}{2Q\,\omega_c C_1}\left[1 \pm \sqrt{1 + \frac{4Q^2(H_0 + 1)}{K}}\right] \qquad (6)$$

and

$$R_3 = \frac{1}{\omega_c^2 C_1^2 R_2 (K)}. \qquad (7)$$

As a design example

Require $H_0 = 1$,

$Q = 1$,

and $f_c = 1\ kHz$ ($\omega_c = 6.28 \times 10^3$ rps)

Start by selecting $C_1 = 300$ pF and $K = 1$ so C_2 is also 300 pF (equation 4)

Now from equation (6)

$$R_2 = \frac{1}{2(1)(6.28 \times 10^3)(3 \times 10^{-10})}\left[1 \pm \sqrt{1 + 4(2)}\right]$$

$$R_2 = 1.06\ M\Omega$$

Then from equation (5)

$$R_1 = R_2 = 1.00\ M\Omega$$

and finally from equation (7)

$$R_3 = \frac{}{(6.28 \times 10^3)^2 (3 \times 10^{-10})^2 (1.0 \times 10^6)(1)}$$

$$R_3 = 266\ k\Omega$$

To select R_4 we assume the DC input level is $\frac{1}{2}V_{DC}$ and the DC output of this filter is to be 7 V_{DC}. This gives us the circuit of Figure 36. Notice that $H_0 = 1$ gives us not only

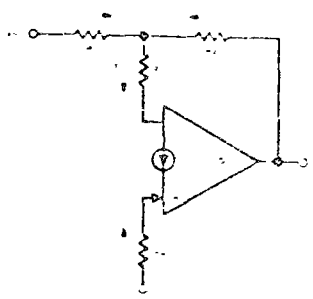


FIGURE 36 Biasing the Low Pass Filter

equal resistor values (R_1 and R_2) but simplifies the DC bias calculation as $I_1 = I_2$ and we have a DC amplifier with a gain of -1 (so if the DC input voltage increases 1 V_{DC}, the output voltage decreases 1 V_{DC}). The resistors R_1 and R_2 are in parallel so that the circuit simplifies to that shown in Figure 37 where the actual resistance values have been added. The resistor R_4 is given by

$$R_4 = 2\left(\frac{R_1}{2} + R_3\right) + R_3$$

or, using values

$$R_4 = 2\left(\frac{1\ M\Omega}{2} + 266\ k\right) \cong 1.5\ M\Omega$$

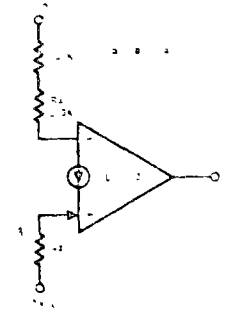


FIGURE 37 Biasing Equivalent Circuit

6.4 A Single amplifier Bandpass Active Filter

[illegible] esting. For low Q bandpass [illegible] gain and low Q (<10) requirements a single amplifier realization can be used. A one amplifier circuit is shown in Figure 38 and the design procedure is as follows:

Given H_0, Q and $\omega_c = 2\pi f$

To find R_1, R_2, R_3, R_4, C_1 and C_2

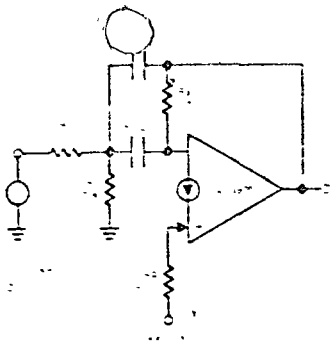


FIGURE 38. A One Op Amp Bandpass Filter

Let $C_1 = C_2$ and select a convenient starting value

Then

$$R_1 = \frac{Q}{H_O\,\omega_o\,C_1} \qquad (8)$$

$$R_2 = \frac{Q}{(2Q^2 - H_O)\,\omega_o\,C_1} \qquad (9)$$

$$R_3 = \frac{2Q}{\omega_o\,C_1} \qquad (10)$$

and

$$R_4 = 2R_3 \text{ (for } V_{REF} = V^+) \qquad (11)$$

As a design example

Require $H_O = 1$

$Q = 5$

$f_o = 1\ kHz\ (\omega_o = 6.28 \times 10^3\ rad)$.

Start by selecting

$$C_1 = C_2 = 510\ pF$$

Then using equation (8)

$$R_1 = \frac{5}{(6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_1 = 1.57\ M\Omega.$$

and using equation (9)

$$R_2 = \frac{5}{[2(25) - 1](6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_2 = 32\ k\Omega$$

from equation (10)

$$R_3 = \frac{2(5)}{(6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_3 = 3.13\ M\Omega$$

and finally, for biasing using equation (11)

$$R_4 = 6.2\ M\Omega$$

6.5 A Two-amplifier Bandpass Active Filter

To allow higher Q (between 10 and 50) and higher gain a two amplifier filter is required. This circuit shown in Figure 39 uses only two capacitors. It is similar to the previous single amplifier bandpass circuit and the added amplifier supplies a controlled amount of positive feedback to improve the response characteristics. The resistors R_5 and R_8 are used to bias the output voltage of the amplifiers at $V^+/2$.

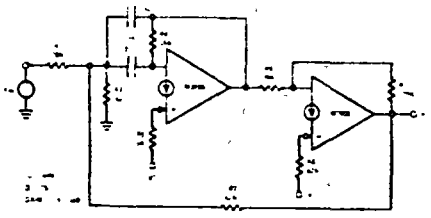


FIGURE 39. A Two Op Amp Bandpass Filter

Again R_5 is simply chosen as twice R_4 and R_8 must be selected after R_6 and R_7 have been assigned values. The design procedure is as follows

Given Q and f_o

To find R_1 through R_7 and C_1 and C_2

Let $C_1 = C_2$ and choose a convenient starting value and choose a value for K to reduce the spread of element values or to optimize sensitivity ($1 \le K_{Typically} \le 10$)

Then

$$R_1 = R_4 = R_6 = \frac{Q}{\omega_o\,C_1} \qquad (12)$$

$$R_2 = R_1\,\frac{KQ}{(2Q - 1)} \qquad (13)$$

$$R_3 = \frac{R_1}{Q^2 - 1 - 2K + 1/KQ} \qquad (14)$$

and

$$R_7 = KR_1 \qquad (15)$$

$$H_O = 3 - K \qquad (16)$$

As a design example

Require $Q = 25$ and $f_o = 1\ kHz$

Select $C_1 = C_2 = 0.1\ \mu F$

and $K = 3$

Then from equation (12)

$$R_1 = R_4 = R_6 = \frac{25}{(2\pi \times 10^3)(10^{-7})}$$

$$R_1 = 40\ k\Omega$$

and from equation (13)

$$R_2 = (40 \times 10^3)\,\frac{3(25)}{[2(25) - 1]}$$

$$R_2 = 61\ k\Omega$$

and from equation (14)

$$R_3 = \frac{40 \times 10^3}{(25)^2 - 1 - 2/3 + \frac{1}{3(25)}}$$

$$R_3 = 64\ \Omega$$

And R_7 is given by equation (15)

$$R_7 = 3(40\ k\Omega) = 120\ k\Omega.$$

and the gain is obtained from equation (16)

$$H_O = \sqrt{25}\ (3) = 15\ (23.5\ dB)$$

To properly bias the first amplifier

$$R_5 = 2R_4 = 80\ k\Omega$$

and the second amplifier is biased by R_8. Notice that the outputs of both amplifiers will be at $V^+/2$. Therefore R_6 and R_7 can be paralleled and

$$R_8 = 2(R_6 \parallel R_7)$$

or

$$R_8 = 2\left[\frac{(40)(120) \times 10^3}{160}\right] = 59\ k\Omega$$

These values (to the closest standard resistor values) have been added to Figure 39

6.6 A Three-amplifier Bandpass Active Filter

To reduce Q sensitivity to element variation even further or to provide higher Q ($Q > 50$) a three amplifier bandpass filter can be used. This circuit, Figure 40, predates most of the literature on RC active filters and has been used on analog computers. Due to the use of three amplifiers it often is considered too costly—especially for low Q applications. The multiple amplifiers of the LM3900 make this a very useful circuit. It has been called the Bi-Quad as it can produce a transfer function which is "Quad — ratic in both numerator and denominator (to give the Bi-). A newer realization technique for this type of filter is the second-degree state variable network. Outputs can be taken at any of three points to give low pass, high pass or bandpass response characteristics (see the reference cited).

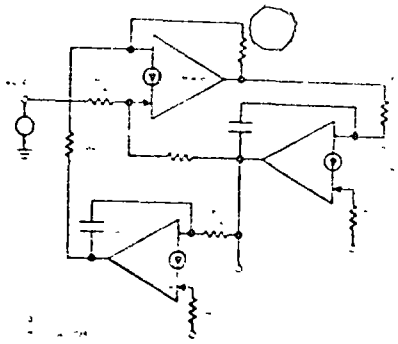


FIGURE 40. The "Bi-quad" RC Active Bandpass Filter

The bandpass filter is shown in Figure 40 and the design procedure is

Given Q and f_o

To simplify Let $C_1 = C_2$ and choose a convenient starting value and also let $2R_1 = R_2 = R_3$ and choose a convenient starting value

Then.

$$R_4 = R_1(2Q - 1). \qquad (17)$$

$$R_5 = R_7 = \frac{1}{\omega_o\,C_1}. \qquad (18)$$

and for biasing the amplifiers we require

$$R_6 = R_8 = 2R_5 \qquad (19)$$

The mid-band gain is

$$H_O = \frac{R_4}{R_1} \qquad (20)$$

As a design example,

Require $f_o = 1\ kHz$ and $Q = 50$.

To find C_1, C_2 and R_1 through R_8

Choose $C_1 = C_2 = 330\ pF$

and $2R_1 = R_2 = R_3 = 360\ k\Omega$ and $R_1 = 180\ k\Omega$

Then from equation (17)

$$R_4 = (1.8 \times 10^5)[2 \quad 1]$$

$$R_4 = 17.8\ M\Omega$$

From equation (18),

$$R_5 = R_7 = \frac{1}{(2\pi \times 10^3)(3.3 \times 10^{-10})}$$

$$R_5 = 433\ k\Omega$$

And from equation (19)

$$R_6 = R_8 \cong 1\ M\Omega$$

m equation (20) the midband gain is 100 dB). The value of R_4 is high and can be ered by scaling only R_1 through R_4 by the or 1.78 to give

$$= R_2 = R_3 = \frac{360 \times 10^3}{1.78} = 200\ k\Omega,\ R_1 = 100\ k\Omega$$

$$R_4 = \frac{17.8 \times 10^6}{1.78} = 10\ M\Omega$$

se values (to the nearest 5% standard) have n added to Figure 40

Conclusions

e unity-gain cross frequency of the LM3900 2.5 MHz which is approximately three times t of a 741 op amp. The performance of the plifier does limit the performance of the e. Historically RC active filters started n little concern for these practical problems e sensitivity functions were a big step for- rd in these areas and that many of the lier suggested realization techniques for RC ive filters had passive component sensitivity ctions which varied as Q or even Q^2. The Quad circuit has reduced the problems with passive components (sensitivity functions 1 or 1/2) and recently the contributions of e amplifier on the performance of the filter e being investigated. An excellent treatment The Biquad Part I — Some Practical Design nsiderations" L.C. Thomas, IEEE Transac- s on Circuit Theory, Vol. CT-18, No. 3, May 71) has indicated the limits imposed by the aracteristics of the amplifier by showing that e design value of Q (Q_D) will differ from the ual measured value of Q (Q_A) by the given ationship

$$Q_A = \frac{Q_D}{1 + \frac{2Q_D}{A_O \omega_a}(\omega_a - 2\omega_p)} \qquad (21)$$

ere A_O is the open loop gain of the amplifier s the dominant pole of the amplifier and ω_p the resonant frequency of the filter. The ult is that the trade off between Q and cen- frequency (ω_p) can be determined for a en set of amplifier characteristics. When Q_A differs significantly from Q_D excessive de- ndence on amplifier characteristics is indi- ed. An estimate of the limitations of an plifier can be made by arbitrarily allowing ximum, a 10% effect on Q_A and then re- s f

$$\frac{2Q_D}{A_O \omega_a}(\omega_a - 2\omega_p) = 0.1$$

$$\left(\frac{\omega_p}{\omega_a}\right) = 2.5 \times 10^{-2}\left(\frac{A_O}{Q_D}\right) + 0.5 \qquad (22)$$

As an example using $A_O = 2800$ for the LM3900 we can estimate the maximum frequency where a $Q_D = 50$ would be reasonable as

$$\frac{f_p}{f_a} = 2.5 \times 10^{-2}\left(\frac{2.8 \times 10^3}{5 \times 10}\right) + 0.5$$

or

$$\frac{f_p}{f_a} = 1.9$$

therefore

$$f_p = 1.9 f_a$$

Again using data of the LM3900 $f_a = 1$ kHz so this upper frequency limit is approximately 2 kHz for the assumed Q of 50. As indicated in equation (26) the value of Q_A can actually exceed the value of Q_D (Q enhancement) and as expected the filter can even provide its own input (oscillating). Excess phase shift in the high frequency characteristics of the amplifier typically cause unexpected oscillations. Phase compensation can be used in the Bi-Quad network to reduce this problem (see L.C. Thomas paper).

Designing for large passband gain also increases filter dependency on the characteristics of the amplifier and finally signal to noise ratio can usually be improved by taking gain in an input RC active filter (again see L.C. Thomas paper).

Somewhat larger Q's can be achieved by adding more filter sections in either a synchronously tuned cascade (filters tuned to same center frequency and taking advantage of the bandwidth shrinkage factor which results from the series connection) or as a standard multiple pole filter. All of the conventional filters can be realized and selection is based upon all of the performance requirements which the application demands. The cost advantages of the LM3900, the relatively large bandwidth and the ease of operation on a single power supply voltage make this product an excellent building block for RC active filters.

7.0 DESIGNING WAVEFORM GENERATORS

The multiple amplifiers of the LM3900 can be used to easily generate a wide variety of waveforms in the low frequency range (f < 10 kHz). Voltage controlled oscillators (VCO's) are also possible and are presented in section 8.0 "Designing Phase-locked Loops and Voltage Controlled Oscillators." In addition, power oscillators (such as noise makers, etc.) are presented in section 10.11.3. The waveform generators which will be presented in this section are mainly of the sine-wave type, but for completeness a square-wave oscillator has been included.

7.1 A Sinewave Oscillator

The design of a sinewave oscillator presents problems in both amplitude stability (and predictability) and output waveform purity (THD). If an RC bandpass filter is used as a high Q resonator for the oscillator circuit we can obtain an output waveform with low distortion and eliminate the problem of relative center frequency drift which exists if the active filter were used simply to filter the output of a separate oscillator.

A sinewave oscillator which is based on this principle is shown in Figure 41. The two-amplifier RC active filter is used as it requires only two capacitors and provides an overall non-inverting phase characteristic. If we add a non-inverting gain controlled amplifier around the filter we obtain the desired oscillator configuration. Finally, the sinewave output voltage is sensed and regulated as the average value is compared to a DC reference voltage V_{REF} by use of a differential averaging circuit. It can be shown that with the values selected for R_{15} and R_{16} (ratio of 0.64:1) that there is first order temperature compensation for CR_3 and the internal input diodes of the IC amplifier which is used for the difference averager. Further, this also provides a simple way to regulate and to predict the magnitude of the output sinewave as

$$V_{O\,peak} = 2V_{REF}$$

which is essentially independent of both temperature and the magnitude of the power supply voltage (if V_{REF} is derived from a stable voltage source).

7.2 Squarewave Generator

The standard op amp squarewave generator has been modified as shown in Figure 42. The

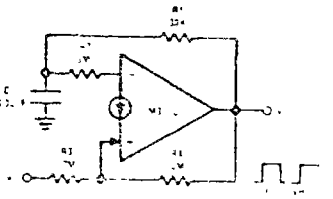


FIGURE 42. A Squarewave Oscillator

capacitor C_1 alternately charges and discharges (via R_1) between the voltage limits which are established by the resistors R_2, R_3 and R_4. This combination produces a Schmitt-Trigger circuit and the operation can be understood by noticing that when the output is low (and if we neglect the current flow through R_4) the resistor R_2 (3M) will cause the trigger to fire when the current through this resistor equals the current which enters the (+) input (via R_3). This gives a firing voltage of approximately $R_2/(R_3)\ V^+$ for $V^+/3$. The other trip point when the output voltage is high is approximately $[2(R_2\ R_3)]\ V^+$ as $R_3 = R_4$, or $2/3(V^+)$. Therefore the voltage across the capacitor C_1 will be the first one-half of an exponential waveform between these voltage trip limits and will have good symmetry, and be essentially independent of the magnitude of the power supply voltage. If an unsymmetrical squarewave is desired, the trip points can be shifted to produce any desired mark/space ratio.

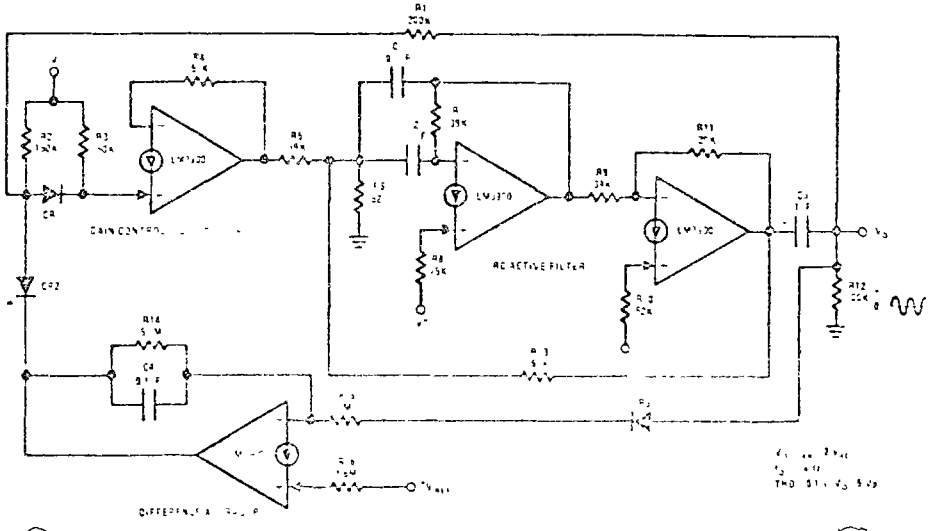


FIGURE 41. A Sinewave Oscillator

7.3 Pulse Generator

The squarewave generator can be slightly modified to provide a pulse generator. The slew rate limits of the LM3900 (0.5V μsec) must be kept in mind as this limits the ability to produce a narrow pulse when operating at a high power supply voltage level. For example with a ±15 V_{DC} power supply the rise time t_r to change 15V is given by

$$t_r = \frac{15V}{\text{Slew Rate}} = \frac{15V}{0.5V/\mu\text{sec}}$$

$$t_r = 30\,\mu\text{sec}$$

The schematic of a pulse generator is shown in Figure 43. A diode has been added (CR_1) to allow separating the charge path to C_1 (via R_1)

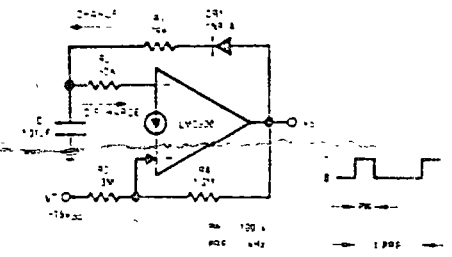


FIGURE 43. A Pulse Generator

from the discharge path (via R_2). The circuit operates as follows: assume first that the output voltage has just switched low (and we will neglect the current flow through R_4). The voltage across C_1 is high and the magnitude of the discharge current (through R_2) is given by

$$I_{Discharge} \cong \frac{V_{C_1} - V_{BE}}{R_2}$$

This current is larger than that entering the (-) input which is given by

$$I_{R_3} = \frac{V^+ - V_{BE}}{R_3}$$

The excess current entering the (-) input terminal causes the amplifier to be driven to a low output voltage state (saturation). This condition remains for the long time interval (Pulse Repetition Frequency) during which R_2C_1 discharge current equals the I_{R_3} value (as CR_1 is OFF during this interval). The voltage across C_1 at the trip point V_L is given by

$$V_L = (I_{R_3})(R_2),$$

or

$$V_L = (V^+ - V_{BE})\left(\frac{R_2}{R_3}\right) \qquad (1)$$

At this time the output voltage will switch to a high state V_{OH}, and the current entering the (-) input will increase to

$$I_M^+ = \frac{V^+ - V_{BE}}{R_3} + \frac{V_{OH_1} - V_{BE}}{R_4}$$

Also CR_1 goes ON and the capacitor, C_1 charges via R_1. Some of this charge current is diverted via R_2 to ground (the (-) input is at $V_{CE_{SAT}}$ during this interval as the current mirror is demanding more current than the (-) input terminal can provide). The high trip voltage V_H is given by

$$V_H = (I_M^+)\,R_2 \quad \text{or}$$

$$V_H = \left(\frac{V^+ - V_{BE}}{R_3} + \frac{V_{OH_1} - V_{BE}}{R_4}\right) R_2. \qquad (2)$$

A design proceeds by first choosing the trip points for the voltage across C_1. The resistors R_3 and R_4 are used only for this trip voltage control. The resistor R_2 affects the discharge time (the long interval) and also both of the trip voltages so this resistor is determined first from the required pulse repetition frequency (PRF). The value of R_2 is determined by the RC exponential discharge from V_H to V_L as this time interval T_1 controls the PRF (T_1 = 1/PRF). If we start with the equation for the RC discharge we have

$$V_L = V_H\, e^{-\frac{T_1}{R_2C_1}}$$

or

$$\ln \frac{V_L}{V_H} = -\frac{T_1}{R_2C_1}$$

or

$$T_1 = R_2C_1 \ln \frac{V_H}{V_L} \qquad (3)$$

To provide a low duty cycle pulse train we select small values for both V_H and V_L (such as 3V and 1.5V) and choose a starting value for C_1. Then R_2 is given by

$$R_2 = \frac{T_1}{C_1 \ln \frac{V_H}{V_L}}. \qquad (4)$$

If R_2 from (4) is not in the range of approximately 100 kΩ to 1 MΩ, choose another value for C_1. Now equation (1) can be used to find a value for R_3 to provide the V_L which was initially assumed. Similarly equation (2) allows R_4 to be calculated. Finally R_1 is determined by the required pulse width (PW) as the capacitor C_1 must be charged from V_L to V_H by R_1. This RC charging is given by (neglecting the loading due to R_2)

$$V_H \cong (V_{OH_1} - V_D)\left(1 - e^{-\frac{T_2}{R_1C_1}}\right)$$

or

$$T_2 \cong -R_1C_1 \ln\left[1 - \frac{V_H}{V_{OH_1} - V_D}\right], \text{ and finally}$$

$$R_1 \cong \frac{T_2}{-C_1 \ln\left[1 - \frac{V_H}{V_{OH_1} - V_D}\right]} \qquad (5)$$

where T_2 is the pulse width desired and V_D is the forward voltage drop across CR_1.

As a design example

Required: Provide a 100 μs pulse every 1 ms. The power supply voltage is ±15 V_{DC}.

1.0 Start by choosing V_L = 1.5V

and V_H = 3.0V

2.0 Find R_2 from equation (4) assuming C_1 = 0.01 μF.

$$R_2 = \frac{10^{-3}}{10^{-8} \ln\left(\frac{3.0}{1.5}\right)}$$

$$R_2 = \frac{10^5}{0.693} = 144\,\text{k}\Omega.$$

3.0 Find R_3 from equation (1)

$$R_3 = \frac{(V^+ - V_{BE})\,R_2}{V_L}$$

$$R_3 = \frac{(15 - 0.5)\,1.44 \times 10^5}{1.5}$$

$$R_3 = 1.39\,\text{M}\Omega$$

4.0 Find R_4 from equation (2).

$$R_4 = \frac{(V_{OH} - V_{BE})}{\frac{V_H}{R_2} - \frac{V^+ - V_{BE}}{R_3}}$$

$$R_4 = \frac{(14.2 - 0.5)}{\frac{3}{1.44 \times 10^5} - \frac{15 - 0.5}{1.39 \times 10^6}}$$

$$R_4 = 1.32\,\text{M}\Omega$$

5.0 Find R_1 from equation (5).

$$R_1 = \frac{10^{-4}}{-10^{-8} \ln\left(1 - \frac{3}{(14.2 - 0.7)}\right)}$$

$$R_1 = \frac{10^4}{-\ln\left(1 - \frac{3}{13.5}\right)}$$

$$R_1 = \frac{10^4}{0.252} = 39.7\,\text{k}\Omega.$$

These values (to the nearest 5% standard) have been added to Figure 43.

7.4 Triangle Waveform Generator

Triangle waveforms are usually generated by an integrator which receives first a positive DC input voltage then a negative DC input voltage. The LM3900 easily provides this operation in a system which operates with only a single power supply voltage by making use of the current mirror which exists at the (+) input. This allows the generation of a triangle waveform without requiring a negative DC input voltage.

The schematic diagram of a triangle waveform generator is shown in Figure 44. One amplifier

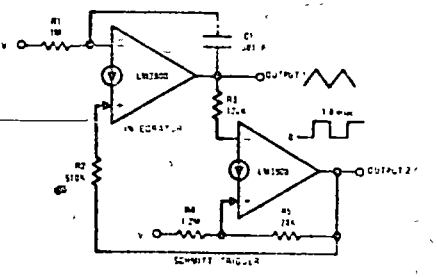


FIGURE 44. A Triangle Waveform Generator

is doing the integration by operating first with the current through R_1, to produce the negative output voltage slope, and then when the output of the second amplifier (the Schmitt-Trigger) is high, the current through R_2 causes the output voltage to increase. If $R_1 = 2R_2$, the output waveform will have good symmetry. The timing for one-half of the period (T/2) is given by

$$\frac{T}{2} = \frac{(R_1C_1)\,\Delta V_O}{V^+ - V_{BE}}$$

or the output frequency becomes

$$f_o = \frac{V^+ - V_{BE}}{2R_1C_1\,\Delta V_O}$$

where we have assumed $R_1 = 2R_2$. V_{BE} is the DC voltage at the (-) input (0.5 V_{DC}) and ΔV_O

...he difference between the two points of the ...m a Trigger. The design of the Schm... ...gger has been presented in the section on ...ital and Switching Circuits. With and the ...e voltages control the peak-to-peak excursion of the triangle output voltage waveform ...e output of the Schmitt circuit provides a ...uarewave of the same frequency.

...5 Sawtooth Waveform Generator

...e previously described triangle waveform ...nerator (Figure 44) can be modified to pro...ce a sawtooth waveform. Two types of ...veforms can be provided, both a positive ...mp and a negative ramp sawtooth waveform ... selecting R_1 and R_2. The reset time is also ...ntrolled by the ratio of R_1 to R_2. For example ... $R_1 = 10\ R_2$, a positive ramp sawtooth results ...d if $R_2 = 10\ R_1$, a negative ramp sawtooth ...n be obtained. Again, the slew rate limits of ...e amplifier (0.5V/μs) will limit the minimum ...race time, and the increased slew rate of a ...gative going output will allow a faster re...ce for a positive ramp sawtooth waveform.

... provide a gated sawtooth waveform, the cir...its shown in Figure 45 can be used. In Fig...e 45(a), a positive ramp is generated by inte...rating the current I which is entering the (-) ...ut. Reset is provided via R_1 and CR_1 keeps ... from loading at the (-) input during the ...eep interval. This will sweep from $V_{O\ MIN}$ ... $V_{O\ MAX}$ and will reset at ... discharge of the output (see Figure 45(b)). ... generate a negative ramp from $V_{O\ MAX}$ ... $V_{O\ MIN}$.

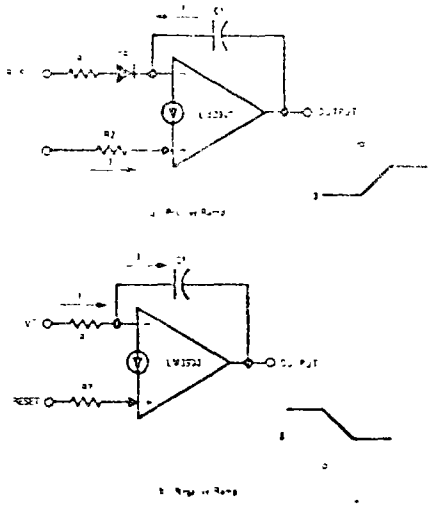


FIGURE 45. Gated Sawtooth Generators

7.5.1 Generating a Very Slow Sawtooth Waveform

The LM3900 can be used to generate a very slow sawtooth waveform which can be used to generate long time delay intervals. The circuit is shown in Figure 46 and uses four amplifiers. Amp 1 is ... encoded to increase the gain of the integrator and the output is the desired very slow sawtooth waveform. Amp 3 is used to exactly supply the bias current to Amp 1.

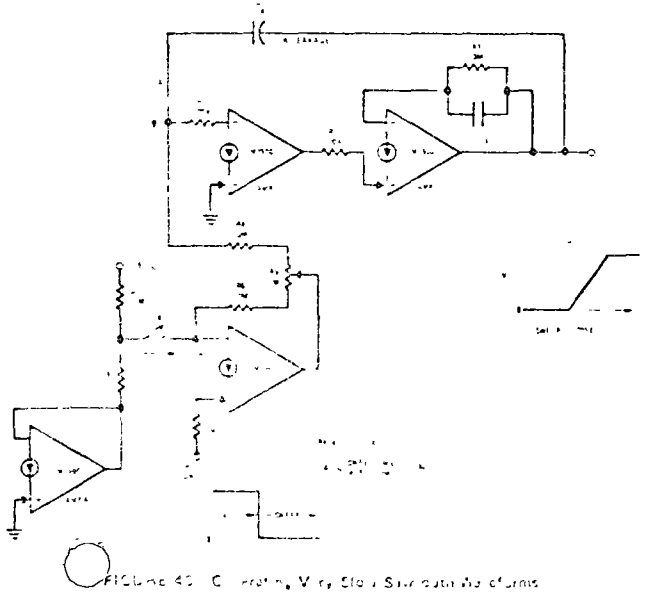


FIGURE 46. Generating Very Slow Sawtooth Waveforms

With resistor R_8 opened (...) and the reset control at zero volts, the potentiometer R_5 is adjusted to minimize the drift in the output voltage of Amp 2 (this output must be kept in the linear range to insure that Amp 2 is not in saturation). Amp 4 is used to provide a bias reference which equals the DC voltage at the (-) input of Amp 3. The resistor divider R_7 and R_9 provides a 0.1 V_{DC} reference voltage across R_9 which also appears across R_8. The current which flows through R_8 ... enters the (-) input of Amp 3 and causes the current through R_5 to drop by this amount. This causes an imbalance as now the current flow through R_4 is no longer adequate to supply the input current of Amp 1. The net result is that this same current I, is drawn from capacitor C_1 and causes the output voltage of Amp 2 to sweep slowly positive. As a result of the high impedance values used, the PC component board used for this circuit must first be cleaned and then coated with silicone rubber to eliminate the effects of leakage currents across the surface of the board. The DC leakage currents of the capacitor C_1 must also be small compared to the 10 nA charging current. For example, an insulation resistance of 100,000 MΩ will leak 0.1 nA with 10 V_{DC} across the capacitor and this leakage rapidly increases at higher temperatures. Dielectric polarization of the dielectric material may not cause problems if the circuit is not rapidly cycled. The resistor R_8, and the capacitor, C_1 can be scaled to provide other basic sweep rates. For the values shown on Figure 46 the 10 nA current and the 1μF capacitor establish a sweep rate of 100 sec/volt. The reset control pulse (Amp 3 (-) input) causes Amp 3 to go to the positive output saturation state and the 10 MΩ (R_4) gives a reset rate of 0.7 sec/volt. The resistor R_1 prevents a large discharge current of C_1 from overdriving the (-) input and overloading the input clamp device. For larger charging currents a resistor divider can be placed from the output of Amp 4 to ground and R_8 can tie from this tap point directly to the (-) input of Amp 1.

7.6 Staircase Waveform Generators

A staircase generator can be realized by supplying pulses to an integrator circuit. The LM3900 also can be used with a square wave input signal and a differentiating network. With each transition of the input square wave causes a step in the output waveform (or two steps per input cycle). This is shown in Figure 47. These pulses of current are the charge and discharge currents of the input capacitor C_1. The charge current, I_C, enters the (-) input and is mirrored about ground and is directed into the (+) input. The discharge current I_D is ... through the diode at the input (CR_1 ...) and also causes a step on the output staircase.

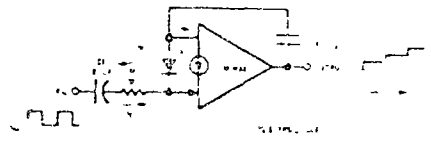


FIGURE 47. Pumping the Staircase Via Input Differentiator

A free running staircase generator is shown in Figure 48. This uses all four of the amplifiers which are available in one LM3900 package.

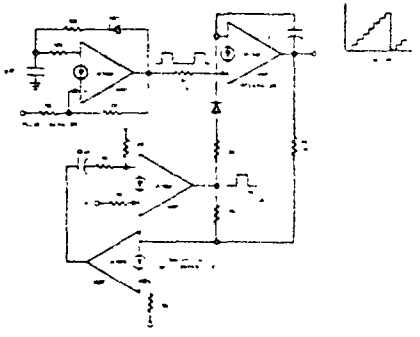


FIGURE 48. A Free Running Staircase Generator

Amp 1 provides the input pulses which 'pump up' the staircase via resistor R_1 (see section 7.3 for the design of this pulse generator). Amp 2 does the integrate and hold function and also supplies the output staircase waveform. Amps 3 and 4 provide both a compare and a one-shot multivibrator function (see the section on Digital and Switching Circuits for the design of this dual function one-shot). Resistor R_4 is used to sample the staircase output voltage and to compare it with the power supply voltage (V^+) via R_3. When the output exceeds approximately 60% of V^+ the connection of Amps 3 and 4 cause a 100 μsec reset pulse to be generated. This is coupled to the integrator (Amp 2) via R_2 and causes the staircase output voltage to fall to approximately zero volts. The next pulse out of Amp 1 then starts a new stepping cycle.

7.7 A Pulse Counter and a Voltage Variable Pulse Counter

The basic circuit of Figure 48 can be used as a pulse counter simply by omitting Amp 1 and feeding input voltage pulses directly to R_1. A simpler one-shot comparator which requires only one amplifier can also be used in place of Amps 3 and 4 (again see the section on Digital and Switching Circuits). To extend the time interval between pulses, an additional amplifier can be used to supply base current to

Amp 2 to eliminate any tendency for the output voltage to drift because of the 30 nA input current (see section 7.5.1). The pulse count can be made voltage variable simply by removing the comparator reference (R_3) from V^+ and using this as a control voltage input. Finally, the input could be derived from differentiating a squarewave input as was shown in Figure 47 and if only one step per cycle were desired the diode (CR_1 of Figure 47) can be eliminated.

7.8 An Up-down Staircase Waveform Generator

A staircase waveform which first steps up and then steps down is provided by the circuit shown in Figure 49. An input pulse generator

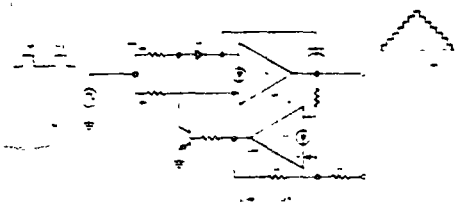


FIGURE 49. An Up-down Staircase Generator

provides the pulses which cause the output to step up or down depending on the conduction of the clamp transistor Q_1. When this is ON the down current pulse is diverted to ground and the staircase then steps up. When the upper voltage trip point of Amp 2 (Schmitt-Trigger—see section on Digital and Switching Circuits) is reached Q_1 goes OFF and as a result of the smaller down input resistor (one-half the value of the up resistor R_1) the staircase steps down to the low voltage trip point of Amp 2. The output voltage therefore steps up and down between the trip voltages of the Schmitt-Trigger.

8.0 DESIGNING PHASE LOCKED LOOPS AND VOLTAGE CONTROLLED OSCILLATORS

The LM3900 can be connected to provide a low frequency (f < 10 kHz) phase-locked loop (PL^2). This is a useful circuit building block for many applications. Tracking filters, FM demodulators, FM modulators and demodulators are applications of a PL^2.

8.1 Voltage Controlled Oscillators (VCO)

The heart of a PL^2 is the voltage controlled oscillator (VCO). As the PL^2 can be used for many functions the required linearity of the transfer characteristic (frequency out to DC voltage in) depends upon the application. For low distortion demodulation of an FM signal a high degree of linearity is necessary whereas a tracking filter application would not require this performance in the VCO.

A VCO circuit is shown in Figure 50. Only two amplifiers are required: one is used to integrate the DC input control voltage V_C and the other is connected as a Schmitt-trigger which monitors the output of the integrator. The trigger circuit is used to control the clamp transistor Q_1. When Q_1 is conducting the input current, I_2 is shunted to ground. During this one-half cycle the input current, I_1 causes the output voltage of the integrator to ramp down. At the minimum point of the triangle waveform (output 1) the Schmitt circuit changes state and transistor Q_1 goes OFF. The current I_2 is exactly twice the value of I_1 ($R_2 = R_1/2$) such that a charge current (which is equal to the magnitude of the discharge current) is drawn through the capacitor C to provide the increasing portion of the triangular waveform (output 1).

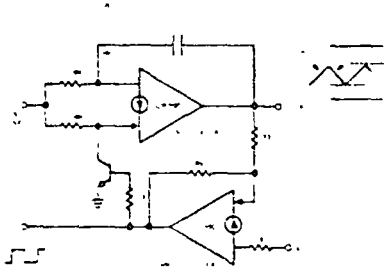


FIGURE 50. A Voltage Controlled Oscillator

The output frequency for a given DC input control voltage depends on the trip voltages of the Schmitt circuit (V_H and V_L) and the components R_1 and C_1 (as $R_2 = R_1/2$). The time to ramp down from V_H to V_L corresponds to one-half the period (T) of the output frequency and can be found by starting with the basic equation of the integrator

$$V_O = -\frac{1}{C}\int I_1\,dt \qquad (1)$$

as I_1 is a constant (for a given value of V_C) which is given by

$$I_1 = \frac{V_C - V_{BE}}{R_1} \qquad (2)$$

Equation (1) simplifies to

$$\Delta V_O = -\frac{I_1}{C}(\Delta t)$$

or

$$\frac{\Delta V_O}{\Delta t} = -\frac{I_1}{C} \qquad (3)$$

Now the time, Δt, to sweep from V_H to V_L becomes

$$\Delta t_1 = \frac{(V_H - V_L)C}{I_1} \quad \text{or}$$

$$T = \frac{2(V_H - V_L)C}{I_1} \quad \text{and}$$

$$f = \frac{1}{T} = \frac{I_1}{2(V_H - V_L)C} \qquad (4)$$

Therefore, once V_H, V_L, R_1 and C are fixed in value, the output frequency f is a linear function of I_1 (as desired for a VCO).

The circuit shown in Figure 50 will require $V_C > V_{BE}$ to oscillate. A value of $V_C = 0$ provides $f_{OUT} = 0$, which may or may not be desired. Two common-mode input biasing resistors can be added as shown in Figure 51 to allow $f_{OUT} = f_{MIN}$ for $V_C = 0$. In general if these resistors are a factor of 10 larger than their corresponding resistor (R_1 or R_2) a large control frequency ratio can be realized. Actually V_C could range outside the supply voltage limit of V^+ and this circuit will still function properly.

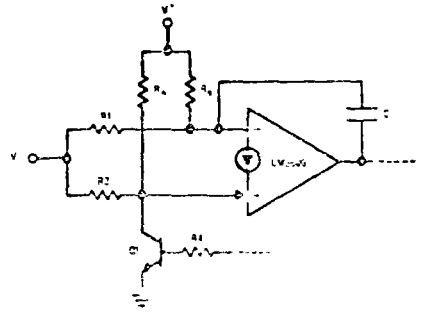


FIGURE 51. Adding Input Common-mode Biasing Resistors

The output frequency of this circuit can be increased by reducing the peak-to-peak excursion of the triangle waveform (output 1) by design of the trip points of the Schmitt circuit.

A limit is reached when the triangular sweep output waveform exceeds the slew rate limit of the LM3900 (0.5V/μs). Note that the output of the Schmitt circuit has to move up only one V_{BE} to bring the clamp transistor Q_1 ON and therefore output slew rate of this circuit is not a limit.

To improve the temperature stability of the VCO a PNP emitter follower can be used to give approximate compensation for the V_{BE}'s at the inputs to the amplifier (see Figure 52). Finally to improve the mark to space ratio accuracy over temperature and at low control voltages an additional amplifier can be added such that both reference currents are applied to

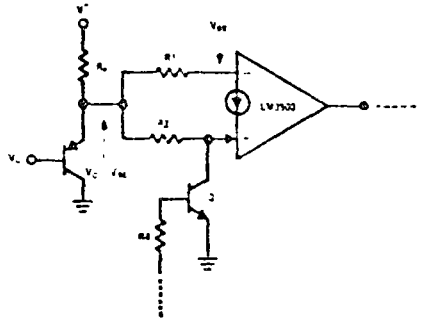


FIGURE 52. Reducing Temperature Drift

the same type of (inverting) inputs of the LM3900. The circuit to accomplish this is shown within dotted lines in Figure 53.

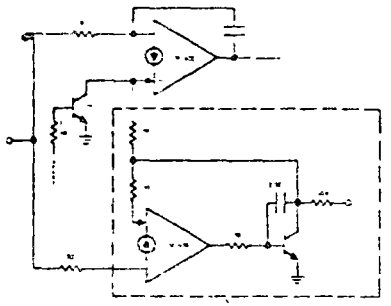


FIGURE 53. Improving Mark/Space Ratio

8.2 Phase Comparator

A basic phase comparator is shown in Figure 54. This circuit provides a pulse-width modulated output voltage waveform V_O[1] which must be filtered to provide a DC output voltage (this filter can be the same as the one needed in the PL^2). The resistor R_2 is made smaller than R_1 so the (+) input serves to maintain the (-) ...

...nal. The center of the dynamic range is indicated by the waveforms shown on the figure (0° phase difference between f_{IN} and f_{VCO})

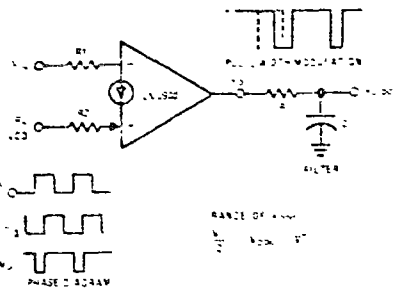


FIGURE 54 Phase Comparator

...e filtered DC output voltage will center at ...4 and can range from V⁺/2 to V⁺ as the ...ase error ranges from 0 degrees to 180 ...grees

8 A Complete Phase-locked Loop

...phase-locked loop can be realized with three ... the amplifiers as shown in Figure 55 This ...s a center frequency of approximately 3 kHz

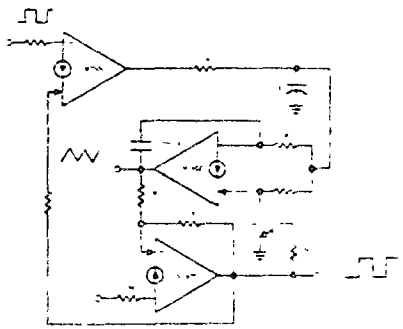


FIGURE 55 A Phase-locked Loop

... increase the lock range DC gain can be ...ded at the input to the VCO by using the ...rth amplifier of the LM3900 If the gain is ...ering the limited DC dynamic range out of ... phase detector can be increased to improve ... frequency lock range With lowering gain ... input to the VCO could go to zero volts ...s will cause the output of the VCO to go high ... and will latch if applied to the (+) input of ... phase comparator Therefore apply the ...O signal to the (-) input of the phase compar... ...ts or add the components shown in the ... of Figure 54

8.4 Conclusions

One LM3900 package (4 amplifiers) can provide all of the operations necessary to make a phase-locked loop In addition a VCO is a generally useful component for other system applications

9.0 DESIGNING DIGITAL AND SWITCHING CIRCUITS

The amplifiers of the LM3900 can be overdriven and used to provide a large number of low speed digital and switching circuit applications for control systems which operate off of single power supply voltages larger than the standard +5 V_{DC} digital limit The large voltage swing and slower speed are both advantages for most industrial control systems Each amplifier of the LM3900 can be thought of as "a super transistor" with a β of 1 000 000 (25 nA input current and 25 mA output current) and with a non-inverting input feature In addition the active pull-up and pull-down which exists at the output will supply larger currents than the simple resistor pull-ups which are used in digital logic gates Finally the low input currents allow timing circuits which minimize the capacitor values as large impedance levels can be used with the LM3900

9.1 An "OR" GATE

An OR gate can be realized by the circuit shown in Figure 56 A resistor (150 kΩ) from V⁺ to the (-) input keeps the output of the amplifier in a low voltage saturated state for all inputs A, B and C at 0V If any one of the input signals were to go high (≅V⁺) the current flow through the 75 kΩ input resistor will cause the amplifier to switch to the positive output saturation state ($V_O \cong V^+$) The current loss through the other input resistors (which have an input in the low voltage state) represents an insignificant amount of the total input current which is provided by the at least one high voltage input More than three inputs can be OR'ed if desired

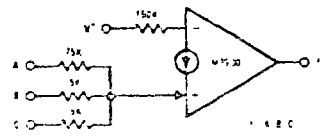


FIGURE 56 An OR Gate

The "fan-out" or logical drive capability is large (50 gates if each gate input has a 75 kΩ resistor) due to the 10 mA output current capability of the LM3900 An OR gate can be obtained by inverting the inputs to the LM3900

9.2 An "AND" Gate

A three input AND gate is shown in Figure 57 This gate requires all three inputs to be high in order to have sufficient current entering the (+) input to cause the output of the amplifier to switch high The addition of R_2 causes a smaller current to enter the (+) input when only two of the inputs are high (A two input AND gate would not require a resistor as R_2) More than three inputs becomes difficult with this resistor summing approach as the (+) input is too close to having the necessary current to switch just prior to the last input going high For a larger fan-in an input diode network (similar to DTL) is recommended as shown in Figure 58 Interchange the inputs for a NAND gate

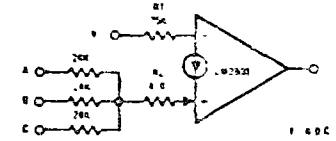


FIGURE 57. An "AND" Gate

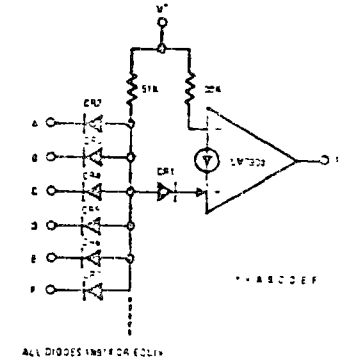


FIGURE 58 A Large Fan-in "AND" Gate

9.3 A Bi-stable Multivibrator

A bi-stable multivibrator (an asynchronous RS flip-flop) can be realized as shown in Figure 59 Positive feedback is provided by resistor R_4 which causes the latching A positive pulse at the set input causes the output to go high and a reset positive pulse will return the output to essentially 0V

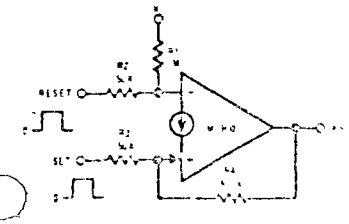


FIGURE 59 A Bi-stable Multivibrator

9.4 Trigger Flip Flops

Trigger flip flops are useful to divide an input frequency as each input pulse will cause the output of a trigger flip flop to change state Again due to the absence of a clocking signal input this is for an asynchronous logic application A circuit which uses only one amplifier is shown in Figure 60 Steering of the differentiated positive input trigger is provided by the diode CR2 For a low output voltage state,

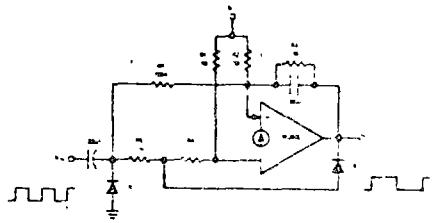


FIGURE 60. A Trigger Flip Flop

CR2 shunts the trigger away from the (-) input and resistor R_3 couples this positive input trigger to the (-) input terminal This causes the output to switch high The high voltage output state now keeps CR2 OFF and the smaller value of (R_5 + R_6) compared with R_3 causes a larger positive input trigger to be coupled to the (-) input which causes the output to switch to the low voltage state

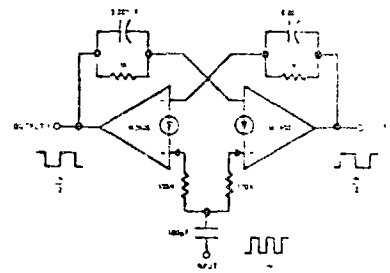


FIGURE 61 A Two-amplifier Trigger Flip Flop

A second trigger flip flop can be made which consists of two amplifiers and also provides a complimentary output This connection is shown in Figure 61

9.5 Monostable Multivibrators (One shots)

Monostable multivibrators can be ... using one or two of the amplifiers of the LM3900 In addition the output can be designed to be

either high or low in the quiescent state. Further, to increase the versatility, a one-shot can be designed which triggers on a particular DC input voltage level to save the cost/size of providing first a comparator and then a pulse generator.

9.5.1 A Two-amplifier One-shot

A circuit for a two-amplifier one-shot is shown in Figure 62. As the resistor R_2 from V^+ to the (+) input is smaller than R_3 from V^+ to the (−) input, amplifier 2 will be biased to a low-voltage output in the quiescent state. As a

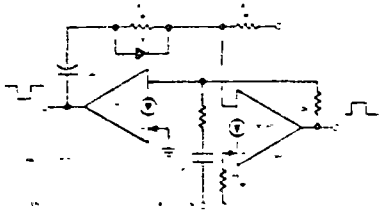


FIGURE 62. A One-Shot Multivibrator

result, no current is supplied to the (−) input of amplifier 1 (via R_3) which causes the output of this amplifier to be in the high voltage state. Capacitor C_1 therefore has essentially the full V^+ supply voltage across it ($V^+ - 2V_{BE}$). Now when a differentiated trigger due to C_2 causes amplifier 1 to be driven OIK (output voltage drops to essentially zero volts) this negative transient is coupled (via C_1) to the (−) input of amplifier 2 which causes the output of this amplifier to be driven high (to positive saturation). This condition remains while C_1 discharges via (R_1) from approximately V^+ to approximately $V^+/2$. This time interval is the pulse width (PW). After C_1 no longer delivers sufficient current of R_2 away from the (−) input of amplifier 2, or C_1 is discharged to approximately $V^+/2$, the stable DC state is re-established (amplifier 2 output low and amplifier 1 output high).

This circuit can be rapidly retriggered due to the action of the diode CR_1. This re-charges C_1 as amplifier 1 drives full output current capability (approximately 10 mA) through C_1, CR_1, and into the saturated (−) input of amplifier 2 to ground. The only time limit is the 10 mA available from amplifier 1 and the value of C_1. If a rapid reset is not required, CR_1 can be omitted.

9.5.2 A Combination One-shot/Comparator Circuit

In many applications a pulse is required [illegible]

value. This exists in free-running oscillators where after a particular output level has been reached a reset pulse must be generated to recycle the oscillator. This double function is provided with the circuit of Figure 63. The

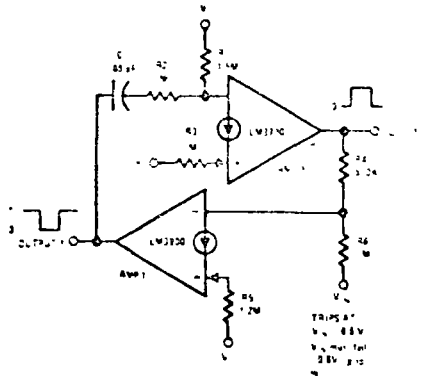


FIGURE 63. A One-shot Multivibrator with an Input Comparator

resistors R_5 and R_6 of amplifier 1 provide the inputs to a comparator and, as shown, an input signal V_{IN} is compared with the supply voltage V^+. The output voltage of amplifier 1 is normally in a high voltage state and will fall and initiate the generation of the output pulse when V_{IN} is R_6/R_5 V^+ or approximately 80% of V^+. To keep V_{IN} from disturbing the pulse generation it is required that V_{IN} fall to less than the trip voltage prior to the termination of the output pulse. This is the case when this circuit is used to generate a reset pulse and therefore this causes no problems.

9.5.3 A One-amplifier One-shot (Positive Pulse)

A one-shot circuit can be realized using only one amplifier as shown in Figure 64.

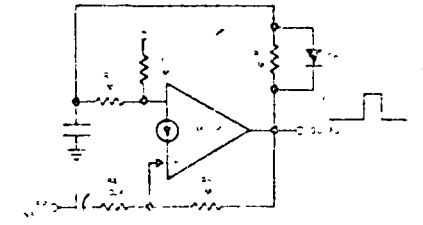


FIGURE 64. A One-amplifier One-shot (Positive Output)

The resistor R_2 keeps the output in the low voltage state. A differentiated positive trigger causes the output to switch to the high voltage state and resistor R_3 latches this state. The capacitor C_1 charges from essentially ground to approximately $V^+/2$ where the circuit latches back to the quiescent state. The diode CR_1 is used to allow a rapid re-triggering.

9.5.4 A One-amplifier One-shot (Negative Pulse)

A one-amplifier one-shot multivibrator which has a quiescent state with the output high and which falls to zero volts for the pulse duration is shown in Figure 65.

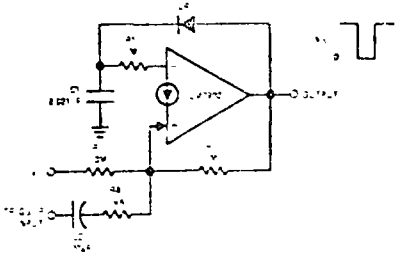


FIGURE 65. A One-amplifier One-shot (Negative Output)

The sum of the currents through R_2 and R_3 keeps the (−) input at essentially ground. This causes V_O to be in the high voltage state. A differentiated negative trigger waveform causes the output to switch to the low voltage state. The large voltage across C_1 now provides input current via R_1 to keep the output low until C_1 is discharged to approximately $V^+/10$. At this time the output switches to the stable high voltage state.

If the R_4 C_2 network were moved to the (−) input terminal, the circuit will trigger on a differentiated positive trigger waveform.

9.6 Comparators

The voltage comparator is a function required for most system operations and can easily be performed by the LM3900. Both an inverting and a non-inverting comparator can be obtained.

9.6.1 A Comparator for Positive Input Voltages

*The circuit in Figure 66 is an inverting [illegible]

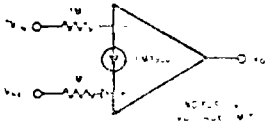


FIGURE 66. An Inverting Voltage Comparator

[illegible] must be high to V_{BE} but it is not critical. This [illegible] large enough to guarantee that [illegible] not exceed 200 µA.

9.6.2 A Comparator for Negative Input Voltages

Adding a common-mode biasing network to the comparator in Figure 66 makes it possible to compare voltages between zero and V^+ as well as the comparison of referenced negative voltages. Figure 67. When comparing negative voltages the current supplied by the common-mode network must be large enough to satisfy both the current drain demands of the input voltages and the bias current requirement of the amplifier.

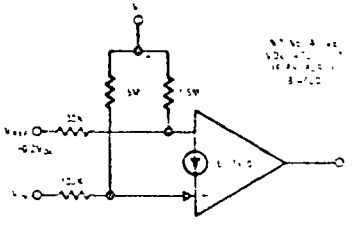


FIGURE 67. A Non-inverting Low-voltage Comparator

9.6.3 A Power Comparator

When used in conjunction with an external transistor, this power comparator will drive loads which require more current than the IC amplifier is capable of supplying. Figure 68 shows a non-inverting comparator which is capable of driving a 12V, 40 mA pane lamp.

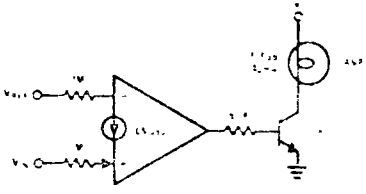


FIGURE 68. A Non-inverting Power Comparator

9.6.4 A [illegible]

A more precise comparator can be obtained by using a second amplifier such that the input voltages of the same type of input are compared. The input voltages of the [illegible] are nearly more closely matched and track well with temperature changes. Comparator of Figure 66 uses this [illegible]

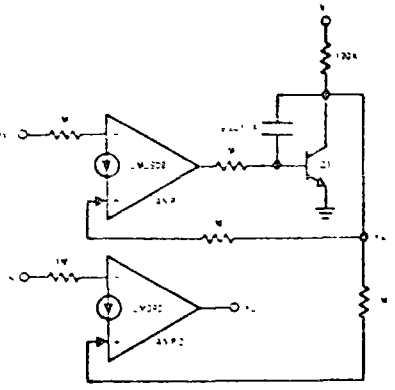


FIGURE 69. A More Precise Comparator

e current established by V_{REF} at the invert- input of amplifier 1 will cause transistor to adjust the value of V_A to supply this rent. This value of V_A will cause an equal rent to flow into the non-inverting input of plifier 2. This current corresponds more ctly to the reference current of amplifier 1.

differential input stage can also be added the LM3900 (see section 10.16) and the re- ing circuit can provide a precision compar- r circuit.

Schmitt-Triggers

steresis may be designed into comparators ch use the LM3900 as shown in Figure 70.

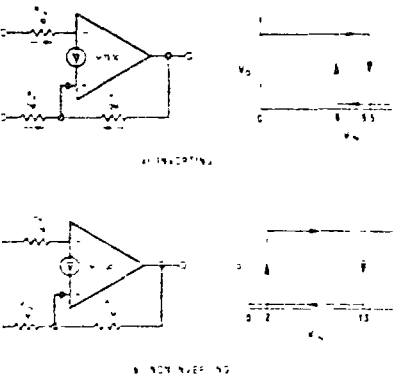


FIGURE 70. Schmitt Triggers

lower switch point for the inverting -Trigger is determined by the amount of ing into the positive input and the voltage level. The input current I_3 prior required by the current mirror the output will switch to the high limit. With V_O high the current demanded by the mirror is increased by a fixed amount I_2. As a result the I_3 required to switch the output increases this same amount. Therefore the switch points are determined by selecting resistors which will establish the required currents at the desired input voltages. Reference current (I_1) and feedback current (I_2) are set by the following equation:

$$I_1 = \frac{V^+ - 0}{R_B}$$

$$I_2 = \frac{V_{O\,MAX} - 0}{R_F}$$

By adjusting the values of R_B, R_F, and R_{IN} the switching values of V_{IN} may be set to any levels desired.

The non-inverting Schmitt-Trigger works in the same way except that the input voltage is applied to the (-) input. The range of V_{IN} may be very large when compared with the operating voltage of the amplifier.

10.0 SOME SPECIAL CIRCUIT APPLICATIONS

This section contains various special circuits which did not fit the order of things or which are one-of-a-kind type of applications.

10.1 Current Sources and Sinks

The amplifiers of the LM3900 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks. These can be multiple sources or single sources which are fixed in value or made voltage variable.

10.1.1 A Fixed Current Source

A multiple fixed current source is provided by the circuit of Figure 71. A reference voltage of V_{BE} is established across resistor R_3 by the resistive divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to also be 1 V_{BE}. This controls the emitter current of transistor Q_1 and if we neglect the small current supplied to the (-) input via the input resistor (10 kΩ) and the base current of Q_1 and Q_2 (which is the 2% loss if the β of these transistors is 100), essentially this same current is available out of the collector of Q_1.

Larger input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

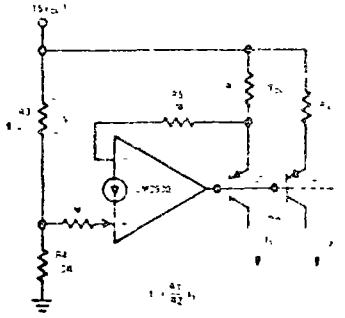


FIGURE 71. Fixed Current Sources

The resistor R_2 can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

10.1.2 A Voltage Variable Current Source

A voltage variable current source is shown in Figure 72. The transconductance is $-(1/R_2)$ as the voltage gain from the input terminal to the emitter of Q_1 is -1. For a V_{IN} = 0 V_{DC} the output current is essentially zero mA DC. The resistors R_1 and R_5 guarantee that the amplifier can turn OFF transistor Q_1.

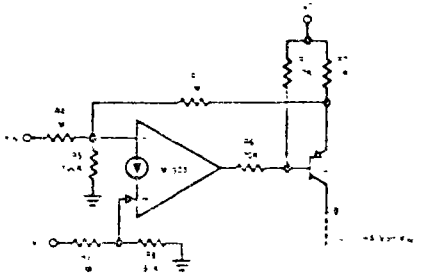


FIGURE 72. A Voltage Controlled Current Source

10.1.3 A Fixed Current Sink

Two current sinks are shown in Figure 73. The circuit of Figure 73a establishes a 1 mA reference and supplies an output current which is directly proportional to this 1 mA value. A negative temperature coefficient will result due to the 0.5 V_{DC} reference being the base-emitter junction voltage of the (-) input transistor. If temperature stability is required, the circuit of Figure 73b can be employed.

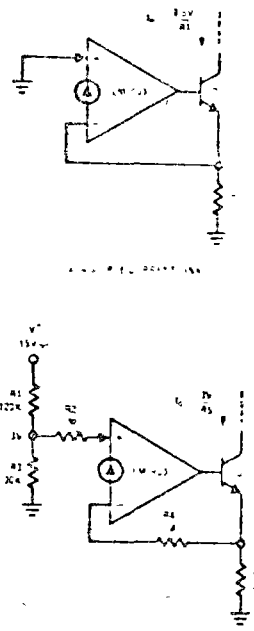


FIGURE 73. Fixed Current Sinks

10.1.4 A Voltage Variable Current Sink

A voltage variable current sink is shown in Figure 74. The output current is 1 mA per volt of V_{IN} (as R_5 = 1 kΩ and the gain is +1). This circuit provides approximately 0 mA output current for V_{IN} = 0 V_{DC}.

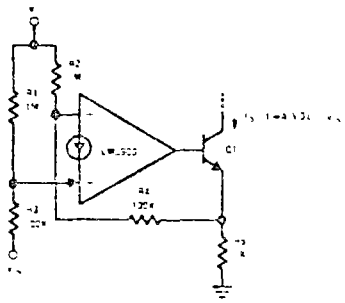


FIGURE 74. A Voltage Variable Current Sink

10.2 Operation From ±15 V_{DC} Power Supplies

If the ground pin (no. 7) is returned to a negative voltage and some changes are made in the biasing circuits, the LM3900 can be operated from ±15 V_{DC} power supplies.

10.2.1 An AC Amplifier Operating with ±15 V_{DC} Power Supplies

An AC coupled amplifier is shown in Figure 75. The biasing resistor R_B is now returned to ground and both inputs bias at one V_{BE} above the $-V_{EE}$ voltage (approximately −15 V_{DC}).

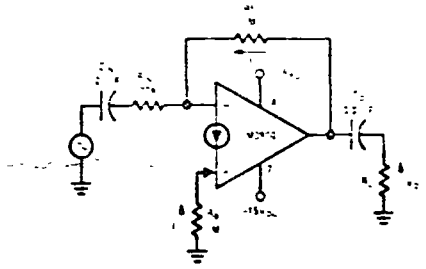


FIGURE 75. An AC Amplifier Operating with ±15 V_{DC}

With $R_f = R_B$, V_O will bias at approximately 0 V_{DC} to allow a maximum output voltage swing. As pin 7 is common to all four of the amplifiers and all are in the same package, the other amplifiers are also biased for operation off of ±15 V_{DC}.

10.2.2 A DC Amplifier Operating with ±15 V_{DC} Power Supplies

Biasing a DC amplifier is more difficult and requires that the ± power supplies be complementary tracking (i.e. $-V_{CC} = -V_{EE}$). The operation of this biasing can be easier understood if we start by first considering the amplifier without including the feedback resistors as shown in Figure 76. If $R_1 = R_2 = R_3 = R_4 = 1\ M\Omega$ and $-V_{CC} = -V_{EE}$, then the current

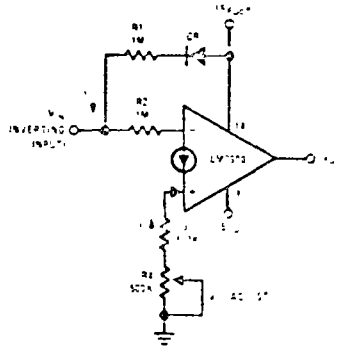


FIGURE 76. DC Biasing for the V_{IO} Operation

[illegible] $-V_{IO}$ [illegible] C_{IN} [illegible] R_{IN} [illegible]

been added for temperature compensation of this biasing. Now if we include these biasing resistors we have a DC amplifier with the input biased at approximately zero volts. If feedback resistors are added around this biased amplifier we get the schematic shown in Figure 77.

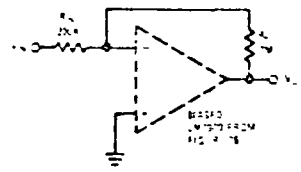


FIGURE 77. A DC Amplifier Operating with ± 15 V_{DC}

This is a standard inverting DC amplifier connection. The (+) input is "effectively" at ground and the biasing shown in Figure 76 is used to take care of DC levels at the inputs.

10.3 Tachometers

Many pulse averaging tachometers can be built using the LM3900. Inputs can be voltage pulses, current pulses or the differentiated transitions of squarewaves. The DC output voltage can be made to increase with increasing input frequency, can be made proportional to twice the input frequency (frequency doubling for reduced output ripple) and can also be made proportional to either the sum or the difference between two input frequencies. Due to the small bias current and the high gain of the LM3900, the transfer function is linear between the saturation states of the amplifier.

10.3.1 A Basic Tachometer

If an RC averaging network is added from the output to the (−) input, the basic tachometer of Figure 78 results. Current pulse inputs will provide the desired transfer function shown on the figure. Each input current pulse causes a small change in the output voltage. Neglecting the effects of R we have

$$\pm V_O \cong \frac{I_{in}\,t}{C}$$

The inclusion of R gives a discharge path so the output voltage [illegible] to integrate but rather produces the time dependency which is necessary to average the input pulses. If an additional signal source is simply placed in parallel with the one shown, the output becomes proportional to the sum of these input frequencies. If the additional source were applied to the [illegible] input, the output voltage would be proportional to the difference between these input frequencies. Voltage pulses can be converted to current pulses by using an input resistor. A [illegible] should be used if

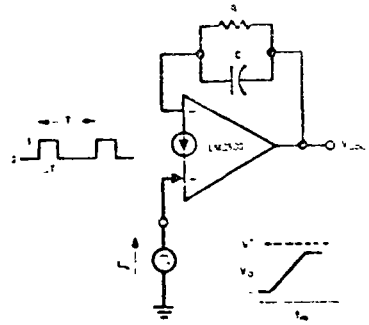


FIGURE 78. A Basic Tachometer

a signal is applied to the (−) input to prevent loading during the low voltage state of this input signal.

10.3.2 Extending V_{OUT} (Minimum) to Ground

The output voltage of the circuit of Figure 78 does not go to ground level but has a minimum value which is equal to the V_{BE} of the (−) input (0.5 V_{DC}). If it is desired that the output voltage go exactly to ground, the circuit of Figure 79 can be used. Now with $V_{IN} = 0\ V_{DC}$, $V_O = 0 V_{DC}$ due to the addition of the common-mode biasing resistors (180 kΩ). The diode

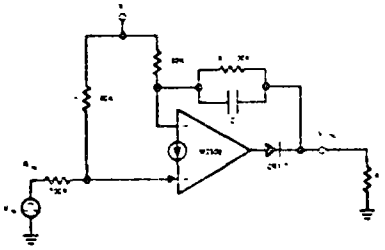


FIGURE 79. Adding Biasing to Provide $V_O = 0\ V_{DC}$

CR_1 allows the output to go below $V_{CE\ SAT}$ of the output if desired (a load is required to provide a DC path for the biasing current flow via the R of the averaging network).

10.3.3 A Frequency Doubling Tachometer

To reduce the ripple on the DC output voltage the circuit of Figure 80 can be used to effectively double the input frequency. Input pulses are not required, a square wave is all that is needed. The operation of the circuit is to average the charge and discharge transient currents of the input capacitor C_{IN}. The resistor R_{IN} is used to convert the voltage pulses to current pulses and to limit the surge currents (to approximately 200 μA peak or less if operating at high temperatures).

When the input voltage goes [illegible] current of C_{IN}, I_{CHARGE}, is [illegible] mirrored about ground and is drawn from the RC averaging network into the (−) input terminal. When the input voltage goes back to ground the discharge current of C_{IN}, $I_{DISCHARGE}$, will also be drawn from the RC averaging network via the now conducting diode CR_1. This full wave action causes two current pulses to be drawn through the RC averaging network for each cycle of the input frequency.

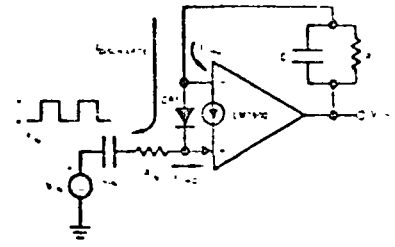


FIGURE 80. A Frequency Doubling Tachometer

10.4 A Squaring Amplifier

A squaring amplifier which incorporates symmetrical hysteresis above and below the zero output state (for noise immunity) is often needed to amplify the low level signals which are provided by variable reluctance transducers. In addition a high frequency, roll-off flow pass characteristic is desirable both to reduce the natural voltage buildup at high frequencies and to also filter high frequency input noise disturbances. A simple circuit which accomplishes this function is shown in Figure 81. The input

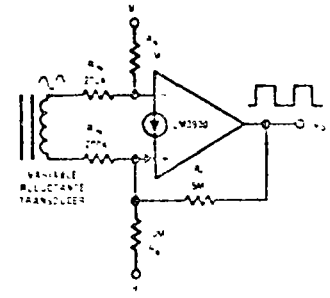


FIGURE 81. A Squaring Amplifier with Hysteresis

voltage is converted to input currents by using the input resistors R_{IN}. Common-mode biasing is provided by R_{B1} and R_{B2}. Finally positive feedback (hysteresis) is provided by R_f. The large source resistance R_{IN} provides a low pass filter due to the "Miller effect" input capacitance of the amplifier (approximately 0.03 μF). The amount of hysteresis and the [illegible] about the zero volt input are controlled by the positive feedback resistors R_f and R_{B1} and R_{B2}.

th the values shown in Figure 81 the two
tages are approximately ±150 mV centered
cut the zero output voltage state of the trans-
cer (at low frequencies where the low pass
er is not attenuating the input signal)

5 A Differentiator

input differentiating capacitor can cause the
ut of the LM3900 to swing below ground
d actuate the input clamp circuit Again
mmon-mode biasing can be used to prevent
s negative swing at the input terminals of the
3900 The schematic of a differentiator
cuit is shown in Figure 82 Common-mode

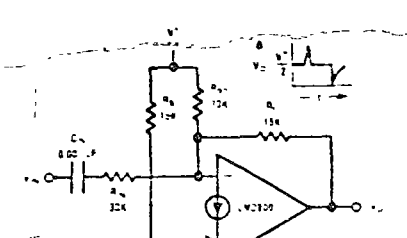


FIGURE 82. A Differentiator Circuit

asing is provided by R_{B1} and R_{B2} The feed-
ck resistor R_f is one-half the value of R_{IN}
the gain is −2 The output voltage will bias
$V^+/2$ which thereby allows both a positive
d a negative swing above and below this bias
int The resistor R_{IN} keeps the negative
ing isolated from the (−) input terminal and
erefore both inputs remain biased at $-V_{BE}$

6 A Difference Integrator

difference integrator is the basis of many of
sweep circuits which can be realized using
LM3900 operating on only a single power
ply voltage This circuit can also be used
provide the time integral of the difference
tween two input waveforms The schematic
the difference integrator is shown in Fig-
e 83

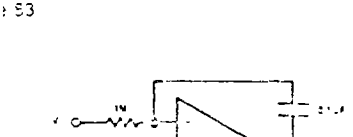


FIGURE 83 A Differentiator

10 7 A Low Drift Sample and Hold Circuit

In sample and hold applications a very low input biasing current is required This is usually achieved by using a FET transistor or a special low input current IC op amp The existance of many matched amplifiers in the same package allows the LM3900 to provide some interesting low equivalent input biasing current applications

10 7.1 Reducing the "Effective" Input Biasing Current

One amplifier can be used to bias one or more additional amplifiers as shown in Figure 84

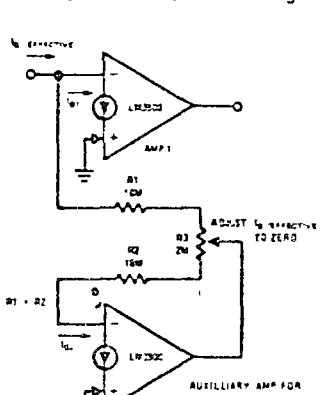


FIGURE 84 Reducing I_B "Effective" to Zero

The input terminal of Amp 1 will only need to supply the signal current if the DC biasing current I_{B_1} is accurately supplied via R_1 The adjustment R_3 allows a zeroing of I_B effective but simply omitting R_3 and letting $R_1 = R_2$ (and relying on amplifier symmetry) can cause I_B effective to be less than $I_B/10$ (3 nA) This is useful in circuit applications such as sample and hold where small values of I_B effective are desirable

10 7.2 A Low Drift Ramp and Hold Circuit

The input current reduction technique of the previous section allows a relatively simple ramp and hold circuit to be built which can be ramped up or down or allowed to remain at any desired input DC level in a hold mode This is shown in Figure 85 If both inputs are at 0 V_{DC} the circuit is in a hold mode Raising either input will cause the DC output voltage to ramp either up or down depending on which one is positive The slope is a function of the

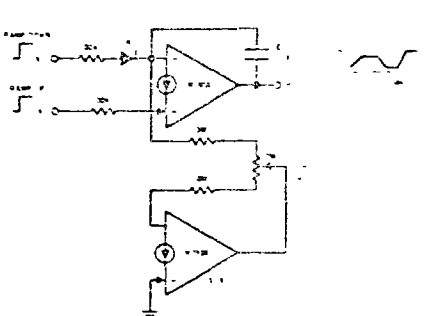


FIGURE 85 A Low-drift Ramp and Hold Circuit

10.7.3 Sample-hold and Compare with New $+V_{IN}$

An example of using the circuit of the previous section is shown in Figure 86 where clamping transistors Q_1 and Q_2 put the circuit in a hold mode when they are driven ON When OFF the output voltage of Amp 1 can ramp either up or down as needed to guarantee that the output voltage of Amp 1 is equal to the DC input voltage which is applied to Amp 3 Resistor R_1 provides a fixed down ramp current which is balanced or controlled via the comparator Amp 3 and the resistor R_4 When Q_1 and Q_2 are OFF a feedback loop guarantees that V_{01} (from Amp 1) is equal to $-V_{IN}$ (to Amp 3) Amplifier 2 is used to supply the input biasing current to Amp 1

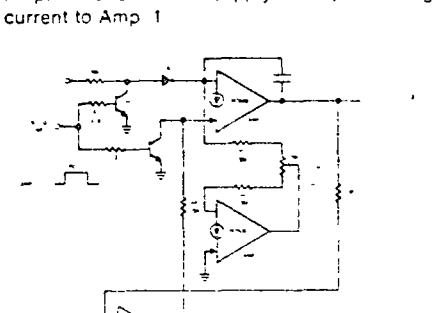


FIGURE 86 Sample-hold and Compare with New $+V_{IN}$

The stored voltage appears at the output V_{01} of Amp 1 and as Amp 3 is acting as a continued comparison is made between V_{01} and V_{IN} and the output of Amp 3 (V_{02}) is a measure of this comparison A second loop is used to cause V_{IN} to be maintained at the stored value (V_{01}) by making use of V_{02} as an error signal for this second loop Therefore a control system could be manually controlled to bring it to a particular operating condition then by exercising the control the system would maintain this operating condition due to the analog memory provided by V_{01}

10 8 Audio Mixer or Channel Selector

The multiple amplifiers of the LM3900 can be used for audio mixing (many amplifiers simultaneously providing signals which are added to generate a composite output signal) or for channel selection (only one channel enabled at a time) Three amplifiers are shown being summed into a fourth amplifier in Figure 87

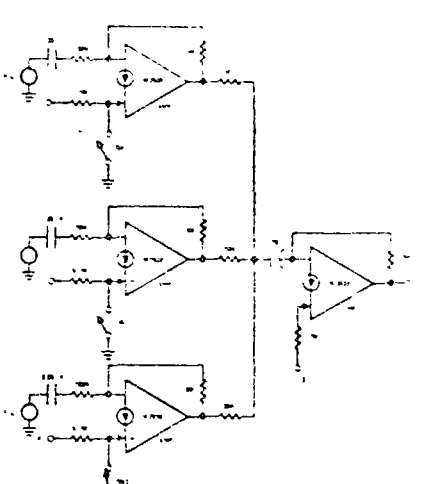


FIGURE 87 Audio Mixing or Selection

If a power amplifier were available all four amplifiers could feed the single input of the power amplifier For audio mixing all amplifiers are simultaneously active Particular amplifiers can be gated OFF by making use of DC control signals which are applied to the (+) inputs to provide a channel select feature As shown on Figure 87 Amp 3 is active (as sw 3 is closed) and Amps 1 and 2 are driven to positive output voltage saturation by the 5 V which is applied to the (+) inputs The DC output voltage bias level of the active amplifier is approximately 0 6 V_{DC} and could be raised if larger signal levels were to be accommodated Frequency shaping networks can be added either to the individual amplifiers or to the common amplifier as desired Switching transients may need to be filtered at the DC control points if the signal amplitudes present during

10 9 A Low Frequency Mixer

The diode which exists at the (+) input can be used for non-linear signal processing An example of this is a mixer which allows two audio frequencies to produce a sum and a difference frequency (in addition to other high frequency

configuration. Using the amplifier of the LM3900 gain and filtering can also be accomplished with the circuit. In addition to the high input impedance and low output impedance of an opamp. The schematic of Figure 88 shows a mixer with a gain of 10 and a low pass single pole filter (1M and 150 pF feedback elements) with a corner frequency of 1 kHz. With

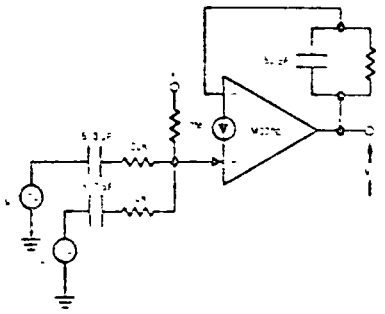


FIGURE 88 A Low Frequency Mixer

one signal larger in amplitude to serve as the local oscillator input (V_1) the transconductance of the input diode is gated at this rate (I_D). A smaller signal (V_2) can now be added at the second input and the difference frequency is filtered from the composite resulting waveform and is made available at the output. Relatively high frequencies can be applied at the inputs as long as the desired difference frequency is within the bandwidth capabilities of the amplifier and the RC low pass filter.

10.10 A Peak Detector

A peak detector is often used to rapidly charge a capacitor to the peak value of an input waveform. The voltage drop across the rectifying diode is placed within the feedback loop of an op amp to prevent voltage losses and temperature drifts in the output voltage. The LM3900 can be used as a peak detector as shown in Figure 89. The feedback resistor R_1 is kept

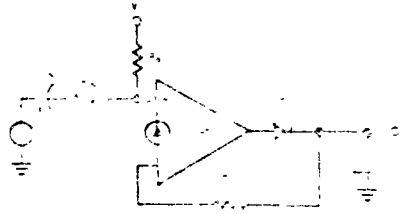


FIGURE 89 A Peak Detector

feedback resistor is constantly loading C in addition to the current drawn by the circuitry which samples V_O. These loading effects must be considered when selecting a value for C.

The biasing resistor R_B allows a minimum DC voltage to exist across the capacitor and the input resistor R_{IN} can be selected to provide gain to the input signal.

10.11 Power Circuits

The amplifier of the LM3900 will source a maximum current of approximately 10 mA and will sink maximum currents of approximately 80 mA (if overdriven at the (-) input). If the output is driven to a saturated state to reduce device dissipation some interesting power circuits can be realized. These maximum values of current are typical values for the unit operating at 25°C and therefore have to be derated for reliable operation. For fully switched operation amplifiers can be paralleled to increase current capability.

10.11.1 Lamp and/or Relay Drivers (≤ 30 mA)

Low power lamps and relays (as reed relays) can be directly controlled by making use of the larger value of sink current than source current. A schematic is shown in Figure 90 where the input resistor R is selected such that V_{IN} supplies at least 0.1 mA of input current.

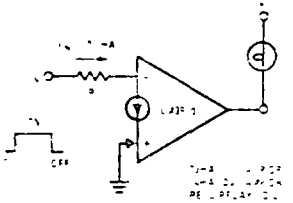


FIGURE 90 Sinking 20 to 30 mA Loads

10.11.2 Lamp and/or Relay Drivers (≤ 300 mA)

To [illegible] power capability an external [illegible] feedback [illegible] resistor [illegible] to the same power supply as the amplifier's Q to guarantee that Q_1 can be fully OFF. If an inductive load is used such as a relay coil a [illegible] should be added to prevent large inductive [illegible] when switching [illegible] ON [illegible]

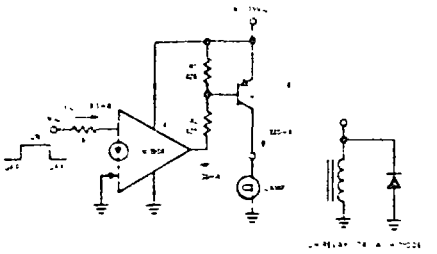


FIGURE 91 Boosting to 300 mA Loads

10.11.3 Positive Feedback Oscillators

If the LM3900 is biased into the active region and a resonant circuit is connected from the output to the (+) input a positive feedback oscillator results. A driver for a piezoelectric transducer (a warning type of noise maker) is shown in Figure 92. The resistors R_1 and R_2 bias the output voltage at $V^+/2$ and keep the amplifier active. Large currents can be entered into the (-) input and negative currents (or currents out of this terminal) are provided by the epi-substrate diode of the IC fabrication.

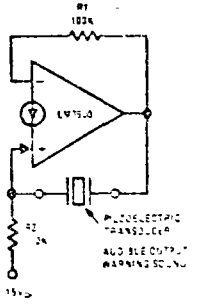


FIGURE 92 Positive Feedback Power Oscillators

When one of the amplifiers is operated in this large negative input current mode the other amplifiers will be disturbed due to interaction. Multiple sounds may be generated as a result of using two or more transducers in various combinations but this has not been investigated. Other two-terminal RC RLC or piezoelectric resonators can be connected in this circuit to produce an oscillator.

10.12 High [illegible]

The amplifiers of the LM3900 can drive an external high voltage NPN transistor to provide a large output voltage swing (as for an electrostatic CRT deflection system) or to operate off of an existing high voltage power supply (as the +50 V_{DC} required here). Examples of both types of circuits are presented in this section.

10.12.1 A High Voltage Inverting Amplifier

An inverting amplifier with an output voltage swing from essentially 0 V_{DC} to +300 V_{DC} is shown in Figure 93. The transistor Q_1 must be a high breakdown device as it will have the full HV supply across it. The biasing resistor R_3 is used to center the transfer characteristic and the gain is the ratio of R_2 to R_1. The load resistor R_L can be increased if desired to reduce the HV current drain.

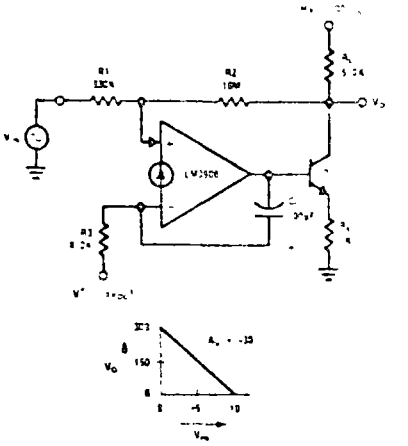


FIGURE 93 A High Voltage Inverting Amplifier

10.12.2 A High Voltage Non-inverting Amplifier

A high voltage non-inverting amplifier is shown in Figure 94. Common-mode biasing resistors

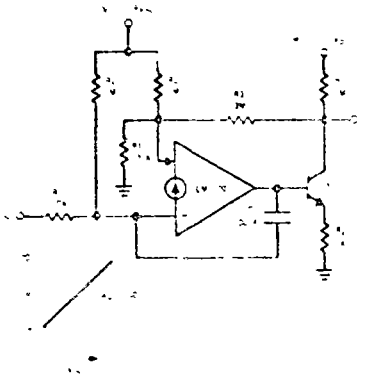


FIGURE 94 A High Voltage Non-inverting Amplifier

(R_2) are used to allow V_{IN} to go to 0 V_{DC}. The output voltage V_O will not actually go to 0 due to R_S but should go to approximately

V_{DC}. Again the gain is 30 and a range of input voltage of from 0 to +10 V_{DC} will use the output voltage to range from approximately 0 to -300 V_{DC}.

12.3 A Line Operated Audio Amplifier

An audio amplifier which operates off a V_{DC} power supply (the rectified line voltage) is often used in consumer products. The internal high voltage transistor Q_1 of Figure 95 is biased and controlled by the LM3900. A voltage divider of the DC biasing voltage which appears across the emitter resistor of Q_1 is connected by the resistor which is placed from the input to ground.

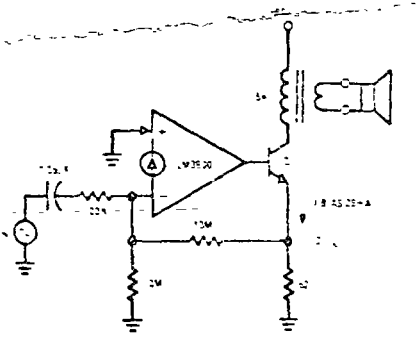


FIGURE 95 A Line Operated Audio Amplifier

13 A Dual-channel Class-A Driver for Auto Radios

A germanium power transistor is widely used in complementary class A audio amplifiers. As shown in Figure 96, two amplifiers can be cascaded

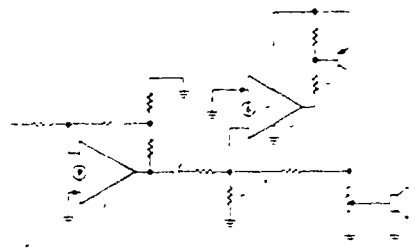


FIGURE 96 A Dual-channel IC Driver for Class A Car Radios

...ed and to control the 2N178 pair of transistors. This circuit has many advantages over the conventional circuit which is used as

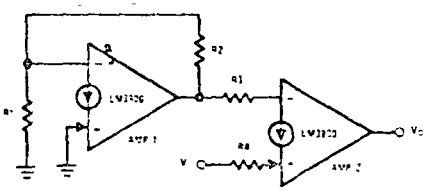
...ecause only a capacitor and a ...

3) The input impedance is high (1 MΩ)
4) A large closed loop gain is easily achieved (80 dB)
5) The slow start-up delay is eliminated
6) Two channels are available in one package

Again the pin 14 voltage must be at least as high as the power supply used at the emitter of Q_1 to guarantee an OFF control for Q_1.

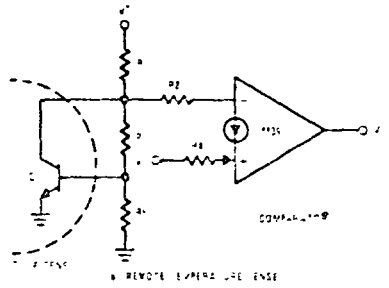
10.14 Temperature Sensing

The LM3900 can be used to monitor the junction temperature of the monolithic chip as shown in Figure 97(a). Amp 1 will generate an output voltage which can be designed to undergo a large negative temperature change by design of R_1 and R_2. The second amplifier compares this temperature dependent voltage with the power supply voltage and goes high at a designed maximum T_j of the IC.



T SENSE COMPARATOR

A IC T MONITOR



B REMOTE EMITTER SENSE

FIGURE 97 Temperature Sensing

For remote sensing an NPN transistor Q_1 of Figure 97(b) is connected as an N V_{BE} generator with R_3 and R_5) and is biased via R_1 from the power supply voltage V^+. The LM3900 again compares a temperature dependent voltage with the supply voltage and can be designed to make V_O go high at a maximum

10.15 A "Programmable Unijunction"

If a diode is added to the Schmitt-trigger a "programmable unijunction" function can be obtained as shown in Figure 98. For a low input voltage the output voltage of the LM3900 is high and CR1 is OFF. When the input voltage rises to the high trip voltage the output fails to essentially 0V and CR1 goes ON to discharge the input capacitor C. The low trip voltage

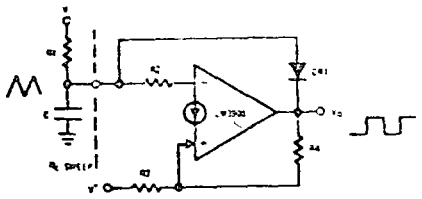


FIGURE 98 A "Programmable Unijunction"

must be larger than approximately 1V to guarantee that the forward drop of CR1 added to the output voltage of the LM3900 will be less than the low trip voltage. The discharge current can be increased by using smaller values for R_2 to provide pull down currents larger than the 1.3 mA bias current source. The trip voltages of the Schmitt-Trigger are designed as shown in section 9.7.

10.16 Adding a Differential Input Stage

A differential amplifier can be added to the input of the LM3900 as shown in Figure 99.

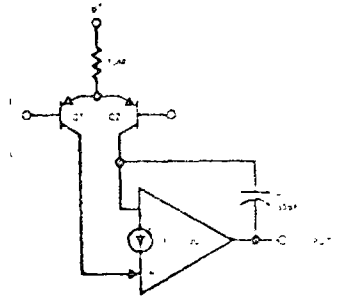


FIGURE 99 Adding a Differential Input Stage

This will increase the gain and reduce the offset voltage. Frequency compensation can be added as shown. The BV_{EBO} limit of the input transistors must not be exceeded during a large differential input condition or diodes and input limiting resistors should be added to restrict the input voltage which is applied to the bases of Q_1 and Q_2 to $\pm V_D$.

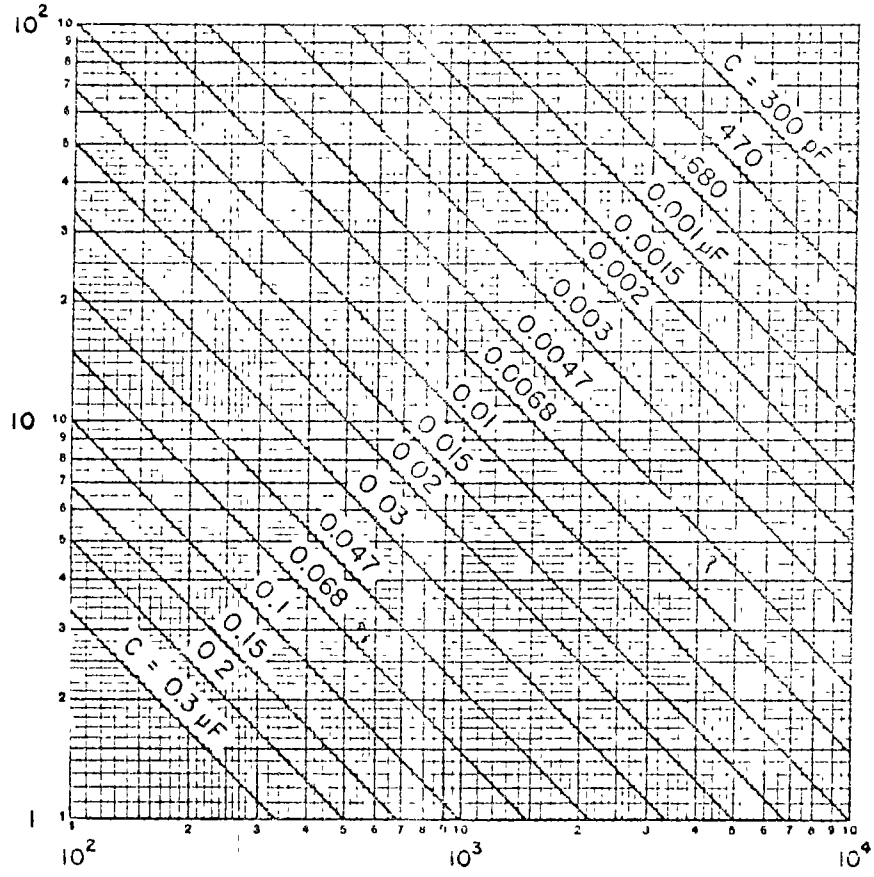
The input common-mode voltage range does not go exactly to ground as a few tenths of a volt are needed to guarantee that Q_1 or Q_2 will not saturate and cause a phase change (and a resulting latch-up). The input currents will be small but could be reduced further if desired by using FETS for Q_1 and Q_2. This circuit can also be operated off of ± 15 V_{DC} supplies

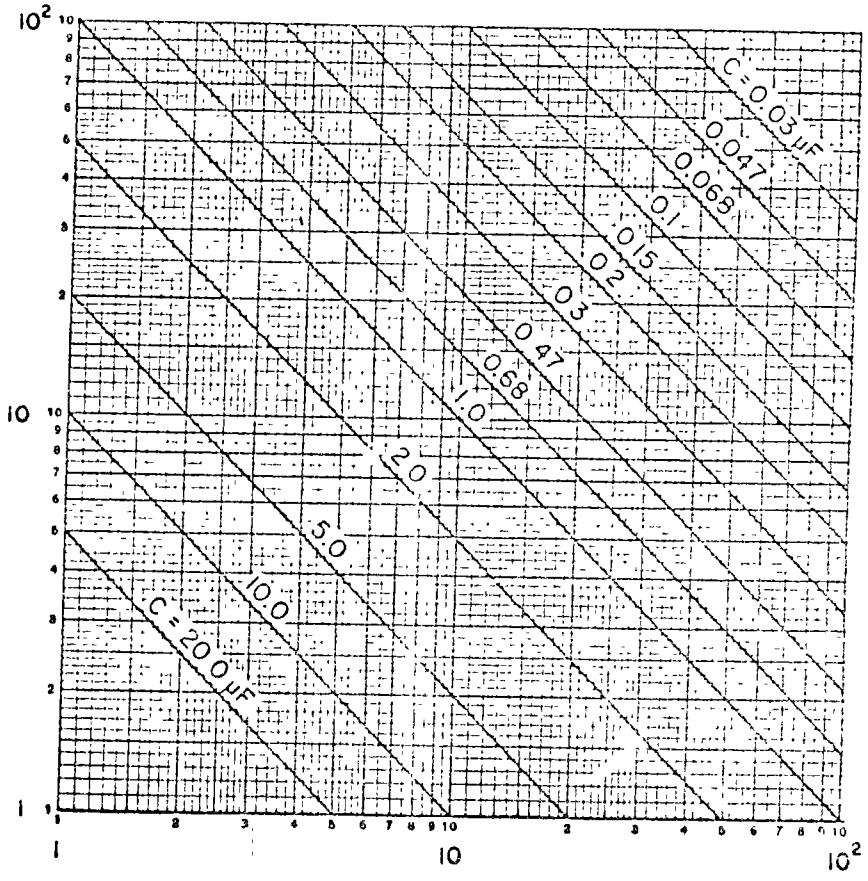
GUIA PARA EL USO DE LAS GRAFICAS DE LA PAG. I.141 a I.146

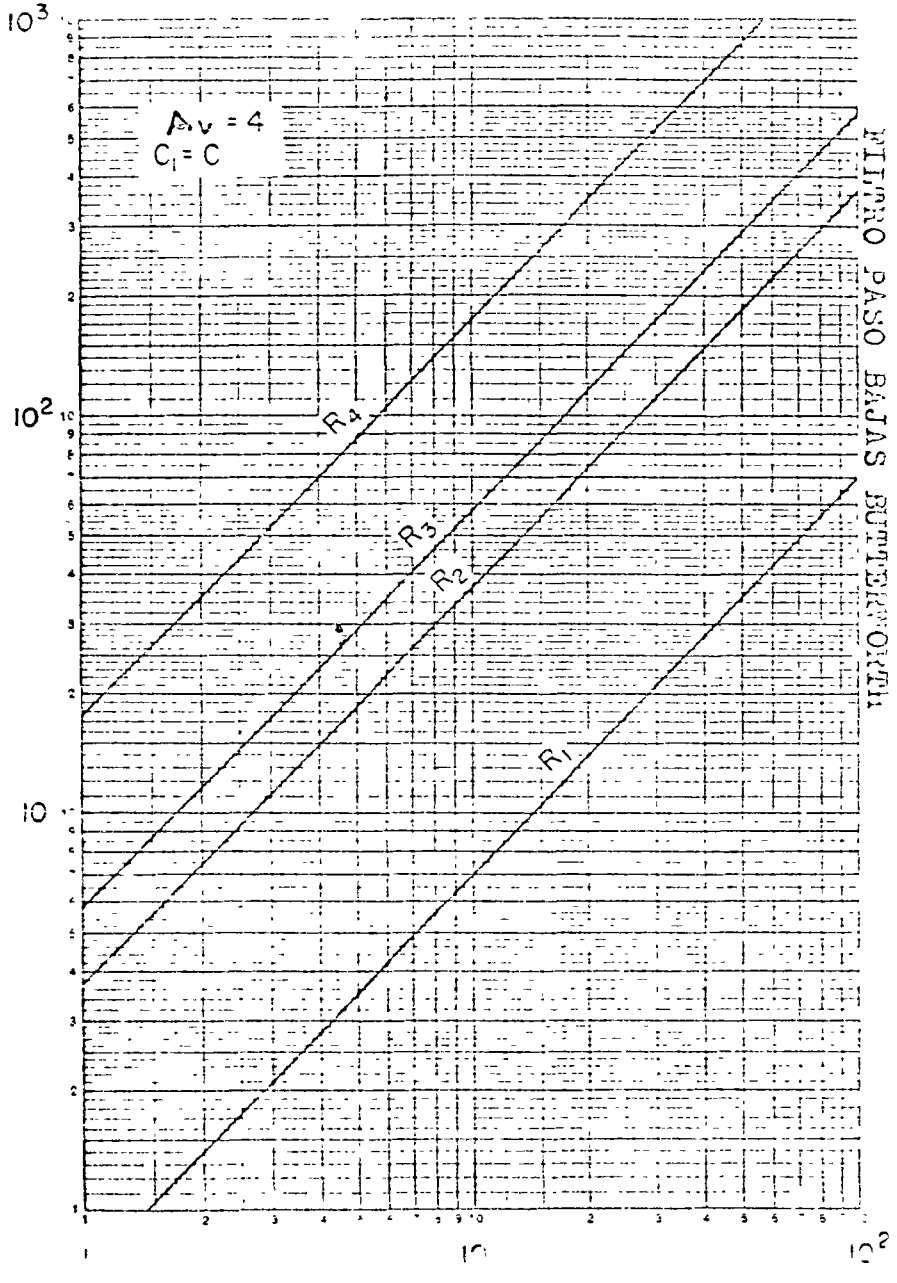
Una vez determinado el tipo de filtro a usar, asi como los parametros correspondientes, el procedimiento a seguir será:

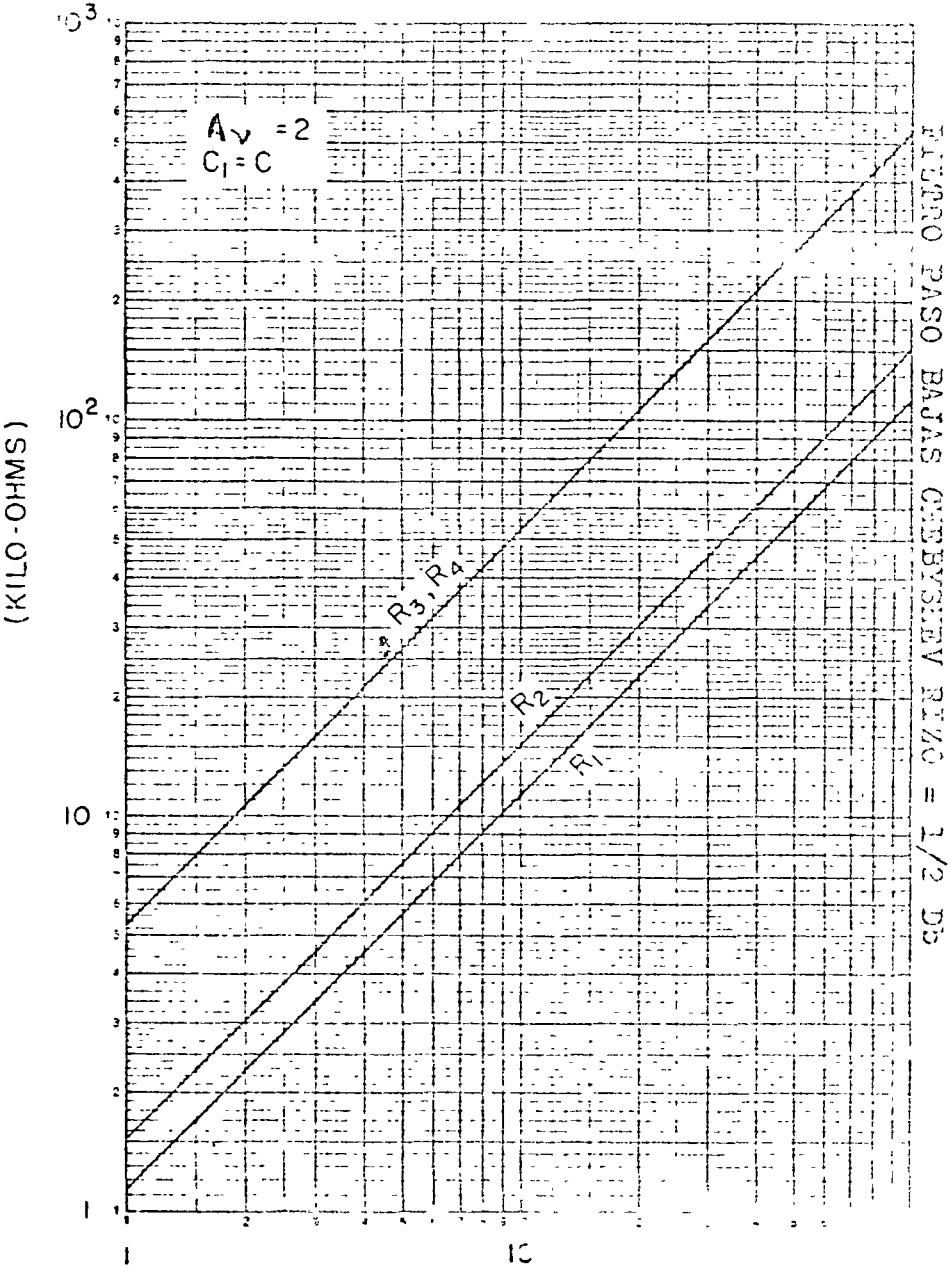
-Proponer un valor de capacitancia y determinar el valor correspondiente del párametro K(pg. 1.141)
-Localizar las gráficas correspondientes al tipo de filtro deseado(pgs. I.142 a L.146)
-Obtener de la gráfica correspondiente los valores de l s resistencias
-Si los valores de resistencias encontrados en el paso anterior no son adecuados con respecto al A.O. o con respecto al resto del circuito(p.ej. causan impedancias de entrada muy bajas) regresamos al paso inicial o cambiamos de configuración.

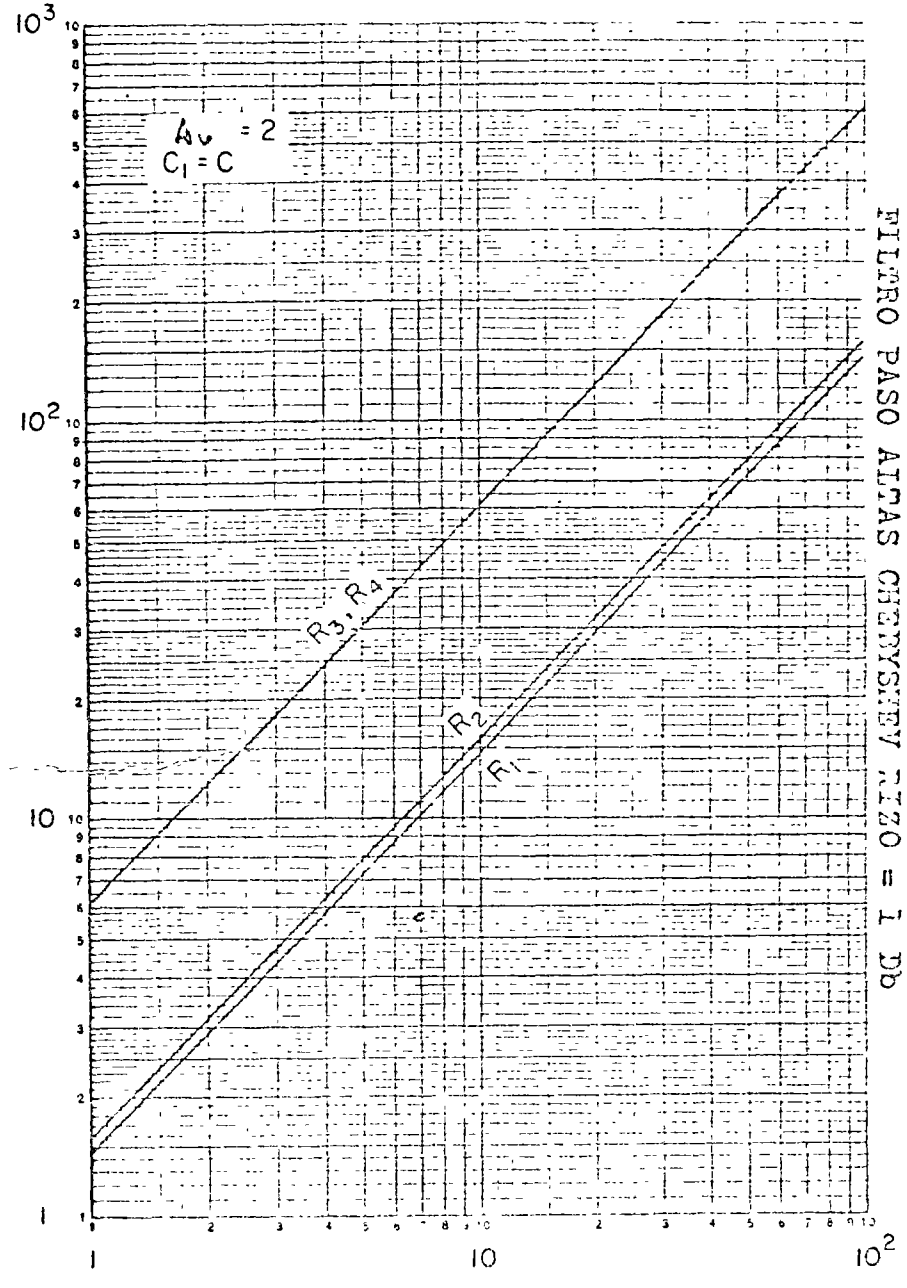
FRECUENCIA DE CORTE VS K



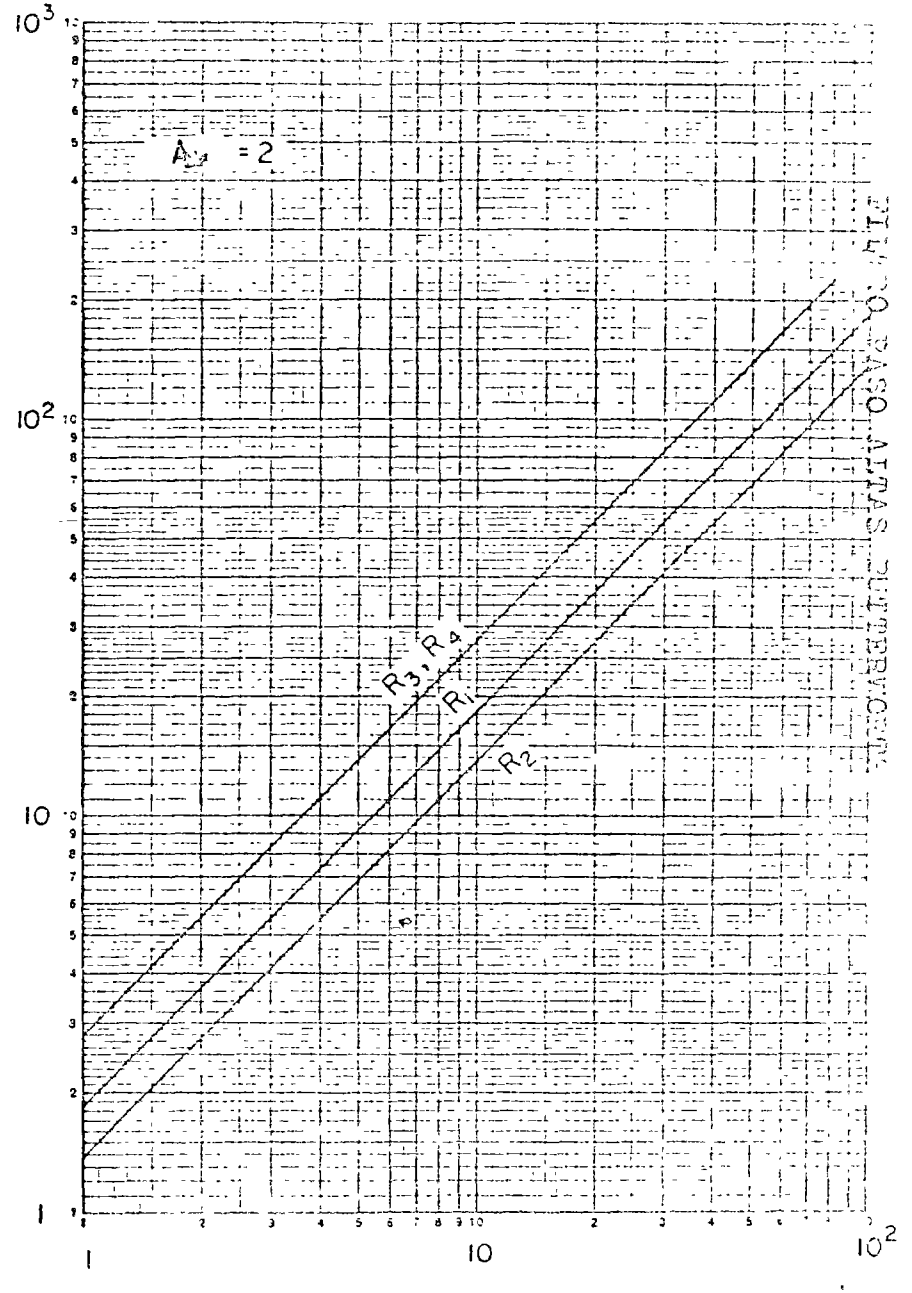



FILTRO PASO BAJAS BUTTERWORTH
$A_V = 4$
$C_1 = C$
R_4
R_3
R_2
R_1
10^3
10^2
10
1
1
10
10^2


FILTRO PASO BAJAS CHEBYSHEV RIZO = 1/2 DB
$A_V = 2$
$C_1 = C$
R_3, R_4
R_2
R_1
(KILO-OHMS)
10^3
10^2
10
1
1
10

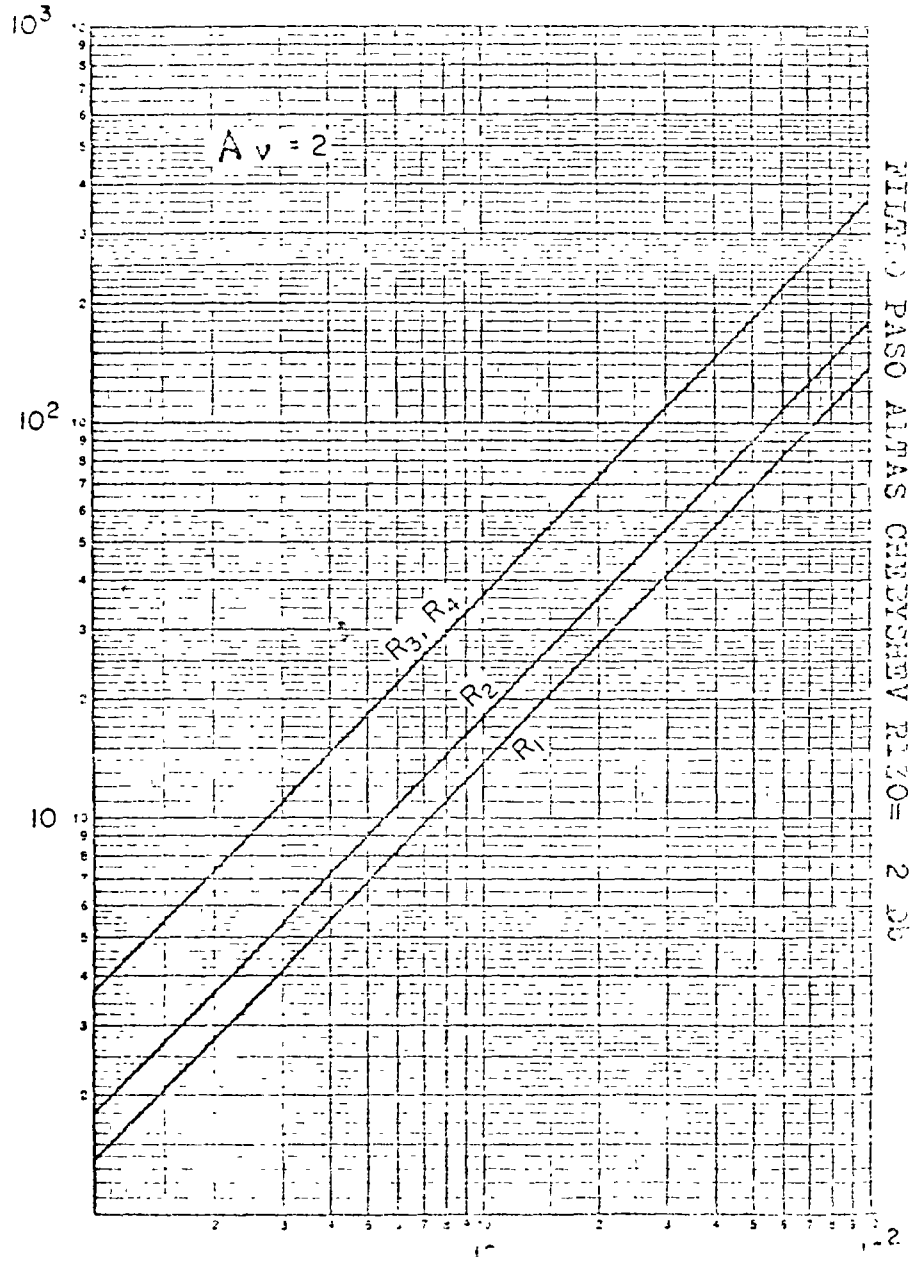


FILTRO PASO ALTAS CHEBYSHEV, 2720 = 1 Db

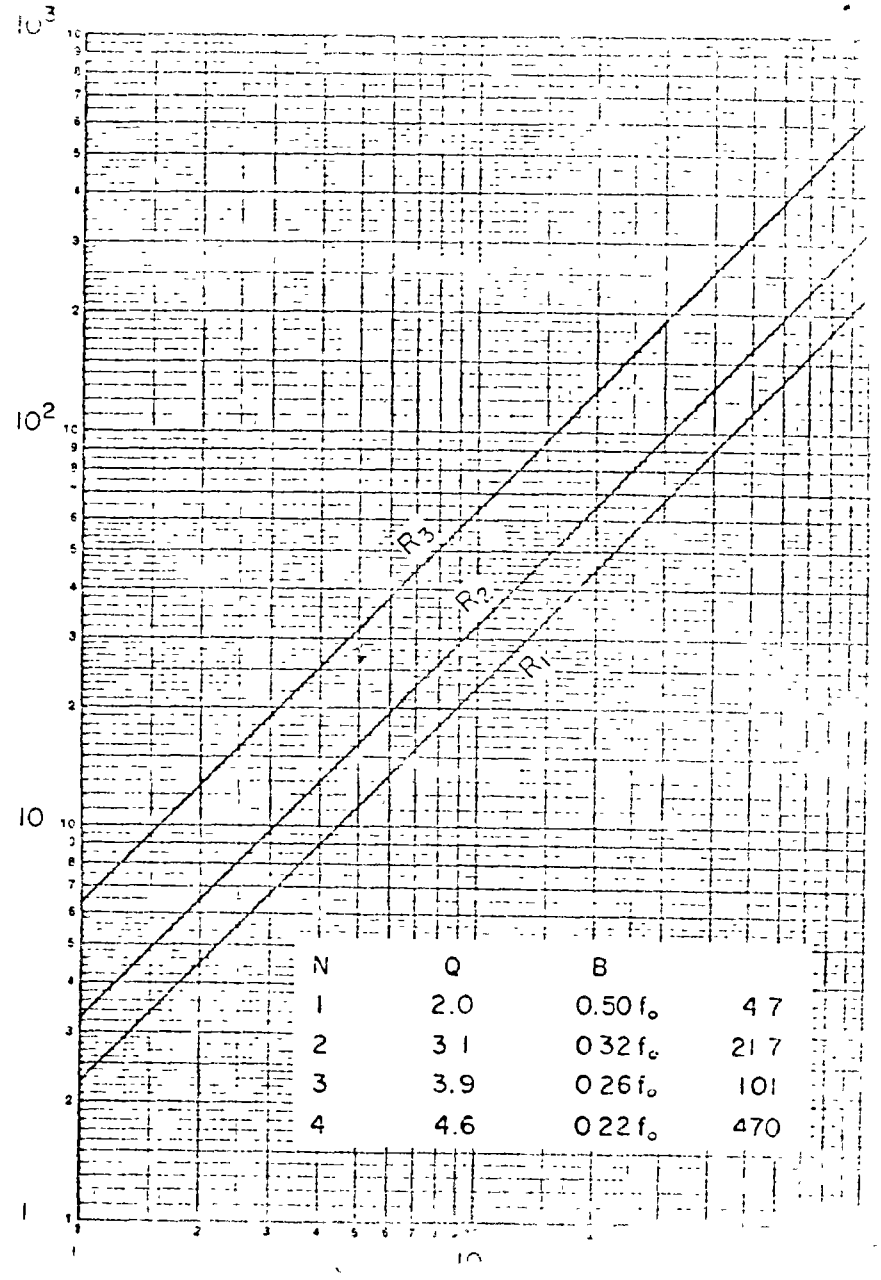


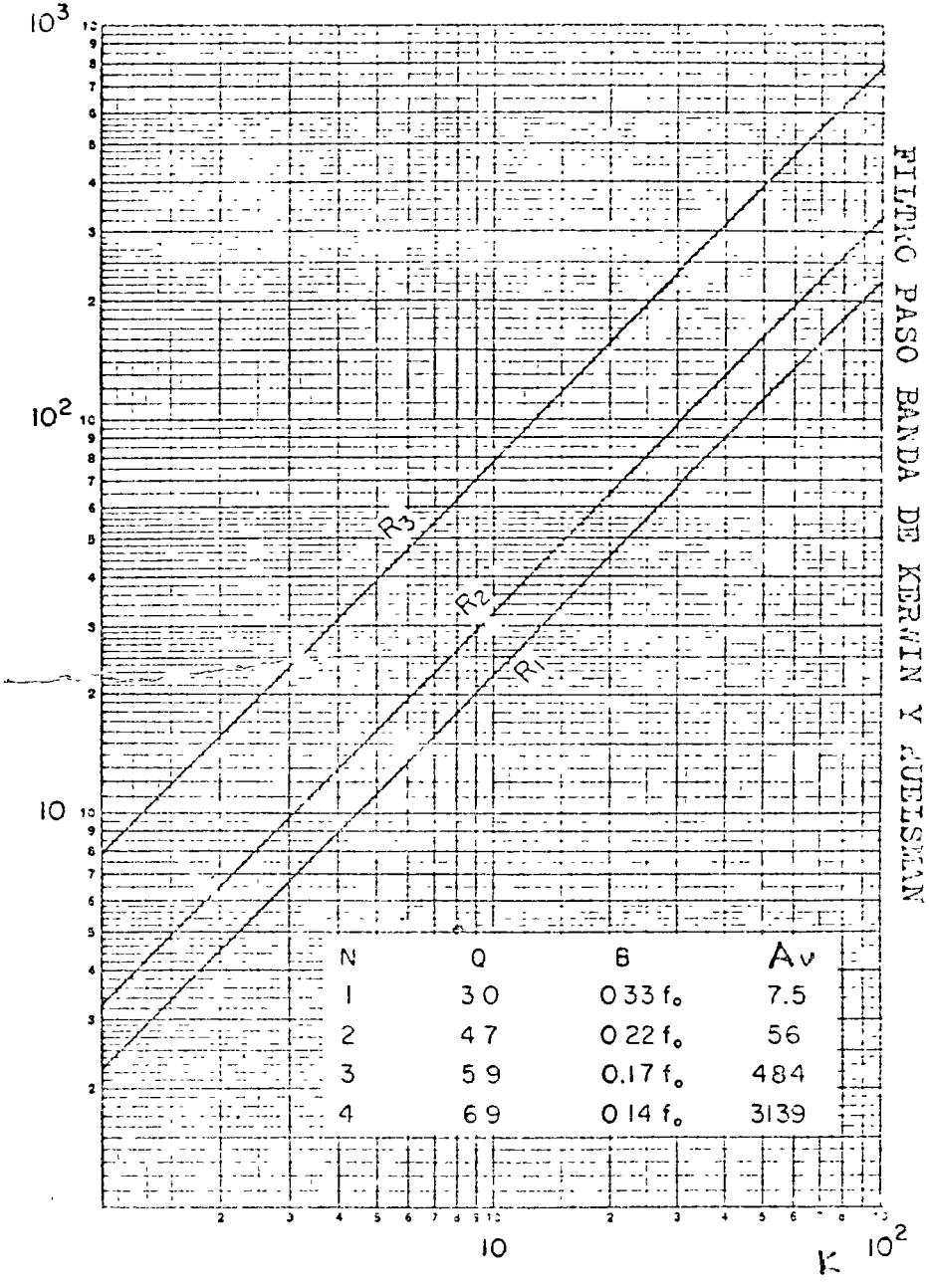
(KILO-OHMS)

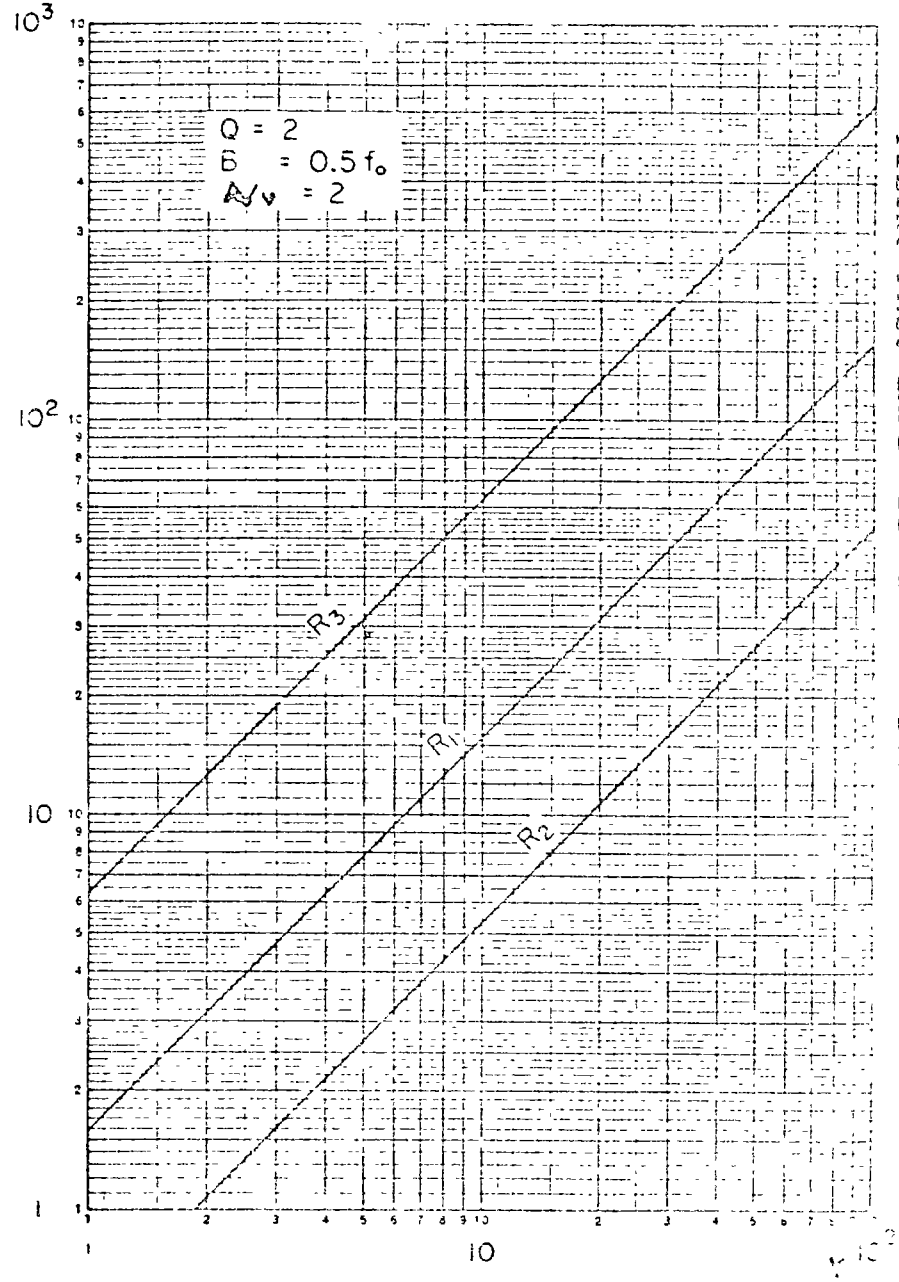
FILTRO PASO ALTAS BUTTERWORTH



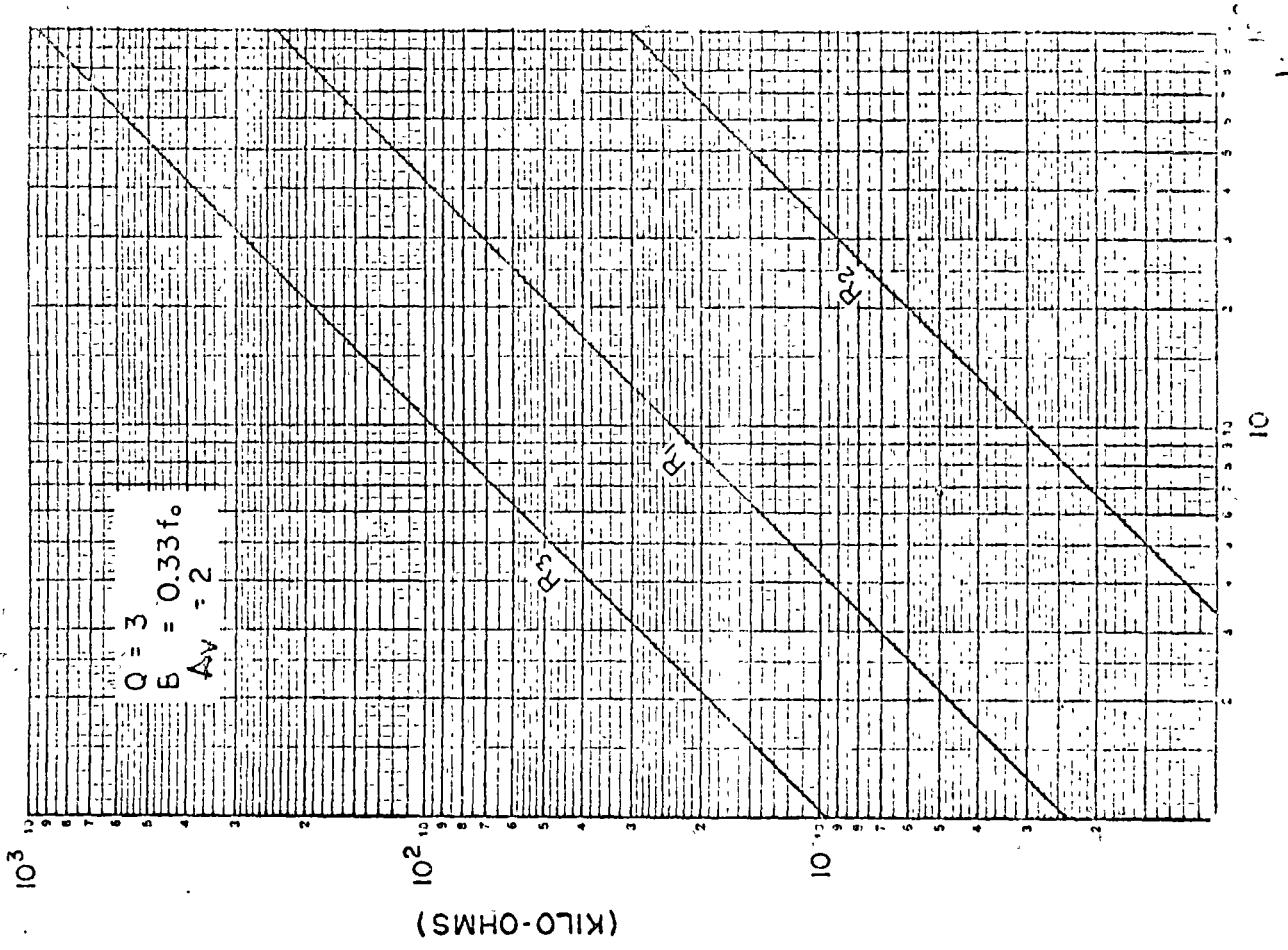
FILTRO PASO ALTAS CHEBYSHEV RIZO= 2 dB




FILTRO PASO BANDA DE KERWIN Y HUELSMAN
(KILO-OHMS)
R3
R2
R1
10³
10²
10
10
10²
K
N Q B Av
1 3 0 0 33 f₀ 7.5
2 4 7 0 22 f₀ 56
3 5 9 0.17 f₀ 484
4 6 9 0 14 f₀ 3139


Q = 2
B = 0.5 f₀
Av = 2
R3
R1
R2
10³
10²
10
1
10

FILTRO PASO BANDA DE REALIMENTACION MULTIPLE



APPENDIX

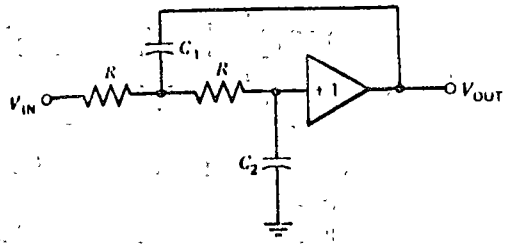
Design Criteria for Second-Order Active Filters[1]

Low-Pass

1. Transfer function

$$H(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

2. Circuit configuration:



3. Cutoff frequency:

$$\omega_0 = \frac{1}{R\sqrt{C_1 C_2}}$$

4. Damping factor:

$$\zeta = \sqrt{\frac{C_2}{C_1}}$$

5. Stability functions:

(a) $$\frac{\Delta\omega_0}{\omega_0} = -\left(\frac{\Delta R}{R} + \frac{1}{2}\frac{\Delta C_1}{C_1} + \frac{1}{2}\frac{\Delta C_2}{C_2}\right)$$

(b) $$\frac{\Delta\zeta}{\zeta} = \frac{1}{2}\left(\frac{\Delta C_2}{C_2} - \frac{\Delta C_1}{C_1}\right)$$

6. Component values:

$$R = \left(\frac{\zeta}{\omega_0}\right)\frac{1}{C_2}$$

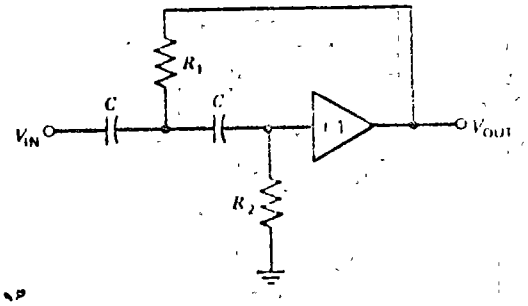
$$C_1 = \left(\frac{1}{\zeta^2}\right)\frac{1}{C_2}$$

High-Pass

1. Transfer function:

$$H(s) = \frac{s^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

2. Circuit configuration:



3. Cutoff frequency:

$$\omega_0 = \frac{1}{C\sqrt{R_1 R_2}}$$

4. Damping factor:

$$\zeta = \sqrt{\frac{R_1}{R_2}}$$

5. Stability functions:

(a) $$\frac{\Delta\omega_0}{\omega_0} = -\left(\frac{\Delta C}{C} + \frac{1}{2}\frac{\Delta R_1}{R_1} + \frac{1}{2}\frac{\Delta R_2}{R_2}\right)$$

(b) $$\frac{\Delta\zeta}{\zeta} = \frac{1}{2}\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right)$$

6. Component values:

$$C = \left(\frac{\zeta}{\omega_0}\right)\frac{1}{R_1}$$

$$R_2 = \left(\frac{1}{\zeta^2}\right)\frac{1}{R_1}$$

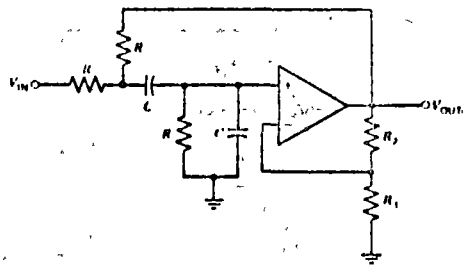
[1] H. T. Russell, "Design Active Filters with Less Effort," *Electronics*, June 7, 1971

Band Pass A

1. Transfer function:

$$H(s) = \frac{K_0(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

2. Circuit configuration:



3. Center frequency:

$$\omega_0 = \frac{\sqrt{2}}{RC}$$

4. Quality factor and center frequency gain:

$$Q = \frac{\sqrt{2}}{5 - K}$$

$$K_0 = \frac{K}{5 - K}$$

where

$$K = 1 + \frac{R_2}{R_1}$$

5. Stability functions:

(a) $\dfrac{\Delta\omega_0}{\omega_0} = -\sqrt{2}\left(\dfrac{\Delta R}{R} + \dfrac{\Delta C}{C}\right)$

(b) $\dfrac{\Delta Q}{Q} = (2\sqrt{2}Q - 1)\left(\dfrac{\Delta R_2}{R_2} - \dfrac{\Delta R_1}{R_1}\right)$

(c) $\dfrac{\Delta K_0}{K_0} = (3.54Q)\left(\dfrac{2.84Q - 1}{3.54Q - 1}\right) \times \left(\dfrac{\Delta R_2}{R_2} - \dfrac{\Delta R_1}{R_1}\right)$

6. Component values:

$$R = \frac{\sqrt{2}}{\omega_0 C}$$

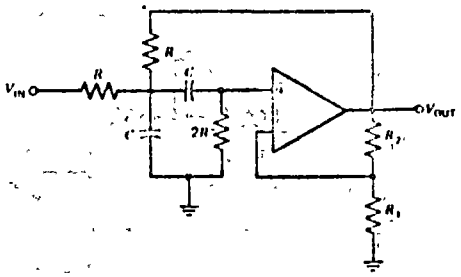
$$R_2 = \left(4 - \frac{\sqrt{4}}{Q}\right)R_1 = (K - 1)R_1$$

Band Pass B

1. Transfer function:

$$H(s) = \frac{K_0(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

2. Circuit configuration:



3. Center frequency:

$$\omega_0 = \frac{1}{RC}$$

4. Quality factor and center frequency gain:

$$Q = \frac{1}{3 - K}$$

$$K_0 = \frac{K}{3 - K}$$

where

$$K = 1 + \frac{R_2}{R_1}$$

5. Stability functions:

(a) $\dfrac{\Delta\omega_0}{\omega_0} = -\left(\dfrac{\Delta R}{R} + \dfrac{\Delta C}{C}\right)$

(b) $\dfrac{\Delta Q}{Q} = (2Q - 1)\left(\dfrac{\Delta R_2}{R_2} - \dfrac{\Delta R_1}{R_1}\right)$

(c) $\dfrac{\Delta K_0}{K_0} = 3Q\left(\dfrac{2Q - 1}{3Q - 1}\right) \times \left(\dfrac{\Delta R_2}{R_2} - \dfrac{\Delta R_1}{R_1}\right)$

6. Component values:

$$R = \frac{1}{\omega_0 C}$$

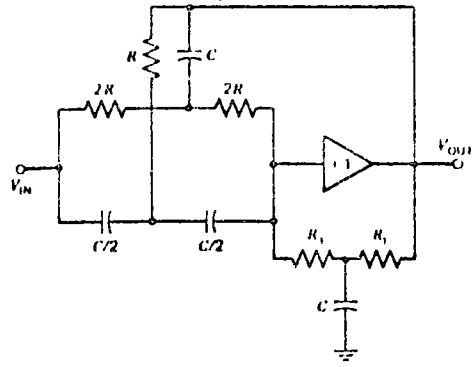
$$R_2 = \left(2 - \frac{1}{Q}\right)R_1 = (K - 1)R_1$$

Band-Reject

1. Transfer function:

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

2. Circuit configuration:



3. Center frequency:

$$\omega_0 = \frac{1}{RC}$$

4. Quality factor:

$$Q = \frac{R_1}{4R}$$

5. Stability functions:

(a) $$\frac{\Delta\omega_0}{\omega_0} = -\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)$$

(b) $$\frac{\Delta Q}{Q} = \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R}{R}\right)$$

6. Component values:

$$R = \frac{1}{\omega_0 C}$$

$$R_1 = \left(\frac{4Q}{\omega_0}\right)\frac{1}{C}$$

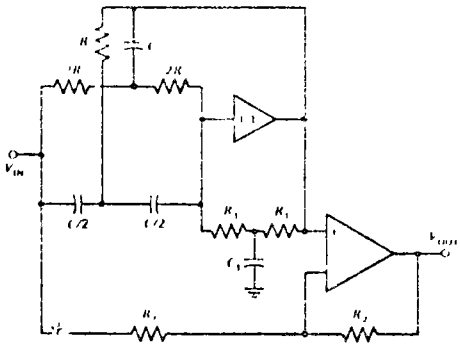
$$C_1 = \left(\frac{1}{2Q}\right)C$$

All-Pass (360°)

1. Transfer function:

$$H(s) = \frac{s^2 - (\omega_0/Q)s + \omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}$$

2. Circuit configuration



3. Center frequency:

$$\omega_0 = \frac{1}{RC}$$

4. Quality factor:

$$Q = \frac{R_1}{4R}$$

5. Stability functions:

(a) $$\frac{\Delta\omega_0}{\omega_0} = -\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)$$

(b) $$\frac{\Delta\omega}{Q} = \left(\frac{\Delta R_1}{R_1} - \frac{\Delta R}{R}\right)$$

6. Component values:

$$R = \frac{1}{\omega_0 C}$$

$$R_1 = \left(\frac{4Q}{\omega_0}\right)\frac{1}{C}$$

$$C = \left(\frac{1}{2Q}\right)C$$

Simple arithmetic: an easy way to design active bandpass filters

A time-saving approach to active filter design works for both high and low values of Q; the method uses a multiple-feedback network whose performance is close to the theoretical ideal

by Ferrel G. Stremler, *University of Wisconsin, Madison, Wis.*

The process of designing a filter is often long and tedious, demanding much fortitude and slide-rule duty from the engineer. But now there is a step-by-step technique for designing second-order active bandpass filters that saves time, conserves engineering effort, and is easy to understand. Unlike other filter design methods, this one can be used for both high-Q and low-Q circuits.

At least three different active networks can perform the bandpass function. They are the bridged-T, the twin-T and the multiple-feedback filters. The first two have only one feedback path, while the third has two. That additional path gives the multiple-feedback active bandpass filter (Fig. 1) several distinct advantages.

For example, it uses fewer components. And its response approaches that of an ideal second-order bandpass filter because its operational amplifier operates with nearly infinite gain. Moreover, its output impedance, which is typically 200 to 300 ohms, is really the output impedance of the op amp used. This means that several filters can be cascaded without extreme loading problems between stages. It's also an improvement on the other two active bandpass filters, which usually have a nominal output impedance of 1 kilohm.

The multiple-feedback network is particularly useful in phase-sensitive bandpass systems when precise compromises must be made between frequency selectivity and phase-shift sensitivity. Difficulty in achieving very high values of Q is the single major drawback of the circuit. The maximum Q that can be achieved is approximately 20. When circuit Q is very high, the shunt resistance, R_2, must be low in value. This severely attenuates the input signal, and taxes the amplifier and feedback path.

Because of its superior performance, the multiple-feedback filter is the best circuit model for a simplified design procedure. The first step is to consider the voltage transfer function for an ideal second-order bandpass filter with a −3-dB bandwidth of B Hz, a center frequency of f_o Hz, and a midband voltage gain of A. The transfer function has the well-known general form:

$$H(s) = \frac{E_2(s)}{E_1(s)} = \frac{H\omega_o s}{s^2 + \alpha\omega_o s + \omega_o^2} \quad (1)$$

where
$$\omega_o = 2\pi f_o \quad (2)$$
$$Q = f_o/B \quad (3)$$
$$\alpha = 1/Q \quad (4)$$
$$H = \alpha|A_o| \quad (5)$$

Figure 2 shows the filter's magnitude and phase characteristics as a function of normalized frequency, with Q as a third parameter. As can be seen, both the magnitude selectivity and the phase-shift sensitivity increase for higher values of Q. Besides helping to visualize filter response, the graph can be used to determine Q when bandwidth is unknown but frequency rejection and phase shift are specified with respect to some center frequency.

Now consider the multiple-feedback active bandpass filter. When operating in the inverting mode with infinite gain, its voltage transfer function is:

$$\frac{E_2(s)}{E_1(s)} = -(s/R_1C_1)/\{s^2 + [s(C_1 + C_2)/R_2C_1C_2] + [(R_1 + R_2)/R_1R_2R_3C_1C_2]\} \quad (6)$$

Just inspecting Eqs. 1 and 6 shows five component values to be determined with only three known constants. Equating the two transfer functions and solving for corresponding coefficients to obtain a new set of equations does not help either. There are still five unknowns and only three equations. The design procedure, therefore, must begin with an assumed relationship between selected components and proceed from there.

Let R_{eq} represent the parallel combination of R_1 and R_2:

$$R_{eq} = R_1R_2/(R_1 + R_2) \quad (7)$$

Setting Eq. 1 equal to Eq. 6 and equating the coefficients of like terms yields:

$$R_{eq}R_3C_1C_2 = 1/\omega_o^2 \quad (8)$$
$$R_{eq}(C_1 + C_2) = \alpha/\omega_o \quad (9)$$
$$R_{eq}R_3C_2/R_1 = H/\omega_o \quad (10)$$

Any numerical values satisfying Eqs. 8, 9 and 10 are an acceptable solution. A simple step-by-step procedure can be used to determine the components and is valid for all values of Q.

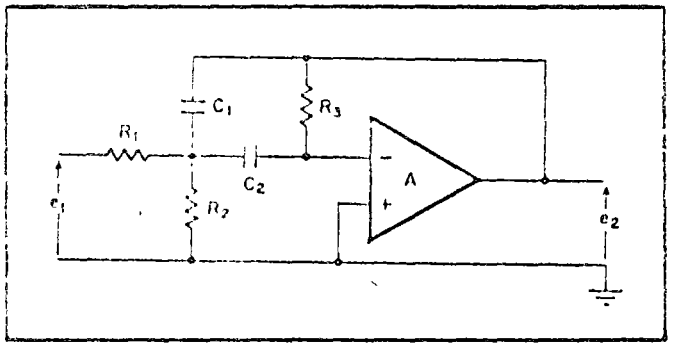
Since filter bandwidth, center frequency and midband voltage gain are known desired specifications, Q can be found using the relationship of Eq. 2. Then

the inequality, $Q > \sqrt{|A_o|}/2$, must be checked so that all the components are real—for example, the resistors must be positive numbers.

If the inequality is true, the capacitors are assigned values and the resistors are computed. Set C_1 equal to C_2 and choose an appropriate capacitance value for C_1. This value should be some standard capacitance that will yield resistances in the order of kilohms. The right resistors help to hold noise down and maintain circuit stability.

Next, solve for ω_o, α and H with Eqs. 2, 4 and 5, respectively. Now R_1 can be determined using Eqs. 8 and 10:

$$R_1 = 1/H\omega_o C_1 \qquad (11)$$



1. Basic network. This active bandpass RC filter provides two feedback paths via R_3 and C_1 for precise trade-off control between gain response and phase shift. The circuit also keeps component count low. When R_2 is very large compared to R_1, it can be omitted altogether.

R_{eq} can be computed from Eqs. 4 and 9:

$$R_{eq} = 1/Q(C_1 + C_2)\omega_o \qquad (12)$$

Using Eq. 7, it is a simple matter to determine R_2:

$$R_2 = R_1R_{eq}/(R_1 - R_{eq}) \qquad (13)$$

The final component, R_3, is found by dividing Eq. 9 into Eq. 8 and applying Eq. 4:

$$R_3 = \frac{Q(C_1 + C_2)}{C_1C_2\omega_o} = |A_o|R_1\left(1 + \frac{C_1}{C_2}\right) \qquad (14)$$

Standard impedance-scaling techniques may be used to normalize the computed component values. One way is to multiply all capacitances and divide all resistances by the same numerical factor.

If the inequality, $Q > \sqrt{|A_o|}/2$, does not hold, select reasonable (in the order of kilohms) values for R_1 and R_2 and calculate the capacitance values. The resistance chosen for R_1 should include the output impedance of the previous stage. Now R_{eq} can be found using Eq. 7. To minimize the number of components, R_2 can be made infinitely large so that $R_{eq} = R_1$.

The final resistor value, R_3, can be computed with Eqs. 4, 8, 9, and 10.

$$R_3 = HQR_1/(1 - QR_{eq}/HR_1)$$

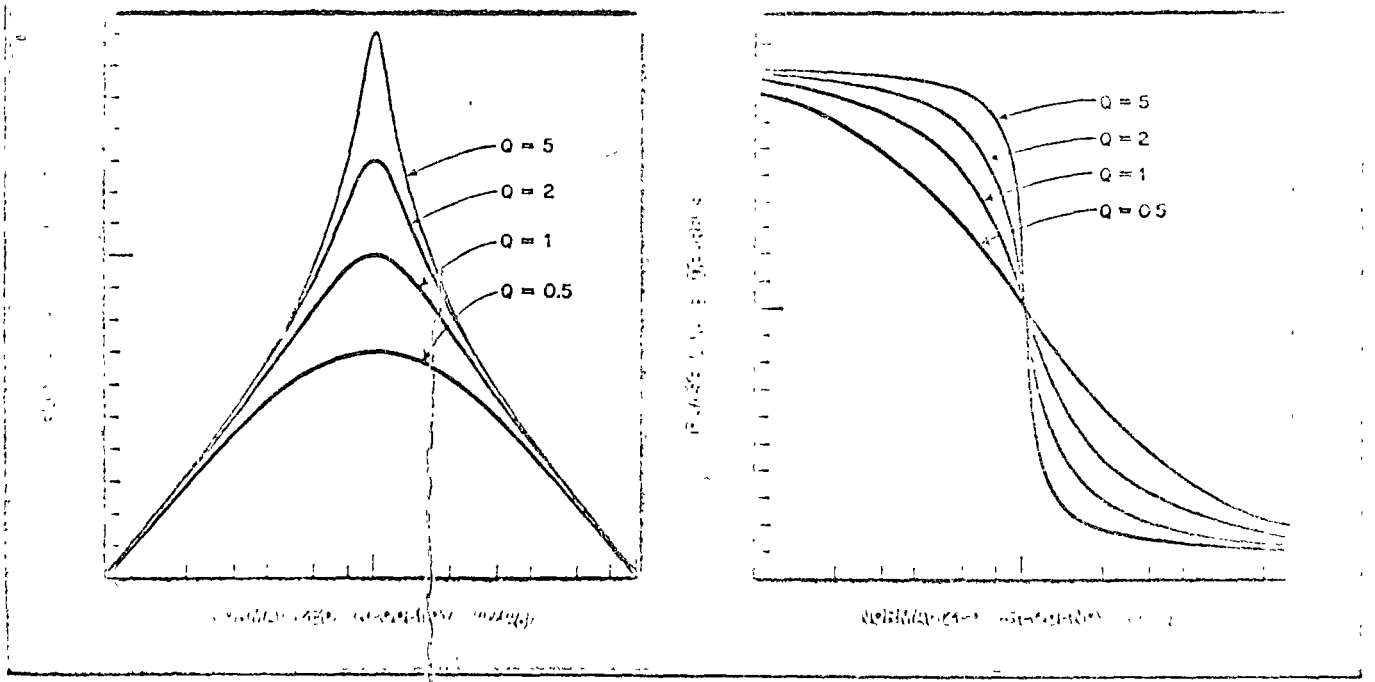
From Eq. 9,

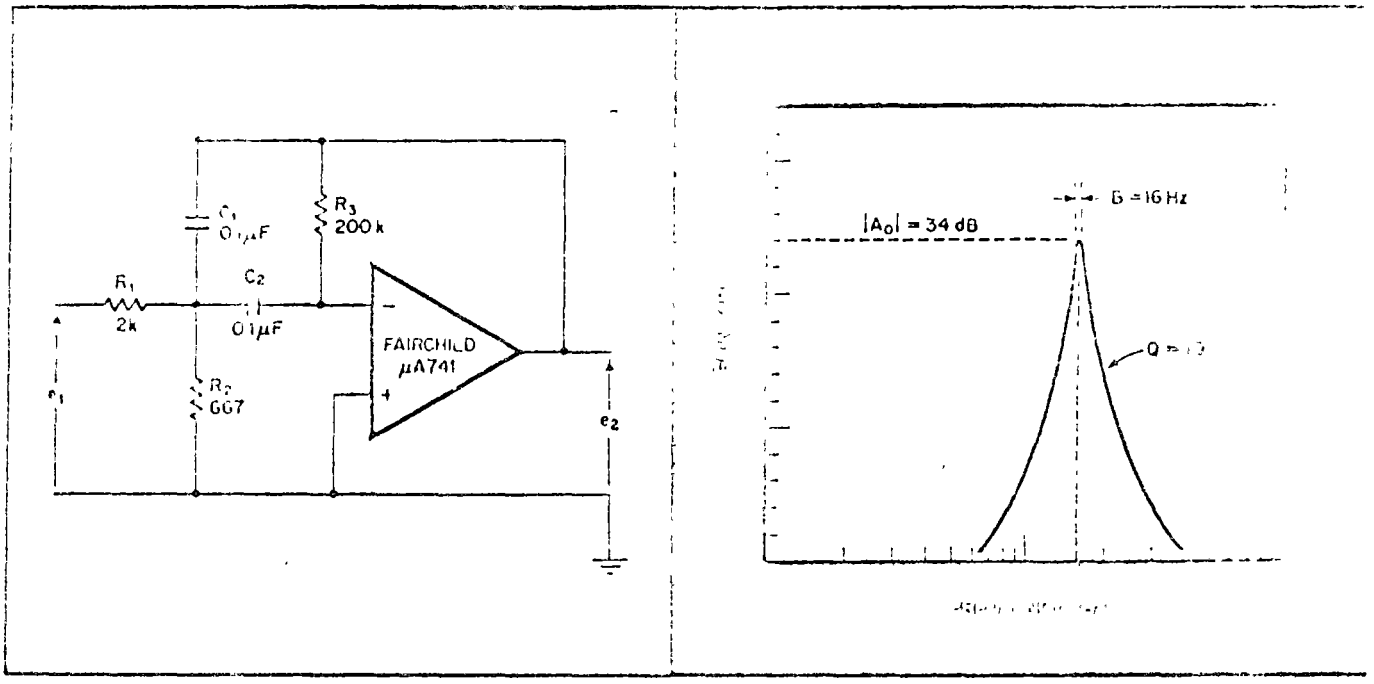
$$C_2 = HR_1/R_{eq}R_1\omega_o$$

Dividing Eq. 10 into Eq. 8 yields C_1

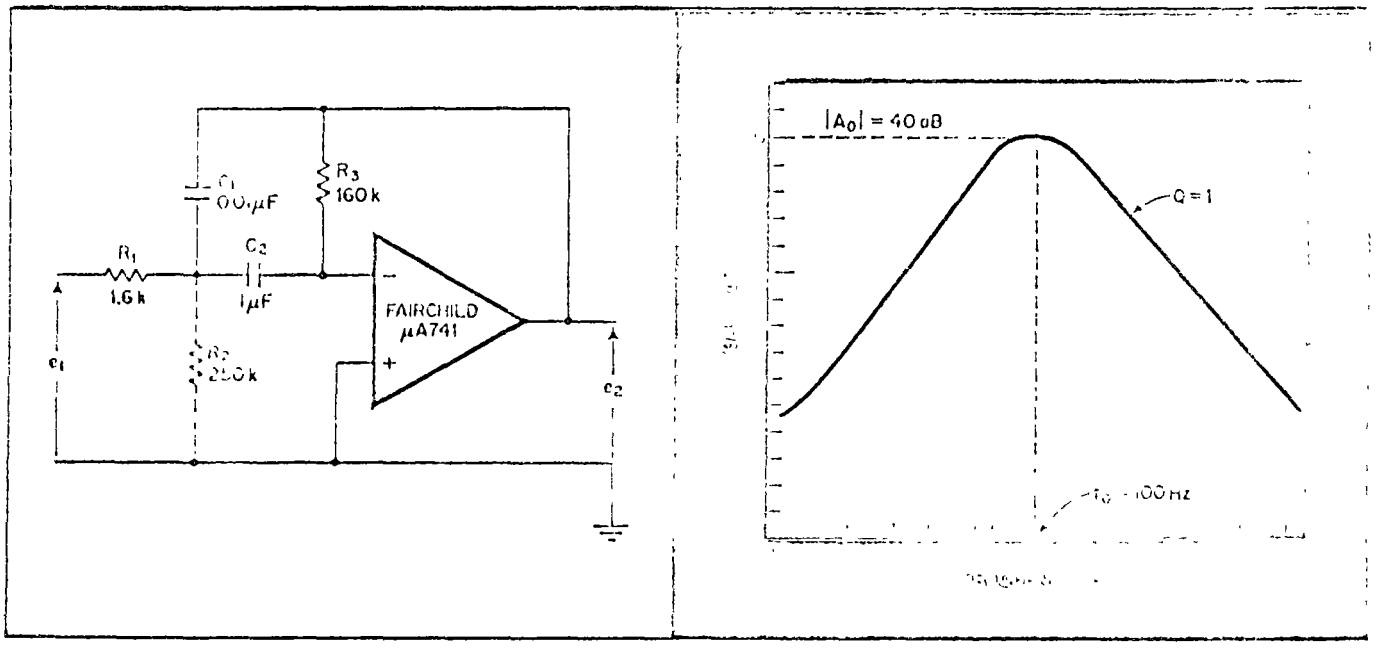
$$C_1 = 1/HR_1\omega_o$$

2. Filter curves. Magnitude and phase responses of an ideal second-order bandpass filter show effect of Q on network voltage transfer function. High Q gives good frequency selectivity at the expense of phase sensitivity. Low Q means large bandwidth and critical phase response. Curves can be used for the multiple-feedback active filter since its performance approximates the ideal.





3. High Q. Filter with Q of 10, 16-hertz bandwidth, center frequency of 160 Hz, and gain of 34 decibels is designed by selecting the same standard capacitance for C_1 and C_2 and then calculating resistances with handy plug-in formulas. Filter requires only six components, including op amp.



4. Low Q. Five-component filter, which has Q of 1 and gain of 40 decibels, rolls off at rate of 20 dB per decade and keeps phase shift within 10° about the center frequency. Resistor R_2 is not needed since it is "infinitely large" compared to R_1. Network is designed by choosing R_1 and then computing capacitances.

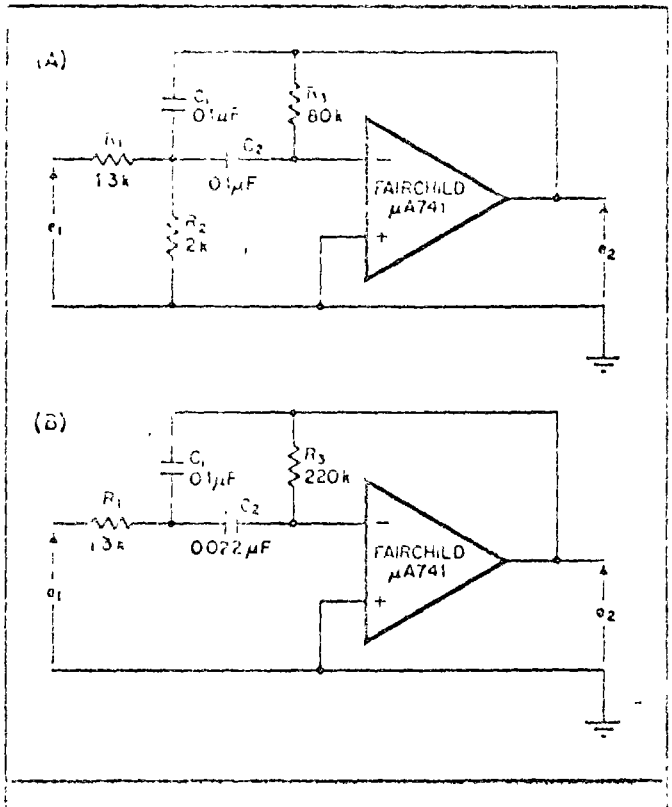
This procedure will in general give unequal, nonstandard capacitance values for C_1 and C_2. It is better to pick standard capacitor values that are close to the computed figures, and then redetermine the resistors from Eqs. 11 through 14. Since standard resistor values are graduated in small steps, it is not difficult to select resistors that will do the job.

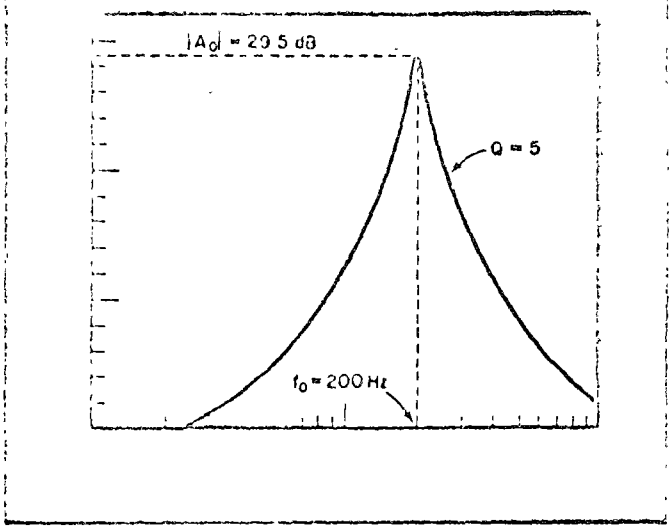
Sometimes there is an intermediate range of Q values for which either of the two design procedures will work. For this case, the quality ratio falls within the limits established by the condition:

$$\sqrt{\frac{C_1|A_0|}{C_1+C_2}} < Q < \sqrt{\frac{R_1|A_0|}{R_{eq}}}$$

The second design approach, however, offers a distinct advantage over the first—it minimizes component count by allowing R_2 to be infinite. A few examples will help to illustrate the technique.

First, suppose the problem is to design a bandpass





5. Intermediate Q. Two filter designs give the same gain response (C). Though arrived at by differing methods, either is valid, but one (A) uses six components, the other (B) only five. Filter gain is 29.5 dB, center frequency is 200 Hz, and Q is 5. For this case, the Q value is intermediate.

filter with a midband voltage gain of 50 (34 dB), a center frequency of 160 Hz, and a 3 dB bandwidth of 16 Hz.

This filter requires a Q of 10 (160/16). The condition, $Q > \sqrt{|A_o|}/2$, is satisfied since

$$10 > \sqrt{50}/2 = 5$$

Find the other needed constants:

$$H = \alpha|A_o| = |A_o|/Q = 50/10 = 5$$

$\omega_o = 2\pi f_o = 2\pi(160) = 1{,}000$ radians/second.

Assume $C_1 = C_2 = 0.1\ \mu F$

Find

$$R_1 = 1/HC_2\omega_o = 2k\Omega$$
$$R_{eq} = 1/Q(C_1 + C_2)\omega_o = 560\Omega$$
$$R_2 = R_1R_{eq}/(R_1 - R_{eq}) = 667\Omega$$
$$R_3 = |A_o|R_1(1 + C_1/C_2) = 200k\Omega$$

The completed design and its gain response are shown in Fig. 5.

The second problem is to design a bandpass filter that has a midband voltage gain of 50 (34 dB), a center frequency of 160 Hz, and no specific bandwidth. However, the circuit must provide at least 20 dB of frequency rejection one decade from the center frequency, and hold phase shift to $\pm 30°$ maximum for a 10% change in the center frequency.

The gain and phase plots of Fig. 2 show that the filter must have $Q \approx 1$ to satisfy these two requirements. The other constants are:

$$H = |A_o|/Q = 100$$
$$\omega_o = 2\pi f_o = 628\ \text{rad/s}$$

The check, $Q > \sqrt{|A_o|}/2$, does not hold because $1 < \sqrt{50}$. It is now necessary to estimate values for R_1 and R_2. Let $R_1 = 1\ k\Omega$ and $R_2 = \infty$, then $R_{eq} = R_1 = 1\ k\Omega$. Compute the other components.

$$R_3 = \frac{HQR_1}{1 - QR_{eq}/HR_1} = \frac{HQR_1}{1 - Q/H} = 101\ k\Omega$$

$$C_2 = \frac{HR_1}{R_{eq}R_3\omega_o} = \frac{H}{R_3\omega_o} = 1.58\mu F$$

$$C_1 = 1/HR_1\omega_o = 0.0159\ \mu F$$

Standardize the capacitor values by letting $C_1 = 0.01\ \mu F$ and $C_2 = 1\ \mu F$, then adjust the resistors.

$$R_1 = 1/HC_2\omega_o = 1.59\ k\Omega$$
$$R_{eq} = 1/Q(C_1 + C_2)\omega_o = 1.58\ k\Omega$$
$$R_2 = R_1R_{eq}/(R_1 - R_{eq}) = 250\ k\Omega$$
(which is "infinite" compared to R_1)
$$R_3 = |A_o|R_1(1 + C_1/C_2) = 161\ k\Omega$$

Figure 4 illustrates the filter and its gain curve.

For a third problem, design a filter with a midband voltage gain of 30 (29.5 dB), a center frequency of 200 Hz, and a Q of 5. Here the intermediate Q test, $\sqrt{|A_o|}/2 < Q < \sqrt{|A_o|}$, holds for both design procedures, so that both yield valid results, which it is interesting to compare.

First choose $C_1 = C_2 = 0.1\ \mu F$. Then solve for $R_1 = 1.33\ k\Omega$, $R_{eq} = 797\Omega$, $R_2 = 2k\Omega$ and $R_3 = 80\ k\Omega$. From this the design in Fig. 5A results.

Now try the other procedure. Let $R_1 = 1\ k\Omega$ and $R_2 = \infty$. This requires that $R_3 = 189\ k\Omega$, $C_1 = 0.133\ \mu F$, and $C_2 = 0.0266\ \mu F$. Standardize the capacitor values by setting $C_1 = 0.1\ \mu F$ and $C_2 = 0.022\ \mu F$. Compute the resistances $R_1 = 1.36\ k\Omega$, $R_{eq} = 1.31\ k\Omega$, $R_2 = \infty$, and $R_3 = 222\ k\Omega$. The filter that results is shown in Fig. 5B.

The gain response (Fig. 5C) for each of these filters is identical.

Active resonators save steps in designing active filters

Resonator model allows active filter sections to be treated as common components, side-stepping design details that bog down analysis; the model employs a simulated inductance that remains inherently lossless

by Randy Brandt, *Integrated Electronics Inc., Los Gatos, Calif.*

☐ Active filters make possible the realization of inexpensive high-Q networks at low frequencies. Passive filters, on the other hand, tend to become costly, lossy, and unwieldy in physical size when large inductances are required. Since active filters simulate inductance, extremely large values can be realized while holding down filter cost, losses, and size. Furthermore, the ever-decreasing price of today's monolithic operational amplifier, the heart of any active filter, is constantly improving the attractiveness of building an active, rather than passive, filter.

However, because of the proliferation of active filter analysis techniques, only a core of full-time design specialists can differentiate between the merits of various approaches and select the optimum solution. The occasional filter designer finds it easier to build a passive circuit, despite the advantages of the active approach.

But a basic building block, called the active resonator, allows even the occasional filter designer to handle an active filter as an ordinary circuit component. This active resonator model is common to all active filter sections. It consists of a tuned RLC circuit for resonance and an op amp for the necessary gain and isolation.

Modeling the active resonator

An active filter section, regardless of how many amplifiers it contains, is the fundamental repetitive portion of a complete active filter. Generally, the active filter section can perform as a filter itself or be cascaded to realize higher-order filter functions. The term "active resonator" is simply another label for active filter section. With varying degrees of difficulty, any active filter can be reduced to active resonator form.

Because of its utility and simplicity, a sound choice for demonstrating how to form an active resonator model is the popular biquad active filter. This filter is particularly noted for its insensitivity to variations in component values. When it has three amplifiers, as shown in Fig. 1(a), the biquad filter provides both low-pass and bandpass outputs. By adding a fourth summing amplifier, the circuit can supply a high-pass, all-pass, or notch output.[1]

The network's transfer function between its bandpass output, $(V_o)_{BP}$, and its low-pass output, $(V_o)_{LP}$, is that of a non-inverting integrator:

$$(V_o)_{LP}/(V_o)_{BP} = 1/sR'C'$$

where s is the Laplace variable. Feedback current is:

$$I_f = (V_o)_{LP}/R_f = (V_o)_{BP}/sR'R_fC'$$

Solving for the equivalent impedance of the loop with these two equations gives:

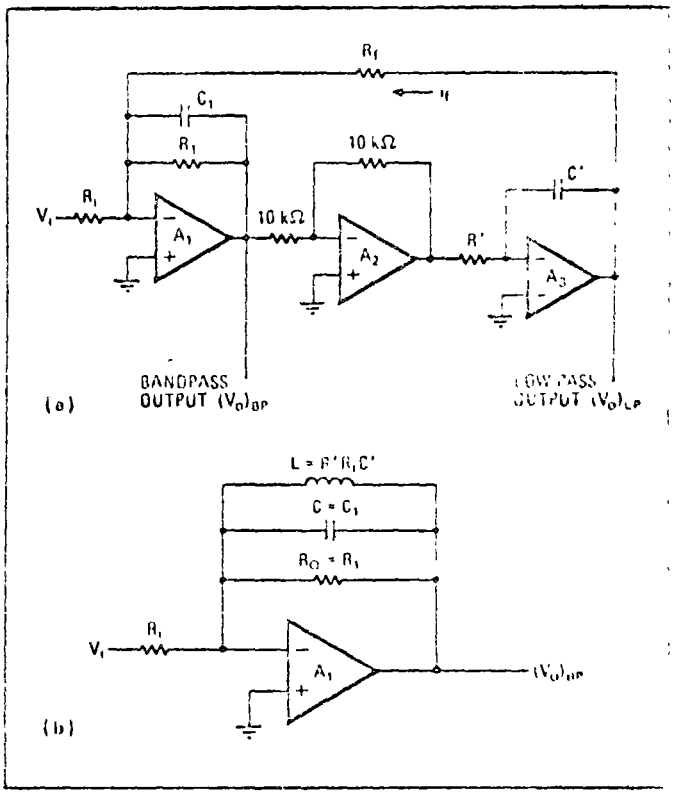
$$Z_L = (V_o)_{BP}/I_f = sR'R_fC'$$

showing Z_L to be inductive in nature. Therefore, amplifiers A_2 and A_3, and feedback resistor R_f can be replaced with the equivalent inductance:

$$L = R'R_fC' \qquad (1)$$

connected in a negative feedback loop around amplifier A_1. Now the general form of the active resonator can be drawn as depicted in Fig. 1(b).

Identifying equivalent inductance L is the key to deriving the active resonator model. Once L is defined in terms of existing components in an active filter section,



1. Resonator model. Biquad filter section (a) can be reduced to active resonator model (b) by replacing amplifiers A_2 and A_3 + equivalent inductance L. This simulates L with non-inverting integrator in negative feedback loop, but other techniques can be used. Very high but lossless inductances can be realized. Single-amp resonator can be treated as complete filter section.

the active resonator model can be used to represent that particular active filter section.

Since L is known for the three-amplifier biquad network, it can be handled as a single-amplifier circuit. This reduces analysis complexity and allows the designer to concentrate on his over-all filter requirements without being unduly concerned with the details of each filter section.

For the biquad filter, inductance L may be simulated in several ways by using different non-inverting integrators in a negative feedback loop around an operational amplifier.[2] Of course, any other technique for simulating a stable inductance is also suitable for the biquad network or whatever filter section is being modeled as an active resonator.

Because L is simulated, its inductance can be very large and yet remain absolutely lossless if ideal amplifiers are used. Although ideal operational amplifiers are fictitious, practical op amps can approach the ideal so that inductance L stays virtually pure (lossless). This is true whenever resistance into the summing junction is an order of magnitude less than the amplifier open-loop input impedance, and when the gain of the feedback loop is high enough to prevent open-loop rolloff from affecting desired Q.

Therefore, assuming that loop gain and amplifier input impedance are sufficiently large, the only lossy element in the network is the parallel resistor, R_Q. It can be regarded as the Q-setting resistor, even though the product of R_QC really determines the 3-decibel bandwidth, and both the R_QC and the LC products establish the Q of the active resonator.

Matching the transfer function

The transfer function of the resonator's tuned circuit must be identical to that of its passive counterpart. For the entire resonator of Fig. 1(b):

$$V_o/V_i = s/R_iC(s^2 + s/R_QC + 1/LC)$$

Analyzing this function in the complex s-plane yields the graph of Fig. 2(a). The location of the complex-conjugate pair of poles is determined by the roots of the denominator, while the positions of two transmission zeros (roots of the numerator) are fixed at frequencies of zero and infinity.

This means that the logarithmic magnitude response has a bandpass characteristic with a shape as illustrated in Fig. 2(b). The slope of each curve in the vicinity of resonant frequency f_o is a function of Q. The slope away from resonance is eventually 6 dB per octave because of the zeros that are located at zero and infinity.

The transfer function of a passive parallel RLC network can be written as

$$G(s) = hs/(s^2 + \Delta\omega s + \omega_o^2)$$

where h is the attenuation factor of the network, and $\Delta\omega = \omega_o/Q$. Comparing the coefficients of G(s) to the coefficients of V_o/V_i for the active resonator yields:

$$\omega_o = 1/(LC)^{1/2} \quad (2)$$

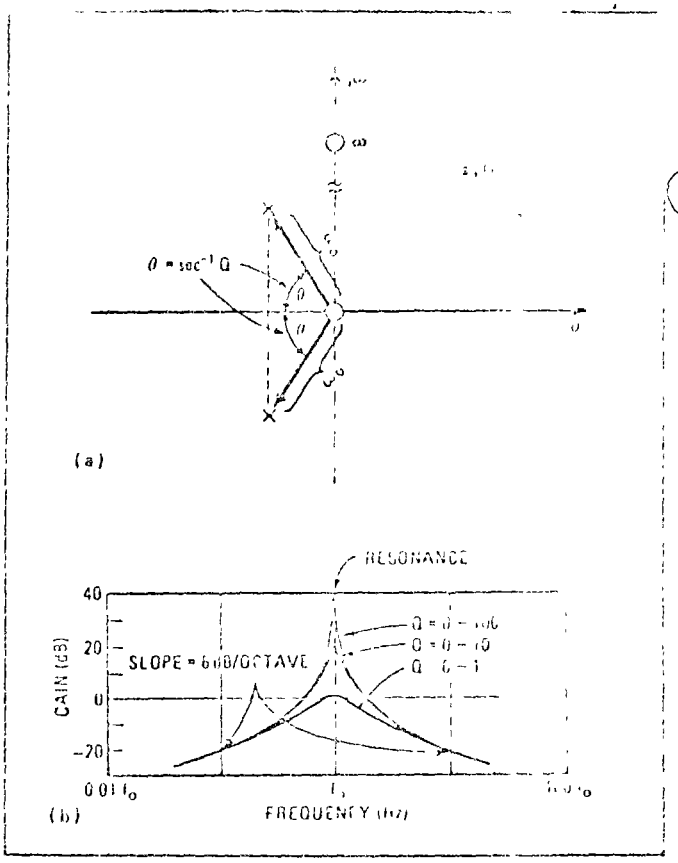
and,

$$\Delta\omega = 1/R_QC \text{ or } Q = \omega_oR_QC \quad (3)$$

and:

$$h = 1/R_iC$$

The magnitude response of G(s) reaches a maximum at $\omega = \omega_o$, and the 3-dB bandwidth is determined by the



2. **Resonator response.** Characteristic behavior of active resonator is identical to that of tuned RLC circuit. Pole-zero plot (a) illustrates bandpass nature of resonator transfer function—the two zeros, two complex-conjugate poles and two zeros. Magnitude of pole vector is fixed by radian center frequency ω_o, while vector direction is function of Q. Slope of resonator magnitude response (b) goes from 0 on Q near resonance and then becomes a constant value.

$\Delta\omega$ coefficient of s in the denominator. At $\omega = \omega_o$, response magnitude becomes:

$$A(\omega_o) = h/\Delta\omega$$

For the active resonator, the response magnitude at ω_o is found by substituting $h = 1/R_iC$ and $\Delta\omega = 1/R_QC$ in this last equation. Then:

$$A(\omega_o) = R_Q/R_i \quad (4)$$

Since the impedance, at resonance, of a parallel tuned LC network with lossless inductors is infinite, the closed-loop gain of the active resonator at resonance is simply equal to a resistance ratio. The active resonator then, has all the properties of a parallel RLC network and can be described in familiar terms once inductance L is identified.

Designing with the resonator

The placement of poles and zeros in the complex-frequency plane fully defines the shape of a filter's response. Furthermore, the locations of these poles and zeros are determined strictly by the Q and ω_o of the transfer function. And since Q and ω_o are known for the active resonator, complete active filter networks can now be designed.

In general, filter design with either active or passive sections is a matter of obtaining the best curve fit over a band of frequencies for a given set of specifications. The designer usually begins by searching through tables or

Bandpass transformations

The appropriate low-pass approximation function for transforming to a second-order bandpass function has a single pair of complex-conjugate poles in the left-hand s-plane. To transform fourth-order functions, the transformation equations for the second-order functions are used twice.

Transforming each low-pass complex-conjugate pole (a) into its bandpass equivalent requires six parameters, the over-all Q of the bandpass filter at its center frequency (Q_c), the bandpass center frequency (f_o), and the real and imaginary parts of the two low-pass poles.

Since the vectors drawn from the origin to the poles in (a) are defined in terms of Q and f_o, it is convenient to write the transforms with Q and f_o as dependent variables. As shown in (b), the low-pass complex-conjugate pole pair transforms into the bandpass plane as two pairs of complex-conjugate poles and two pairs of zeros.

The bandpass pole Qs are identical, and the center frequencies are geometrically symmetrical about the center frequency of the over-all filter. The zero pairs are located at $\omega = 0$ and $\omega = \infty$, thereby establishing the bandpass character. Further, for each pair of complex-conjugate poles and each pair of zeros, there is a filter section with Q and f_o given by the Q and f_o of the transformed pole pair.

The bandpass Q transformation for a low-pass complex-conjugate pole pair can be written as

$$Q_o = \left[\frac{4 + ry + (r^2y^2 + 8ry - 16y + 16)^{1/2}}{8y}\right]^{1/2}$$

Here, y is defined as:

$y = (Re/Q_c)^2$

where Re is the real part of the low-pass pole pair, and Q_c is the cutoff-frequency Q. And r is defined as:

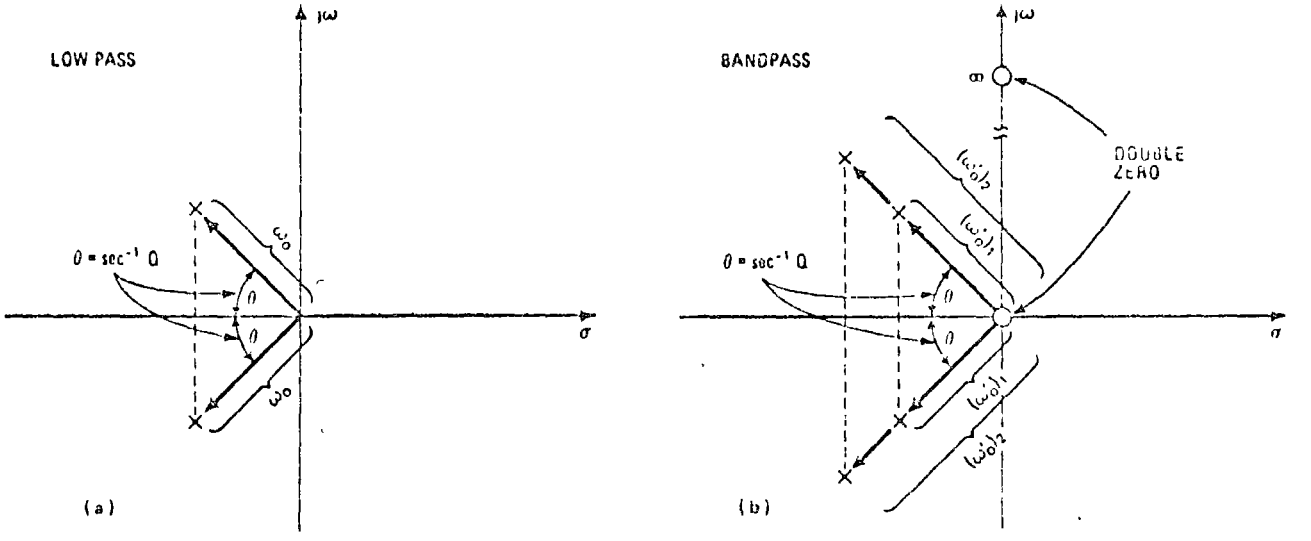
$r = 1 + (Im/Re)^2$

where Im is the imaginary part of the low-pass pole pair. The f_o transformation is

$(f_o')_1 = [Q_p y^{1/2} + (Q_p^2 y - 1)^{1/2}]f_o$

$(f_o')_2 = f_o/[Q_p y^{1/2} + (Q_p^2 y - 1)^{1/2}]$

where $(f_o')_1$ and $(f_o')_2$ are the resonant frequencies of the bandpass filter sections, and f_o is the resonant frequency of the low-pass filter.



by using a computer program to find the mathematical function that most closely approximates his requirements. In doing so, he may select any one or a combination of such well-known functions as Butterworth, Chebyshev, or Bessel.

Once the function or functions are chosen, the designer decides on the order of the filter, based on characteristics such as shape, minimum stopband attenuation, maximum passband ripple, group delay, and phase response. The order of a filter function fixes the number of sections needed for a given response. And the coefficients of the filter's characteristic equation determine how each section is to be tuned for Q and f_o.

As an example, a typical fourth-order bandpass filter—the type frequently used in low-speed telephone data communications systems—illustrates designing with the active resonator. Suppose the specifications are a center frequency (f_c) of 2,125 hertz, an over-all passband gain [$A(\omega_o)$] of 200 (46 dB), a 3-dB bandwidth (Δf_3) of 400 Hz, a minimum stopband attenuation (A_{min}) of 60 dB at a lower cutoff frequency (f_{l_0}) of 1,270 Hz, a maximum passband ripple (A_{max}) of 0.1 dB, and geometrical symmetry.

First, the filter type and function order that best fit the specifications must be found. To do this, the bandwidth at -60 dB (Δf_{60}) is computed from the upper (f_u) and lower (f_{l_0}) frequencies about geometric mean f_c:

$f_u = f_c^2/f_{l_0} = (2,125)^2/1,270 = 3,560$ Hz

Then, for this case,

$\Delta f_{60} = f_u - f_{l_0} = 3,560 - 1,270 = 2,290$ Hz

And the center-frequency Q (Q_c) of the entire filter is,

$Q_c = f_o/\Delta f_3 = 2,125/400 = 5.32$

Shape factor Ω_s is determined next:

$\Omega_s = \Delta f_{60}/\Delta f_3 = 2,290/400 = 5.13$

The design step that follows often involves the transformation of a normalized filter function into the s-plane filtering plane. After transforming and denormalizing this function, the designer can tune each resonator to a particular Q and cutoff frequency. Tables of transfer functions are usually written for low-pass functions so that realizing other filter types requires transforming the low-pass function into the desired function.

Using the computed value of Ω_s and specified values of A_{max} and A_{min}, and published filter data[4] shows that a fourth-order Chebyshev filter will satisfy the example's skirt, bandwidth, and ripple requirements. The normalized coefficients of the low-pass Chebyshev function are found in a table of low-pass Chebyshev polynomials.[4] For a ripple of 0.1 dB and an order of four, the filter's characteristic equation is given as:

$$D(s) = (s^2 + 0.558s + 1.153)(s^2 + 1.616s + 0.789)$$

Solving for the roots of D(s) yields:

$$s_{A1,A2} = -0.229 \pm 1.05j, \; s_{B1,B2} = -0.808 \pm 0.369j$$

These low-pass roots contain two complex-conjugate pole pairs, which transform (see panel, "Bandpass transformations") into bandpass equivalents of four complex-conjugate pole pairs and eight zeros. Since there are four pairs of poles, four active resonators are needed to attain the requirements.

Finding resonator components

From the low-pass-to-bandpass transform equations in the panel, the values of Q and f_o can be computed for each resonator in the bandpass filter. Low-pass roots s_{A1} and s_{A2} characterize the first two resonators.

$Q_1 = 23.3, (f_o)_1 = 2,350$ Hz

$Q_2 = 23.3, (f_o)_2 = 1,925$ Hz

while s_{B1} and s_{B2} characterize the last two resonators:

$Q_3 = 6.6, (f_o)_3 = 2,135$ Hz

$Q_4 = 6.6, (f_o)_4 = 2,120$ Hz

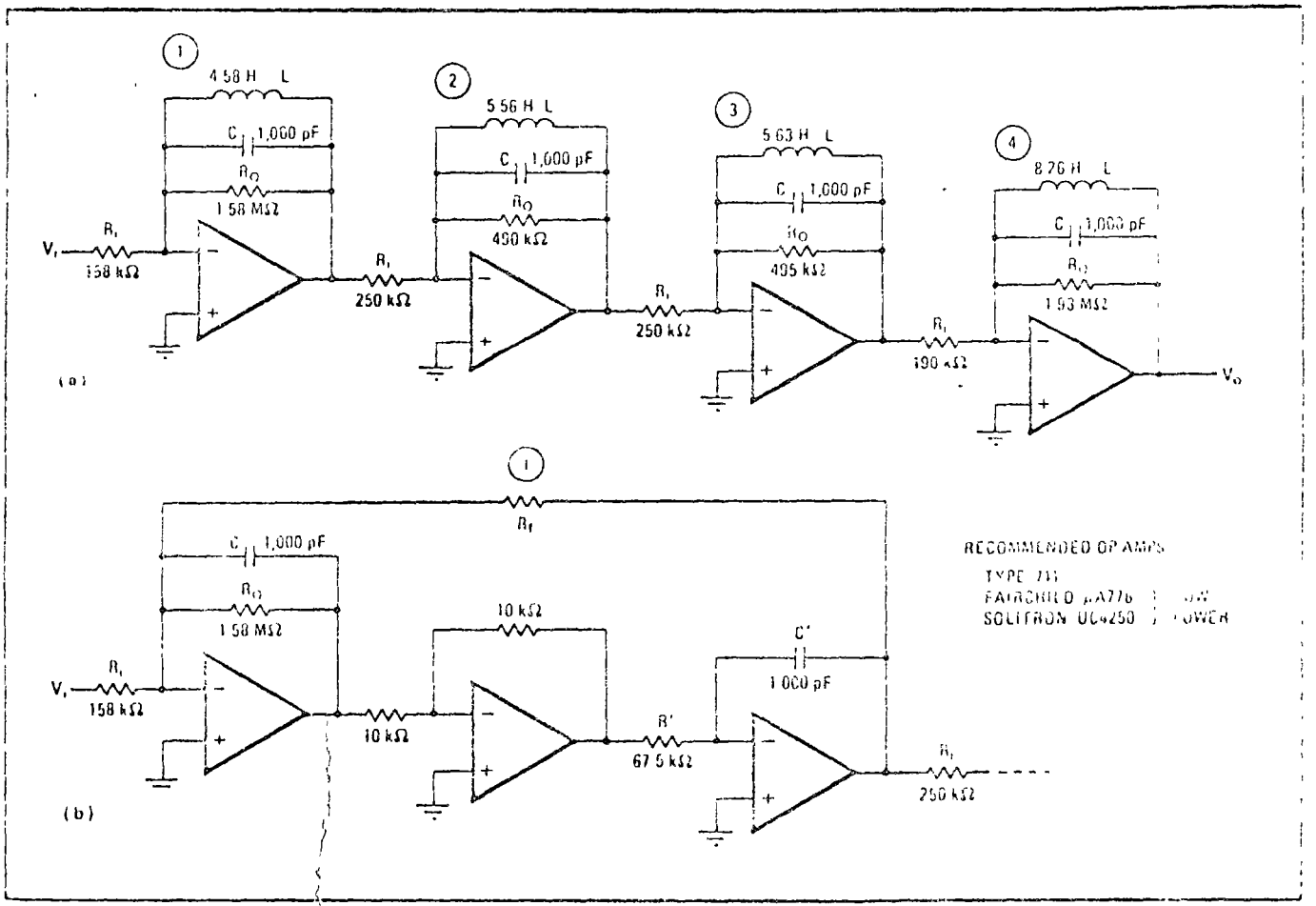
Off-the-shelf resonators

Packaged active resonators [illegible] product lines from more than a dozen [illegible] almost reduce active filter design to a [illegible] sistor selection. Some manufacturers [illegible] lines of active resonators as universal [illegible] the circuit function is the same.

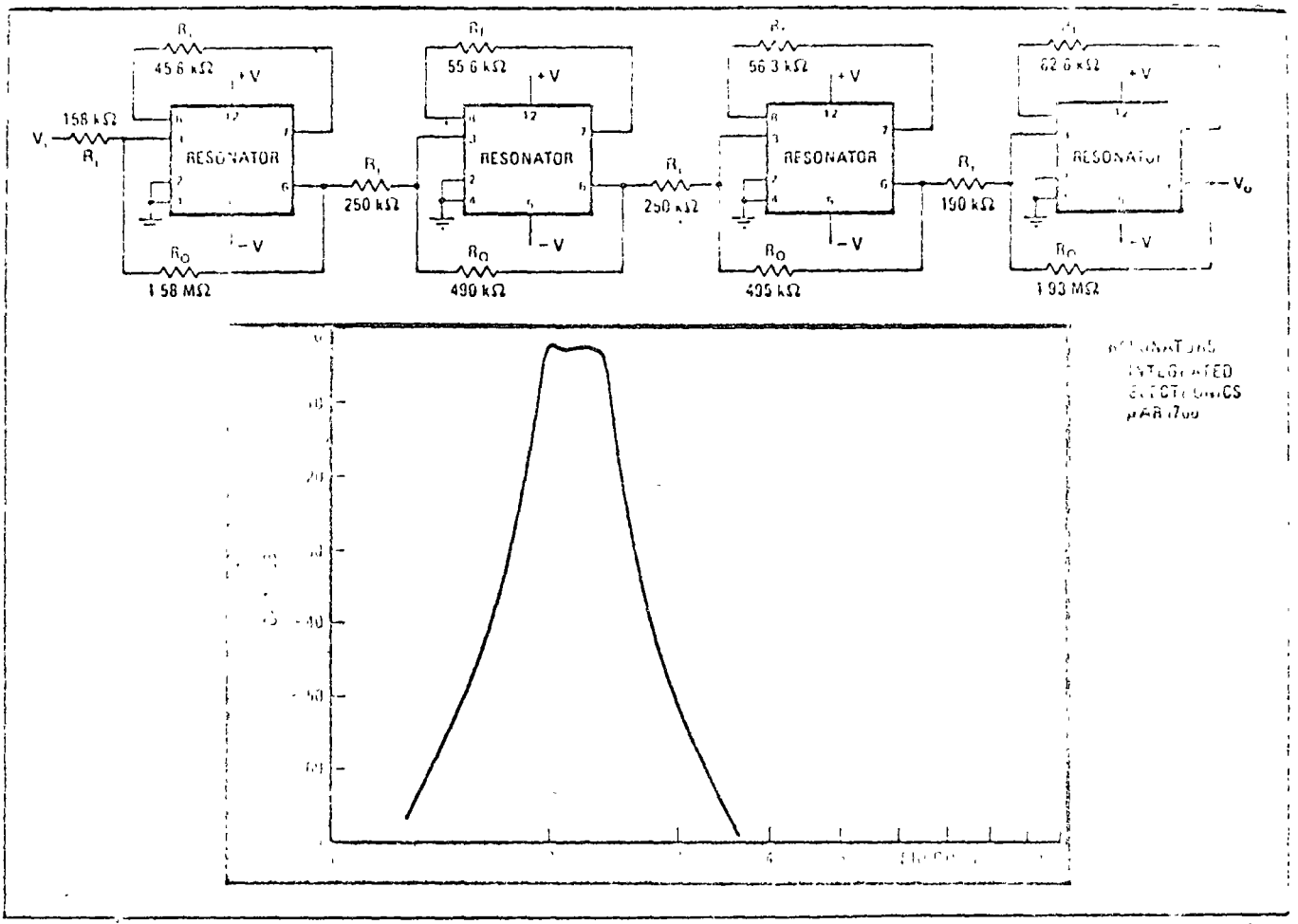
The larger suppliers include Beckman [illegible] Inc., Fullerton, Calif., Datel Systems [illegible] Mass., Kinetic Technology Inc., Santa [illegible] Calif., Optical Electronics Inc., Tucson, Ariz. and [illegible] conductor division, Lawndale, Calif.

A standard family of hybrid microcircuit active resonators also is offered by Integrated Electronics Inc., principally for use in audio and subaudio applications. In large quantities, they range in price from about $5 to $8.

Figure 3(a) shows the bandpass filter configuration using the active resonator representation. It should be remembered that the resonator model employs an equivalent inductance requiring practical simulation and that each resonator section actually consists of three amplifiers and associated circuitry, as noted in Fig. 3(b) for the input resonator. Once the components for the resonators are known, those required to complete each



3. From model to design. Fourth-order bandpass filter (a) is represented by four cascaded resonators. Each resonator, with its simulated inductance, actually requires three amplifiers (b), making 12 op amps necessary for entire filter. Component values can be found once Q and f_o are known for each resonator. Capacitor values are assigned for computation convenience. R_Q principally determines Q of resonator.



4. Ready-made resonators. Active filter design is considerably simplified by using packaged resonators that are available for a number of filtering functions. Those in this diagram are biquad networks connected to realize bandpass filter of Fig. 3. Only three components must be added to each package—R_i for gain adjustment, R_Q to fix resonator Q, and R_f to set resonant frequency.

filter section can be found.

To keep the analysis simple (neglecting the input impedance of practical operational amplifiers), a convenient value is chosen for capacitor C. Generally, C should vary between 800 and 1,000 picofarads for resistor values to remain reasonable. By letting C = 1,000 pF and computing the radian center frequency ($\omega_o = 2\pi f_o$) for each resonator, L can be found from Eq. 2:

$$L = 1/\omega_o^2 C$$

The value of resistor R_Q is determined with Eq. 3:

$$R_Q = Q/\omega_o C$$

Since there are four resonators and the over-all required gain is 200, then each resonator must provide a gain of 50. Eq. 4 becomes:

$$A(\omega_o) = R_Q/R_i = 50$$

which can be solved for input resistor R_i:

$$R_i = R_Q/50$$

After the component values for the four resonators are computed, the other components needed to simulate inductance L can be found. Again, the value of 1,000 pF is chosen for capacitor C′ to simplify the calculations. Feedback resistor R_f is set equal to resistor R′:

$$R_i = R' = R$$

so that Eq. 1 can be used to find R:

$$R = (L/C')^{1/2}$$

Active resonators, however, are available as standard products from several manufacturers, as noted in the panel, "Off-the-shelf resonators." These packaged circuits often reduce the final design step to choosing resistor values, once Q and f_o are known.

For instance, the μAR 1700 resonator from Integrated Electronics is a biquad network that can be used for the resonator sections in the fourth-order bandpass filter design example. Components C, L, R_Q, and R_i are computed as before; of these, only R_Q and R_i are required for the actual filter implementation, as illustrated in Fig. 4. None of these component values differ from those already calculated.

Next, the "internal" resonator parts are found. In addition to setting C′ = 1,000 pF, R′ is assigned a value of 100 kilohms for convenience, and then R_f is computed from Eq. 1:

$$R_f = L/R'C'$$

The resulting values of R_f are noted in the figure. When the μAR 1700 resonator is used to build an active filter, R_Q effectively sets resonator Q, and R_f effectively sets resonator f_o. The magnitude response of the fourth-order bandpass filter is also illustrated.

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Noise and Dynamic Range of Active Filters with Operational Amplifiers

JACEK ŻURADA AND MICHAŁ BIAŁKO

Abstract—Output noise spectral density and total rms output noise of filters with operational amplifiers can be determined by means of transformation of passive part of the filter under the condition that the noise model of the operational amplifier is known. This problem can be solved through sequential calculation of spot noise factors for cascaded passive and active parts of the transformed filter without feedback. In this paper, this approach is used for comparison and discussion of dynamic range of low-pass op-amp filters with positive and negative feedback.

I. Introduction

THE SIGNAL-TO-NOISE RATIO and the dynamic range of the filter is determined through its output noise spectral density and the rms noise voltage value. The noise performance of each filter can be analyzed directly as indicated by the formula [1], [2]

$$V_{n\,out}^2(\omega) = \sum_{j=1}^{k} |T_{i,j}(j\omega)|^2 i_{j,n}^2(\omega) + \sum_{i=1}^{m} |T_{v,i}(j\omega)|^2 v_{i,n}^2(\omega) \tag{1}$$

where $T_i(j\omega), T_v(j\omega)$ are transfer functions from a noise current and noise voltage generators having efficiency i and v, respectively.

The method shown in [2] introduces some simplification to calculations given by (1). Some typical transfer functions $T(s)$ and a list of integrals for the filters under consideration can be formulated.

The concept of adjoint network [3] can also be used for calculation $V_{n\,out}^2(\omega)$. Both approaches make the evaluation of filter noise a difficult task. In this paper a new method for noise investigation of active filters is developed. In comparison with two methods mentioned above, this method gives a systematic noise factor characterization for every filter section and for overall filter network as well. Other noise characteristics for active filters can be easily obtained based on noise factor determination.

II. Noisy Active and Passive Sections

The stationary noise sources within the operational amplifiers may be represented by the equivalent circuit as shown in Fig. 1. It contains a noise free active element with three noise sources appearing at the input. Noise efficiency of each source determines the noise resistance of the op-amp denoted as r_n and its noise conductances denoted as g_{n1}, g_{n2}. If the op-amp with a feedback loop has a gain value K, its noise model can be represented as

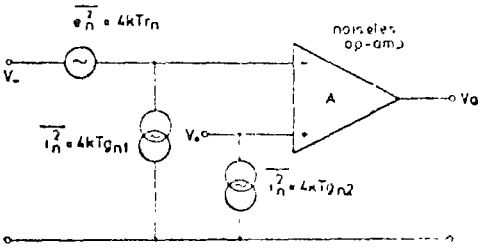

Fig. 1. Equivalent circuit for a noisy op-amp.

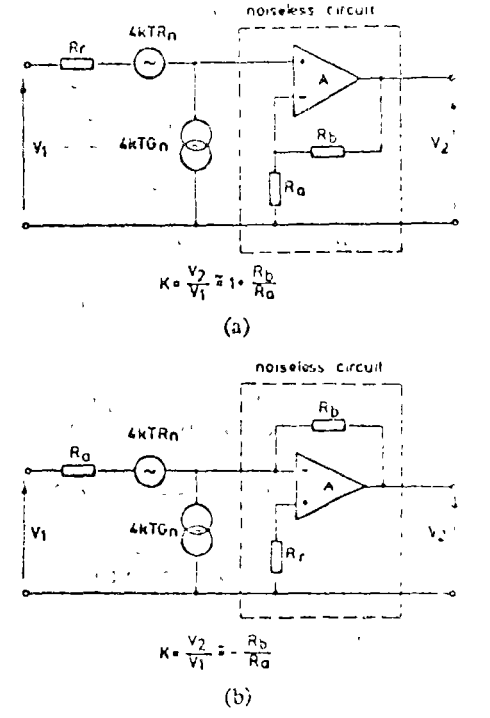

Fig. 2. Equivalent circuit for a noisy VCVS (op-amp) in (a) non-inverting configuration, (b) inverting configuration.

shown in Fig. 2(a) and (b). The equivalent noise resistance R_n and the noise conductance G_n for these two cases of voltage controlled voltage sources using op-amps can be expressed for the circuit of Fig. 2(a) as follows [4] (see Appendix):

$$R_n = r_n + R_r + g_{n1}R_r^2$$
$$G_n = g_{n2} \tag{2}$$

and for the circuit of Fig. 2(b)

$$R_n = \left(1 + \frac{1}{|K|}\right)^2 (r_n + R_r + g_{n2}R_r^2) + \frac{r_n}{K^2}$$
$$G_n = g_{n1} \tag{3}$$

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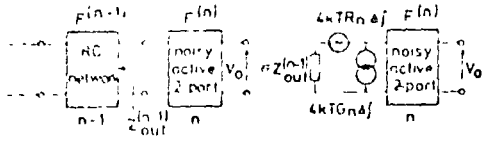


Fig. 3. Equivalent circuits in a chain of passive-active two-ports from a noise factor $F^{(n)}$ equality point of view.

Both formulas (2) and (3) include the influence of noise due to op-amp as well as the noise generated through external resistors R_n, R_p, R_r.

The introduction of r_n, g_{n1}, g_{n2} do not eliminate the possibility of considering the flicker noise by this method. These equivalent noisy elements can be regarded as the frequency dependent values up to their corner frequencies f_{r_n}, f_{g_n} according to following formulas

$$r_n = r_{n0}\left(1 + \frac{f_{r_n}}{f}\right)$$

$$g_{nk} = g_{n0k}\left(1 + \frac{f_{g_n}}{f}\right), \qquad \text{for } k = 1,2 \tag{4}$$

where r_{n0}, g_{n0k} denote constant values of noise resistance and conductances, respectively, for higher frequencies where no flicker noise can be observed.

If the amplifier works as the nth section of the chain-like network shown in Fig. 3, then the noise factor is given by the formula

$$F^{(n)} = 1 + \frac{R_n}{\operatorname{Re} z_{\text{out}}^{(n-1)}} + G_n \frac{|z_{\text{out}}^{(n-1)}|^2}{\operatorname{Re} z_{\text{out}}^{(n-1)}} \tag{5a}$$

where $z_{\text{out}}^{(n-1)}$ denotes the output impedance of $(n-1)$th passive section connected to the voltage amplifier. The real part of that impedance $\operatorname{Re} z_{\text{out}}^{(n-1)}$ is treated here as the internal source resistance. Applying expressions (2) and (3) for the formula (5a), the noise factor can be obtained for the circuit of Fig. 2(a)

$$F^{(n)} = 1 + \frac{R_n + R_r + G_n|z_{\text{out}}^{(n-1)} + R_r|^2}{\operatorname{Re} z_{\text{out}}^{(n-1)}} \tag{5b}$$

and for the circuit of Fig. 2(b)

$$F^{(n)} = 1 + \frac{R_n + R_n + G_n|z_{\text{out}}^{(n-1)} + R_n|^2}{\operatorname{Re} z_{\text{out}}^{(n-1)}}. \tag{5c}$$

Each passive noisy subnetwork occurring in the Fig. 3 has the noise factor $F^{(i)}$ given by the inverse of its available power gain $G_p^{(i)}$ [5]

$$F^{(i)} = \frac{1}{G_p^{(i)}}. \tag{6a}$$

Expression (6a) can be rewritten in the form

$$F^{(i)} = \left|\frac{z_{\text{out}}^{(i-1)} + z_{11}^{(i)}}{T^{(i)}(j\omega) z_{11}^{(i)}}\right|^2 \cdot \frac{\operatorname{Re} z_{\text{out}}^{(i)}}{\operatorname{Re} z_{\text{out}}^{(i-1)}} \tag{6b}$$

for $i = 1, 2, \cdots, n-1$, where $T^{(i)}(j\omega)$ and $z_{11}^{(i)}$ denote voltage frequency response and open-circuited input impedance of the ith section, respectively.

III. Calculation Method for the Noise Factor of the Filter

The structure of the active filter with a single voltage-controlled voltage source (VCVS) considered here is shown in Fig. 4(a). This network configuration can be transformed to its quasi-equivalent noise factor network without feedback which is shown in Fig. 4(b) [6]. This allows the determination of the noise factor using well-known Friis formula

$$F = F^{(1)} + \sum_{i=2}^{n} \frac{F^{(i)} - 1}{\prod_{j=1}^{i-1} G_p^{(j)}} \tag{7}$$

where F is the noise factor of the overall network without feedback. The passive network can then be treated as a chain-like connection of $n-1$ subnetworks with noise factors $F^{(i)}$ for $i = 1, 2, \cdots, n-1$, connected with the nth active element with known noise factor $F^{(n)}$. In the case discussed above the overall noise factor given by formula (7) can be calculated using expression (6a). The result has the form

$$F = F^{(1)} \cdot F^{(2)} \cdots F^{(n)}. \tag{8}$$

Then using the formulas (5), (6b), (8), the noise factor can be easily found after division of the transformed network without feedback into a convenient sequence of passive sections terminated by a noisy VCVS amplifier based on the (6b) or on a noise factor definition, $F^{(i)}$ values for widely used passive sections can be readily calculated [7]. Some of them are summarized in Table I with the assumption that these sections are driven from a voltage source with a series impedance $z_g = R_g + jX_g$. Output impedances necessary for further calculations using (5), (6b) have been omitted in Table I for simplicity.

It should be noted that the F value of the network is not a final goal of active filter investigation. Based on F value more interesting measures can be found, e.g., broad-band noise factor, signal-to-noise ratio, output noise spectral density, its rms value and dynamic range of the circuit, if a certain output signal level is accepted. Problems with the voltage transfer function of the investigated filter should be taken into account.

IV. Calculation of the Output Noise Level and Dynamic Range for Some Low-Pass Filters

The practical op-amps used in filter synthesis have a finite gain bandwidth (GB) value. Hence in practice the ideal voltage transfer function magnitude $|T_a(j\omega)|$ of the filter takes a nonideal form $|T'(j\omega)|$

$$|T'(j\omega)| = \frac{|T_a(j\omega)|}{\left[1 + \left(\frac{f}{f'}\right)^{2n}\right]^{1/2}} \tag{9}$$

where $T_a(s)$ is the transfer function with slightly displaced zero and pole positions compared to their nominal positions given by $T(s)$. Frequency f' is a 3-dB corner frequency

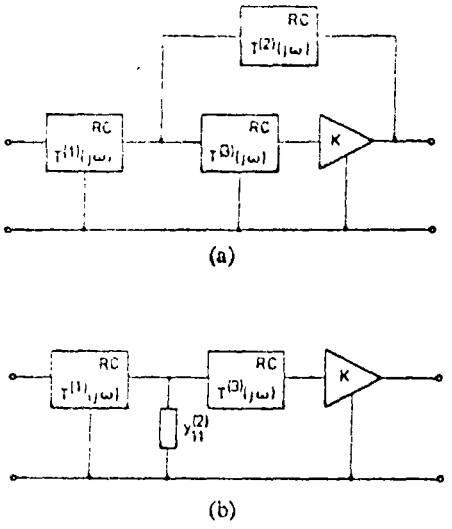
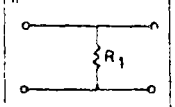
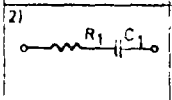
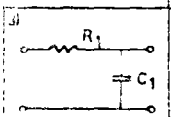
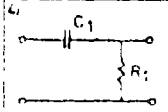
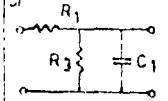
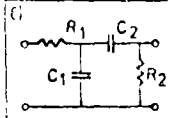
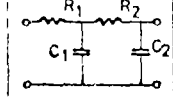


Fig. 4. (a) Synthesis model with VCVS. (b) Its equivalent noise factor configuration.

TABLE I
NOISE FACTORS FOR SOME *RC* SECTIONS

RC network	$F^{(1)}$
1) 	$1+\frac{R_g}{R_1}+\frac{x_g^2}{R_1 R_g}$
2) 	$1+\frac{R_1}{R_g}$
3) 	$1+\frac{R_1}{R_g}$
4) 	$1+\frac{R_g}{R_1}+\frac{R_1}{R_g}+\frac{\omega_0^2}{\omega^2}$ $\omega=\frac{1}{R_1 C_1}$
5) 	$1+\frac{R_1}{R_g}+\frac{R_1^2}{R_3 R_g}+\frac{R_g+2R_1}{R_3}$
6) 	$\left(1+\frac{R_0}{R_2}+\frac{1}{\omega^2 C_2 R_0 R_2}\right)\left(1+\frac{R_1}{R_g}\right)$
7) 	$\left(1+\frac{R_2}{R_0}\right)\left(1+\frac{R_1}{R_g}\right)$
8)	$R_0=\frac{R_1+R_g}{1+\omega^2(R_1+R_g)^2 C_1^2}$

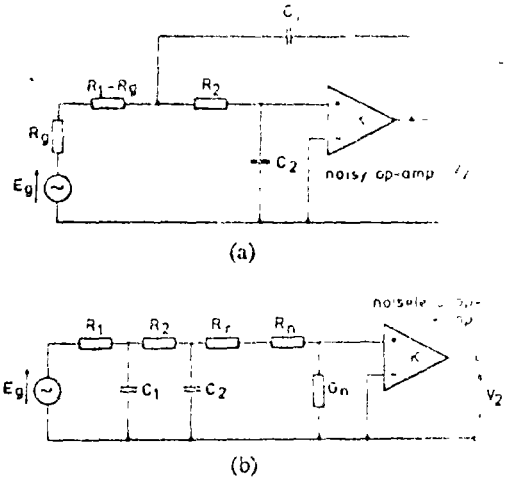


Fig. 5. (a) Sallen and Key low-pass filter. (b) Its noisy equivalent network.

resulting from the finite GB value of the op-amp and can be approximated as

$$f' = \begin{cases} \dfrac{a\ \mathrm{GB}}{|K|}, & \text{for Fig. 2(a)} \\ \dfrac{b\ \mathrm{GB}}{K+1}, & \text{for Fig. 2(b)} \end{cases} \tag{10}$$

where a,b are proportionality factors.

The frequencies f' given by (10) are of importance when the broad-band noise of the filter is considered. Values a,b are equal to 1 or are higher depending of the type of the filter.

The noise voltage spectral density $V_{n\,\mathrm{out}}^2(\omega)$ of the filter can be found using its voltage frequency response $T'(j\omega)$ as follows:

$$V_{n\,\mathrm{out}}^2(\omega) = 4kTR_g F|T'(j\omega)|^2. \tag{11}$$

The rms noise voltage E^2 is then easily expressed as the integral between $\omega = 0$ and $\omega = \infty$

$$E^2 = 4kTR_g \int_0^\infty F(\omega)|T'(j\omega)|^2\, d\omega \tag{12}$$

For the second-order filter the rms noise voltage value can be approximately calculated from the following formula

$$E^2 \cong 4kTR_g \int_0^{f'\cdot\pi/2} F(\omega)|T(j\omega)|^2\, df. \tag{13}$$

Based on the outlined method the output noise level and the dynamic range of Sallen and Key low-pass filters has been considered and compared.

The F value of the filter shown in Fig. 5 is given by the following expression obtained by inspection of the network [7] from Table I

$$F(R_1) = \left(1+\frac{R_2}{R_0}\right)\left(1+\frac{r_n + R_r + g_n|z_{ou}+R_r|^2}{R_{\mathrm{out}}}\right). \tag{14}$$

$F(R_1)$ is the noise factor for the filter assuming that R_1 is

the voltage source internal resistance. The above noise factor takes a nearly constant value $F = F_0$ for frequencies in the passband. Setting $\omega = 0$ and $R_r = 0$ in (14), F_0 can be obtained as

$$F_0(R_1) = 1 + \frac{R_2 + r_n + g_n(R_1 + R_2)^2}{R_1}. \quad (15)$$

The rms noise voltage value E^2 given by (13) then takes a form

$$E^2 = 4kTR_g f_0 F_0 |T(j\omega)|^2_{\omega=0} + E_{SB}^2 \quad (16)$$

where f_0 is the pole frequency of the low-pass filter, $|T(j\omega)|_{\omega=0}$ denotes the magnitude of its voltage frequency response between output and the source for the passband frequencies. The first term of formula (16) can be interpreted as a broad-band noise in the passband of the filter $\langle 0, f_0 \rangle$, while the second as a broad-band noise in the stopband $\langle f_0, f' \cdot \pi/2 \rangle$. These two terms can be easily rearranged to the form (17) after applying formula (15)

$$E^2 = 4kT[R_1 + R_2 + r_n + g_n(R_1 + R_2)^2]K^2 f_0 + 2\pi k T r_n K^2 (f' - f_c). \quad (17)$$

The expression (17) gives an approximated value of the total output noise voltage of the filter. The first and the second term can also be obtained by inspection of noisy elements of the circuit from Fig. 5(b) for the passband and for the stopband, respectively. The application of (17) for the filter shown in Fig. 5 with μA 709 having $r_n = 24.7$ kΩ, $g_n = 20\ \mu$S and $R_1 = R_2 = 17.6$ kΩ, $f_0 = 1$ kHz, $C_1 = C_2$ gives for dynamic range of the filter 109.1 dB for $Q = 1/\sqrt{2}$ and 107.1 dB for $Q = 10$. The output voltage swing is assumed to be $20V_{pp}$. This is not an exact voltage value occurring at the output of the filter with op-amp however. Due to the nonlinearity of the op-amp this level is further strongly limited for each type of the filter. Therefore the results given for the dynamic range can be considered as rather optimistic ones.

The results for E^2 obtained by the described method have been also compared with computation. The output noise voltage spectral density computed using adjoint-network concept program [3] for the filter from Fig. 5 is shown in Fig. 6. Measured points taken for the filter for $Q = 1/\sqrt{2}$ and $Q = 10$ show a good agreement with both curves. Only below $f = 1$ kHz do some differences occur due to the presence of $1/f$ noise. From the computed curves of Fig. 6 it has been calculated through graphical integration that the dynamic range of this filter is 109 dB for $Q = 1/\sqrt{2}$ and 106 dB for $Q = 10$. These results have been directly approximated using the method described and formula (17).

Furthermore, from (17), the noise contribution occurring at the output for all noisy elements is known. In the above type of filter the noise of the passive part of the filter is of importance in the passband, however the noise of op-amp dominates in the stopband. This is only the case occurring in practice when the resistors R_1, R_2 were of kilohm range and $f' \gg f_0$. Then the second term of (17) is dominant and determines the rms noise voltage at the filter output.

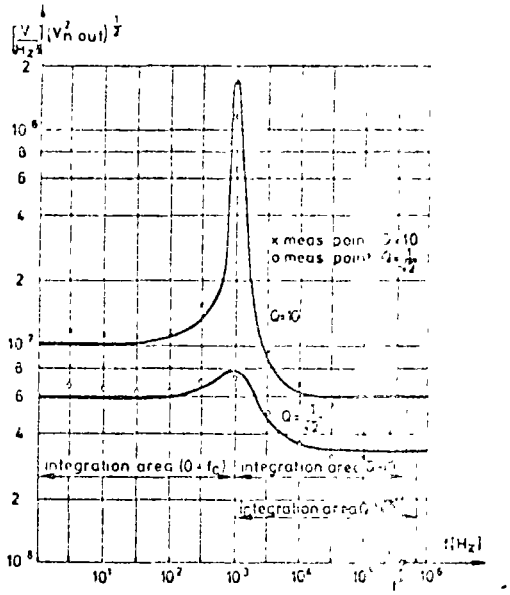


Fig. 6. Output noise voltage spectral density versus frequency for the filter from Fig. 5.

influence of the flicker noise for this type of filter is negligible. The flicker noise remains narrow-band noise with the bandwidth of several kilohertz. Furthermore, it can be shown that the dynamic range for the above type of filters increases with decreasing K of the amplifier. Hence, it depends on the pole Q value of the filter, particularly, when the negative feedback is applied. For a Sallen and Key [8] low-pass filter with $K < 0$ a similar analysis has been made [7]. The dynamic range for this type of filters is of order 100–110 dB for low Q values. However, the dynamic range of a negative feedback filter is further limited for higher Q values. The method presented can be easily applied for filters with voltage controlled current sources having the same type of noise models as VCVS elements realized with op-amps.

V. Summary

The described method of noise calculation gives some specific advantages for RC op-amp filters when compared with the totally algebraic solutions and tabulated integrals in [2]. The results can be obtained and interpreted using Table I and formula (11) after finding the $F(\omega)$ of the transformed filter. In the simple case the noise rms value can also be found by inspection of the transformed network. The method presented here can be extended for other types of single controlled source filters having multiple feedback.

Appendix

The output noise voltage spectral density $V_{n\,out}^2(\omega)$ of the operational amplifier due to its equivalent noise resistance r_n, conductances g_{n1}, g_{n2} and external noisy resistors R_a, R_b, R_r can be expressed, for the Fig. 2(a), as follows:

$$V_{n\,out}^2(\omega) = 4kT[r_n + R_r + g_{n1}(R_a \parallel R_b)^2 + (R_a \parallel R_b) + g_{n2}|z|^2]K^2 \quad (A1)$$

where $4kT = 1.63 \times 10^{-20}$ W, z denotes the impedance seen between noninverting terminal of the op-amp and

The expression (A1) can be interpreted as a sum of noise contributions caused by noisy elements of the single input noninverting voltage source with voltage gain K. Each of these output noise contribution can be replaced by equivalent input noise characteristics. Neglecting the term $4kTR_rK^2$ in (A1) for the noise equivalence considered it can be stated that only the last term of (A1) depends on z value. If the input terminal of the source is open-circuited, then the total noise of the source is only due to the term $4kTg_{n2}/z|^2K^2$, as is seen from the expression (A1). According to general noisy four-pole theory it can be interpreted as the existance in the equivalent circuit of the equivalent noise conductance G_n

$$G_n = g_{n2}. \tag{A2}$$

If the input terminal is short-circuited, the total noise of the source is given by the terms $4kT[r_n + g_{n1}(R_a \parallel R_b)^2 + (R_a \parallel R_b)]K^2$. Therefore, the sum $r_n + g_{n1}(R_a \parallel R_b)^2 + R_a \parallel R_b$ can be treated as the equivalent noise resistance R_n

$$R_n = r_n + g_{n1}R_r^2 + R_r \tag{A3}$$

where

$$R_r = R_a \parallel R_b.$$

In a similar way every noise contribution can be found for the single input source configuration from Fig. 2(b).

Both noise equivalent VCVS are then treated as a cascade connection of the standard noisy four-pole with elements R_n, G_n with the noiseless source having single input impedance equal to infinity. This allows the noise factor determination in a simple manner.

Nomenclature

$V_{n\,out}(\omega), E$	Output noise spectral density, and rms value, respectively.
$T_i(s), T_v(s)$	Transfer function from a noise current and noise voltage generator having efficiency i,v, respectively.
r_n, g_{n1}, g_{n2}	Equivalent noise resistance and noise conductances at the inverting and noninverting input of the op-amp.
f_{rn}, f_{gn}	3-dB corner frequencies of the r_n and g_n values, respectively.
R_n, G_n	Equivalent noise resistance and conductance of the VCVS.
K	Voltage gain of the VCVS.
$F^{(i)}, G_p^{(i)}, T_{(s)}^{(i)}$	Spot noise factor, available power gain, and voltage transfer function of the ith section, respectively.
$Z_{11}^{(i)}, Z_{out}^{(i)}$	Open-circuited input impedance and output impedance of the ith passive section
$F(R), F_0(R)$	Spot noise factor of the filter for $R_g = R$ and its low-frequency value, respectively.
R_g	Series resistance of the voltage source at the input of the filter.
$T(s), T'(s)$	Ideal voltage transfer function of the filter and its frequency scaled transfer
f'	3-dB upper corner frequency of the filter output noise spectral density, resulting from the finite GB value of the op-amp
E_{SB}	Noise voltage rms value at the output of the filter for the stopband frequencies

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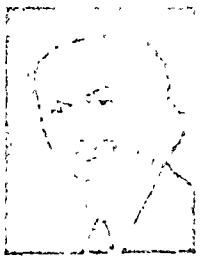
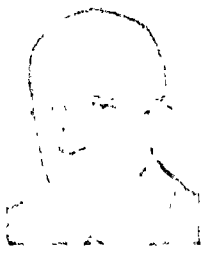
[8] R. P. Sallen and E. L. Key, "A practical method of designing *RC* active filters," *IRE Trans. Circuit Theory*, vol. CT-2, pp. 74–85, Mar. 1955.



Jacek Zurada was born in Sosnowiec, Poland, on July 31, 1944. He received the [illegible] degree in electrical engineering in 1968, from the Politechnika Gdańska, Gdańsk, Poland. In 1974 to 1975, he prepared the Ph.D. on non-ideal behavior of op-amp active filters.

After holding the Postgraduate Fellowship from the Politechnika Gdańska, he joined the staff of this university. He has been concerned in teaching and research with active filters and computer-aided network design. He has written about 10 papers and several unpublished reports. He takes part in Polish-American scientific collaboration supported by the National Science Foundation, U.S.A. Currently, he is on the teaching staff of the Department of Electrical Engineering, Politechnika Gdańsk, and is with the Research Group on Microelectronics.

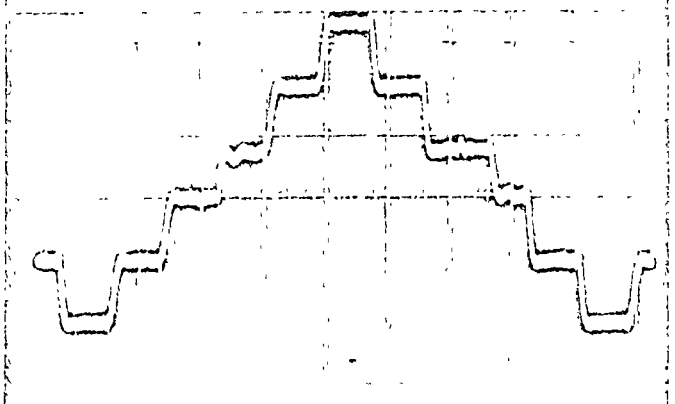


Michał Białko received the [illegible] and M.S. degrees in electronics engineering from Politechnika Gdańska, Gdańsk, Poland, in 1953 and 1955, respectively. In 1961, he obtained the Ph.D. degree in electronics engineering from Politechnika Warszawska, Warsaw, Poland. In 1967, he completed his habilitation work and he received the Docent degree from Politechnika Warszawska, Warsaw, Poland.

Since 1953, Dr. Białko has been on the teaching staff and since 1968, on the professorial staff of Politechnika Gdańska. Since 1972, he has been Professor of Electronics at Politechnika Gdańska. He is the author and coauthor of 3 books and about 100 published research papers on transistor and active *RC* networks. Currently he is the Head of the Laboratory of Electronic Elements and Circuits Technology in Politechnika Gdańska and the Chairman of Senate's Commission for Research and Development of Politechnika Gdańska.

In 1968, 1969, and 1972, Dr. Białko was awarded the distinction prizes by Polish Minister of Higher Education. In 1972 he was also

Digital-to-analog converters trading off bits and bucks



☐ What electronics device has proven so cost-effective over such a range of applications that six times as many are in use today as there were three years ago?

What device is widely accepted without makers having any common agreement about how to produce them and without benefit of any industry standards? Nor has a single maker developed a clearly superior design, nor is there one user large enough to dictate specifications.

Finally, what device, with estimated sales of 120,000 units this year and more growth expected, has moved into the market with low-cost models to anticipate volume requirements and competitive pressures—yet given rise to products with marginal performance? (Or so say some makers about some competitors).

The answer is the digital-to-analog converter (DAC) module.

Once exclusively a measurement and control systems component, the DAC now goes more into such products as X-Y plotters, cathode ray tube display terminals, programable power supplies, and analog-to-digital converters. But lack of electrical, packaging and terminal-connection standards, poor definition of real costs in terms of performance, and technical complexity of the module put the electronics engineer at risk in determining DAC parameters and selecting the proper unit.

All this means that price alone is no guide to the selection of a DAC. By and large, two DACs of the same bit length usually differ in many electrical and performance parameters and options, as well as terminal arrangements, whether they come from different vendors or from two families of DACs made by the same vendor.

Consequently, choosing a DAC module—and so opting to deal with a particular vendor—leaves the system designer has to lay out the circuit board for a sole-source unit. However, if he is concerned about continued availability or long-term performance of the sole-source DAC, the designer can go to the expense of adding extra conductors and holes to his circuit board to make it compatible also with a "second-source" DAC. Or he can search out another vendor who can adapt this unit to be compatible with the first selection.

While competition has little effect on pricing, therefore, the major price determinants are completeness and freedom from error. By completeness of DAC modules is meant whether all of the electronic niceties required to convert a digital data word into a usable analog signal are actually in the package or whether outboard components—an input register or an output amplifier are examples—must be added and paid for by the user.

Six performance parameters

There is a very sharp increase in price as DAC performance improves. The major performance parameters are resolution, accuracy, linearity, temperature stability, settling time, and freedom from switching transients.

In performing conversion, the DAC turns a parallel n-bit data word into 2^n discrete levels of analog output. Thus, a 10-bit DAC has 2^{10}, or 1,024, output levels. The reciprocal of the number of output levels is the DAC's *resolution*. Thus, the resolution of a DAC is implicit in the number of input bits (see table of Resolution Equivalents). Because the smallest change in analog output results from the binary change (from a 1 to and, for example) of the least significant bit (LSB) in the data word, the term "1 LSB" is a customary way of stating resolution, since it is independent of the bit-length of the data word. The LSB is equivalent to stating the percent of full scale for the analog output.

The DAC's *accuracy* refers to net error in the analog output for a given input code. For example, if a 10-bit DAC ought to have a 10-volt output for a full-scale digital word but yields only 9.5 volts because of poor calibration, the error is 5%. While the DAC will provide the necessary 1,024-step resolution, each step will be correspondingly inaccurate. Customarily, accuracy is specified in terms of ±½ LSB error, meaning the accuracy remains consistent with the DAC's resolution capability. Practically speaking, accuracy cannot be better than resolution, but it can be worse.

Linearity defines the constancy of the input-output ratio of the full range of values. A DAC can be linear, but inaccurate.

Changes in the DAC's operating temperature create output error. The better the *temperature stability*, the wider the temperature range that it is possible for the

DAC to tolerate without producing excessive error.

Settling time expresses the delay between introduction of the data word and the analog output reaching some final value. The shorter the setting time, the faster the throughput rate for data conversion.

Switching operations inside the DAC cause transient spikes known as *glitches*. For some applications it's necessary to add a deglitcher circuit to remove them.

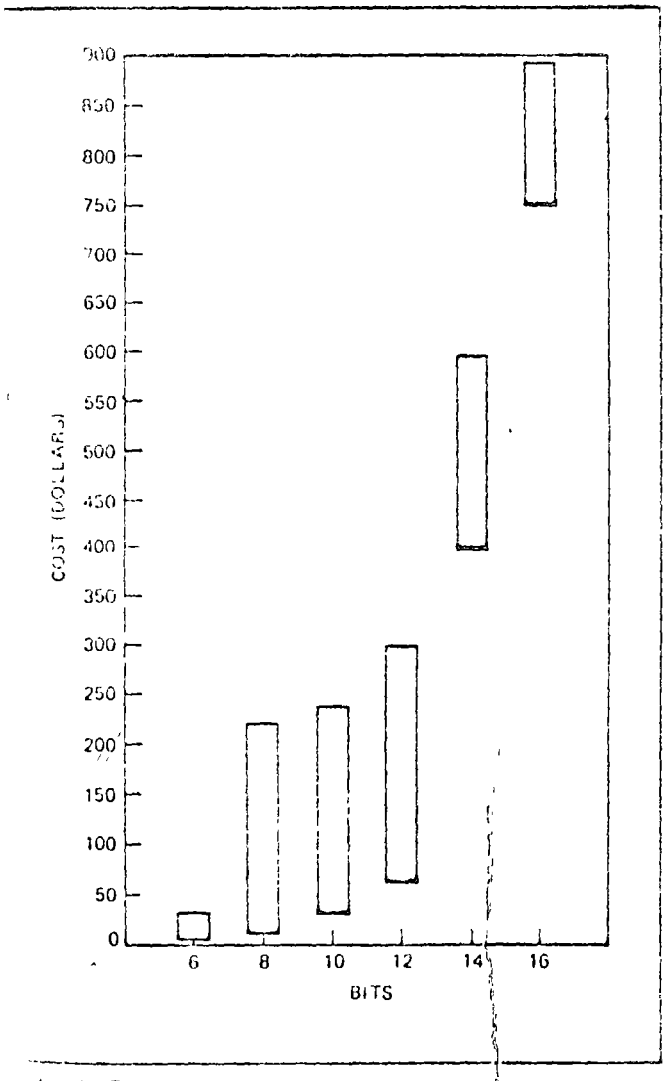
An indication of how the parameters relate to price can be gained from Fig. 1, which is based on information obtained from many manufacturers and charts the lowest and highest prices for DACs ranging from 6 to 16 bits. This price structure reveals the cost to the user of the technological demands placed on the maker to satisfy specific applications. The lowest price for each DAC size can be interpreted as the basic cost of obtaining conversion and resolution. The top of each bar can be construed as the maximum cost of providing maximum completeness, nominal accuracy, temperature stability, deglitching, and so forth. It is interesting to note that this extra cost, about $200, is almost independent of the DAC's bit size—except for 6-bit DACs.

The cost trend for increased resolution is clearly demonstrated in Fig. 2, which uses the data of Fig. 1 to plot cost per bit vs bits. Given the data as expected, the cost per bit goes up with the number of bits—first gradually, then sharply—reflecting both the increased cost of higher-quality components and more exacting manufacturing and testing procedures.

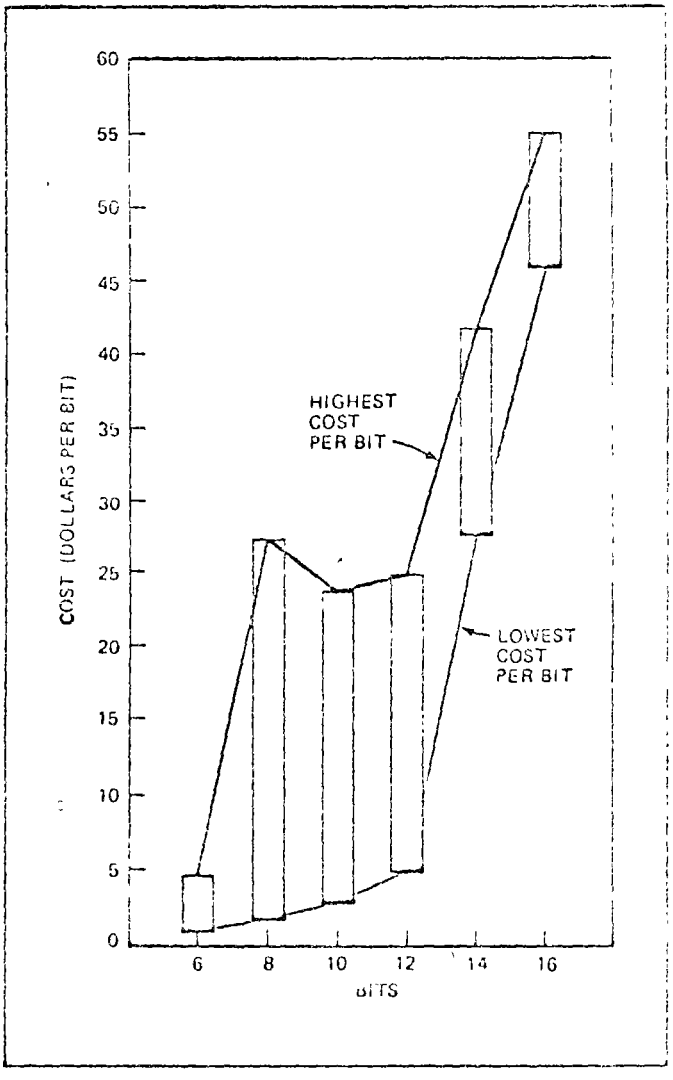
Figures 1 and 2 also show that 6-bit, 14-bit, and 16-bit DACs are each in a class by itself, while 8-bit, 10-bit, and 12-bit DACs together form another class. In fact many makers offer 8-, 10-, and 12-bit DACs in the same family of devices, having started with a 12-bit design and then modified the design to make lesser-bit units.

DACs having 14 and 16 bits provide so much resolution that they are most often used in exotic laboratory and scientific investigations and for applications having a wide dynamic range of digital values—65,536-to-1 for a 16-bit DAC.

The accuracy of a 10-bit DAC, equal to 0.05% of full-scale, equals or betters many types of analog meters and recorders. Such a unit is suited to drive, for example, a strip-chart recorder with outputs from a computer or other digital source. A 12-bit DAC provides sufficient resolution to match the accuracy of an X-Y plotter. And



Insight. Price structure for digital-to-analog converters, based on width, or resolution, reveals sharp rise in cost for more resolution and precision. Height of bar reflects cost-range for performance features over and above that for basic conversion.



2. Premium. Cost-per-bit data, based on Fig. 1, emphasizes the cost increment for attaining and maintaining DAC precision. The gradual price increase for lesser-bit DACs results from volume production and less stringent demand on component tolerances.

an 8-bit DAC could be used to drive a low-accuracy analog meter whose purpose is, for example, to give a test operator a quick but not too accurate look at ongoing results.

The 6-bit DAC produces an analog output having only 64 discrete steps or a resolution of 1.6%. Because of this low resolution, the 6-bit DAC is not normally used in measurement and control applications as are the higher-bit DACs. Instead, the 6-bit DAC programs the output of power supplies, provides multi-level outputs for modems in data communications links, and so on.

For each application, the system designer must develop a set of specifications for such major parameters as resolution, linearity, accuracy, and settling time. And this means answering such questions as, over what temperature range must the DAC operate satisfactorily? For example, a 10-bit DAC required to have 10-bit resolution *and* 10-bit accuracy could degenerate to yield 10-bit resolution but only 9- or 8-bit accuracy—but 10-bit resolution with 8-bit accuracy might be adequate.

Does the application require a current output or a voltage output from the DAC? If voltage, is the performance of the output amplifier supplied with the DAC good enough, or should the user provide a higher-performance outboard amplifier?

The infrastructure

There is a wide enough range of DACs and options available from about 20 manufacturers to meet almost any user requirements. Choosing a DAC wisely, though, involves an understanding of how they operate and how they're made.

The kernel of any DAC is a set of switches and a resistance network, as shown by the colored blocks in Fig. 3. Two popular configurations are shown in some detail in Figs. 4 and 5. Each transistor switch is opened by a 0 level or closed by a 1 level at a corresponding bit-position of the input digital data word. (Or the logic convention might of course reverse this correlation.) Thus, in the case of a 6-bit DAC, the input binary word

1 0 1 0 1 0 Binary
1 2 3 4 5 6 Bit number

would mean the switches for bits 1, 3, and 5 are closed and 2, 4, and 6 open. Here bit 1 is the most significant bit (MSB) and bit 6 the least significant bit (LSB).

The analog output corresponding to 101010 is

$1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 0\times2^{-4} + 1\times2^{-5} + 0\times2^{-6}$

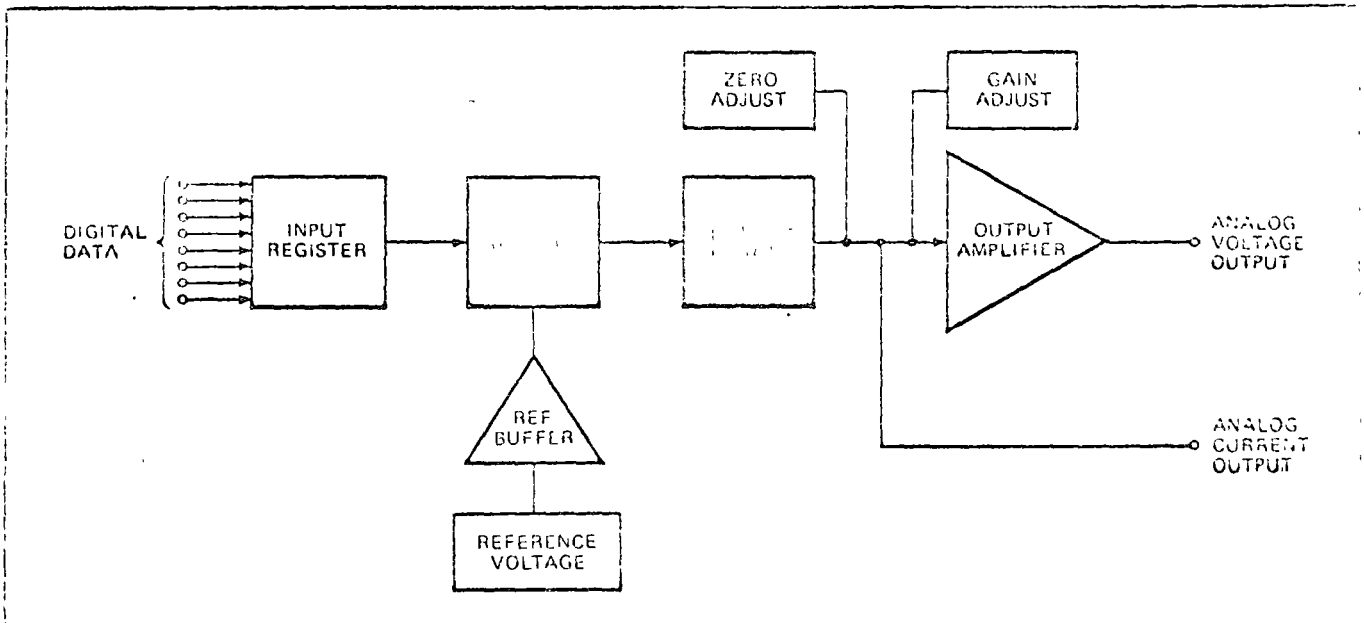
or 21/32 of full-scale value. Here, the MSB contributes one half the analog output.

Basic circuits

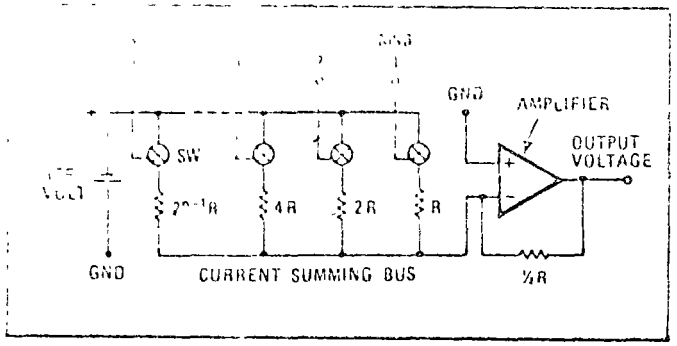
One common way of converting a binary input word to an equivalent analog output is shown in Fig. 4. When the bit-1 switch closes, the reference voltage creates a current through R of, say, 1 milliampere. Since the resistor associated with bit 3 is 4 R, then its current contribution is ¼ milliampere. And so on. The sum of these currents goes to the input of an operational amplifier which in turn produces an output voltage equivalent to the value of the applied digital word.

RESOLUTION EQUIVALENTS

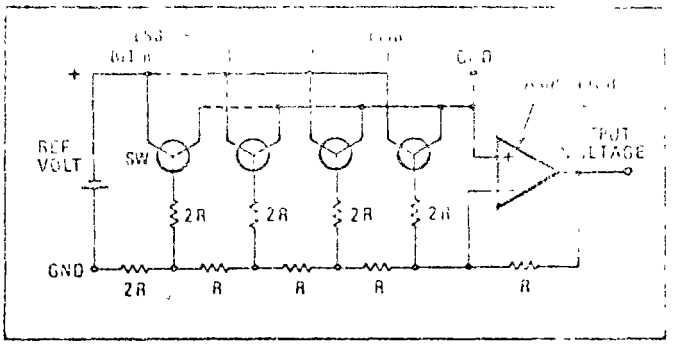
%	PPM		%	PPM	ANALOG OUTPUT STEPS
6.25	62,500		3.125	31,250	16
3.125	31,250		1.563	15,963	32
1.563	15,630		0.781	7,810	64
0.781	7,810		0.391	3,910	128
0.391	3,910		0.195	1,950	256
0.195	1,950		0.0977	977	512
0.0977	977		0.0488	488	1,024
0.0488	488		0.0244	244	2,048
0.0244	244		0.0122	122	4,096
0.0122	122		0.00610	61	8,192
0.00610	61		0.00305	31	16,384
0.00305	31		0.00153	15	32,768
0.00153	15		0.000763	8	65,536



3. Necessities and niceties. Every DAC contains switches and resistors (colored blocks) essential to conversion process, as well as other functions and features selectable for the performance required for the application.



4. **Adding up.** Binary input either opens or closes transistor switches thereby producing binary-weighted currents that are then summed to equivalent current output or voltage output



5. **Network.** A common d-a conversion method uses an R-2R network to produce binary currents. This technique needs only two values of resistances, but takes two resistors per bit

This configuration features one resistor for each bit. However, since each resistance is related to its neighbor by a factor of 2, a DAC with a large number of bits requires a very wide range of resistance values. In a 12-bit DAC, for example, the range is over 4,000-to-1.

Furthermore, if linearity and accuracy are not to fall short of ½ LSB, the tolerance of R—including a resistance variation due to temperature change—must not be allowed to exceed $2^{-(n+1)}R$. In other words, any variation in the current through R (for the MSB) due to a change in the nominal design-value of R should not exceed half the current through the LSB resistor. This is why the allowable tolerance of the resistors decreases rapidly as the number of bits increases in the DAC.

To reduce the number of resistance values for higher-bit DACs, the quad circuit has been developed. The quad is essentially a 4-bit DAC requiring four different resistance values, as in Fig. 4. An 8-bit DAC is obtained by connecting two quad units, with a suitable current-attenuating resistor in the summing bus. In this case, the attenuating resistor reduces the contribution of the quad containing the LSB by 16 (or 2^4) relative to the quad containing the MSB. The two quads are similar, except that the tolerance of the resistors in the MSB quad must be correspondingly tighter than the tolerances in the other unit.

Another way of performing digital-to-analog conversion uses the R-2R network (Fig. 5). This conversion circuit also yields binarily weighted analog contributions when each bit-position switch is closed. While it needs two resistors instead of one for each bit, it also requires only two different resistance values. But again, tolerances are important.

A heating problem

During conversion, single-pole double-throw transistor switches connect each resistor to the reference voltage or to ground. Some voltage drop occurs across the transistor and, ideally, this can be accounted for in the basic design so that the actual current through the resistors remains binarily related. However, the transistor's sensitivity to temperature variations can have an effect on the actual current. As with the resistors, transistor-switch performance becomes more critical as the bit-length of the DAC increases. For this reason, makers often include temperature-compensation in the transistor-switch circuits.

Irrespective of the kind of resistor network, the addition of an internal zener reference, driven by a power supply, provides a regulated voltage to develop the summed currents (see Fig. 3). If the power supply rejection ratio (PSRR) (in percent output change per percent supply voltage change) isn't satisfactory, a reference buffer amplifier helps to stabilize the zener's operating point further, making the DAC even more immune to changes in power supply voltage.

Some DACs come without a zener reference, allowing the user to add his own when he wants a reference common to the whole system or when overall system performance requires a better regulation than ordinarily provided in the DAC package.

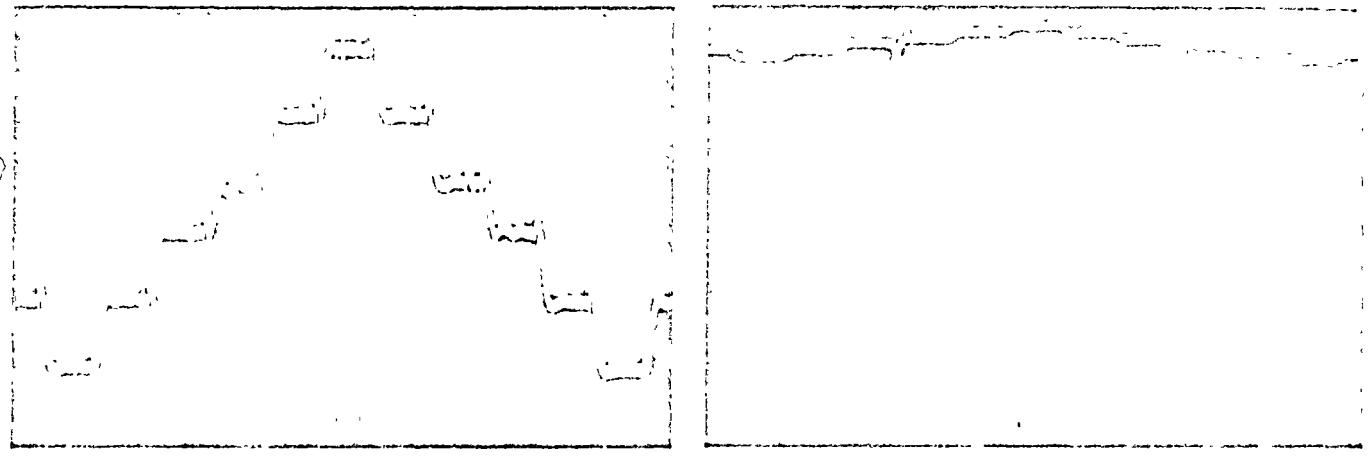
As the switches open and close as the data word changes, the difference in transistor turn-on and turn-off times and the resulting shifts in analog signal level, together with residual capacitance, create spikes called glitches (Fig. 6). The maximum amplitude of the spike, 50% of full-scale value, occurs when all the bit-positions switch simultaneously—as when an input data word changes from 0111 to 1000. Such a code change occurs when a DAC having a bipolarity output—for instance, from +5 v to -5 v—goes through zero.

The glitch can last for several hundred nanoseconds. If the DAC is driving a relatively large time-constant device, such as a d'Arsonval meter for a quick-look display, the effect of the glitches will go unnoticed. However, in a fast-response application—a CRT display—such a spike can be disturbing to the viewer since the glitch energy will "rattle around" in the tube and cause jitter in the displayed characters. For such high-speed applications, makers provide, for a price, a deglitcher that cuts the spike to about 0.02% of full scale value.

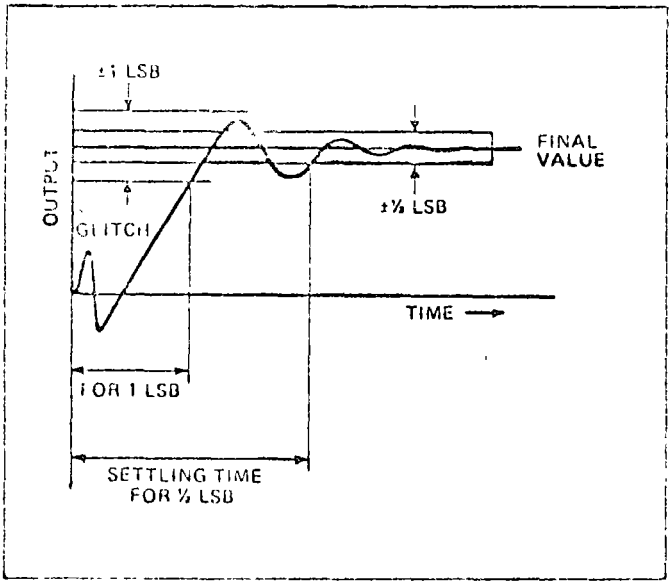
When bits in the parallel-bit data word do not actually arrive at the DAC at the same time, each transistor will then switch at a different time. This nonsimultaneous switching can also cause glitches. The situation can be ameliorated by adding a register in front of the switches. The data word is loaded into the input register, and then a strobe command connects the data word in the register to drive all switches simultaneously.

The register also serves as a data hold. There, the computer loads the register and goes on to other tasks. At a later time, determined by system needs, a strobe command initiates the conversion.

Settling time, one of the DAC's major parameters, de-



6. Deglitching. Oscillogram A shows spikeless output when deglitcher circuit is added to a 10-bit high-speed DAC. In oscillogram B the vertical gain has been reduced by a factor of ten, revealing magnitude of the glitch. Photos, courtesy Analog Devices Inc., have been retouched



7. Settling time. The time interval between initiation of switching operations and attainment of some prescribed final value of analog output is called the settling time

termines the fastest rate at which successive data inputs can be converted without losing accuracy due to premature cutoff of the transient analog output. By definition, it's the interval between the loading of a new data word into the switches and settling of the output to within some error band bracketing the final value (Fig. 7).

Its actual duration depends on the magnitude of the change between successive data words, the presence (or absence) of major code transitions that may create glitches, and the slewing rate and damping of the output amplifier (if any).

Plus and minus an amplifier

This amplifier, as Fig. 3 shows, is not necessary in DACs with a current output, which is available directly from the current summing bus. When a voltage output is needed, an output amplifier transduces the output current to an equivalent voltage. Staying with current output means the settling time is shorter, and the DAC will probably cost less because there's no amplifier in the module. However, analog devices driven by a DAC often require voltage inputs, so it may be more convenient to buy a DAC with the internal output amplifier at the slight additional cost.

By and large, the settling time stated by makers is based on a full-scale change in the input digital word and an error band of ±½ LSB. This value would be much smaller, and therefore appear better, if the error band were ±1 LSB, because of the exponential approach to final value. Thus, to compare settling times, the user must make sure the error bands are within same tolerances.

For current-output DACs, the times quoted range from about 100 to 1,000 nanoseconds due primarily to switching delay. However, with an integral amplifier the net settling time stretches to many microseconds.

This increase arises from the amplifier's inherent rise time, which occurs in response to the step change in current resulting from a change in the input digital word. Despite its duration, the settling time of most voltage DACs is generally adequate. But when the application needs it to be shorter, the user can add a higher-performance amplifier, one having a wider bandwidth, to speed up the output response.

The output amplifier also contributes to the error budget of the overall DAC. Therefore, a high-performance outboard amplifier can be employed not only to improve settling time, but also to reduce zero drift and changes gain in with time and temperature. High-performance amplifiers add appreciably to the overall cost of performing fast, accurate, and repeatable digital-to-analog conversion.

Sources of error

Besides the operating functions available in or with a DAC, the other aspect of DAC performance is the error budget. Some error is left in during manufacture, as indicated by the values on maker's spec sheets for various parameters. Additional error can show up during operation—particularly when the DAC is mounted in a warm or cold environment.

Changes in component values cause several types of error, which may be more or less important in different applications. Suppose it were possible to have an ideally linear and accurate DAC (Fig. 8). Here, the "transfer function" would be a straight line that started at true zero and finished at true full scale. As a result, when the digital input was stepped 1 bit-value at a time, the digi-

...to-analog conversion process would produce a smooth incremental-step staircase output. Figure 8 shows the effect on this output when the transfer function becomes nonlinear, which can occur, for example, when temperature change modifies component values so that the summed currents are no longer related in a binary fashion. The resolution remains, but accuracy decreases: the staircase steps are no longer uniform.

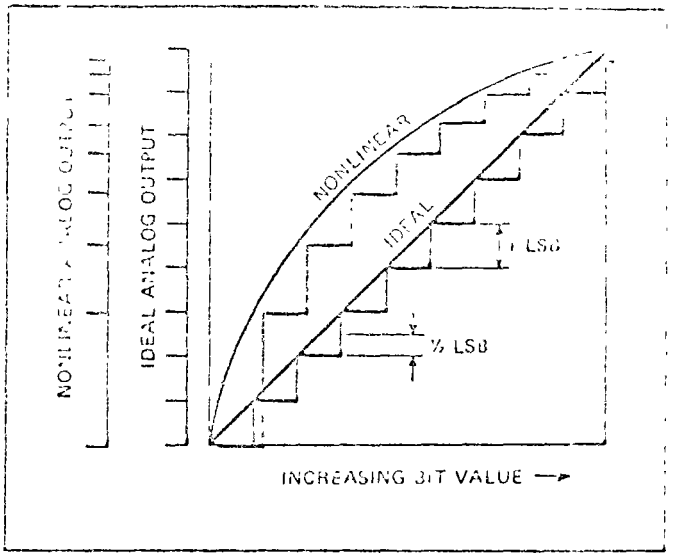
The nonlinearity in Fig. 8 is monotonic, in that increasing bit values yield an increasing-value staircase output and there is a unique analog value corresponding to each digital word. However, the transfer function could degenerate into a non-monotonic nonlinearity, as shown in Fig. 9. Here, the nonlinearity reverses direction. The presence of an excessive non-monotonic nonlinearity means that two different input codes produce the same analog output—which could have serious consequences. For example, it could cause a digital servo to hunt (oscillate) continuously, because of the servo's inability to settle on a single-valued null point. (The nonlinearity in Figs. 8 and 9 has been exaggerated for graphic contrast).

Two other kinds of error, gain error and offset error, are shown in Fig. 10. The former, in which the slope of the transfer function changes and does not go through the ideal full-scale point, is caused by changes in reference voltage, amplifier gain, and resistor values. Offset error, in which the slope does not go through the ideal zero point, is caused by resistor changes and amplifier drift. Some higher-resolution DACs include extra terminals for connection of resistor trimmers, to permit outboard recalibration of offset and gain functions when the DAC ambient is of high or low temperature.

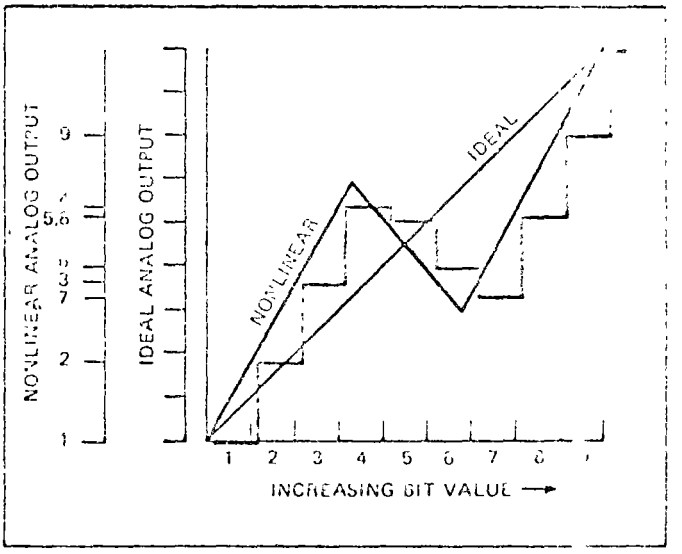
While the effect of temperature change on individual components is to alter nonlinearity, gain, and offset errors, the important thing to the user is the net effect of temperature on the overall unit. This effect on accuracy is specified by the maker as a temperature coefficient (tempco) in parts per million per °C (or as its equivalent percent per °C, see table of Resolution Equivalents). The impact of temperature change on DAC accuracy can be determined from the three charts in Fig. 11. Here, a DAC ambient temperature different from nominal temperature (usually 25 °C) results in a certain ppm error—depending on the DAC's tempco—and this in turn is translated into the equivalent ½ LSB error for each DAC size from 6 to 16 bits.

Suppose a 12-bit DAC has a 100 ppm/°C tempco and must operate at 35°C (or a Δ°C of 10). Figure 11b shows the resulting error is 100 ppm. Since 100 ppm falls within the colored band for the ½ LSB for 12-bit DAC, the DAC retains its ½ LSB accuracy under these conditions. However, in the case of a 14-bit DAC with a 10 ppm/°C tempco (see Fig. 11c), a change of only 4°C is enough to push accuracy past the ½ LSB limit, so that the DAC has 14-bit resolution but only 13-bit accuracy under these conditions. And a change of 10°C would reduce the DAC to 12-bit accuracy.

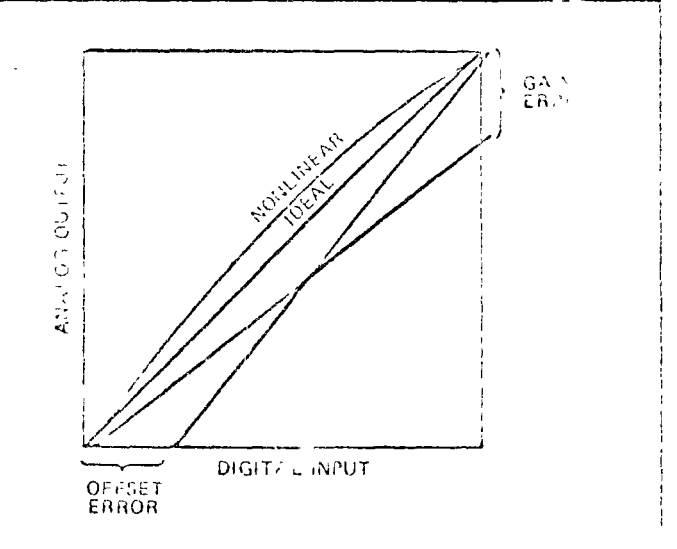
All this brings the user right back to the cost information in Fig. 1. Does he really need a 14-bit DAC that must operate with 14-bit accuracy and, if so, can he maintain the unit's temperature within a relatively narrow band? If yes, the cost is about $500. If, however, 12-



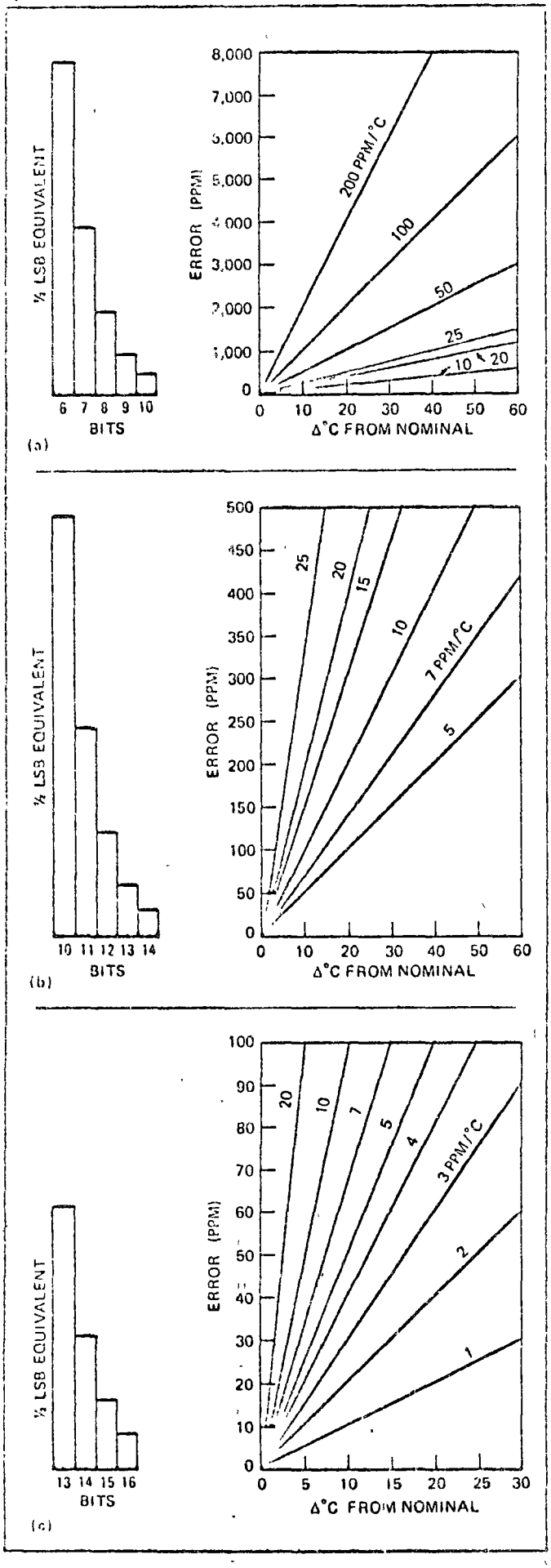
8. Nonlinearity. Any nonlinearity in the DAC's transfer function produces non-uniform steps in the analog output.



9. Non-monotonicity. When the DAC's transfer function reverses direction, output steps will go down when they should go up.



10. Erroneous. Two causes of reduced accuracy in a DAC are gain error and offset error. External correction is possible in some DACs.



11. How temperature affects DAC accuracy. When a DAC operates at a temperature different from the nominal design temperature, an error in parts per million may result. Its value depends on the DAC's temperature coefficient and ambient temperature. Here, the error is related to the corresponding ½-least-significant-bit criterion for each DAC size. If the temperature-induced error falls within the appropriate colored bar, the DAC retains nominal accuracy.

bit accuracy is satisfactory and he can also settle for 12-bit resolution, the cost drops to about $200.

In some applications accuracy less than equivalent resolution can be a definite specification, not a compromise. For example, suppose a wide range of digital values requires the code combinations available in a 16-bit word for their representation, but the analog output need only be accurate to 0.05%, equivalent to the ±½ LSB accuracy of a 10-bit DAC. Asking the manufacturer for a 16-bit DAC with a 10-bit accuracy eases his production and testing problems since acceptable ±½ LSB error can be within 500 ppm rather than less than 10 ppm; the cost drops from about $750 to $200.

Method of manufacture

Interpreting the information on spec sheets however, is just one factor in coming up with a performance rating. The second factor—design and manufacturing method—may weigh heavily in the ultimate selection because it could affect the long-term performance of the relatively low-cost DAC in an expensive electronic system. As the plethora of hybrid, discrete-component, and monolithic DACs reveals, manufacturers themselves have not agreed in the best way to make a DAC—and at the present there may be no single way that's best for every application. The user should add his own judgment, in the light of his particular needs, and then relate the outcome to price.

Many interrelated considerations go into the way the maker chooses to produce his unit. Among these are the DAC's bit length, the conversion method, the expected selling price, and production volume. The bit length sets the accuracy requirements and this in turn determines, for example, whether thick-film resistors can provide the required range of resistance values and tempco for the bit-length of the DAC, or whether the unit should use more precise, discrete wirewound resistors. The conversion method determines, among other things, the parts count of the resistors, and thus affects the decision of whether it's less costly to buy discrete resistors or to deposit them at one time as a thin-film or thick-film network. Production volume can affect whether the maker wants to invest in a hybrid or semiconductor facility, or save on capital investment but opt for higher labor cost in assembling discrete-component DACs.

In general, higher-bit DACs don't enjoy a high volume but do require high precision, and so they are produced from discrete, high-accuracy, low-tempco resistors. Lesser-bit DACs, with higher production volume, are made in a variety of hybrid or discrete designs. The latest innovation in DACs, the 100% monolithic design, may eventually pose a threat to other methods, but so far this approach has resulted in a 6-bit DAC on one chip in a dual in-line package. However, 8- and 10-bit monolithic DACs should be announced soon. □

MC1507L
MC1407L

A-TO-D CONTROL CIRCUIT

Specifications and Applications Information

MONOLITHIC ANALOG – DIGITAL CONTROL CIRCUIT

designed for wide application in analog to digital, interface and high speed instrumentation systems. The MC1507L/MC1407L consists of a wide bandwidth operational amplifier and a high speed, dual threshold comparator.

The comparator, which has separate Up and Down outputs, also possesses a differential reference input that sets both comparator thresholds for equal levels – but of opposite polarities.

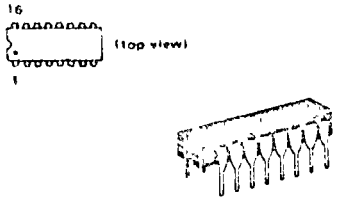
The high slew rate of the amplifier makes it particularly advantageous for use as a current to voltage converter for the MC1506L and the MC1508L 8 D to A converters. Moreover, the operational amplifier is useful as a high speed buffer.

The MC1507L/MC1407L is well suited for application with the above mentioned monolithic D to A converters to produce an inexpensive high speed tracking analog to digital converter.

- Operational Amplifier Features High Slew Rate – 20 V/μs typical and Wide Bandwidth – 24 MHz typical Unity Gain Crossover
- Fast Dual Threshold Schottky Comparator – 75 ns typical Propagation Delay Time and Input Current of Only 0.4 μA typical
- MTTL and CMOS System Compatability
- Standard Supply Voltages of +5.0 and ±15 Vdc
- Compatible with MC1508L 8 and MC1506L D to A Converters
- Comparator Thresholds Simultaneously Adjustable with a Single Reference Input Voltage

ANALOG-DIGITAL CONTROL CIRCUIT

MONOLITHIC SILICON INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 620

FIGURE 1 – MC1507L/MC1407L BLOCK DIAGRAM

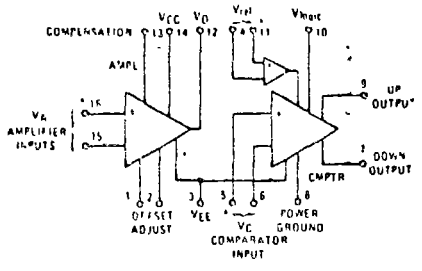
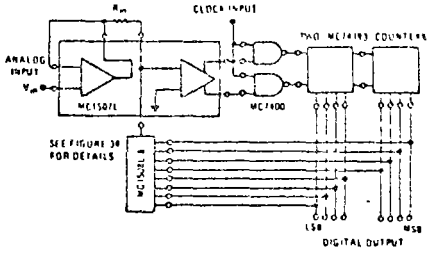


FIGURE 2 – TYPICAL APPLICATION 8 BIT TRACKING A TO D CONVERTER



TYPICAL APPLICATIONS

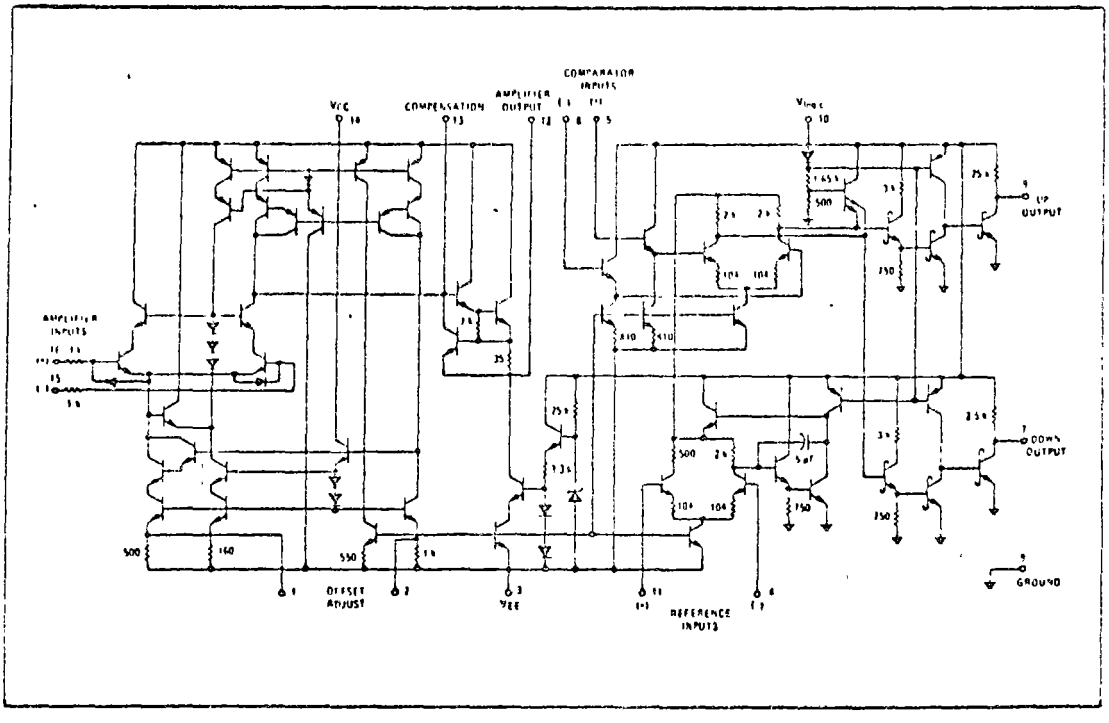
- High Speed Tracking A to D Converters
- Successive Approximation A-to-D Converters
- Speech Conversion
- DAC Current to Voltage Converter
- Control Systems
- Signal Generators
- High Speed Buffer
- Window Comparator
- Peak Detecting Sample and Hold
- Voltage to Frequency Conversion
- Fast Integrator
- Delta Modulation

See Packaging Information Section for outline dimensions

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			
Logic Voltage Supply	V_{logic}	+5.5	Vdc
Positive Voltage Supply	V_{CC}	+16.5	
Negative Voltage Supply	V_{EE}	-16.5	
Differential Input Voltage Signal			
Amplifier Voltage	$V_{16} - V_{15}$	±10	V
Comparator Voltage	$V_6 - V_5$	±10	
Comparator Reference Voltage	$V_{11} - V_4$	±5.0	
Common Mode Input Voltage Swing			
Amplifier Voltage	V_{ICRA}	V_{CC}, V_{EE}	V
Comparator Voltage	V_{ICRC}	V_{logic}, V_{EE}	
Comparator Reference Voltage	$V_{ICRC_{ref}}$	V_{logic}, V_{EE}	
Amplifier Output Short Circuit Duration	t_{SC}	10	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In Line Package		1000	mW
Derate above T_A = +25°C		6.0	mW/°C
Operating Temperature Range	T_A		°C
MC1507L		-55 to +125	
MC1407L		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, V_{logic} = +5.0 Vdc, V_{ref}(+) = 40 mVdc, $V_6 = V_4$ = 0 V, T_A = +25°C unless otherwise noted.)

AMPLIFIER SECTION

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Offset Voltage $R_S \leq 2.0$ kΩ, T_A = +25°C $T_A = T_{low}$* to T_{high}*	$\lvert V_{IO} \rvert$	– –	1.0 –	2.0 3.0	– –	2.0 –	6.0 7.5	mV
Open Loop Voltage Gain (V_O = 0 to +10 V, 0 to -10 V, R_L = 5.0 kΩ, $T_A = T_{low}$ to T_{high})	A_{vol}	10,000	35,000	–	5,000	20,000	–	V/V
Input Bias Current T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IBA}	– –	0.6 –	1.5 2.5	– –	1.2 –	2.5 4.0	μA
Input Offset Current T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IOA}	– –	0.03 –	0.15 0.25	– –	0.06 –	0.30 0.15	μA
Common Mode Input Voltage Swing	V_{ICRA}	±11	–		±11	–	–	V
Common Mode Rejection Ratio	CMRR	10,000	35,000	–	10,000	35,000	–	V/V
Output Impedance (f = 20 Hz)	z_O	–	1.8	–	–	1.8	–	kΩ
Output Voltage Swing (R_L = 5.0 kΩ) V_{IB} = -10 V or A_V = +1 mode, T_A = +25°C V_{IB} = -10 V or A_V = +1 mode, $T_A = T_{low}$ to T_{high} V_{IB} = 0 V, T_A = +25°C V_{IB} = 0 V, $T_A = T_{low}$ to T_{high}	V_O±	±11 ±10 +11,-1.0 +10,-1.0	±12 – +12,-2.0 –	– – – –	±11 ±10 +11,-1.0 +10,-1.0	±12 – +12,-2.0 –	– – – –	V
Unity Gain Crossover Frequency Compensated for Unity Gain C13 = 10 pF (Pulse Margin = 35°C typical) Open Loop Noncompensated (Phase Margin = 0° typical)	f_C	– –	12 24	– –	– –	12 24	– –	MHz
Large Signal Step Response Gain = +1, V_{in} = 0 to 10 V (See Figure 16) Slew Rate Setting time to within 0.1% Gain = +1, V_{in} = -10 to +10 V (See Figure 16) Setting time to within 0.1% Gain = -1, V_{in} = 0 to -10 V Slew Rate Setting time to within 0.1% Gain = -10, V_{in} = 0 to -10 V Slew Rate Setting time to within 0.1% Gain = -10, V_{in} = 0 to -1.0 V Slew Rate Setting time to within 0.1% Gain = -100, V_{in} = 0 to -100 mV Setting time to within 0.1%	SR t_{setlg} t_{setlg} SR t_{setlg} SR t_{setlg} SR t_{setlg} t_{setlg}	10 – – 10 – 10 – 10 – –	20 0.8 1.1 20 0.8 20 0.8 20 0.8 2.0	– – – – – – – – – –	10 – – 10 – 10 – 10 – –	20 – 1.1 20 0.8 20 0.8 20 0.8 2.0	– 0.6 – – – – – – – –	V/μs μs μs V/μs μs V/μs μs V/μs μs μs
Small Signal Step Response Propagation Delay Time (50% to 50%) Gain = +1, V_{in} = -50 mV to +50 mV	t_{pd}±	–	18	–	–	18	–	ns
Power Bandwidth Gain = +1, V_{in} = 10 V(p-p)	BW	320	640	–	320	640	–	kHz
Output Source Current (Short circuit limited)	I_{source}	10	17	30	10	17	30	mA
Output Sink Current	I_{sink}	2.0	3.0	–	2.0	3.0	–	mA
Power Supply Sensitivity V_{CC} varied ±10%, V_{EE} constant V_{EE} varied ±10%, V_{CC} constant	PSSA- PSSA+	– –	– –	150 150	– –	– –	150 150	μV/V

*T_{low} = -55°C for MC1507L, 0°C for MC1407L
*T_{high} = +125°C for MC1507L, +75°C for MC1407L

COMPARATOR SECTION

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Threshold, UP Output	V_{th+}	36	40	44	30	40	50	mV
Input Threshold, DOWN Output	V_{th-}	-36	-40	-44	-30	-40	-50	mV
Input Threshold Range	$\lvert V_{TRI} \rvert$	–	-150 to +320	–	–	-150 to +320	–	mV
Input Bias Current T_A = +25°C $T_A = T_{low}$* to T_{high}*	I_{IBC}	– –	0.4 –	1.5 2.5	– –	0.8 –	2.5 4.0	μA

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, V_{logic} = +5.0 Vdc, V_{ref}(+) = 40 mVdc, V_6 = V_4 = 0 V, T_A = +25°C unless otherwise noted.)

COMPARATOR SECTION (continued)

Characteristic	Symbol	MC1507 Min	MC1507 Typ	MC1507 Max	MC1407 Min	MC1407 Typ	MC1407 Max	Unit
Input Offset Current T_A = +25°C T_A = T_{low} to T_{high}	I_{IOC}	– –	0.01 –	0.15 0.25	– –	0.02 –	0.25 0.40	μA
Reference Input Bias Current	I_{ref}	–	4.0	18	–	4.0	18	μA
Common Mode Input Voltage Swing	V_{ICRC}	-10 to +1.0	–	–	-10 to +1.0	–	–	V
Low Level Logic Output Voltage R_L = 1.4 kΩ, T_A = T_{low} to T_{high}	V_{OL}(D) V_{OL}(U)	– –	0.3 0.3	0.5 0.5	– –	0.3 0.3	0.5 0.5	V
High Level Logic Output Voltage T_A = T_{low} to T_{high}	V_{OL}(D) V_{OL}(U)	4.0 4.0	4.95 4.95	– –	4.0 4.0	4.95 4.95	– –	V
Output Sink Current (each output) T_A = T_{low} to T_{high}	I_{sink}	3.2	–	–	3.2	–	–	mA
Propagation Delay Time (each output) V_{in} = 0 to V_{th} +20 mV, R_L = 1.4 kΩ	t_{PLH} t_{PHL}	– –	75 75	– –	– –	75 75	– –	ns
Power Supply Sensitivity of Input Thresholds V_{logic} varied ±10%, V_{EE} constant V_{EE} varied ±10%, V_{CC} constant	PSSC+ PSSC-	– –	– –	1.0 1.0	– –	– –	1.0 1.0	mV/V

AMPLIFIER AND COMPARATOR SECTIONS

Power Supply Voltage Range (See Note 1.) Positive Supply Voltage Negative Supply Voltage Logic Supply Voltage	V_{CC} V_{EE} V_{logic}	+4.5 -4.5 +4.5	+15 -15 +5.0	+16.5 -16.5 +5.5	+4.5 -4.5 +4.5	+15 -15 +5.0	+16.5 -16.5 +5.5	Vdc
Power Supply Currents Comparator V_{in} = 0, V_{EE} = -15 V, V_{CC} = +15 V, V_{logic} = 5.0 V Positive Supply Current Negative Supply Current Logic Supply Current	I_{CC} I_{EE} I_{logic}	– – –	+4.0 -1.0 +1.6	+6.0 -1.3 +2.0	– – –	+4.0 -1.0 +1.6	+8.0 -1.6 +2.5	mA
Power Dissipation V_{EE} = -5.0 V V_{EE} = -15 V	P_D	– –	190 290	255 385	– –	190 290	325 485	mW

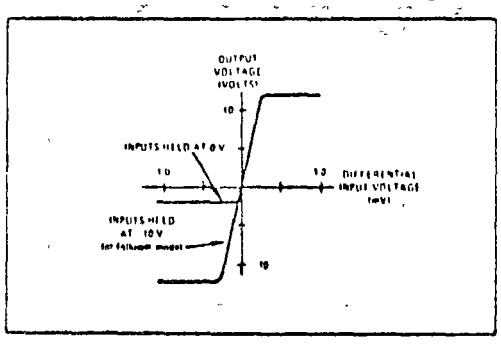
Note 1. Amplifier Output Swing decreases with reduced V_{CC} and V_{EE} supply voltages. At ±5.0-volt supplies, common mode and output swing voltages are typically ±2.0 volts.

*T_{low} = -55°C for MC1507L, 0°C for MC1407L
T_{high} = +125°C for MC1507L, +75°C for MC1407L

THREE QUADRANT OPERATIONAL AMPLIFIER

The amplifier is a single gain stage especially designed for high gain and fast response. Very high impedance current sources provide a typical resistance of 20 megohms at pin 13, which is the gain node of the circuit and its major RC pole. The input of the amplifier is protected against breakdown of the NPN differential pair, and the output is short circuit protected. Since the amplifier is a single gain stage with all NPN transistors in the signal path, it has one limitation when compared with standard operational amplifiers. The amplifier transfer characteristic, Figure 4, shows that the output can swing no more negative than -2.0 volts with respect to the inputs. Hence, the circuit is called a three quadrant operational amplifier. The amplifier may be used as a standard operational amplifier in the noninverting unity gain mode with an output swing of ±11 V minimum, and as an inverting amplifier to convert negative voltages to positive voltages. For output swings under 4.0 volts (p-p), as in active filter applications, the amplifier is especially useful since it offers four quadrant operation with very wide bandwidth.

FIGURE 4 – TYPICAL TRANSFER CHARACTERISTIC FOR THREE QUADRANT OPERATIONAL AMPLIFIER



TEST CIRCUITS AND WAVEFORMS

FIGURE 5 – OPERATING MODES OF THE THREE QUADRANT OPERATIONAL AMPLIFIER

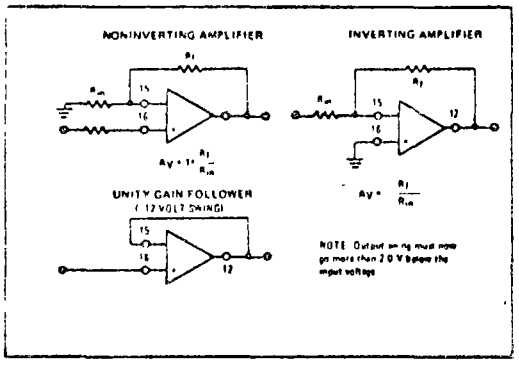


FIGURE 6 – THREE QUADRANT OPERATIONAL AMPLIFIER PULSE RESPONSE WAVEFORMS
(Applicable to Circuits of Figures 8 or 15)
(A_V = -1, R_L = 5.0 kΩ, C_L (total) = 100 pF)

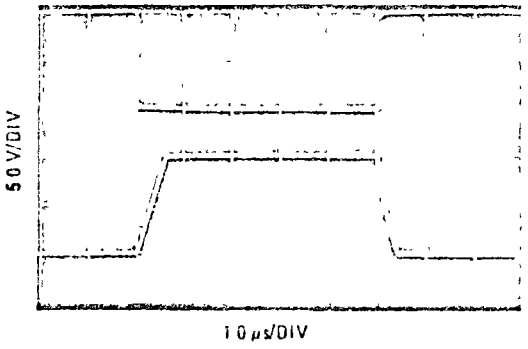


FIGURE 7 – SETTLING TIME DEFINITION

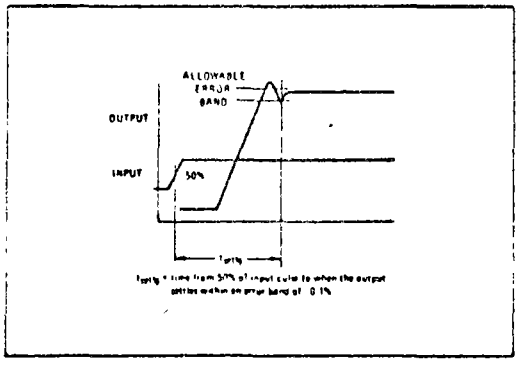


FIGURE 8 – INVERTING GAIN SETTLING TIME TEST CIRCUIT

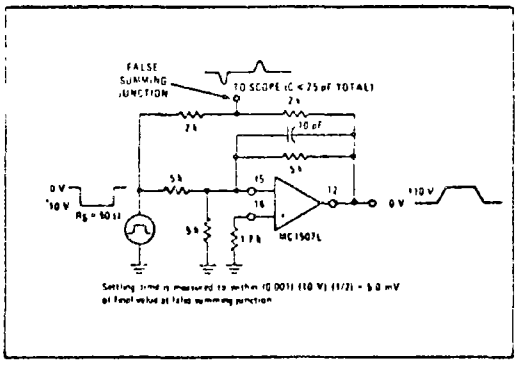


FIGURE 9 – AMPLIFIER PROPAGATION DELAY WAVEFORMS

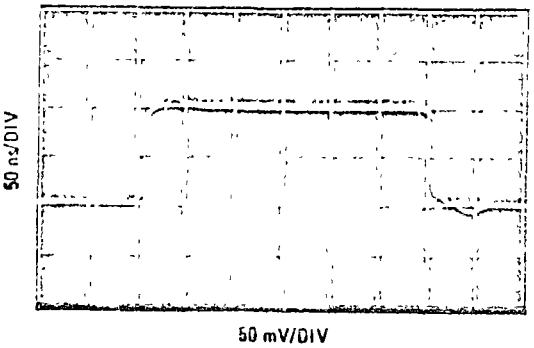
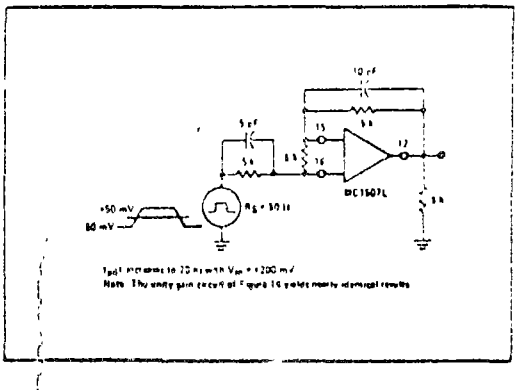


FIGURE 10 – PROPAGATION DELAY TIME TEST CIRCUIT



AMPLIFIER GAIN SELECTION

INVERTING MODE

FIGURE 11 – VOLTAGE GAIN > |-2|

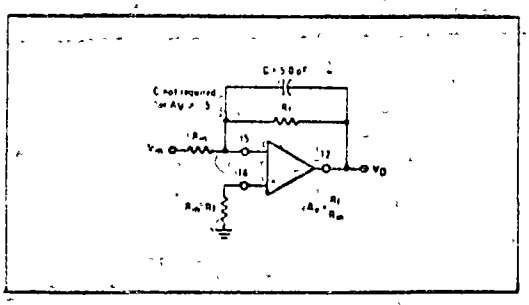


FIGURE 13 – VOLTAGE GAIN = -1

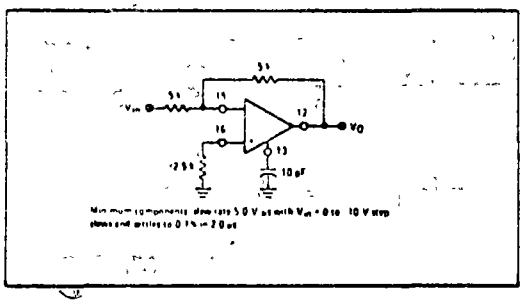
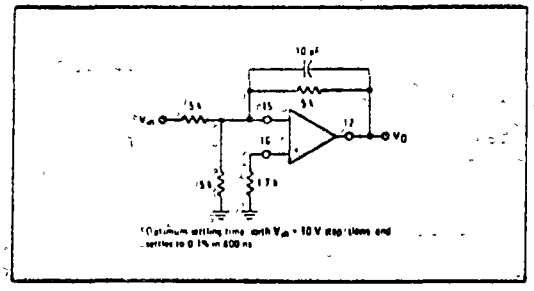


FIGURE 15 – VOLTAGE GAIN = -1



NONINVERTING MODE

FIGURE 12 – VOLTAGE GAIN ≥ +2

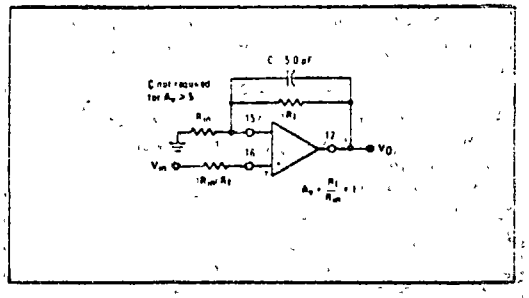


FIGURE 14 – VOLTAGE GAIN = +1

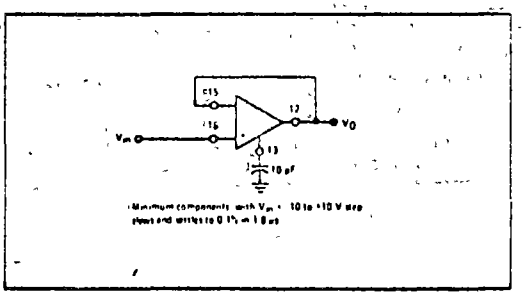


FIGURE 16 – VOLTAGE GAIN = +1

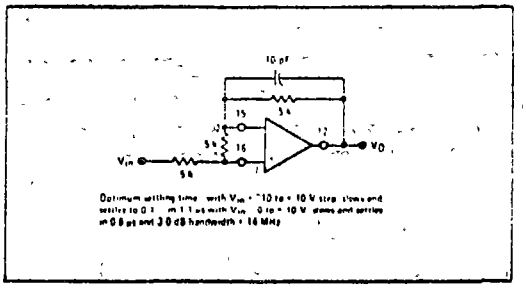
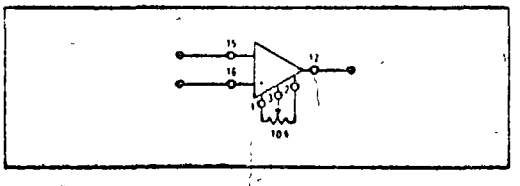


FIGURE 17 – OFFSET VOLTAGE ADJUSTMENT



ADJUSTABLE DUAL THRESHOLD COMPARATOR

COMPARATOR

The comparator equivalent circuit is shown in Figure 18. It may be envisioned as two comparators with common inputs and a reference voltage source which sets equal and opposite thresholds. A positive reference voltage on pin 11 sets the thresholds as in the transfer characteristic of Figure 19. If, for example, pin 6 is grounded, when the input signal on pin 5 exceeds V_{th} (+), the UP output goes high. When the input on pin 5 exceeds V_{th} (-) in the negative direction, the DOWN output goes high.

In applications where a single output is desired, as in a window comparator, the outputs may be connected in "wired OR" if the reference voltage polarity is reversed. This inverts the output polarity so that when the input is between thresholds the outputs are in a normal high state. It also interchanges the outputs so that pin 7 responds to an input of V_{th} (+), and pin 9 to an input of V_{th} (-). See Figure 20, which is the transfer characteristic curve. When the outputs are connected together, a low output state results for an input outside the threshold window.

FIGURE 18 – COMPARATOR EQUIVALENT CIRCUIT

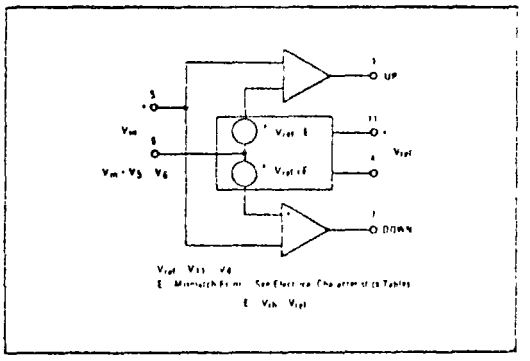


FIGURE 19 – COMPARATOR TRANSFER CHARACTERISTIC, POSITIVE REFERENCE VOLTAGE

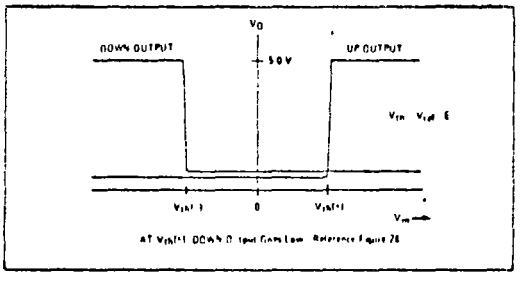
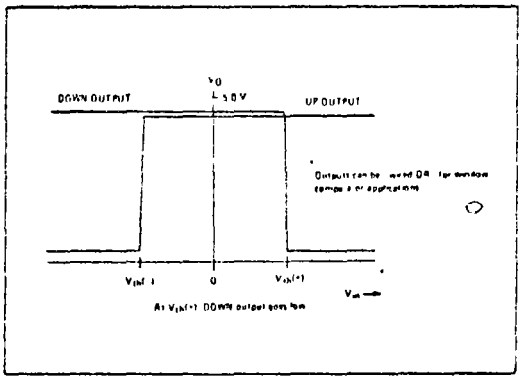


FIGURE 20 – COMPARATOR TRANSFER CHARACTERISTIC, NEGATIVE REFERENCE VOLTAGE



OPERATION OF OPERATIONAL AMPLIFIER OR COMPARATOR ONLY

FIGURE 21 – INDIVIDUAL AMPLIFIER OPERATION ONLY

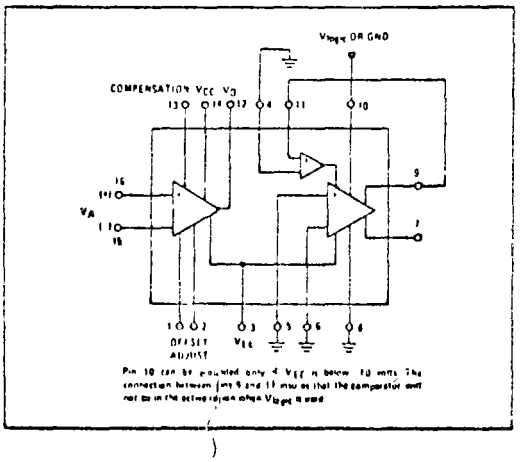
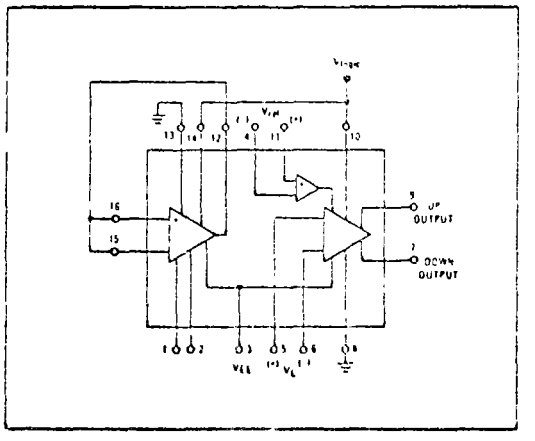


FIGURE 22 – INDIVIDUAL COMPARATOR OPERATION ONLY



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 23 – OPEN-LOOP FREQUENCY RESPONSE (OPERATIONAL AMPLIFIER)

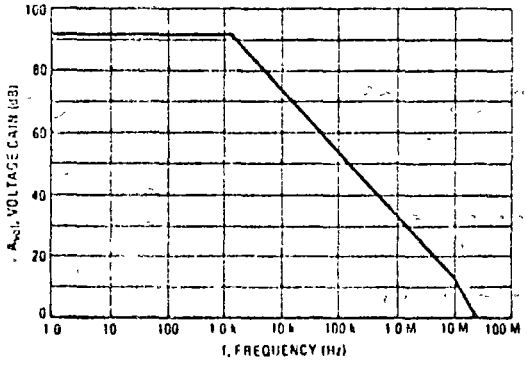


FIGURE 24 – TYPICAL SOURCE CURRENT LIMIT versus TEMPERATURE (OPERATIONAL AMPLIFIER)

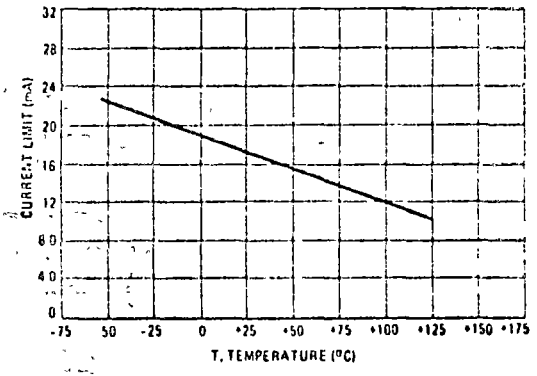


FIGURE 25 – TYPICAL POWER SUPPLY CURRENT versus V_{EE}

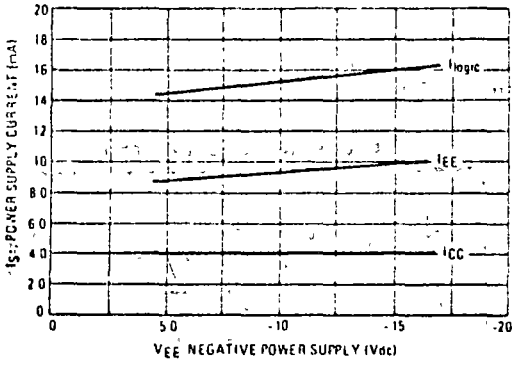


FIGURE 26 – POWER SUPPLY CURRENT versus TEMPERATURE

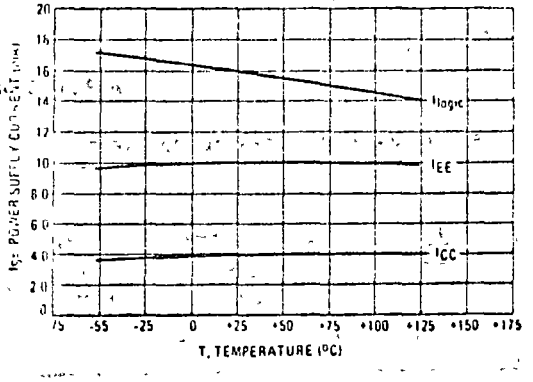


FIGURE 27 – COMPARATOR RESPONSE versus INPUT OVERDRIVE

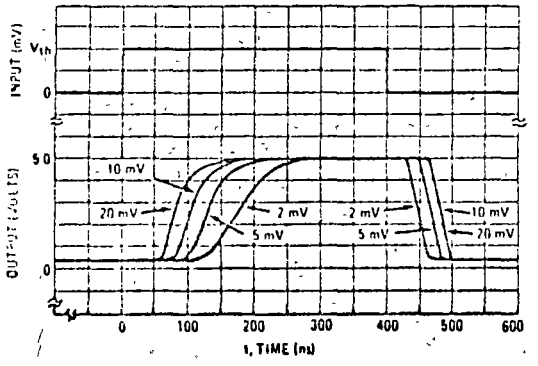
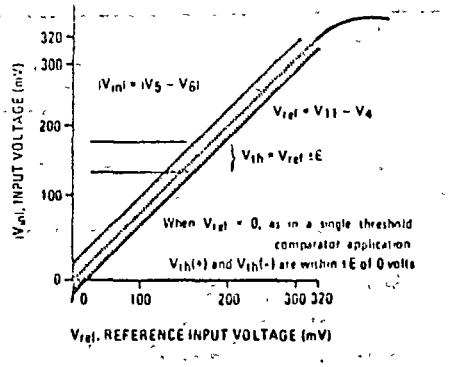
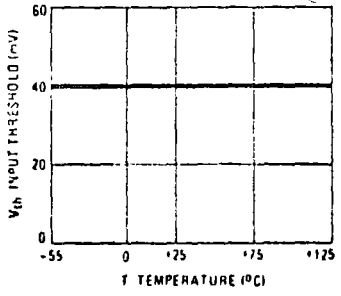


FIGURE 28 – COMPARATOR THRESHOLD versus V_{ref}



TYPICAL CHARACTERISTICS (continued)

FIGURE 29 – COMPARATOR THRESHOLD versus TEMPERATURE



APPLICATIONS INFORMATION

FIGURE 30 – SINGLE THRESHOLD COMPARATOR

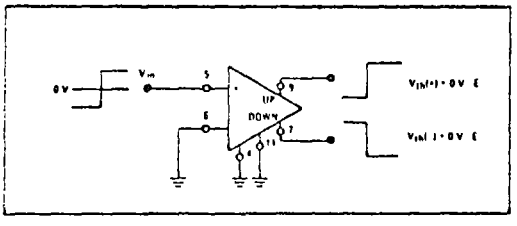


FIGURE 31 – WINDOW COMPARATOR

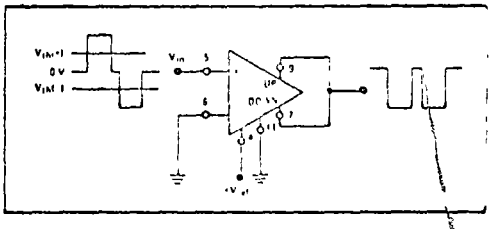


FIGURE 32 – D TO A CURRENT TO VOLTAGE CONVERTER (POSITIVE OUTPUT)

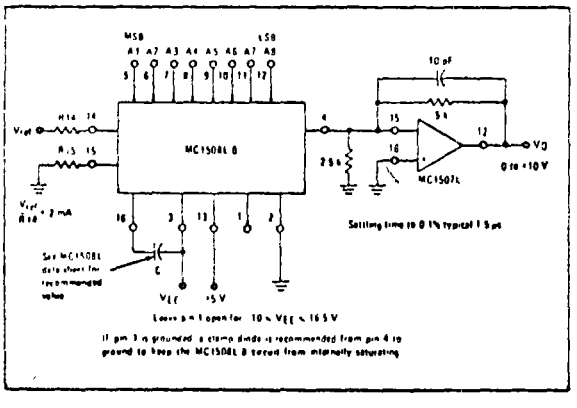
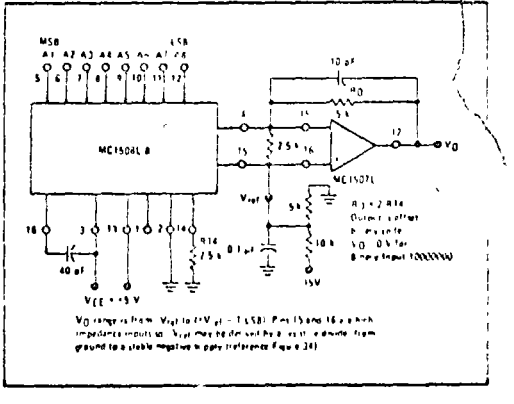


FIGURE 33 – D TO A CURRENT TO VOLTAGE CONVERTER (BIPOLAR OUTPUT)



APPLICATIONS INFORMATION (continued)

TRACKING A TO D CONVERTERS

A tracking A to D converter is a system with a digital output which continuously follows the analog input. It can be thought of as an "analog to digital operational amplifier" since as a system it has many similar specifications - slew rate, propagation delay, settling time, and adjustable scale factor. The tracking converter is normally used in high speed applications which require conversion times on the order of 1 to 100 μs.

Successive approximation conversion is the other major method used for A to D conversion in this speed category. The advantages of the tracking system over successive approximation system include: 1) the elimination of the sample and hold function at the input, 2) a digital output which is continuously present and can be used in asynchronously sampled systems, and 3) a conversion or update period equal to slightly more than one D to A converter settling time. The major disadvantage of the method is that if the system slew rate is exceeded, the conversion time increases. A full scale input step function requires a conversion time of 2^n times the tracking update rate, where n is the number of bits. The full scale conversion time can be shortened, however, using methods which will be described later, and shown in Figure 36.

Another advantage of the tracking system is that, unlike the successive approximation approach, the output always indicates a value equal to the present or very recent input level. Therefore, in many instances latches or special timing are unnecessary for data readout.

BASIC 8-BIT SYSTEM

An easily constructed tracking A to D converter using the MC1407L, two up/down counters, a quad NAND gate, and a monolithic D to A converter such as the MC1406 or MC1408L-8 is shown in Figure 34. Assuming a full scale input range of 10 volts, the reference voltage is chosen so that the UP and DOWN thresholds are at least ±1 LSB from ground. For an 8 bit converter, this would be 10 V/256 or ±40 mV. The converter operation is described by assuming that V_{in} = 0 and the counter output is 00000000. The D to A converter is pulling no current so the drop across R_{in} is essentially zero. Now assume V_{in} rises until it reaches 40 mV, which is the UP comparator threshold. The UP comparator fires and on the next positive edge of the clock, a pulse is fed to the UP input of the counter. As shown in the converter transfer characteristic, the counter output increases to 00000001. The D to A converter now pulls 8 μA, so the summing node voltage drops down to zero. In a similar manner the system could count up to any value up to the full scale 11111111 count.

Since the D to A converter output current levels are rated to be accurate to within ±1/2 LSB, the comparator thresholds must be set to allow for this error. If, for instance, all the D to A converter error occurred at one transition, one output could be 1/2 LSB or 4 μA low and the next would be 4 μA high. This would be a current step of 16 μA instead of 8 μA, and the summing node would pull back to -40 mV instead of zero. If the comparator thresholds were closer to ground than ±40 mV, this transition would cause the DOWN comparator to fire and the D to A current would decrease. Thus the system would oscillate between two output values for this particular transition. This may or may not be undesirable, depending on system requirements. Both outputs would be within ±1 LSB of the correct value, which is a standard A to D converter accuracy specification. However, the end of conversion feature described in a later section cannot be used unless the system settles to a stable value.

With thresholds of ±1 LSB, the system has a typical hysteresis of ± 1 LSB, as shown on the transfer characteristic of Figure 35. If the input voltage is ramping up and has just fired the UP comparator, the summing node pulls back to a typical value of zero. With a change in ramp direction, the input must decrease by 1 LSB to fire the DOWN comparator. This hysteresis allows for D to A converter error and also lends noise immunity to the system.

An A to D converter using a D to A converter in its feedback loop cannot be any more accurate than the accuracy of the D to A converter plus 1/2 LSB quantization error. In the case of the MC1508L-8, MC1408L-8, MC1506, and MC1406, this D to A accuracy is specified as ± 1/2 LSB. In a tracking converter with the comparator thresholds set to zero, the A to D converter output toggles between two values, each value within ±1 LSB of the correct value. The ± 1/2 LSB error of the D to A converter is added to the ±1 LSB error of the converter, resulting in a system error of ±1 1/2 LSB. The comparator offset or mismatch error (±E) can be trimmed out and eliminated as a source of additional error.

If the MC1507 comparator thresholds are set to ±1 LSB, the ±1/2 LSB of the D to A converter must also be added, again, giving a system error of ±1 1/2 LSB. In addition, the comparator mismatch error, (±E), must be added to both the UP threshold and the DOWN threshold.

In order to insure thresholds of at least ±40 mV, V_{ref} for the comparator should be no lower than ±41 mV for the MC1507L and ±50 mV for the MC1407L. This results in an additional ±0.2 LSB error in the MC1507L and an additional ±0.5 LSB error in the MC1407L. Total system error for an 8 bit converter with ±1 LSB threshold to eliminate toggling and to improve noise immunity, is therefore ±1.7 LSB for a system with the MC1507L, ±2.0 LSB for a system with the MC1407L.

High speed operation is possible with this converter due to the use of current summing. No operational amplifier is used in the feedback loop so the principal delays involved are the D to A converter settling time and the comparator delay time. The loop delay in Figure 34 is approximately 500 ns, allowing 150 ns for the MC1507L comparator with a small overdrive. The maximum clock frequency is determined by the loop delay

APPLICATIONS INFORMATION (continued)

Using a clock with a period less than 500 ns would make it possible for two counts to enter the D to A converter before the UP comparator turns "off." The turn "on" time of the MC1508L 8 current switches is longer than the turn "off" time so with a clock of slightly over 2 MHz, the steps on the up side of the sine wave of Figure 38 would be twice as large. However, even though a faster clock provides only 7 bit resolution when tracking a sine wave, the system will still settle to 8 bit accuracy for dc or square wave inputs. This principle is used in the high speed system of Figure 36. When a clock frequency of greater than 2 MHz is used, a 100 pF capacitor between the UP and DOWN comparator outputs improves the overall settling time.

TYPICAL PERFORMANCE TABLE FOR BASIC 8 BIT SYSTEM

	2 MHz CLOCK (for continuously varying inputs)	5 MHz CLOCK (for dc or step inputs)
Normal Conversion or Update Time	0.5 µs	0.2 - 1.0 µs
Typical Full Scale Conversion Time	128 µs	50 µs
Slew Rate (10 V Input Range)	0.08 V/µs	0.2 V/µs
Power Bandwidth (10 Vp-p Input)	2.6 kHz	6.4 kHz

FIGURE 34 – TRACKING A TO D CONVERTER BASIC 8 BIT SYSTEM

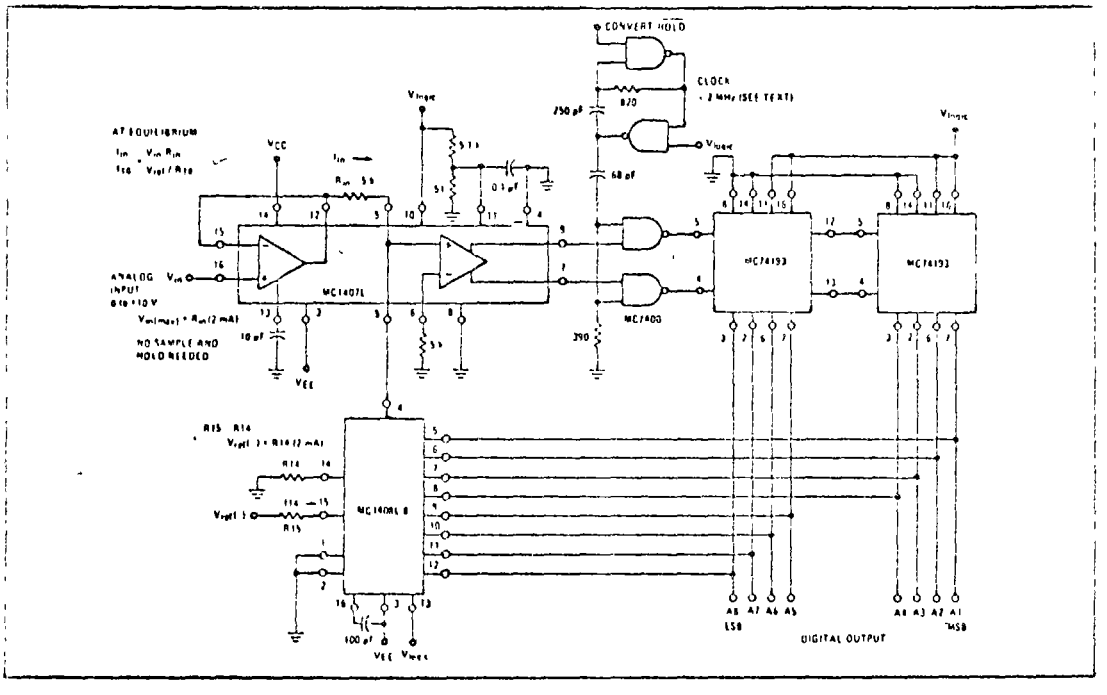
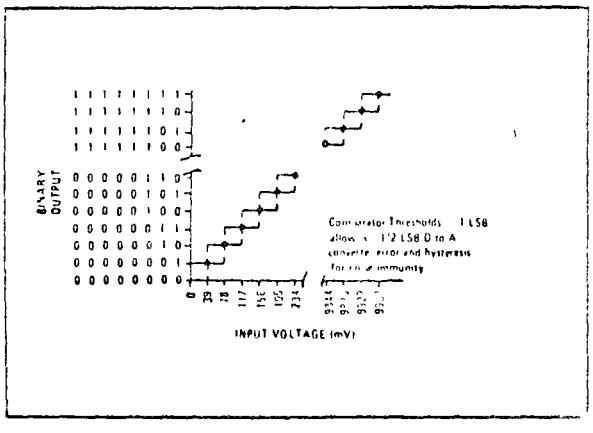


FIGURE 35 – 8 BIT TRACKING A TO D CONVERTER TRANSFER CHARACTERISTIC



APPLICATIONS INFORMATION (continued)

HIGH SPEED SYSTEM

When the input voltage to the tracking A to D converter varies more rapidly than the system slew rate, the output will be unable to follow the input and thus there is no need for the D to A converter to settle between each clock pulse. A second MC1507L may be employed as a window detector to indicate when the converter summing node is more than a given voltage from the comparator deadband, as shown in Figure 36. When the window detector fires, the MC4024 voltage controlled multivibrator quadruples its clock rate, and the system switches to the "Panic Mode". When the summing node comes back within 130 mV of ground, the system resumes its normal clock rate and cleanly settles into the tracking mode.

The Panic Mode system is well suited to multiplexed data acquisition systems where the voltage presented to the input may step quickly between various levels. Also, the power bandwidth has quadrupled and the system will follow 25 kHz full scale sine waves with slightly more distortion than when in the normal tracking mode.

FIGURE 36 – TRACKING A TO D CONVERTER HIGH SPEED SYSTEM (With Panic Mode Operation and Voltage Reference)

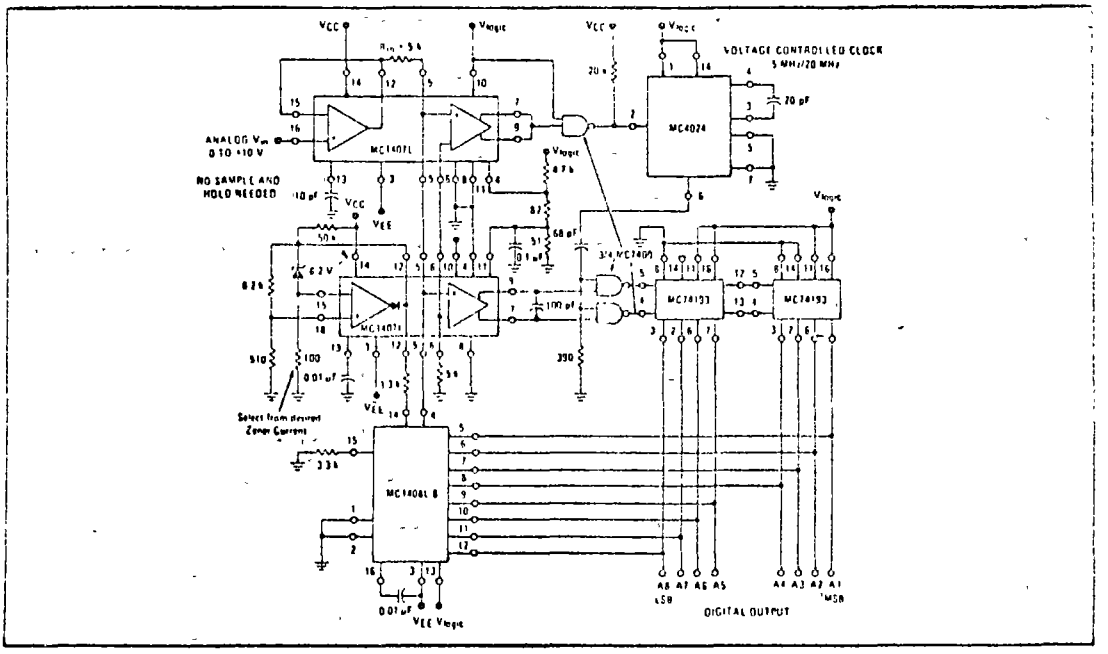
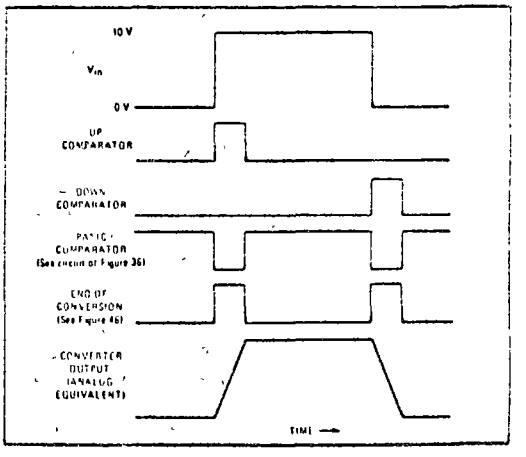


FIGURE 37 – TRACKING A TO D CONVERTER WAVEFORMS WITH STEP INPUT

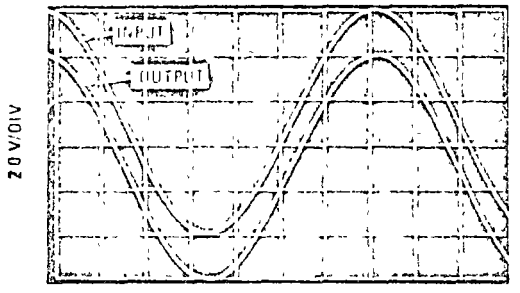


TYPICAL PERFORMANCE TABLE FOR HIGH SPEED SYSTEM

	2 MHz/8 MHz CLOCK (for continuously varying inputs)	5 MHz/20 MHz CLOCK (for dc or step inputs)
Normal Conversion Update Time	0.5 µs	0.2 – 1 µs
Typical Full Scale Conversion Time	32 µs	14 µs
Slew Rate (10 V Input Range)	0.32 V/µs	0.8 V/µs
Power Bandwidth 10 Vp-p Input	10.4 kHz	25.6 kHz

APPLICATIONS INFORMATION (continued)

FIGURE 38 – BASIC 8 BIT TRACKING A TO D CONVERTER SINE WAVE RESPONSE



200 μs/DIV
CLOCK FREQUENCY = 2.0 MHz
Digital output has been converted to analog using an ultra high speed D to A converter

FIGURE 39 – EXPANDED PORTION OF FIGURE 38

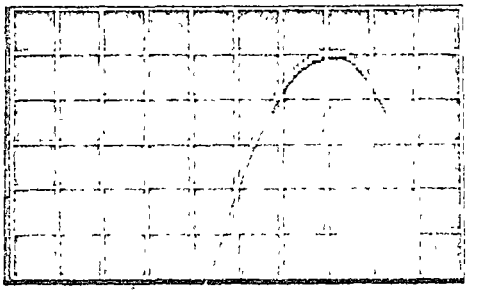
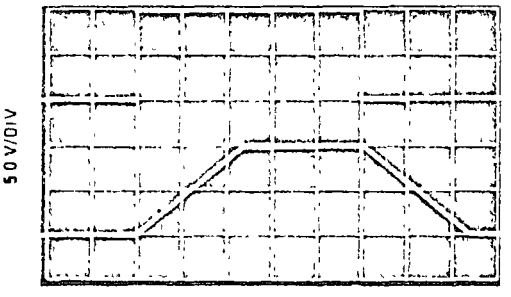
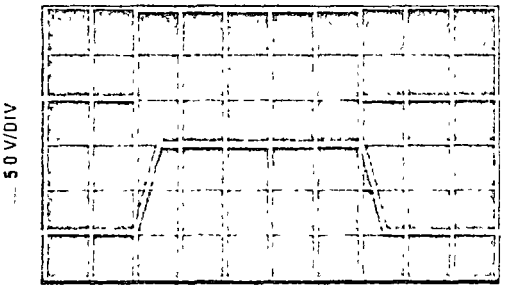


FIGURE 40 – BASIC 8 BIT TRACKING A TO D CONVERTER STEP RESPONSE



20 μs/DIV
CLOCK FREQUENCY = 5.0 MHz

FIGURE 41 – HIGH SPEED 8 BIT TRACKING A TO D CONVERTER STEP RESPONSE



20 μs/DIV
Clock Frequency increases from 5.0 MHz to 20 MHz with voltage controlled MC4024 in Panic Mode operation

6 BIT TRACKING A TO D CONVERTER

A 6 bit tracking A to D converter may be constructed with the MC1506. The circuit differs in one respect from the 8 bit system since the MC1506 has inverting logic inputs. In order to preserve negative feedback in the loop a hex inverter may be used ahead of the D to A converter. However, if inverted logic outputs can be tolerated, the hex inverter is not necessary. By merely interchanging the UP and DOWN comparator outputs the counting direction is inverted, compensating for the inversion in the D to A converter.

The MC1506 has a faster settling time and one fourth the number of output states, so the advantage of this system is higher speed.

TYPICAL PERFORMANCE DATA FOR 6 BIT SYSTEM

	BASIC SYSTEM 3 MHz CLOCK (for continuously varying inputs)	PANIC MODE SYSTEM 5 MHz/20 MHz CLOCK (for dc or step inputs)
Normal Conversion or Update Time	0.33 μs	0.2 – 1.0 μs
Typical Full Scale Conversion Time	21 μs	4.0 μs
Slew Rate (10 V Input Range)	0.5 V/μs	3.3 V/μs
Power BAndwidth 10 V(p-p) Input	16 kHz	105 kHz

APPLICATIONS INFORMATION (continued)

TRACKING CONVERTER SYSTEM OPTIONS

FIGURE 42 – UP/DOWN COUNTER WITH SINGLE CLOCK INPUT

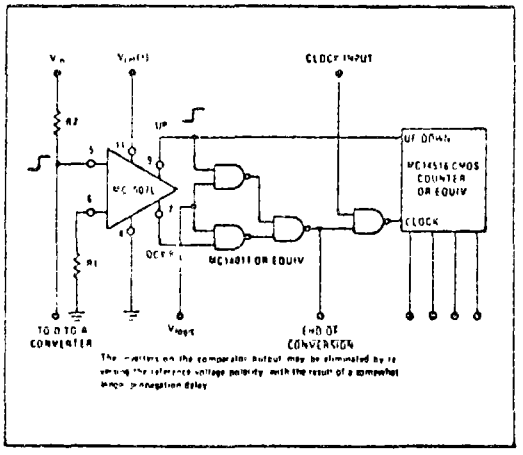


FIGURE 43 – BIPOLAR INPUT

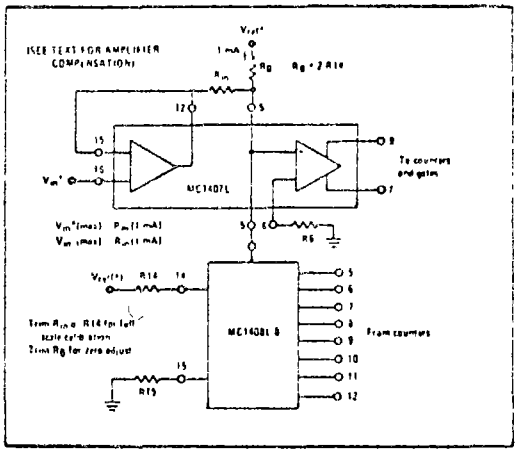


FIGURE 44 – NEGATIVE INPUT

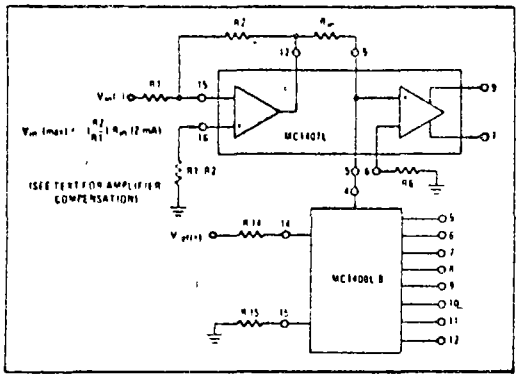
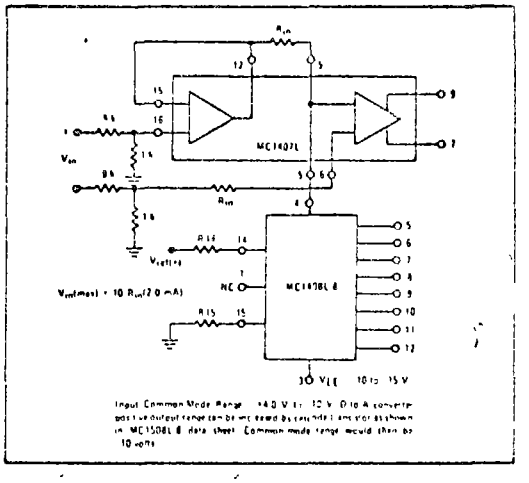


FIGURE 45 – DIFFERENTIAL INPUT

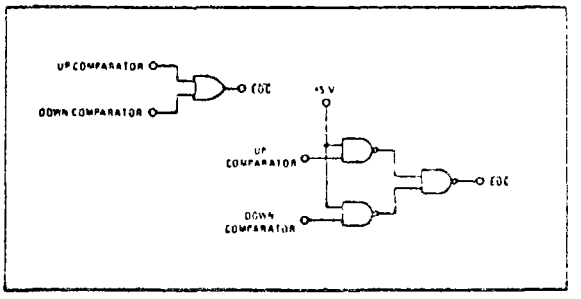


END OF CONVERSION

A useful feature of the dual threshold tracking A to D converter is a simple method of sensing end of conversion. When the system has reached equilibrium the summing node voltage is in the comparator deadband and both UP and DOWN outputs are low. These outputs can be fed to an OR gate to provide an $\overline{EOC}$ indication, or to three NAND gates as shown in Figure 46. This is a feature which is not available with a single threshold system, since its comparator is continually changing state.

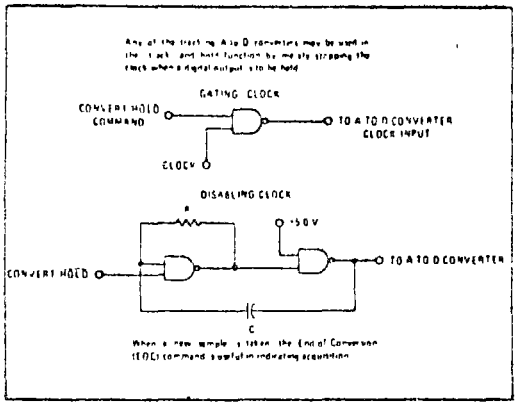
If the A to D converter data is stored in latches, the $\overline{EOC}$ output can be fed to a NAND gate with the latch strobe command to insure accurate data transfer. If the strobe command occurs while the system is searching, the output from the previous conversion will be retained. However, an advantage of the tracking system is that, unlike successive approximation, its output always reflects a value equal to the present or very recent input level.

FIGURE 46 – END OF CONVERSION OPTIONS



APPLICATIONS INFORMATION (continued)

FIGURE 47 - DIGITAL TRACK AND HOLD



PEAK DETECTING TRACK AND HOLD CIRCUIT WITH DIGITAL OUTPUT AND INFINITE HOLD TIME

The basic tracking A to D converter may be used as a positive peak detecting track and hold system by disabling the DOWN counting function. This may be performed by gating or by eliminating the DOWN connections. The system may be reset to zero by the counter reset or by re-enabling the DOWN function, shorting the converter input to ground, and allowing the output to track to zero. If the DOWN gate is disconnected from the MC74193 counter, this counter input must be connected high to allow proper functioning of the UP counter.

A negative peak detecting track and hold system is implemented by modifying the input of the above circuit to accept negative input signals, as shown in Figure 47.

TRACK AND HOLD OR PEAK DETECTION WITH ANALOG OUTPUT

The basic tracking converter system may be modified for use in the track and hold function or as a peak detecting track and hold. Analog output and infinite hold time are available with the methods shown in Figures 48-51.

FIGURE 48 – CONNECTION CONFIGURATION FOR POSITIVE INPUT AND OUTPUT

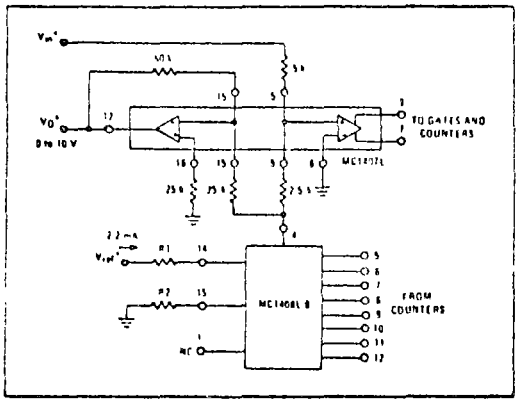


FIGURE 49 – CONNECTION CONFIGURATION FOR NEGATIVE INPUT AND OUTPUT

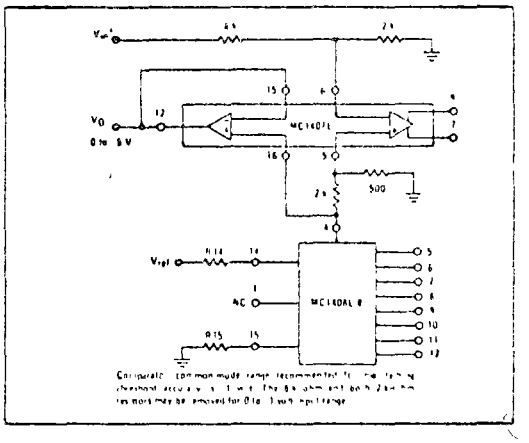


FIGURE 50 – CONNECTION CONFIGURATION FOR POSITIVE INPUT AND NEGATIVE OUTPUT

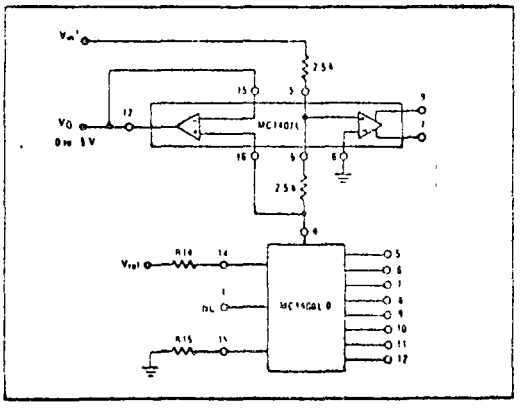
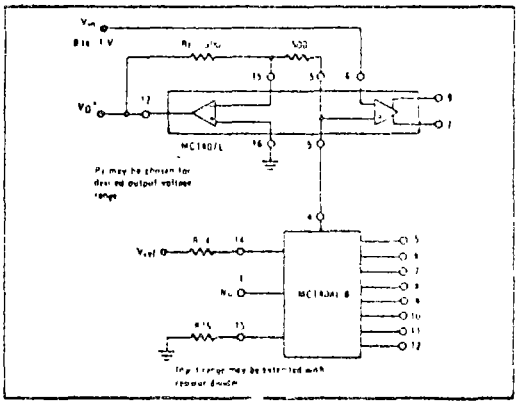


FIGURE 51 – CONNECTION CONFIGURATION FOR NEGATIVE INPUT AND POSITIVE OUTPUT



SUGGESTED DESIGN APPLICATIONS

FIGURE 52 – SUCCESSIVE APPROXIMATION A TO D CONVERTER

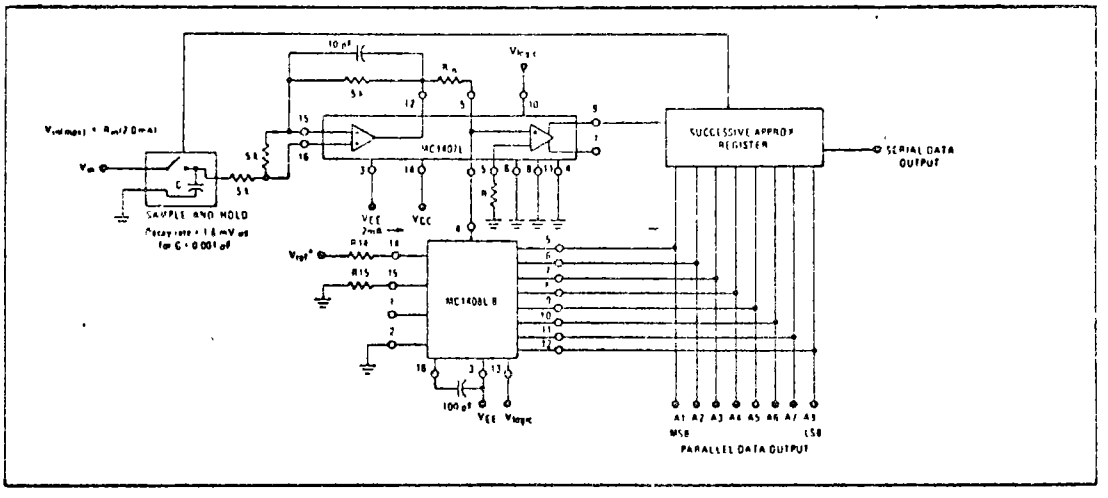


FIGURE 53 – HIGH SPEED INTEGRATOR

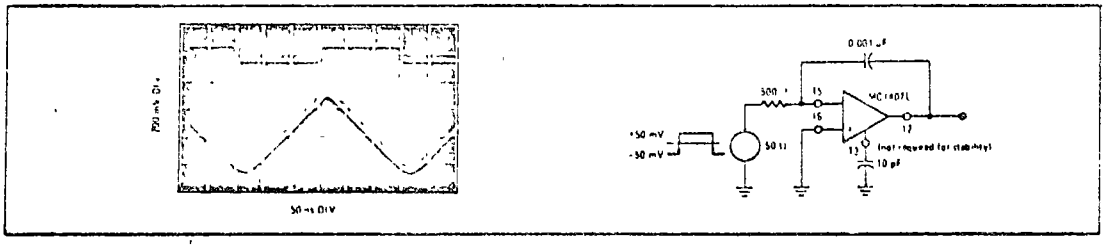
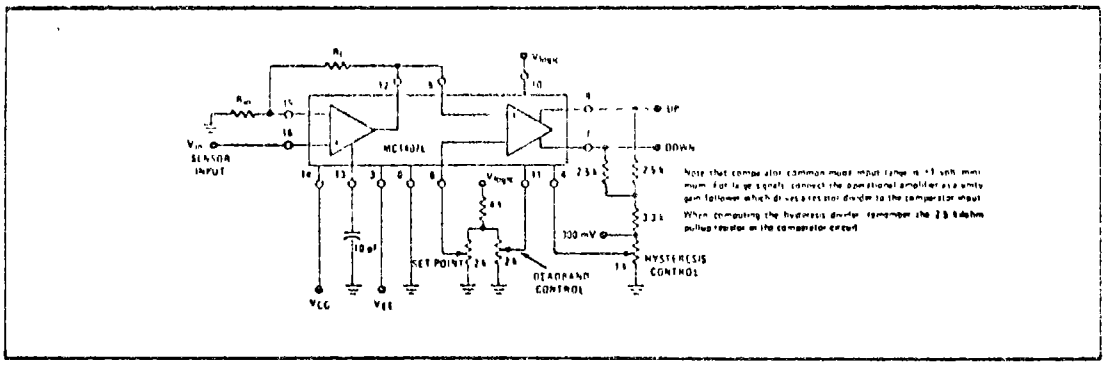
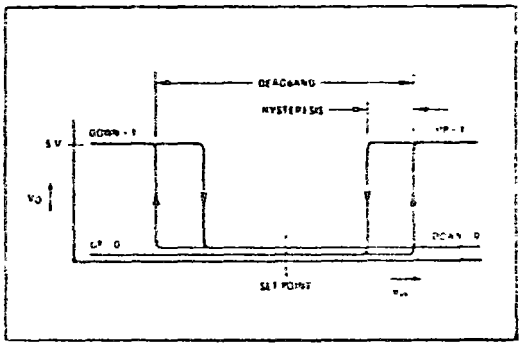


FIGURE 54 – SET POINT CONTROL CIRCUIT
(Featuring variable deadband and hysteresis)



SUGGESTED DESIGN APPLICATIONS (continued)

FIGURE 55 – TRANSFER CHARACTERISTIC OF SET POINT CONTROL



Variable Deadband Set-Point Controls are used in control systems to compensate for large time constants in the controlled systems. The dual output control shown in Figure 54 controls two variables, such as heating and cooling, that keep a controlled variable, such as temperature, centered on the set point or operating point.

The set point voltage need not be produced by the potentiometer but can be a reference voltage supplied by the controlled system. As the set point moves linearly this voltage could come from an MC1508L-8 D to A converter which would provide digital control of the set point. Deadband could be controlled by the system in a similar manner.

FIGURE 56 – HIGH SPEED DELTA MODULATOR
(with optional hysteresis)

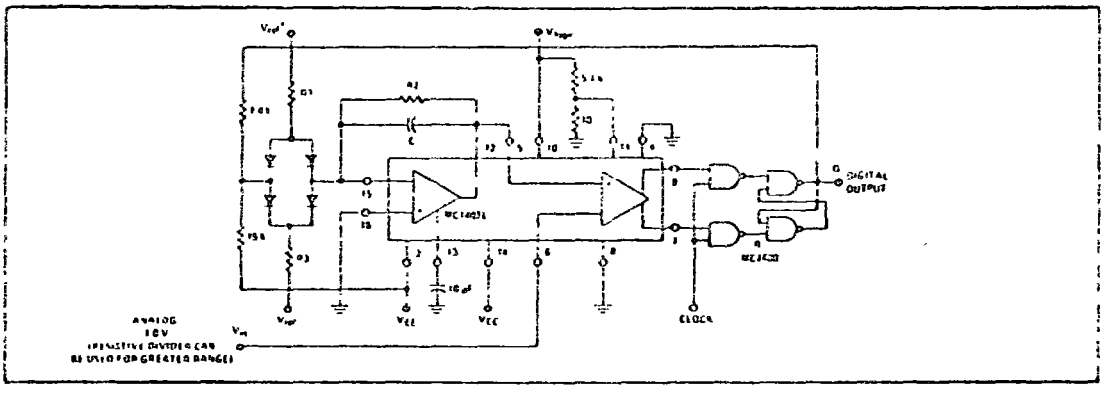
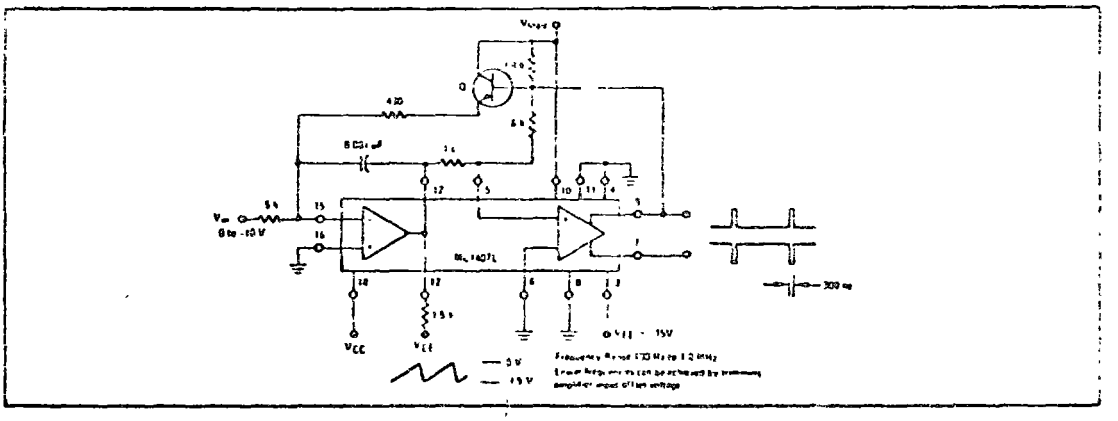


FIGURE 57 – WIDE RANGE VOLTAGE TO FREQUENCY CONVERTER
(Useful As Voltage Controlled Multivibrator, FM Modulator, or Sawtooth Generator)



MC1508L-8
MC1408L-8
MC1408L-7
MC1408L-6

D-TO-A CONVERTER

Specifications and Applications Information

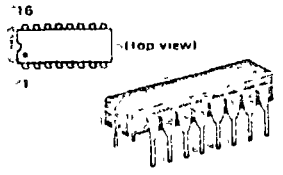
MONOLITHIC EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

designed for use where the output current is a linear product of an eight bit digital word and an analog input voltage.

- Relative Accuracy ±0.19% Error maximum (MC1508L-8/MC1408L-8)
- Seven and Six Bit Accuracy Available (MC1408L-7, MC1408L-6)
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.5 V to -5.0 V
- High Speed Multiplying Input Slew Rate 4.0 mA/μs
- Standard Supply Voltages. +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – D to A TRANSFER CHARACTERISTICS

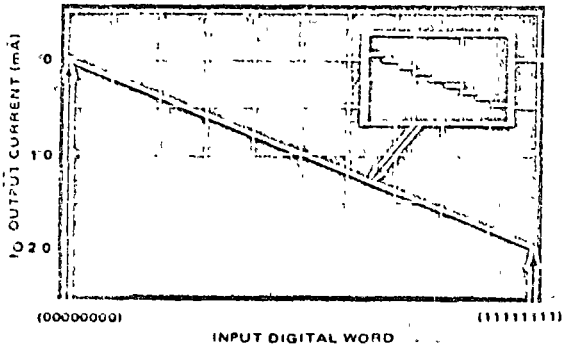
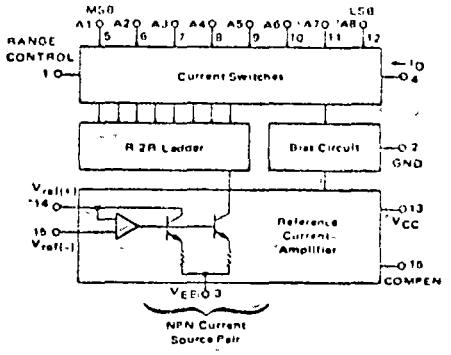


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A to D Converters
- Successive Approximation A to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog Digital Multiplication
- Digital Digital Multiplication
- Analog Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

See Packaging Information Section for outline dimensions.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	+5.5,0	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1508L8 MC1408L Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L-8 T_A = -55°C to +125°C
MC1408L Series T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8 MC1408L7, See Note 1 MC1408L6, See Note 1	4	E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	%
Settling Time to within 1/2 LSB (includes t_{PLH}) (T_A = +25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	±20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.01 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-3.0	µA
Output Current Range V_{EE} = -5.0 V V_{EE} = -6.0 to -15 V	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	1.9	1.99	2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	µA
Output Voltage Compliance (E_r ≤ 0.19% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.6,+0.5 -5.0,+0.5	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/µs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	µA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +125°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT

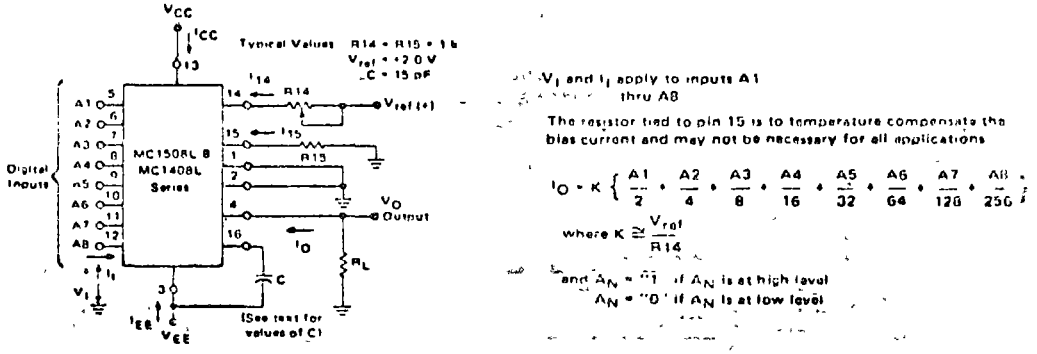


FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

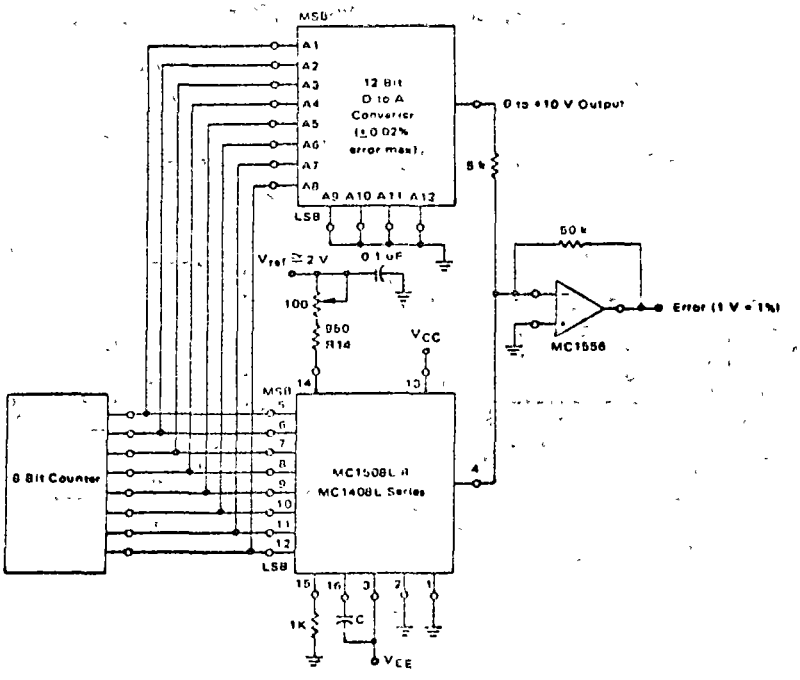
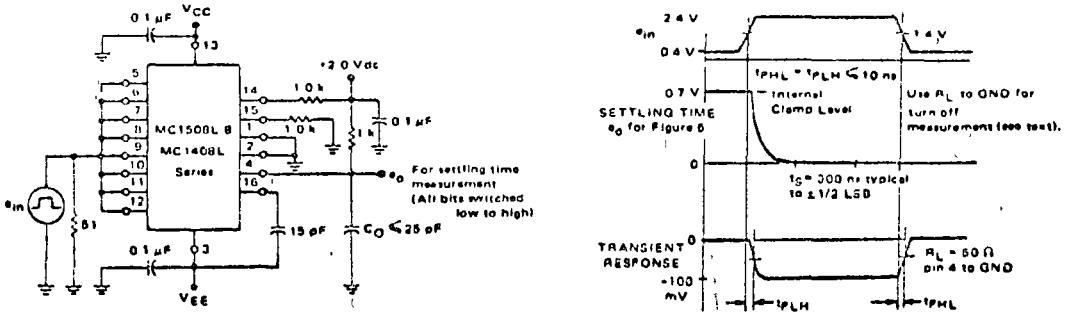


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

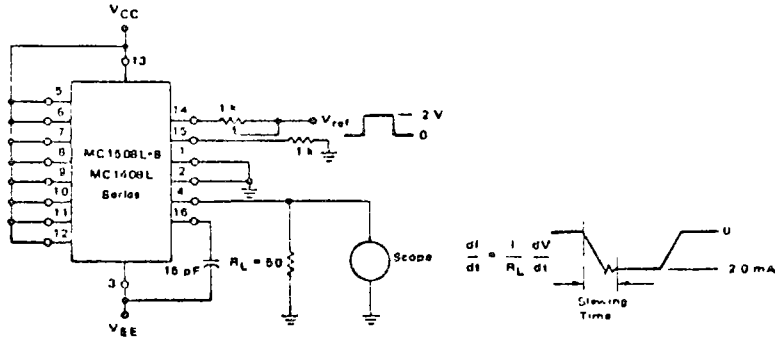


FIGURE 7 – POSITIVE V_{ref}

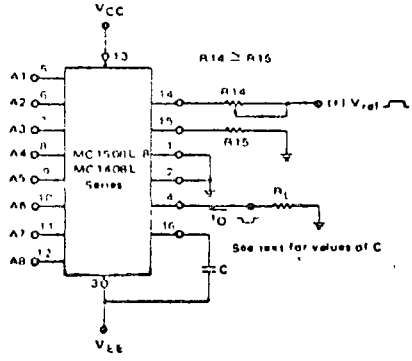


FIGURE 8 – NEGATIVE V_{ref}

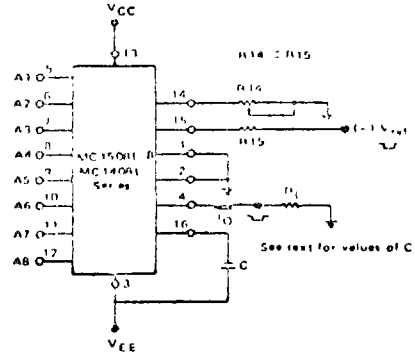
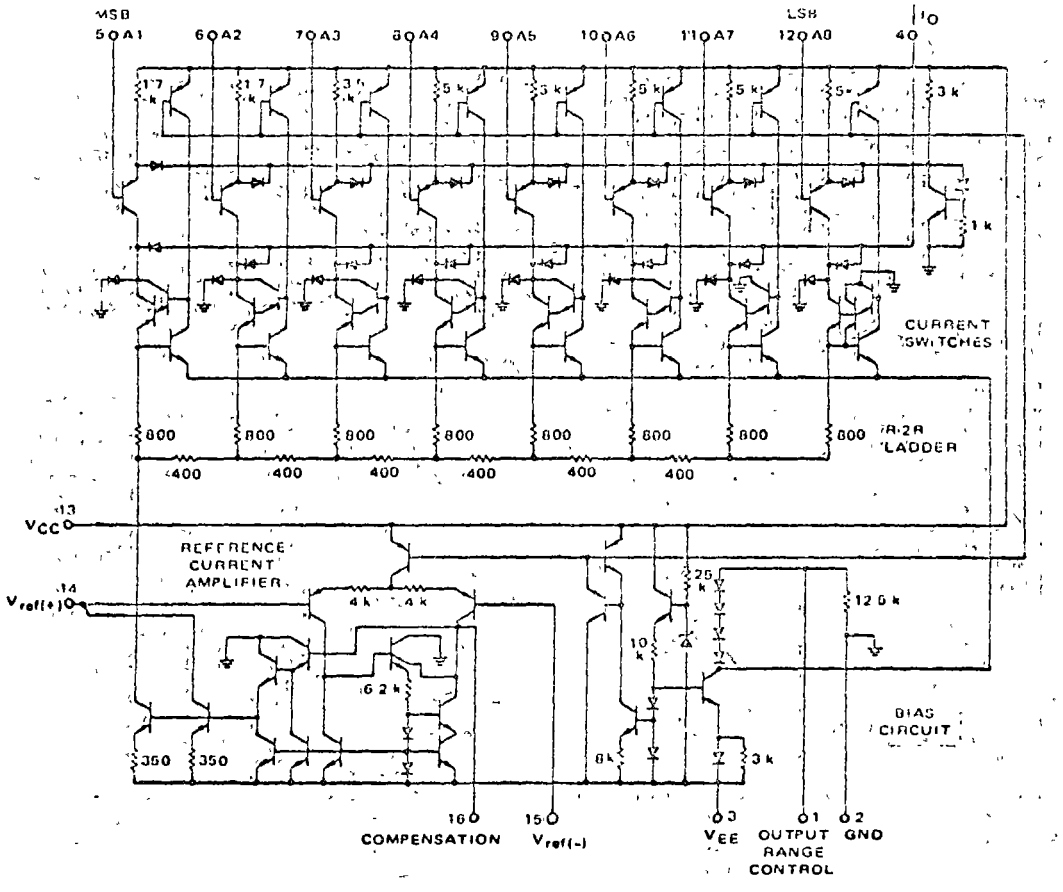


FIGURE 9 – MC1508L-8/MC1408L SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1508L-8 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current-steering for high-speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin. For R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16 using the values of the previous paragraph. The negative reference voltage must be at least 3.0 volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to +0.5 volts at +25°C due to the current switching methods employed in the MC1508L-8. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508L-8 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.4 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -6.0 volts due to the increased voltage drop across the 350 ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508L-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508L-8 has a very low full scale current drift with temperature.

The MC1508L-8/MC1408L-8 series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12 bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1508L-8 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1508L-8 circuits full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8 bit D to A converters may not be used to construct a 16 bit accurate D to A converter. 16 bit accuracy implies a total error of ±1/2 of one part in 65,536 or ±0.0007%, which is much more accurate than the ±0.19% specification provided by the MC1508L-8.

Multiplying Accuracy

The MC1508L-8 may be used in the multiplying mode with eight bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508L-8 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The 'worst case' switching condition occurs when all bits are switched "on", which corresponds to a low to high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB for 8 bit accuracy and 200 ns to 1/2 LSB for 7 and 6 bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D to A converter functions in a positive going ramp mode the "worst case" switching condition does not occur, and the settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A8 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC1508L-8. A 1.0 kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

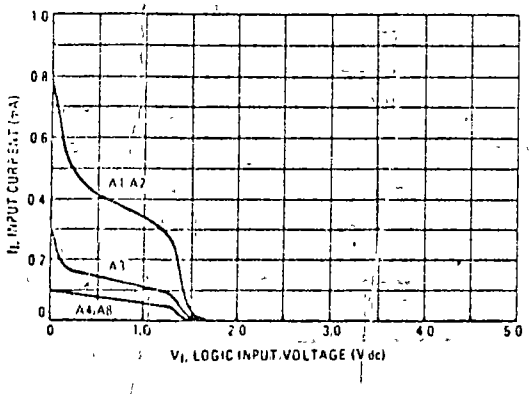


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

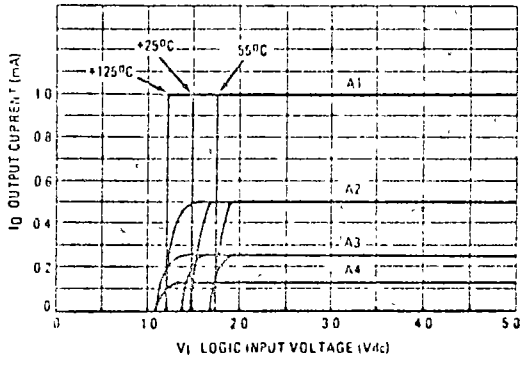


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

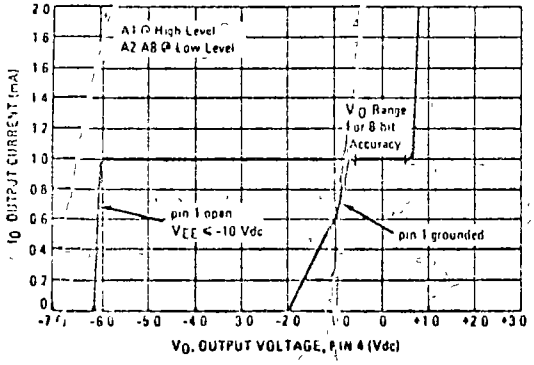
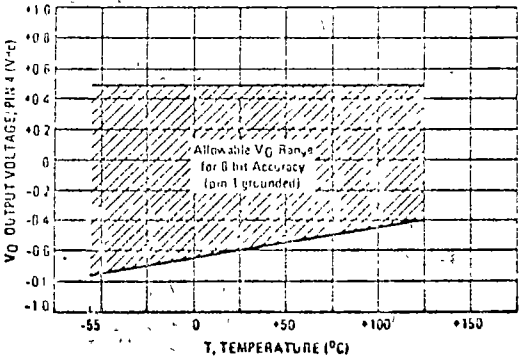


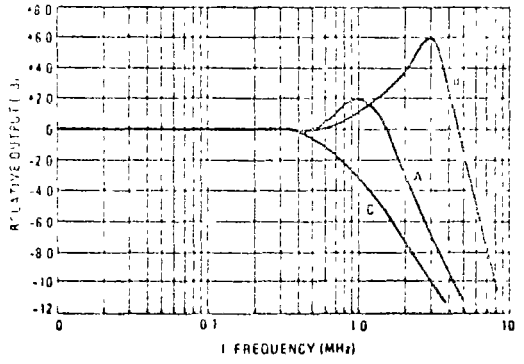
FIGURE 13 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A — Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B — Small Signal Bandwidth
Method of Figure 7, R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C — Large and Small Signal Bandwidth
Method of Figure 25 (no op amp), R_L = 50 Ω
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

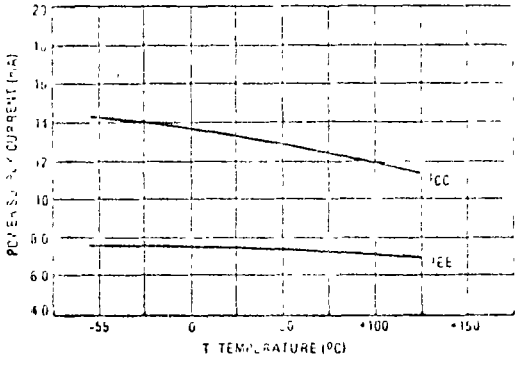
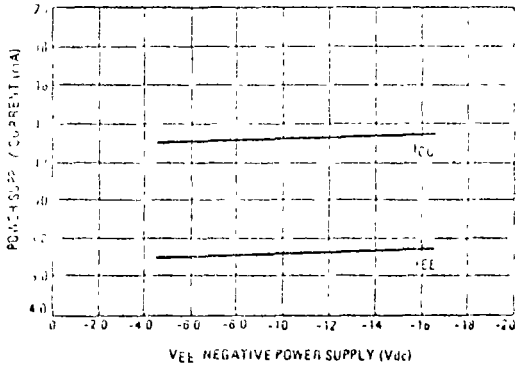
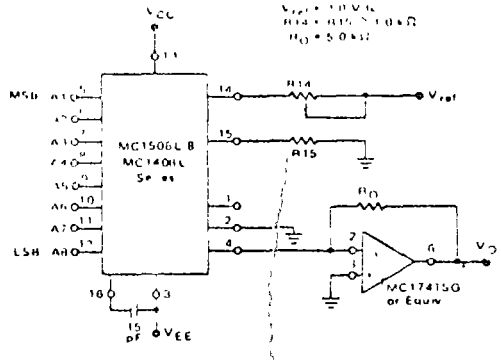


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k\Omega}(5\ k\Omega)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

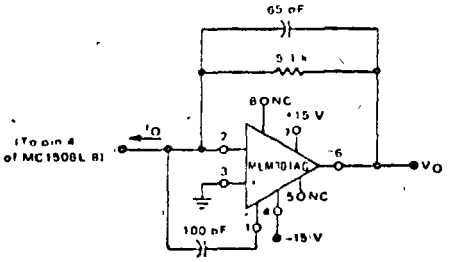
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1508L-8 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

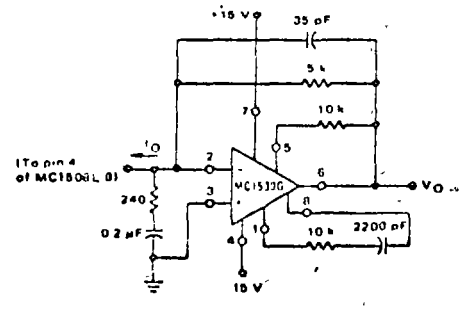
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 18



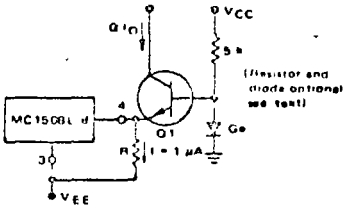
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 µs. See Motorola Application Note AN 459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high speed operation is possible with a large output voltage swing because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are 'off' and insures fast turn on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1508L-8 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common mode signal to the reference amplifier in the D to A converter. This allows use of its output amplifier as a classic current to voltage converter with the non inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital to analog system only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

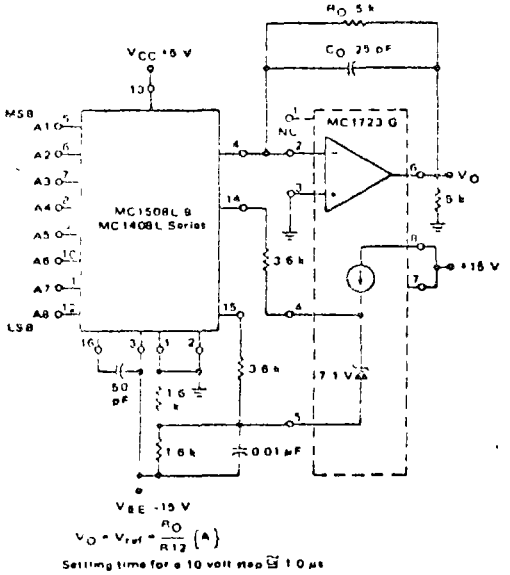
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD to binary converter. The output voltage can be scaled in several ways including 0 to +25.5 volts in 0.1 volt increments, ±0.05 volt, or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



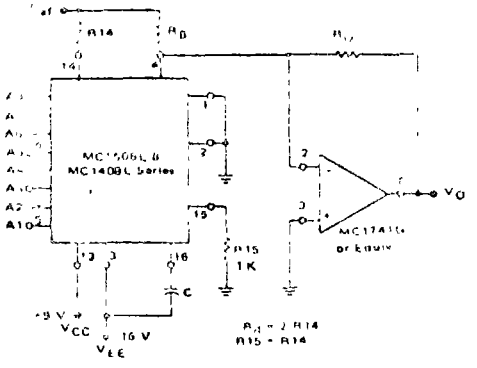
$$V_O = V_{ref} = \frac{R_O}{R12}(A)$$

Settling time for a 10 volt step = 1.0 μs

Bipolar or Negative Output Voltage

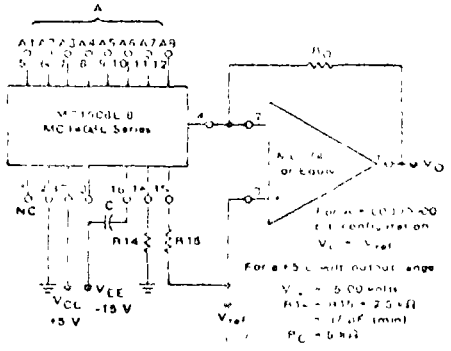
The circuit of Figure 22 is a variation of the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, a 1.0 mA current is used a bipolar output signal results which may be decoded as a B but 1's complement offset binary. V_{ref} may be used as this auxiliary reference. (Note that R_O has been doubled to 10 kilohms because of the anticipated 20 Vp-p output range.)

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



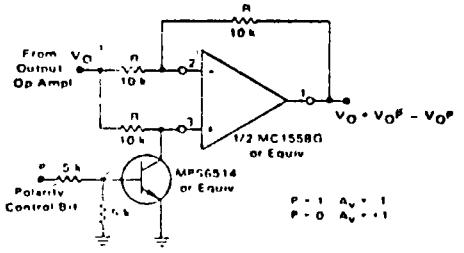
Decrease R_O to 2.5 kΩ for a 0 to -5 V output or range. This application provides some that lower [illegible] previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D to A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8 bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT (8 Bit Magnitude Plus Sign D to A Converter)



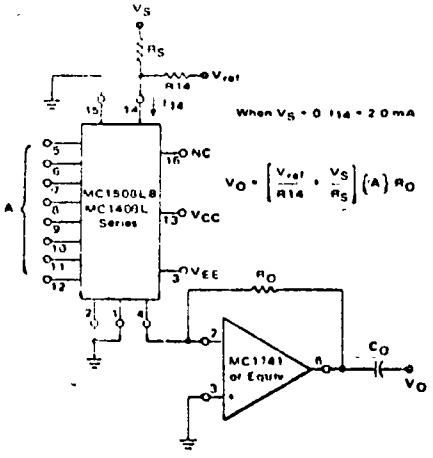
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1508L-8 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1508L-8 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

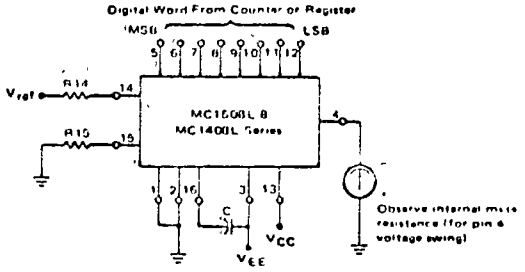
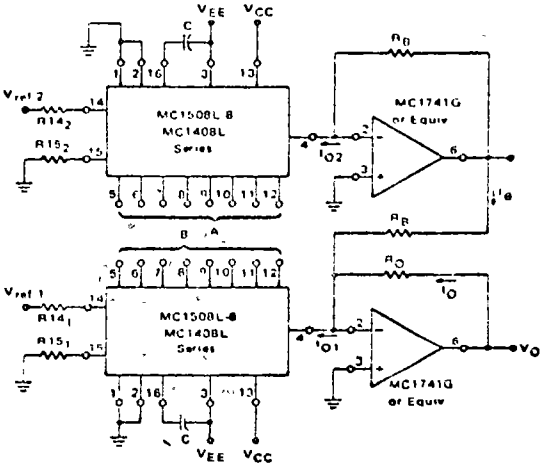


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}(A) - \frac{V_{ref\,2}}{R14_2}(B) \qquad I_{O2} = I_B$$

$$I_B = I_O = I_{O1}$$

Digital Subtraction

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

$$V_O = \frac{V_{ref\,1}}{R15_1} R_O \left[(A) - (B)\right]$$

Programmable Amplifier

Connect Digital Inputs so A = B

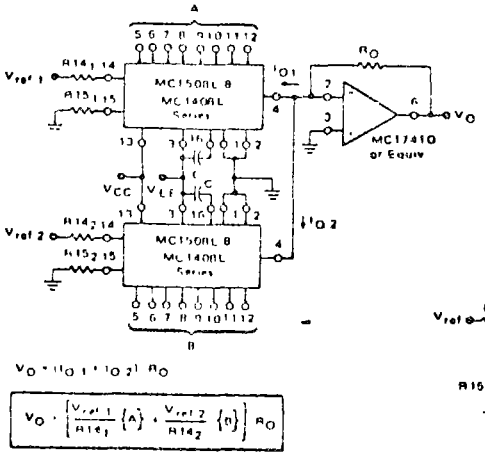
$$V_O = (A)\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]$$

APPLICATIONS INFORMATION (continued)

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input and drive $R15_1$ and $R15_2$. This yields high input impedance, bipolar differential and common mode range.

FIGURE 28 – DIGITAL SUMMING and CHARACTER GENERATION



In a character generation system one MC1508L 8 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16 bit D to A converter (see Accuracy Section).

FIGURE 29 – POSITIVE PEAK DETECTING SAMPLE and HOLD
(Features indefinite hold time and optional digital output)

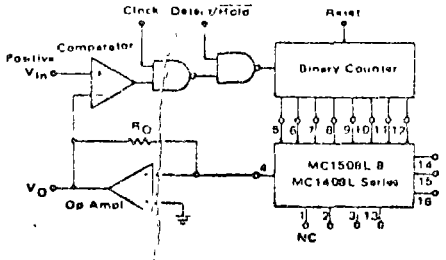


FIGURE 30 – NEGATIVE PEAK DETECTING SAMPLE AND HOLD

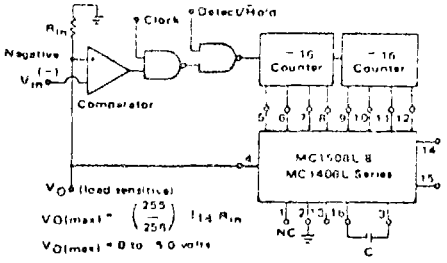
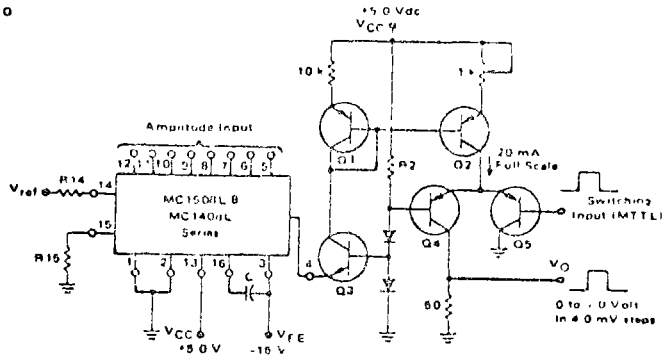
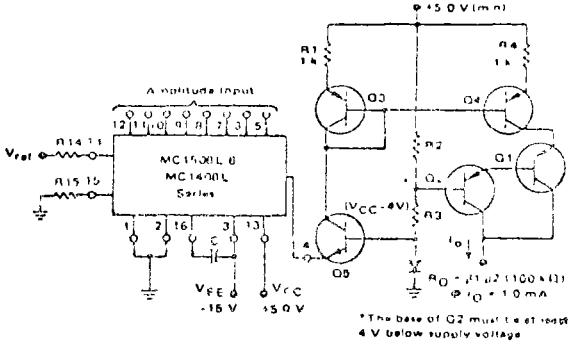


FIGURE 31 – PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high speed switching transistors for the differential pair Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

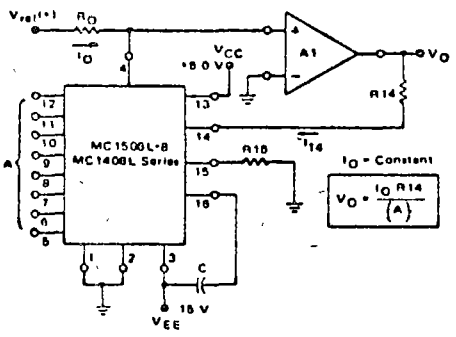
FIGURE 32 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

APPLICATIONS INFORMATION (continued)

FIGURE 33 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 34 - ANALOG QUOTIENT OF TWO DIGITAL WORDS

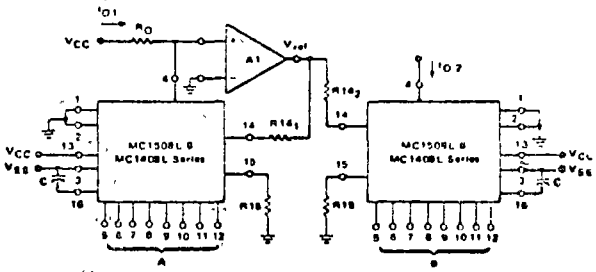
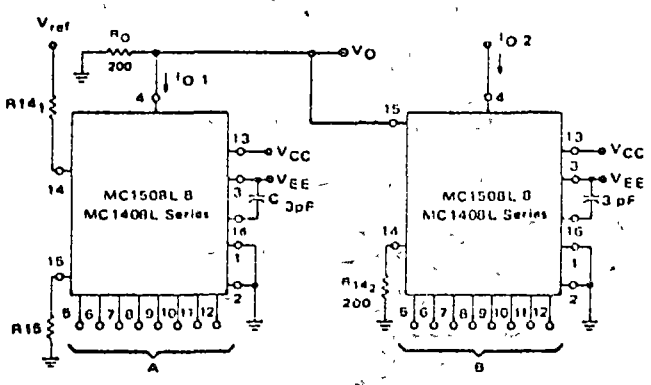


FIGURE 35 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High Speed Operation)



$$V_O = -I_{O1} R_O = \frac{V_{ref}}{R14_1} \{A\} R_O$$

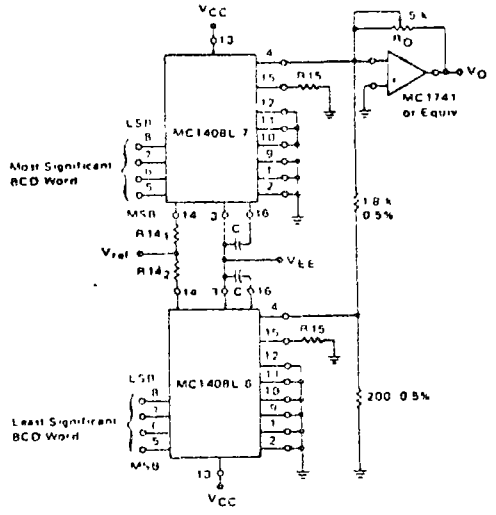
$$I_{O2} = \frac{\{B\} |V_O|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_O \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$I_{O2} = K \{A\} \{B\}$ K can be an analog variable

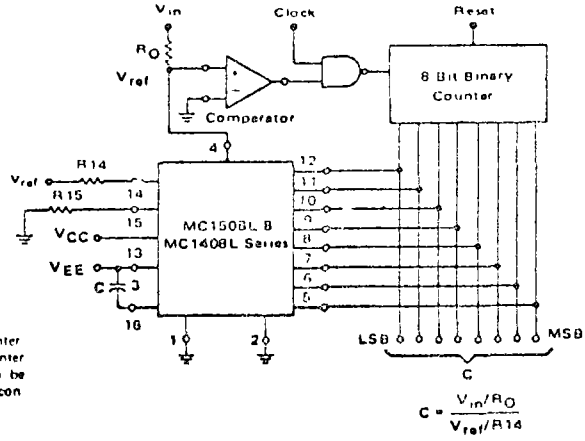
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO DIGIT BCD CONVERSION



Two 8 bit D to A converters can be used to build a two digit BCD D to A or A to D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D to A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L-6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG TO DIGITAL CONVERSION



$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide fast operation and continuous conversion.

MC1596
MC1496

BALANCED MODULATOR-DEMODULATOR

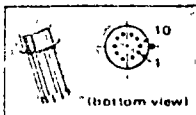
Specifications and Applications Information

MONOLITHIC BALANCED MODULATOR – DEMODULATOR

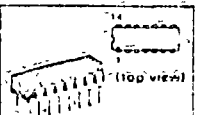
designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression — 65 dB typ @ 0.5 MHz
  — 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection — 85 dB typ

BALANCED MODULATOR—DEMODULATOR
INTEGRATED CIRCUIT
SILICON
EPITAXIAL PASSIVATED



CASE 602A
Metal Package
Suffix G



CASE 632 (TO-116)
Ceramic Package
Suffix L

FIGURE 1 — SUPPRESSED CARRIER OUTPUT WAVEFORM

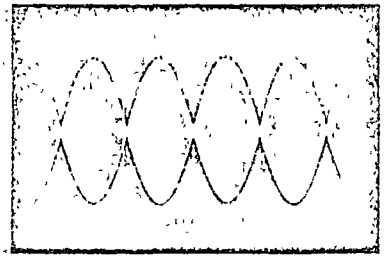


FIGURE 2 — AMPLITUDE MODULATION OUTPUT WAVEFORM

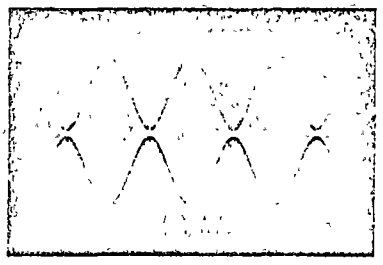


FIGURE 3 — SUPPRESSED CARRIER SPECTRUM

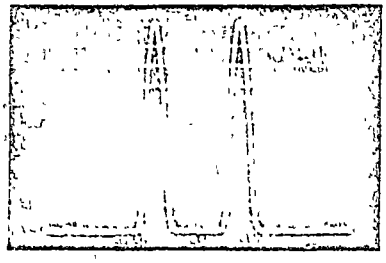


FIGURE 4 — AMPLITUDE MODULATION SPECTRUM

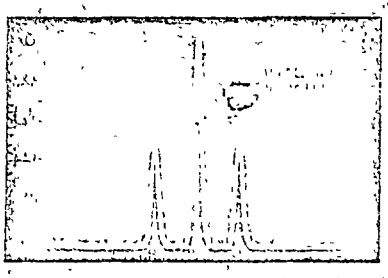
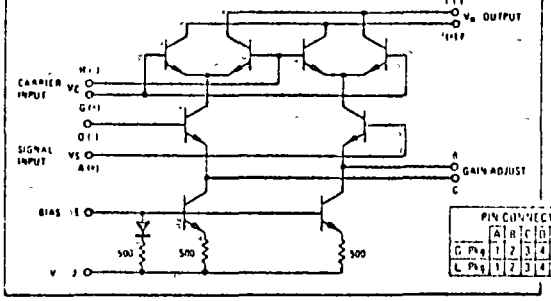


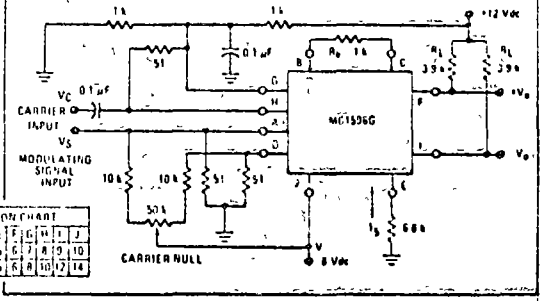
FIGURE 5 — CIRCUIT SCHEMATIC



PIN CONNECTION CHART

	A	B	C	D	E	F	G	H	I	J
G Pkg	1	2	3	4	5	6	7	8	9	10
L Pkg	1	2	3	4	5	6	8	10	12	14

FIGURE 6 — TYPICAL MODULATOR CIRCUIT



See Packaging Information Section for outline dimensions

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	±5.0 ±(I_5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In Line Package		575	mW
Derate above T_A = +25°C		3.65	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V^+ = +12 Vdc, V^- = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single ended unless otherwise noted.)

Characteristic	Fig	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	7	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz				–	40	–	–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mV p-p square wave										mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.7	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression	7	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	10	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave				–	300	–	–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sine wave										
Signal Input Port, V_S = 300 mV(rms) sine wave				–	80	–	–	80	–	
$\lvert V_C \rvert$ = 0.5 Vdc										
Signal Gain	12	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc										
Single Ended Input Impedance, Signal Port, f = 5.0 MHz	8	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single Ended Output Impedance, f = 10 MHz	8	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current	9	–								μA
$I_{bS} = -\frac{I_1 + I_4}{2}$ $I_{bC} = \frac{I_7 + I_8}{2}$			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current	9	–								μA
$I_{oS} = I_1 - I_4$ $I_{oC} = I_7 - I_8$			$\lvert I_{oS} \rvert$	–	0.7	5.0	–	0.7	7.0	
			$\lvert I_{oC} \rvert$	–	0.7	5.0	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	9	–	$\lvert TC_{Io} \rvert$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	9	–	$\lvert I_{oo} \rvert$	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	9	–	$\lvert TC_{Ioo} \rvert$	–	90	–	–	90	–	nA/°C
Common Mode Input Swing, Signal Port, f_S = 1.0 kHz	11	4	CMV	–	5.0	–	–	5.0	–	V p-p
Common Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc	11	–	ACM	–	-85	–	–	-85	–	dB
Common Mode Quiescent Output Voltage (Pin 6 or Pin 9)	12	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	12	–	V_{out}	–	8.0	–	–	8.0	–	V p-p
Power Supply Current	9	6								mAdc
$I_6 + I_9$			I_D^+	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_D^-	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	9	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

GENERAL OPERATING INFORMATION*

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0)

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 7)

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified

Carrier suppression is very dependent on carrier input level, as shown in Figure 24. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input signal amplitude (see Note 3 and Figure 22). Note also that an optimum carrier level is recommended in Figure 24 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}.$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}.$$

Note that in the test circuit of Figure 12, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common Mode Swing

The common mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage current products at each port, i.e. assuming $V_8 = V_G$, $I_5 = I_6 = I_9$ and ignoring base current $P_D = 2\,I_5\,(V_6 - V_{10}) + I_5\,(V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega \quad \text{where} \quad R_5 \text{ is the resistor between pin 5 and ground}$$
$$\phi = 0.75\text{ V at } T_A = +25^\circ\text{C}$$

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L.$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table.

$$30\text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}.$$

The foregoing conditions are based on the following approximations.

$$V_6 = V_9. \quad V_7 = V_8. \quad V_1 = V_4.$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by.

$$Y_{21C} = \left.\frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\right| V_o = 0.$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by.

$$Y_{21S} = \left.\frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\right| V_c = 0.5\text{ Vdc}, V_o = 0.$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

Note 9 – Coupling and Bypass Capacitors C_1 and C_2

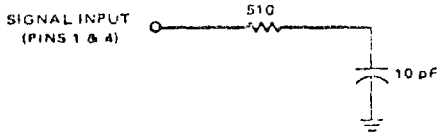
Capacitors C_1 and C_2 (Figure 7) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single ended. Figure 14 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source tuned circuits that cause the oscillation.



An alternate method for low frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 7 – CARRIER REJECTION AND SUPPRESSION

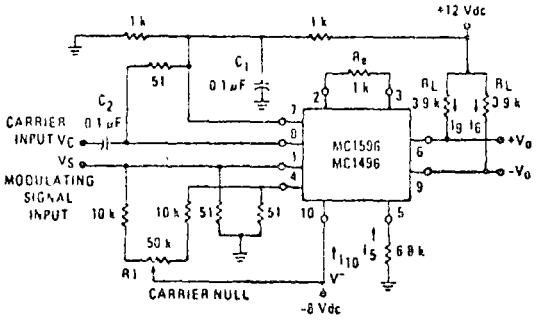


FIGURE 8 – INPUT OUTPUT IMPEDANCE

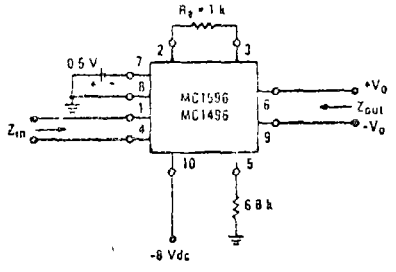


FIGURE 9 – BIAS AND OFFSET CURRENTS

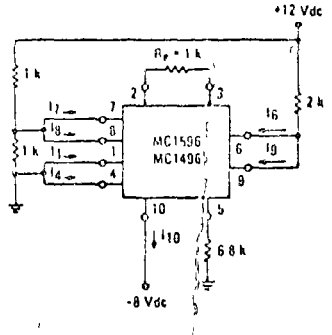
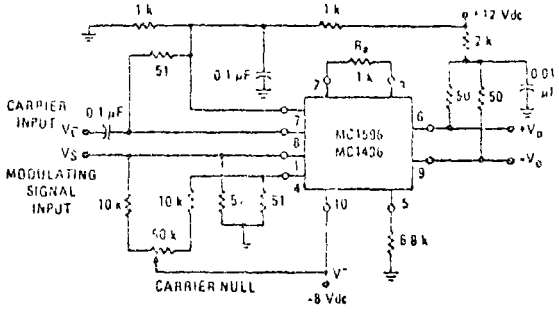


FIGURE 10 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TEST CIRCUITS (continued)

FIGURE 11 – COMMON MODE GAIN

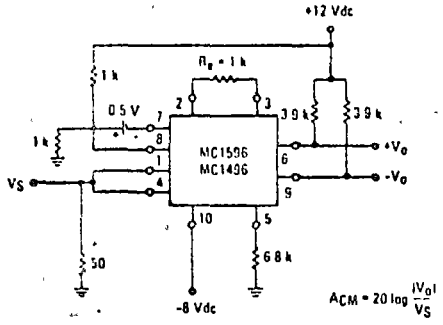
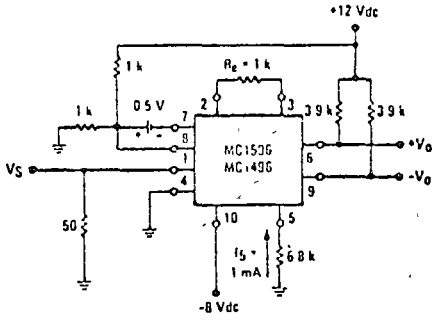


FIGURE 12 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 13 – SIDEBAND OUTPUT versus CARRIER LEVELS

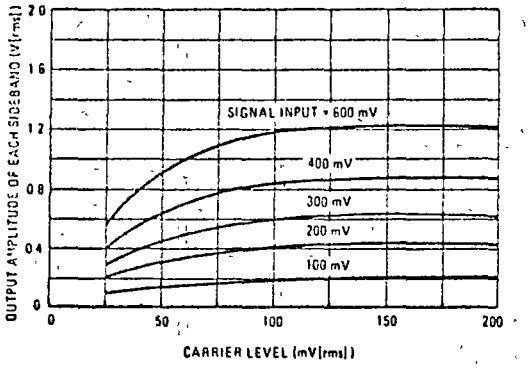


FIGURE 14 – SIGNAL PORT PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

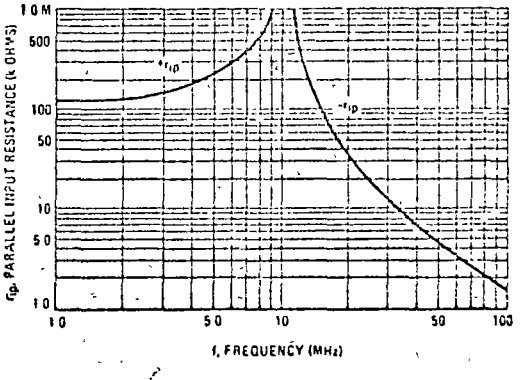


FIGURE 15 – SIGNAL PORT PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

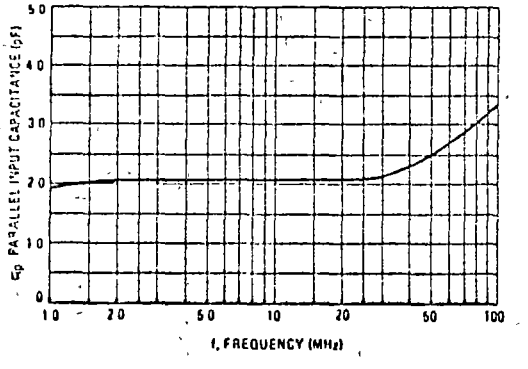
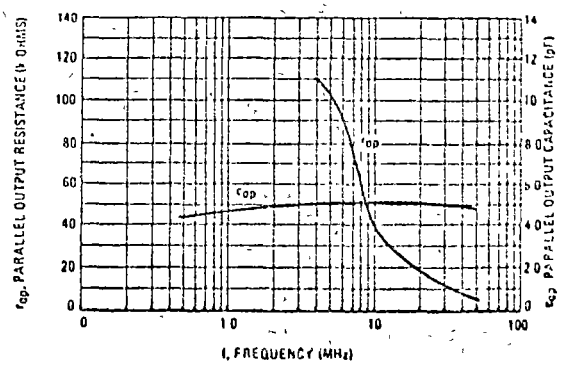


FIGURE 16 – SINGLE ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 7, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 17 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

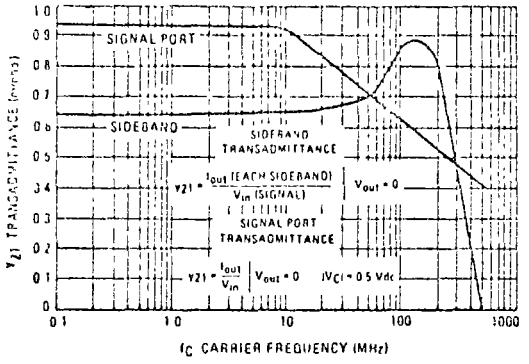


FIGURE 18 – CARRIER SUPPRESSION versus TEMPERATURE

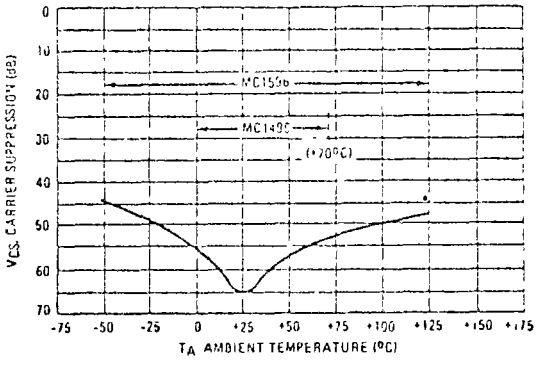


FIGURE 19 – SIGNAL PORT FREQUENCY RESPONSE

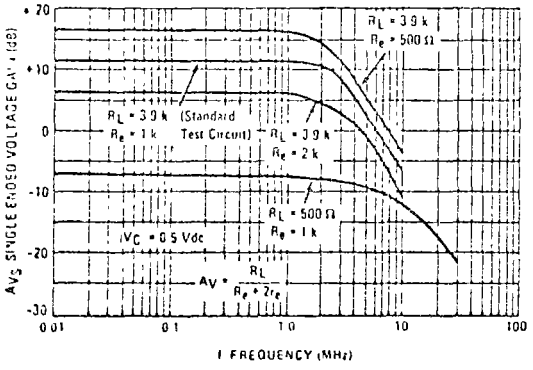


FIGURE 20 – CARRIER SUPPRESSION versus FREQUENCY

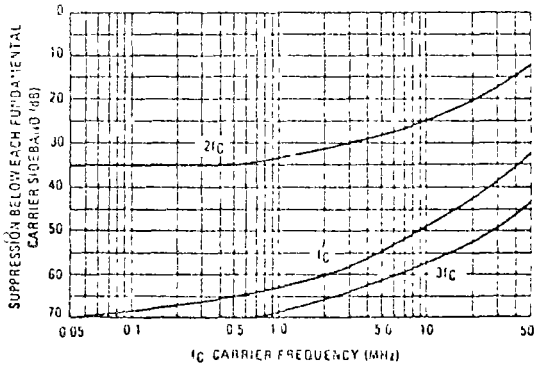


FIGURE 21 – CARRIER FEEDTHROUGH versus FREQUENCY

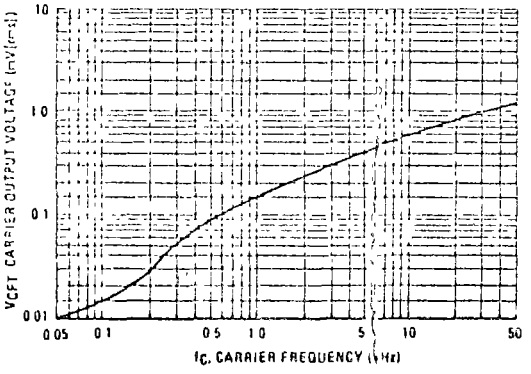
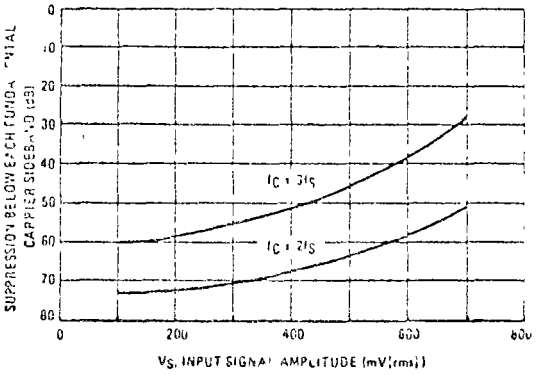


FIGURE 22 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



TYPICAL CHARACTERISTICS (continued)

FIGURE 23 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

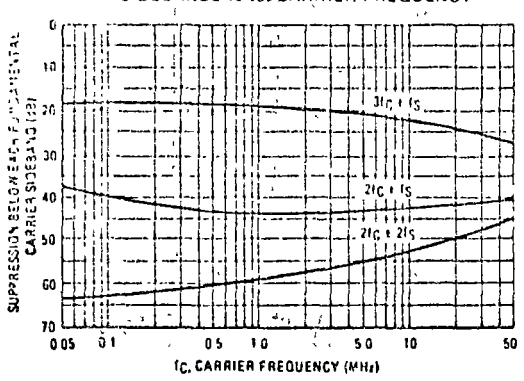
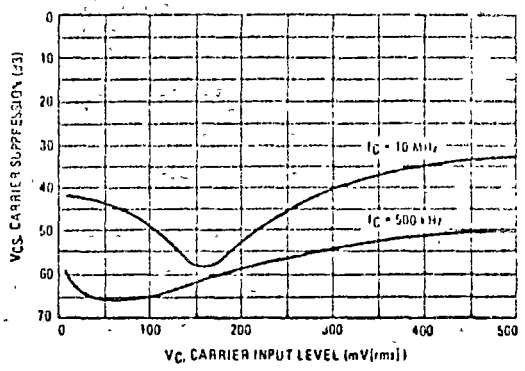


FIGURE 24 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 5

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources The output collectors are cross coupled so that full wave balanced multiplication of the two input voltages occurs That is, the output signal is a constant times the product of the two input signals

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies Thus the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used Also, external load resistors are employed at the device output

The upper quad differential amplifier may be operated either in a linear or a saturated mode The lower differential amplifier is operated in a linear mode for most applications

For low level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes

For high level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency . The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well-defined With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user The maximum input voltage for linear operation may be approximated from the following expression

$$V = (I_5)(R_E) \text{ volts peak}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode Approximate gain expressions have been developed for the MC1596/MC1496 for a low level modulating signal input and the following carrier input conditions

1) Low level dc
2) High level dc
3) Low level ac
4) High level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

Pin number references pertain to this device when packaged in a metal can To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification

OPERATIONS INFORMATION (continued)

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$,

NOTES
1. Low level Modulating Signal, V_M assumed in all cases
   V_C is Carrier Input Voltage
2. When the output signal contains multiple frequencies the gain expression given is for the output amplitude of each of the two desired outputs $f_C + f_M$ and $f_C - f_M$
3. All gain expressions are for a single ended output. For a differential output connection, multiply each expression by two
4. R_L = Load resistance
5. R_E = Emitter resistance between pins 2 and 3
6. r_e = Transistor dynamic emitter resistance, at +25°C

$$r_e \approx \frac{26\ mV}{I_5\ (mA)}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature.}$$

APPLICATION INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of the specification.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

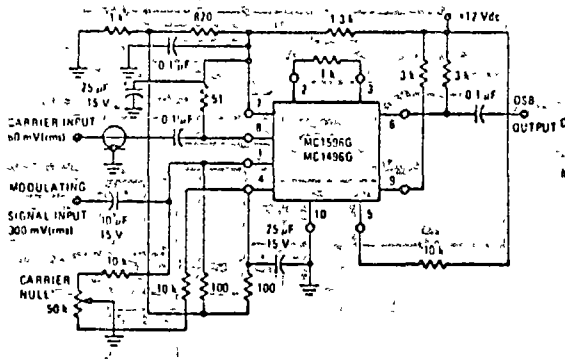


FIGURE 27 – BALANCED MODULATOR DEMODULATOR

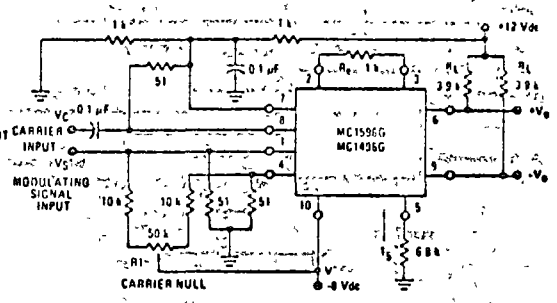


FIGURE 28 – AM MODULATOR CIRCUIT

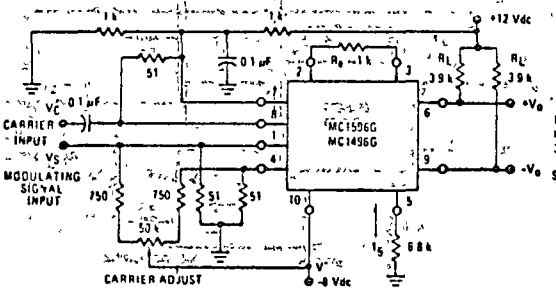


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)

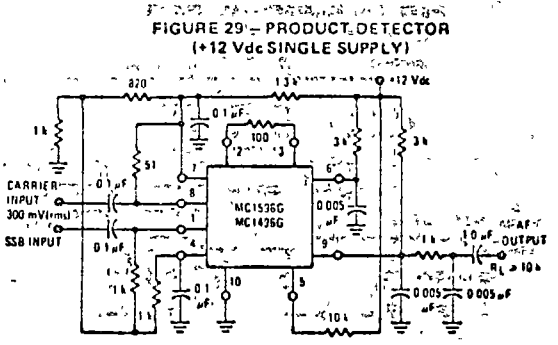
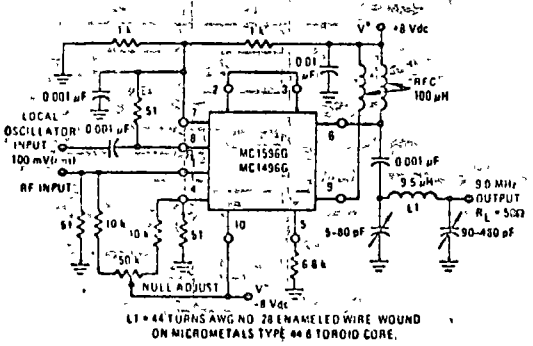
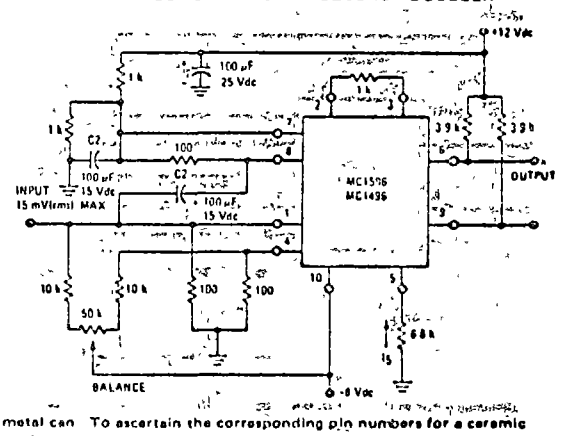


FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

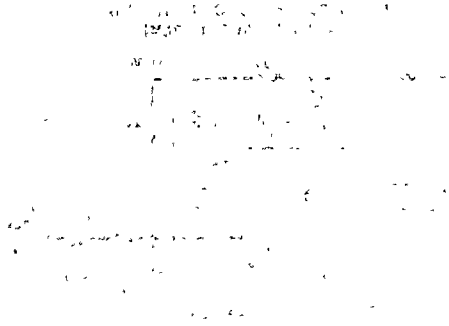


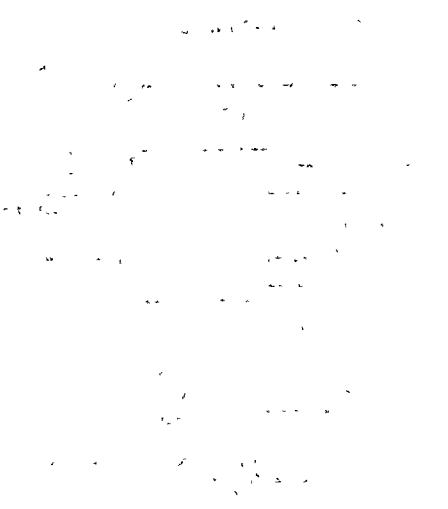
LT = 44 TURNS AWG NO. 28 ENAMELED WIRE WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

FIGURE 31 – LOW FREQUENCY DOUBLER



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for a ceramic packaged device refer to the PIN CONNECTION CHART on the first page of this specification.





MC1595L
MC1495L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

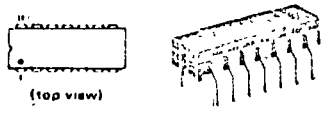
designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X Input, 2% max Error on Y Input – MC1595L
- Excellent Linearity – 2% max Error on X Input, 4% max Error on Y Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

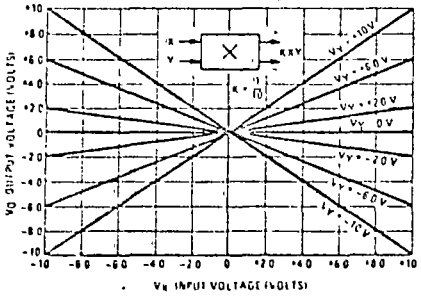


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

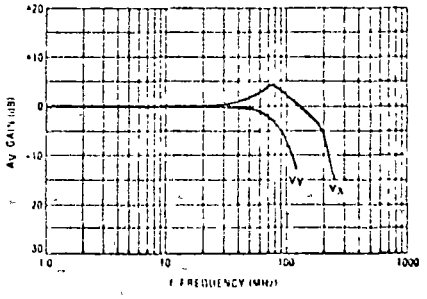
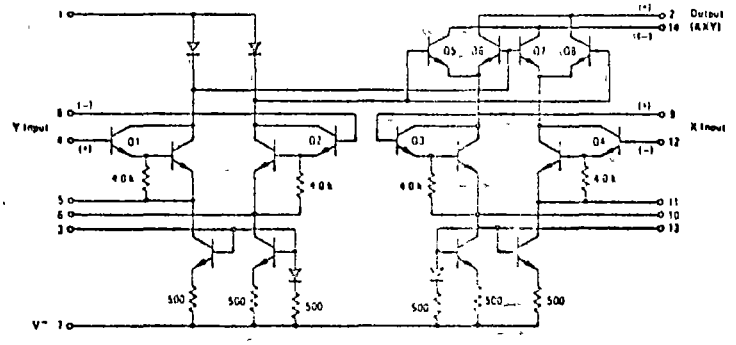


FIGURE 3 – CIRCUIT SCHEMATIC



See Packaging Information Section for outline dimensions

See current MCC1595/1495 data sheet for standard linear chip information

ELECTRICAL CHARACTERISTICS (V^+ = +32V, V^- = -15 V, T_A = +25°C, I_2 = I_{10} = 1 mA, R_A = 10 kΩ, R_L = 11 kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity Output Error in Percent of Full Scale		5					%
T_A = +25°C							
-10 ≤ V_X ≤ +10 (V_Y = ±10 V)	MC1495		E_{RX}	–	±1.0	±2.0	
	MC1595			–	±0.5	±1.0	
-10 ≤ V_Y ≤ +10 (V_X = ±10 V)	MC1495		E_{RY}	–	±2.0	±4.0	
	MC1595			–	±1.0	±2.0	
T_A = 0 to +70°C	MC1495						
-10 ≤ V_X ≤ +10 (V_Y = ±10 V)			E_{RX}		±1.5		
-10 ≤ V_Y ≤ +10 (V_X = ±10 V)			E_{RY}	–	±3.0	–	
T_A = -55°C to +125°C	MC1595						
-10 ≤ V_X ≤ +10 (V_Y = ±10 V)			E_{RX}	–	±0.75		
-10 ≤ V_Y ≤ +10 (V_X = ±10 V)			E_{RY}		±1.50	–	
Scaling Mode Error Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
T_A = +25°C	MC1495				±0.25		
	MC1595			–	±0.5	–	
T_A = 0 to +70°C	MC1495				±1.0		
T_A = -55°C to +125°C	MC1595				±0.75		
Scale Factor (Adjustable) $\left(K = \frac{20_L}{I_3 R_X R_Y}\right)$		–	K		0.1		
Input Resistance (f = 20 Hz)	MC1495	7	R_{INX}		20		Megohms
	MC1595				35	–	
	MC1495		R_{INY}		20		
	MC1595				35		
Differential Output Resistance (f = 20 Hz)		8	R_O	–	300		k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$ $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}		2.0	4.2	μA
	MC1595			–	2.0	4.0	
	MC1495		I_{by}	–	2.0	4.2	
	MC1595			–	2.0	4.0	
Input Offset Current $\lvert I_9 - I_{12}\rvert$	MC1495	6	$\lvert I_{iox}\rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8\rvert$	MC1495		$\lvert I_{ioy}\rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Io}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	2.0	–	
(T_A = -55°C to +125°C)	MC1595			–	7.0		
Output Offset Current $\lvert I_{11} + I_7\rvert$	MC1495	6	I_{oo}	–	20	100	μA
	MC1595				10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Io}\rvert$				nA/°C
(T_A = 0 to +70°C)	MC1495			–	20	–	
(T_A = -55°C to +125°C)	MC1595			–	20	–	
Frequency Response 3.0 dB Bandwidth R_L = 11 kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)			T_{BW3dB}	–	20	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ		750		kHz
3° Absolute Error Due to Input Output Phase Shift			f_ϕ	–	20	–	kHz
Common Mode Input Swing (Either Input)	MC1495	11	CMV	±10.5	±12	–	Vdc
	MC1595			±11.5	±13	–	
Common Mode Gain (Either Input)	MC1495	11	A_{CM}	-40	-50	–	dB
	MC1595			-50	-60		
Common Mode Quiescent Output Voltage		12	V_{o1}	–	22		Vdc
			V_{o2}	–	21		
Differential Output Voltage Swing Capability		9	V_O	–	±10		V_{p-p}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–		–	
Power Supply Current		12	I_7	–	8.0	12	mA
DC Power Dissipation		12	P_D	–	135	170	mW

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2-V_1, $V_{14}-V_1$, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, $V_{12}-V_7$, V_9-V_7, V_8-V_7, V_4-V_7)	aV	30	Vdc
Differential Input Signal	$V_{12}-V_9$ V_4-V_8	$\pm(6+I_{13}R_X)$ $\pm(6+I_3R_Y)$	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)

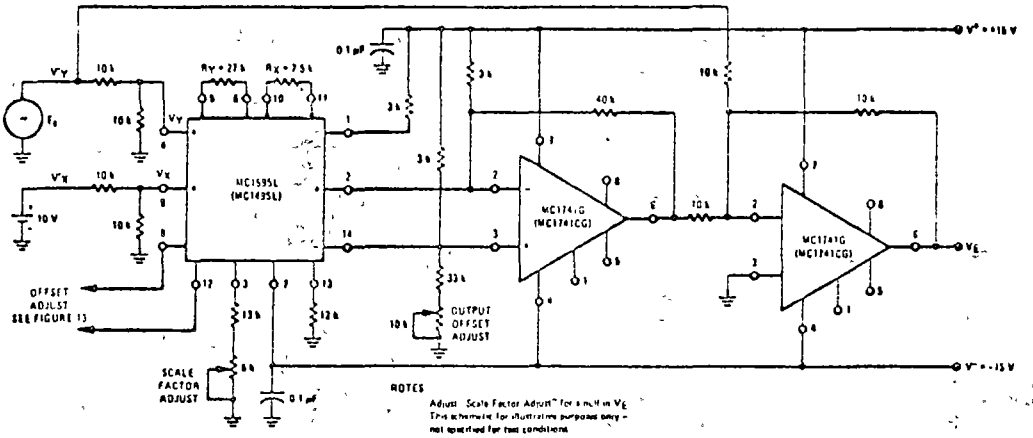
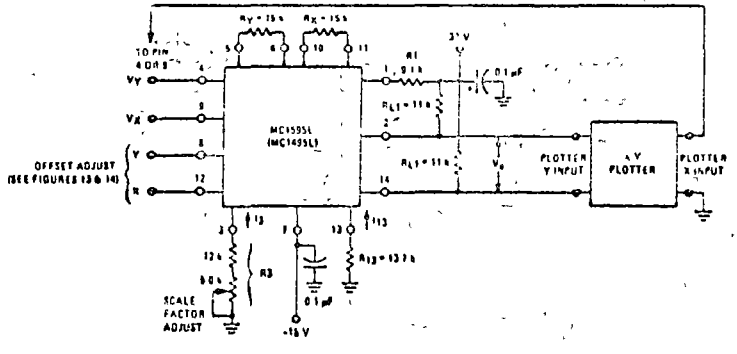


FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

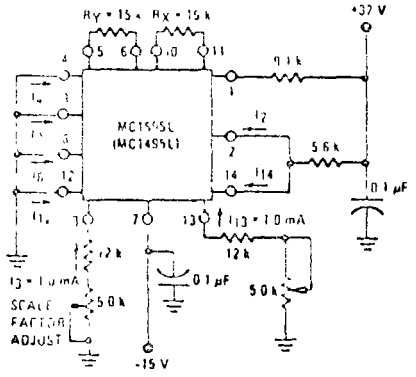


FIGURE 7 – INPUT RESISTANCE

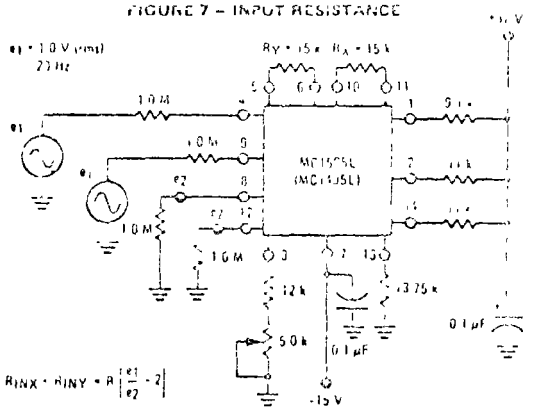


FIGURE 8 – OUTPUT RESISTANCE

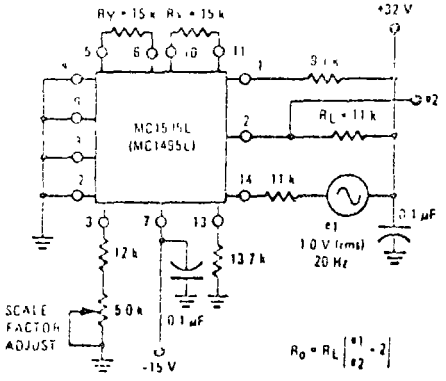


FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

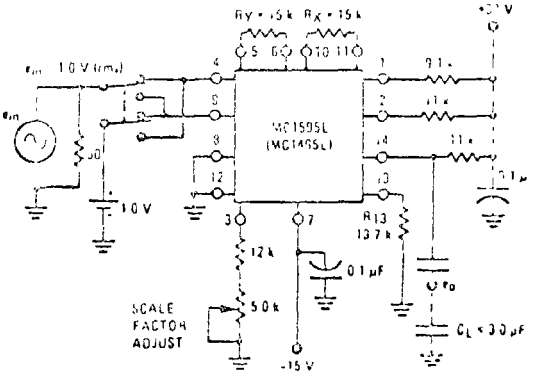


FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

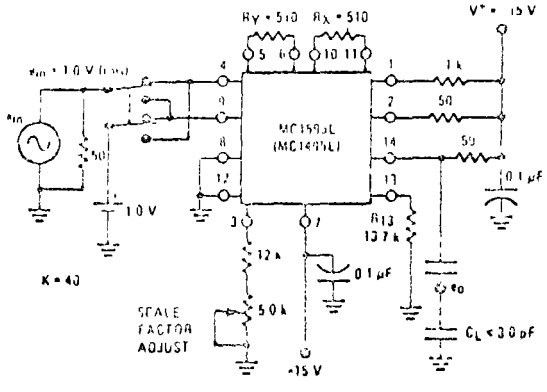
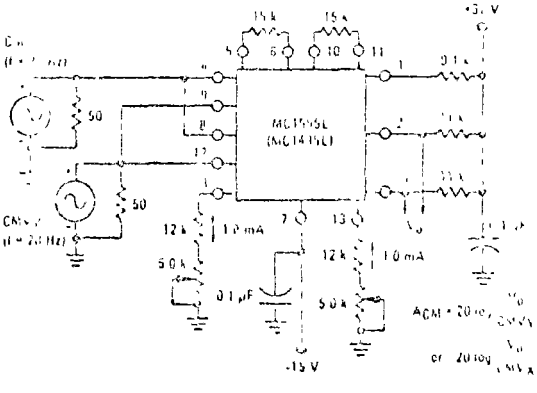


FIGURE 11 – COMMON MODE GAIN and COMMON MODE INPUT SWING



TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

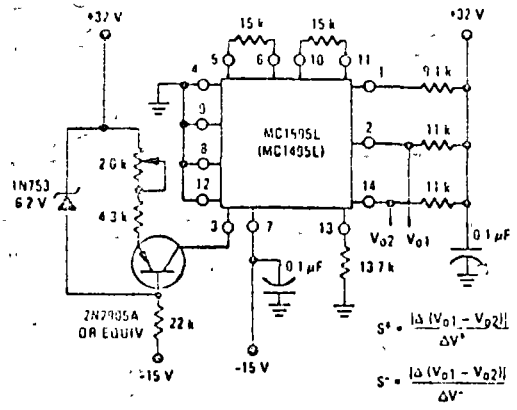
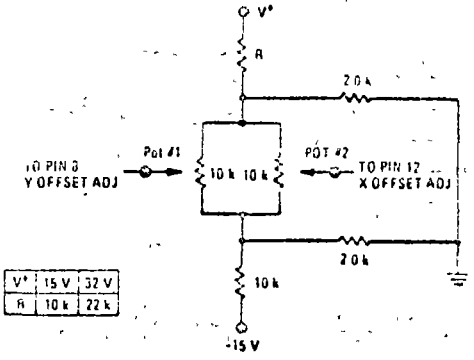
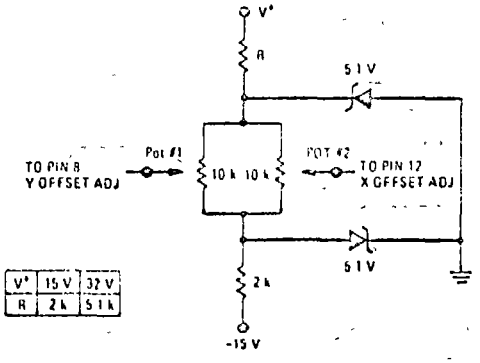


FIGURE 13 – OFFSET ADJUST CIRCUIT



V+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V+	15 V	32 V
R	2 k	5.1 k

TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

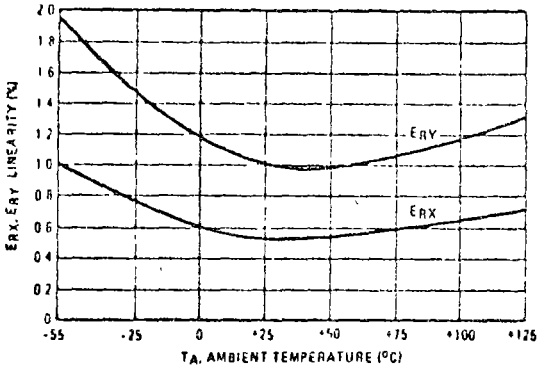


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

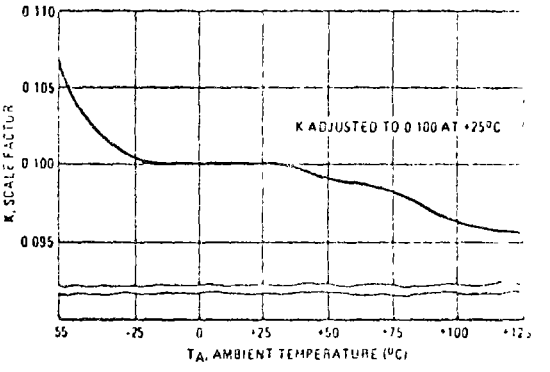


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

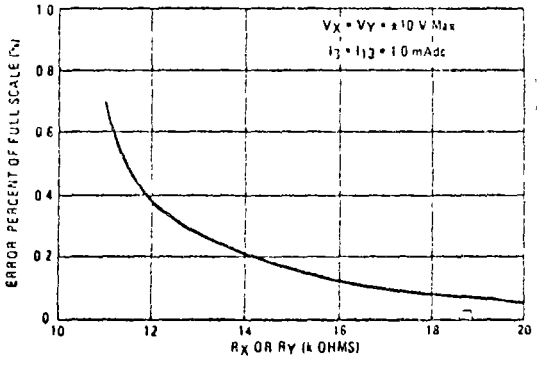


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

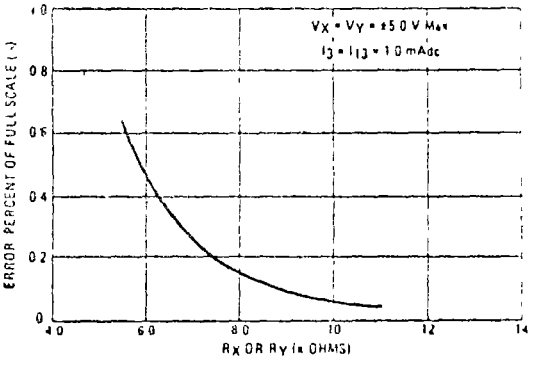
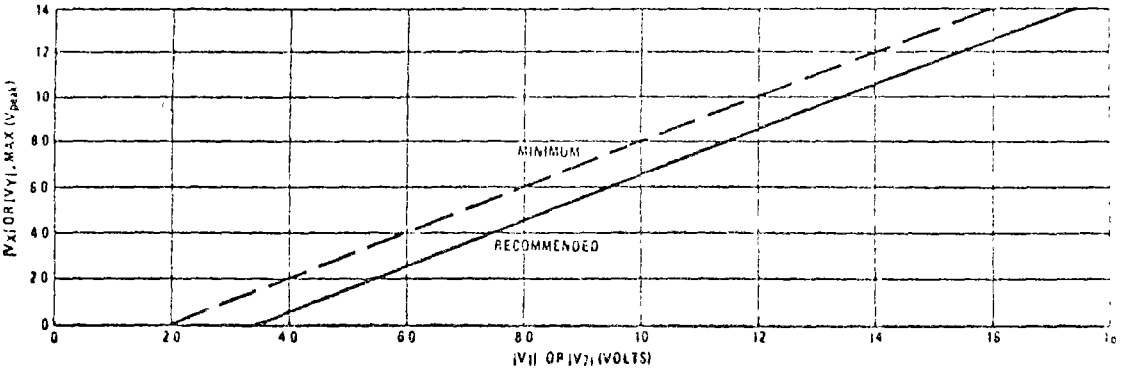


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

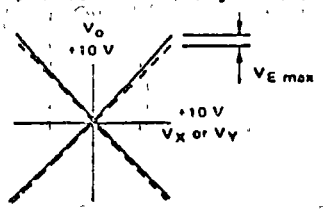
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below):



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega,$$

The equation $I_A - I_B = \frac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \frac{2V_X V_Y}{\left(R_X + \frac{2kT}{qI_{13}}\right)\left(R_Y + \frac{2kT}{qI_3}\right) I_3}$

with the assumption $R_X \gg \frac{2kT}{qI_{13}}$ and $R_Y \gg \frac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10\ k\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

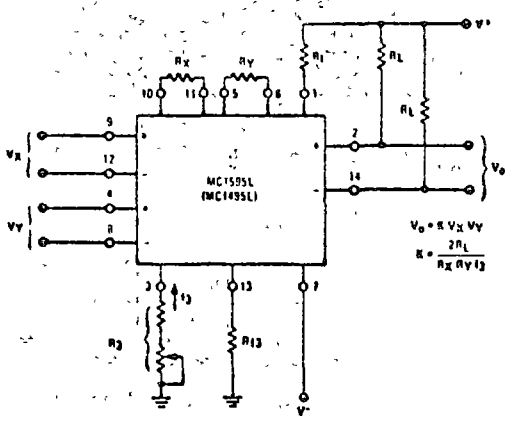
The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3 General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y(max)}$) for a ±10-volt input ($V_X = V_{Y(max)}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X \cdot V_Y}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10\, V_X V_Y .$$

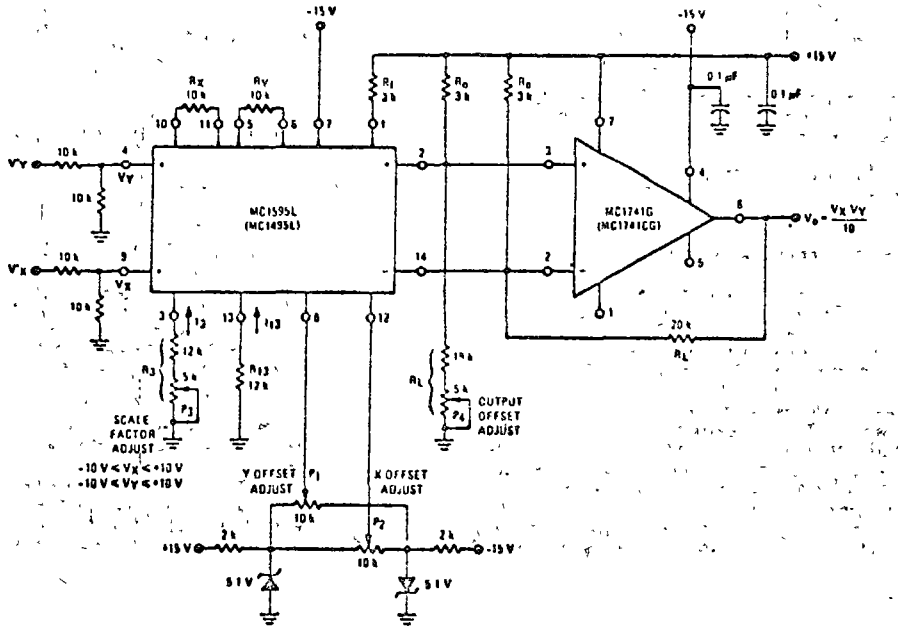
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1\ mA$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMP. LEVEL SHIFT



OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15$ V

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13}R_X \geq 1.5\ V_{X(max)}$.

The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3R_Y = 10$ V

$I_{13}R_X = 10$ V

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined.

$$K = \frac{2R_L'}{R_XR_YI_3} = \frac{4}{10}$$

or $$\frac{(2)\ (R_L')}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' - V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode drops below the voltage at pin 1. Thus, the voltage at pin 1 should be at least two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1, from pin 1 to the positive supply.

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15$ V

Then $R_1 = \frac{15\ V - 9\ V}{(2)(1\ mA)}$

$R_1 = 3\ k\Omega$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

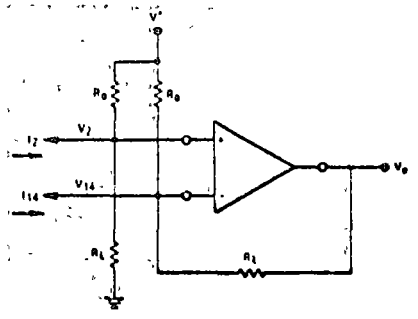
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by

$$V_o = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_XI_Y}{I_3} = \frac{2V_XV_Y}{I_3R_XR_Y}$

Then $V_o = \frac{2R_LV_XV_Y}{4R_XR_XI_3}$ where V_X, V_Y is the voltage at the input to the voltage dividers.

FIGURE 22 – LEVEL SHIFT CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4 V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current).

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1\ mA = \frac{15\ V - 11\ V}{R_o}$

Solving for R_o, $R_o = 2.6\ k\Omega$

Thus, select $R_o = 3.0\ k\Omega$

For $R_o = 3.0\ k\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\ \text{volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity and R_X decreased somewhat so as not to materially affect the X linearity. This avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

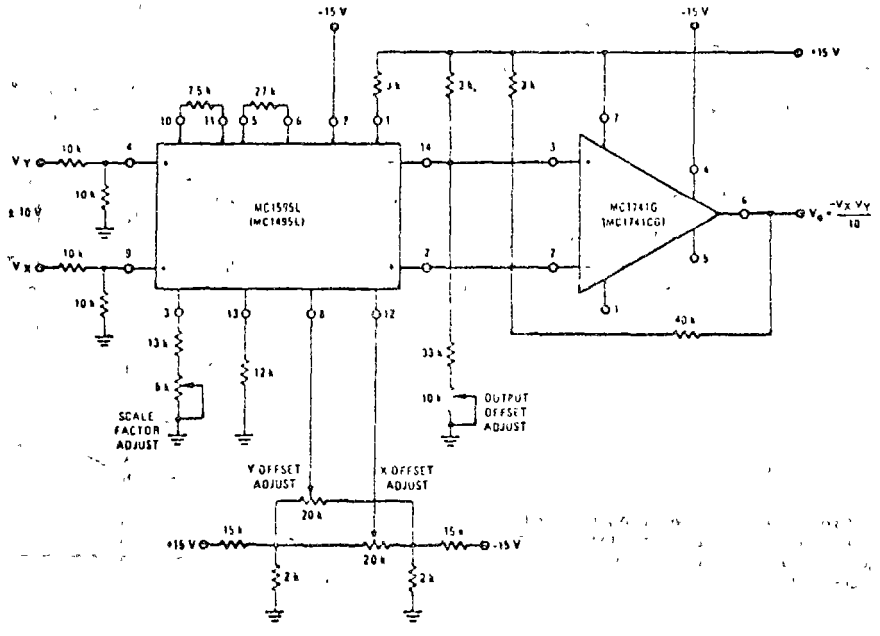
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X input offset voltage, Y input offset voltage, and output offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function.

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \quad (1)$$

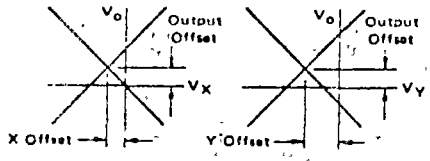
Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31)

If well regulated supply voltages are available the offset adjust circuit of Figure 13 is recommended. Otherwise the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K is set by P_3 (Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi turn, infinite resolution potentiometers with low temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

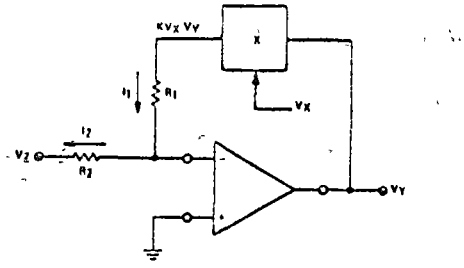
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together the resultant function is squaring, that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustments potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary
2. DC Procedure
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is + 10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \quad (2)$$

If $R1 = R2$

$$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If $R1 = KR2$

$$V_Y = \frac{-V_Z}{V_X}. \quad (4)$$

OPERATION AND APPLICATIONS INFORMATION (continued)

Hence the output voltage is the ratio of V_Z to V_X and provides a division function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{K V_X}, \quad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_X. For example, assume that R1 = R2 and K = 1/10. For these conditions the output of the divide circuit is given by

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \quad (6)$$

From equation 6 it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$PE_D = \frac{\frac{\Delta E}{K V_X}}{\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \quad (7)$$

From equation 7 the percentage error is inversely related to voltage V_Z (i.e. for increasing values of V_Z the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25:

1. The input voltage (V_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifier's input terminals. In this instance Figure 25 differs from the circuit connection shown in Figure 21, necessitated to insure negative feedback around the loop.

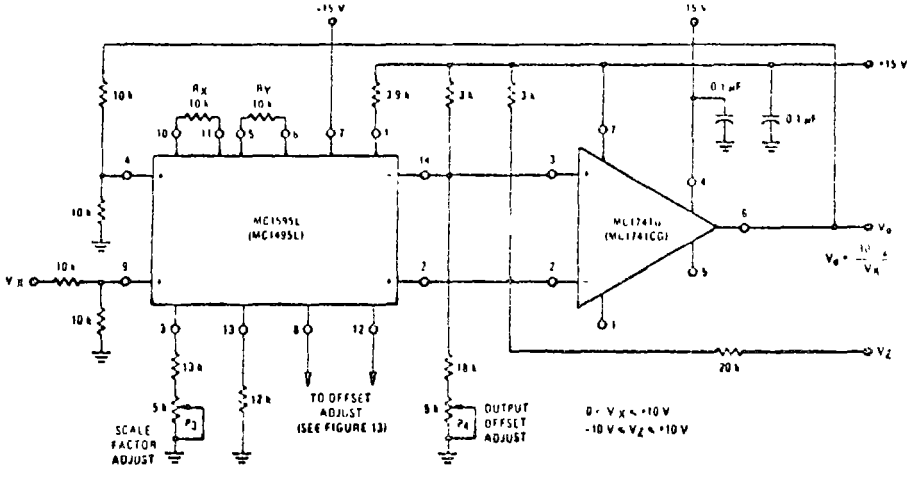
A Suggested Adjustment Procedure for the Divide Circuit:

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P_4) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P_1) until V_O = 0 volts.
3. Let $V_X = V_Z$ and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily −10 volts) constant value as $V_Z = V_X$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_O is −10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

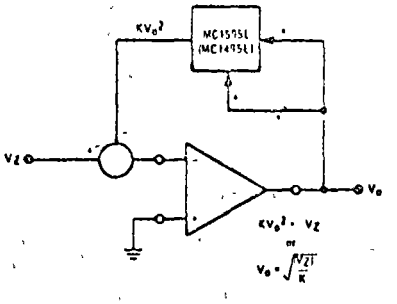
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function.

FIGURE 25 – DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch up.

This circuit also may be adjusted in the closed loop mode as follows:

1. Set V_Z to -0.01 volts and adjust P_4 (output offset) for V_O = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to -0.9 volts and adjust P_2 (X adjust) for V_O = +3.0 volts.
3. Set V_Z to -10 volts and adjust P_3 (scale factor adjust) for V_O = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2}(1 + \cos 2\omega t).$$

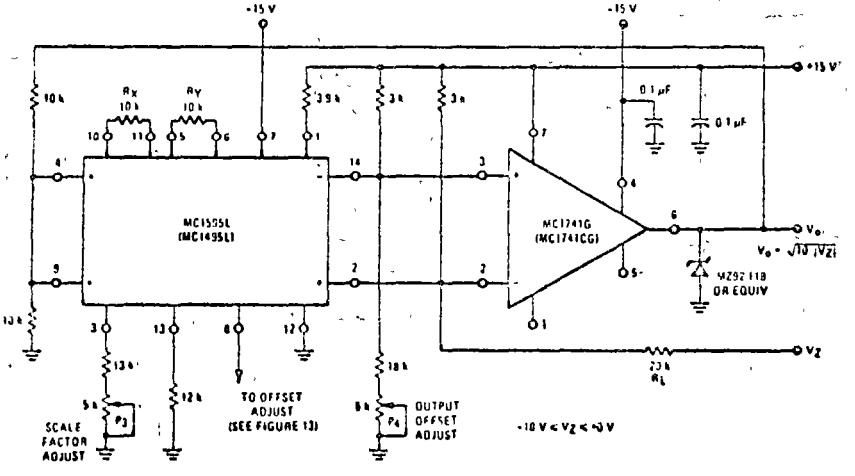
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ±15 volt supplies are used. An input dynamic range of 5.0 volts peak to peak is allowed. The circuit generates wave forms that are double frequency, less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

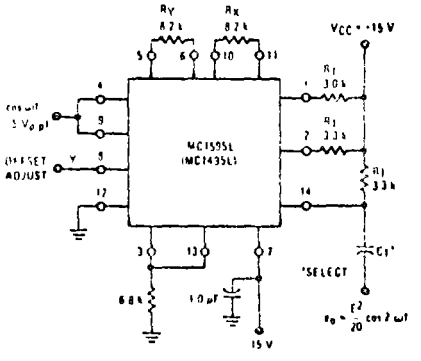
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT



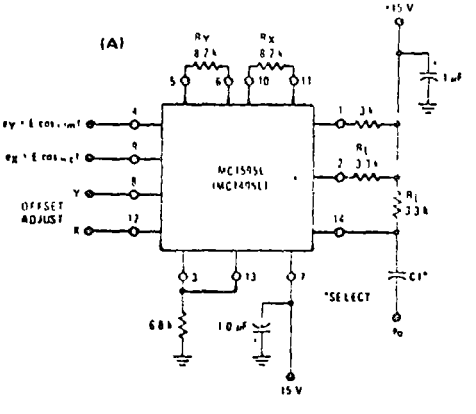
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 – FREQUENCY DOUBLER

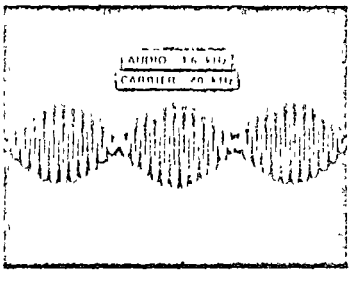


When two equal sine waves are applied to X and Y the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal; output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier, a higher operating frequency results.

A problem common to communications is to extract the intelligence from single sideband receiver signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, $\cos \omega_c t$,

$$e_{ssb} e_{carrier} = \frac{AK}{2}[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t]$$

if the frequency of the band limited carrier signal, ω_c, is accurately known in advance the designer can insert a low pass filter and pull out the $(AK/2)(\cos \omega_c t)$ term with ease. He also can use an operational amplifier for a combination level shift, active filter as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation similar to balanced modulation when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here the identity is

$$E_m(1 + m \cos \omega_m t) E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

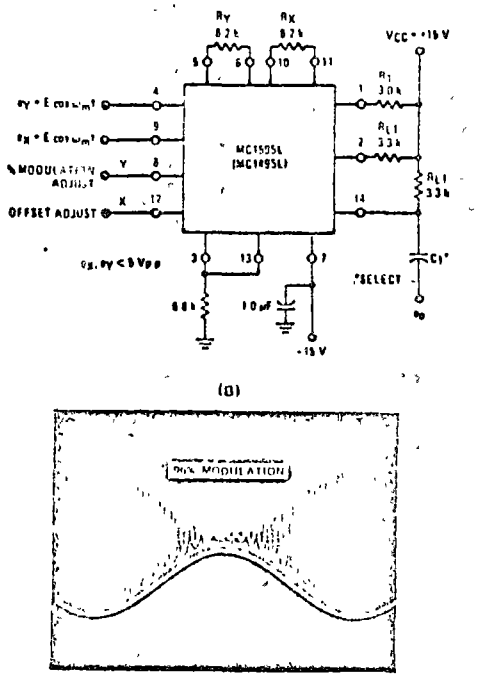
where m indicates the degree of modulation. Since m is adjustable via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 95% modulation may be obtained where ω_c and ω_m are the same as in the balanced modulator example.

6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the features of this application. Suppose a 200 kHz sine wave, 1.0 volt peak to peak, is the signal to which a gain control will be applied. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200 kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



The signal is applied to the unit's Y input. Since the total input range is limited to ± 0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing R_L = 100 assures wide bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

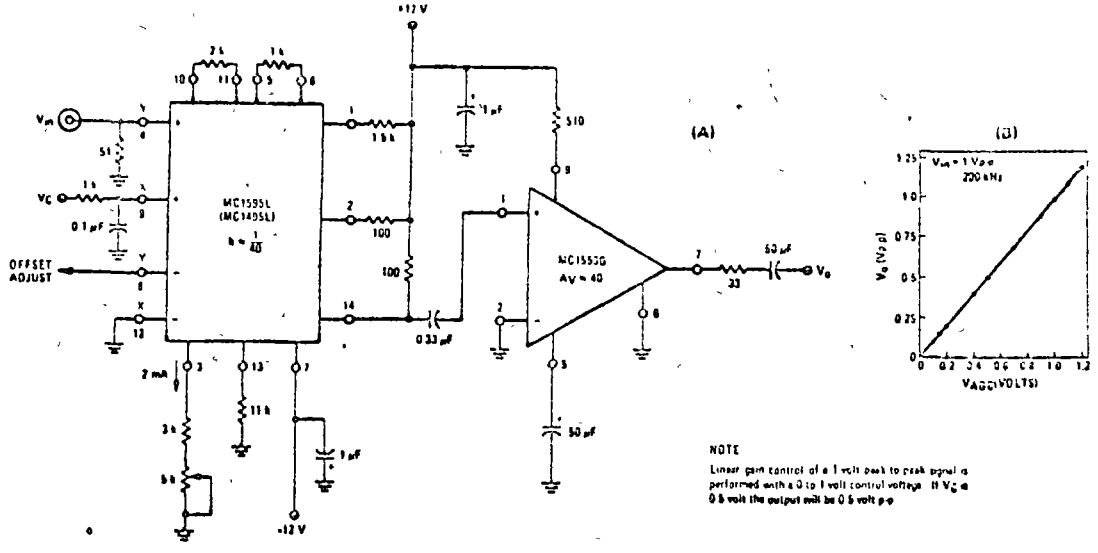
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale factor expression because the output is single-ended and ac coupled.

To recover the gain an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use, and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL



NOTE

Linear gain control of a 1 volt peak to peak signal is performed with a 0 to 1 volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

OPERATIONS AND APPLICATIONS
INFORMATION INDEX

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PRACTICA I

FILTROS ACTIVOS

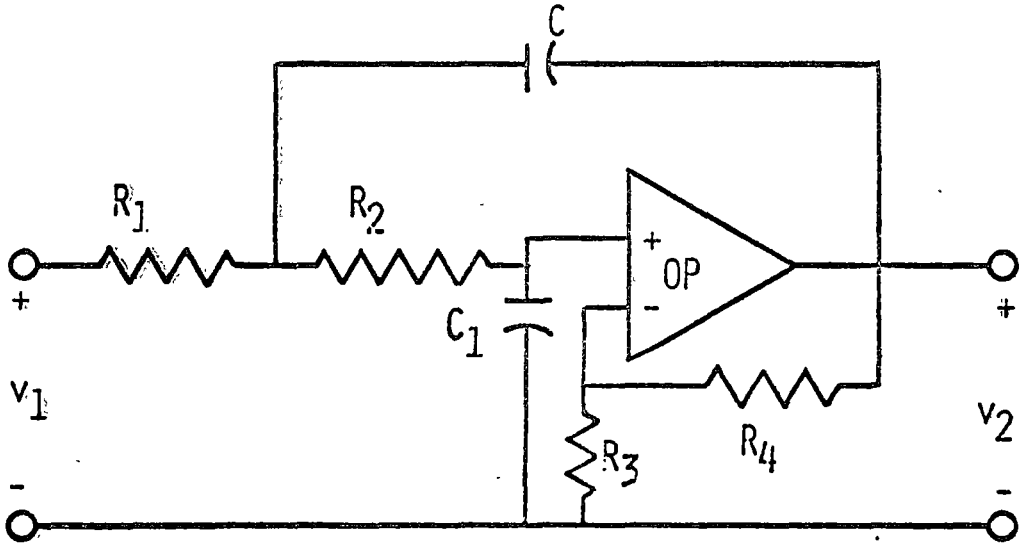
OBJETIVO.- Familiarizar al alumno con el diseño gráfico de filtros activos.

1.a.- Diseño gráfico de un filtro paso bajos de segundo orden

Función de transferencia:

$$\frac{V_2(s)}{V_1(s)} = \frac{K}{s^2 + as + b} \qquad \text{Ganancia} = \frac{k}{b}$$

El circuito empleado para la realización del filtro mencionado anteriormente, se muestra en la figura 1.



CIRCUITO PROTOTIPO DE UN FILTRO PASO BAJOS DE SEGUNDO ORDEN

FIG. 1

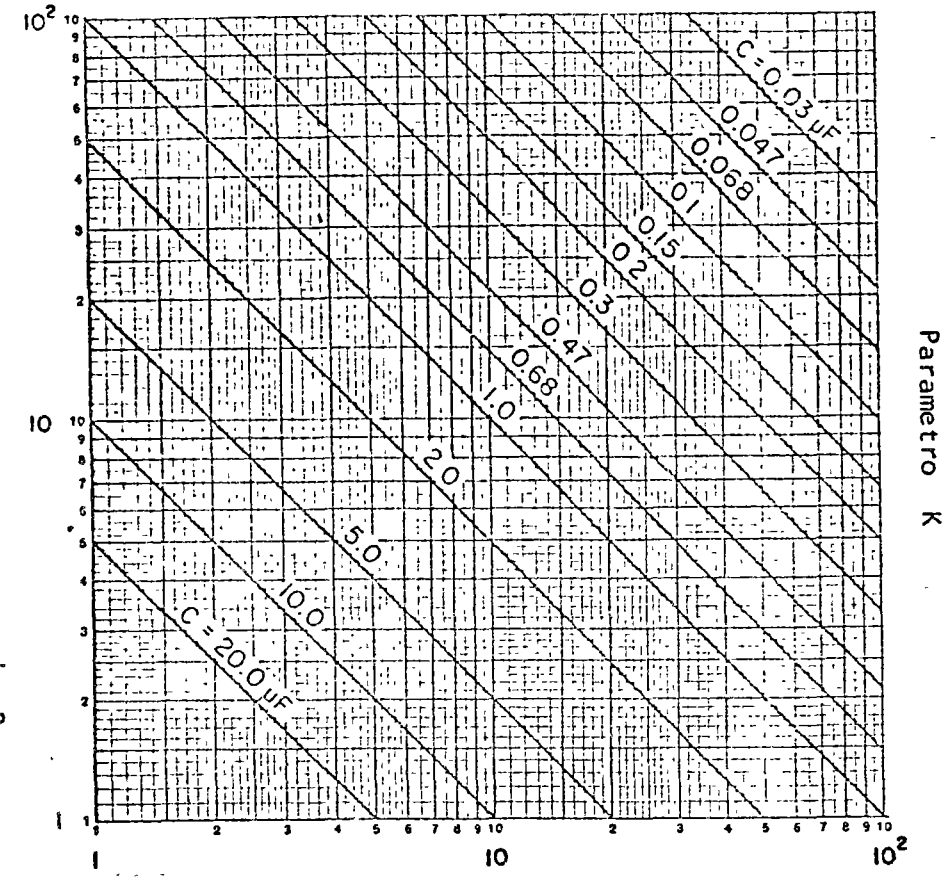
Pasos a seguir para el diseño:

a) Seleccione un valor para la capacitancia C y determine el valor del parametro K a partir de la figura 2a, 2b ó 2c según el valor de la frecuencia de corte "fc" deseada.

b) Usando el valor de K obtenido anteriormente determine el valor de los restantes elementos del circuito usando la figura 3a, 3b, 3c, 3d ó 3e según sea el valor de la ganancia deseada para el filtro.

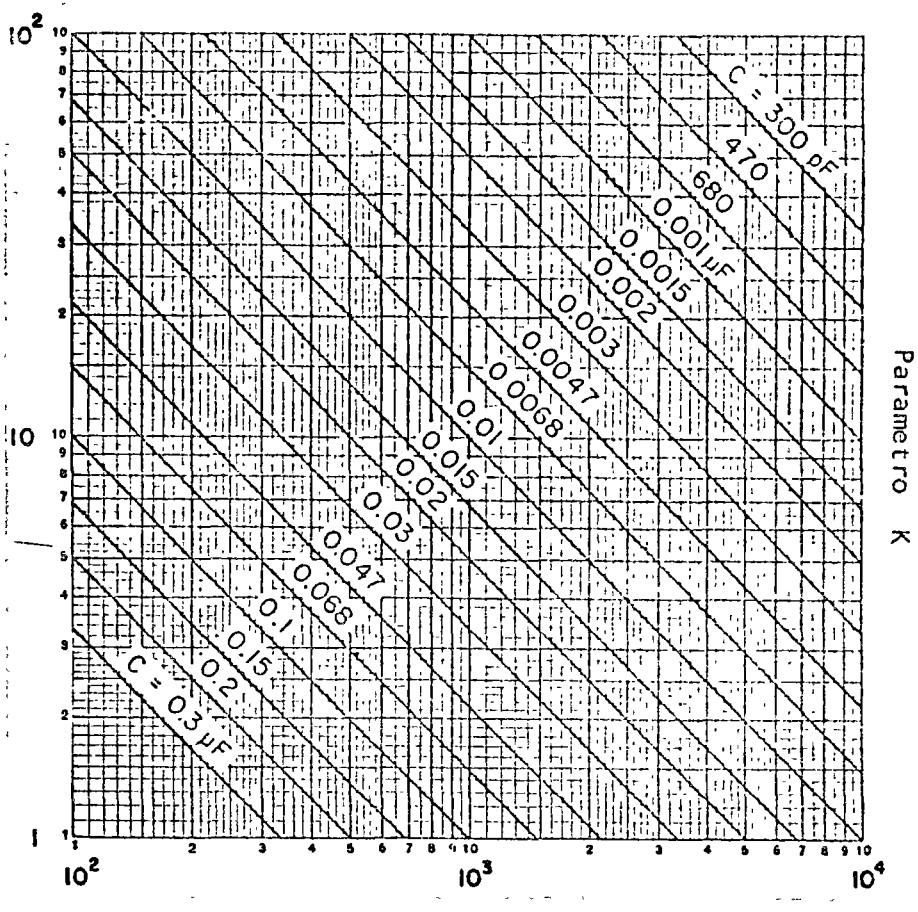
c) Construya el filtro y complete la tabla siguiente. Tome fc = 100 Hz.

f (Hz)	v_2 (Volts)	v_1 (Volts)	v_2/v_1
20			
40			
60			
80			
100			
200			
400			
600			
800			
1000			



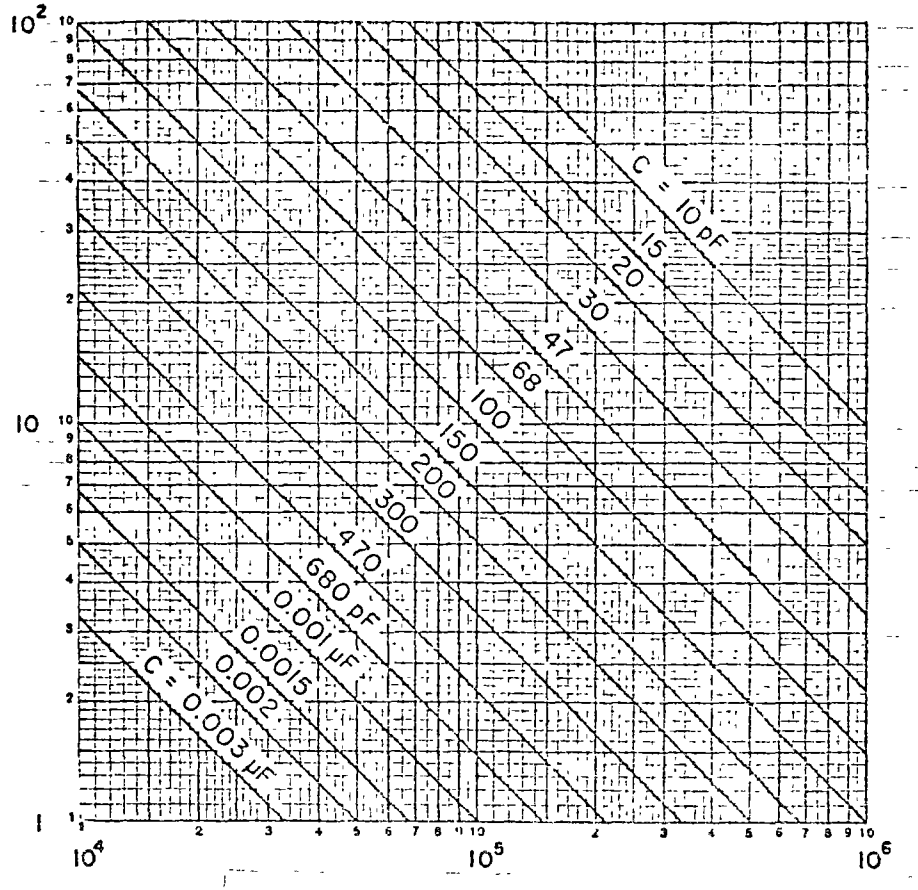
GRAFICA PARA DETERMINAR EL PARAMETRO K PARA fc
COMPRENDIDA ENTRE 1 y 10^2 Hz

Fig. 2a



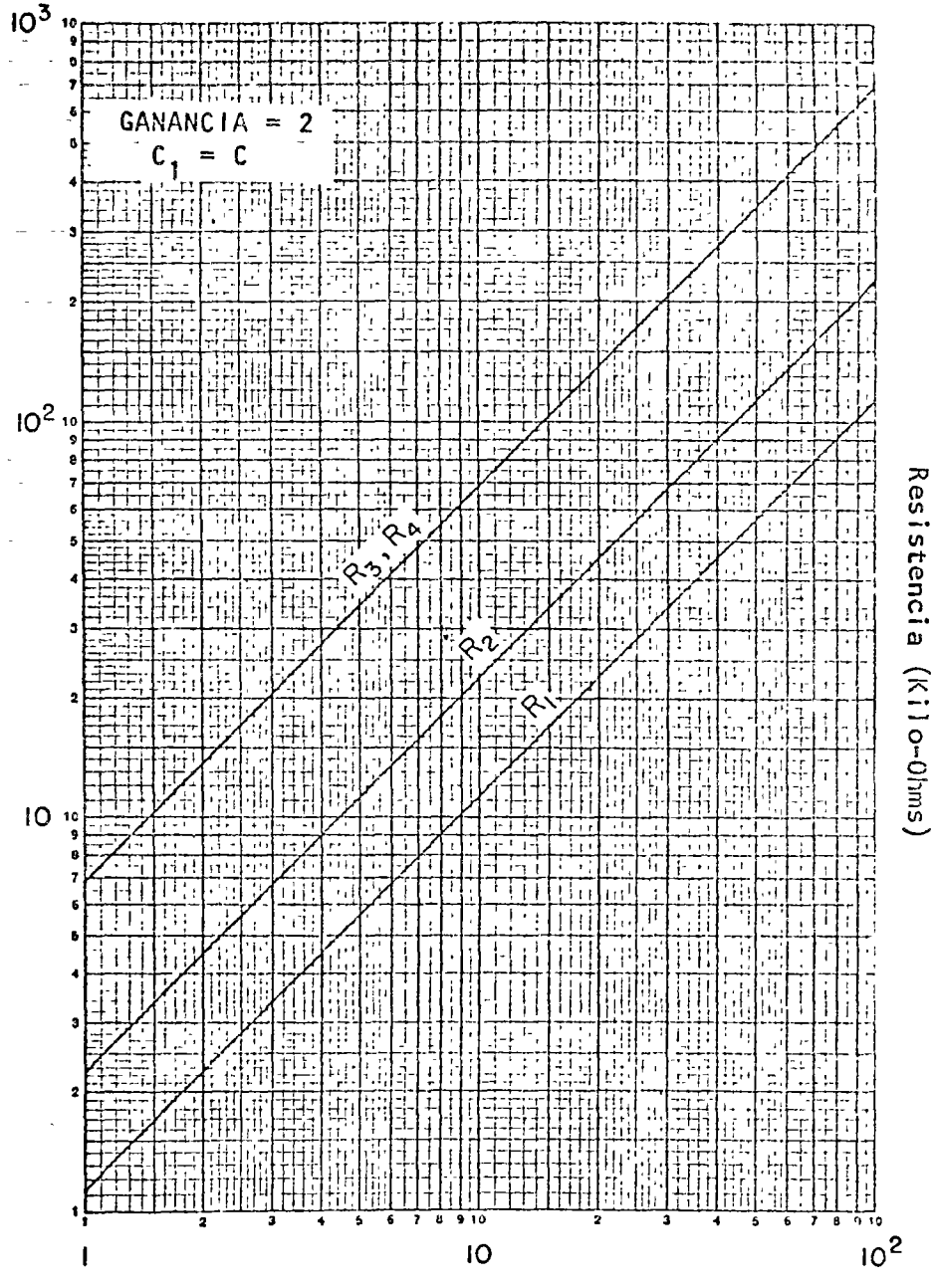
GRAFICA PARA DETERMINAR EL PARAMETRO K PARA fc
COMPRENDIDA ENTRE 10^2 y 10^4 Hz

Fig. 2b



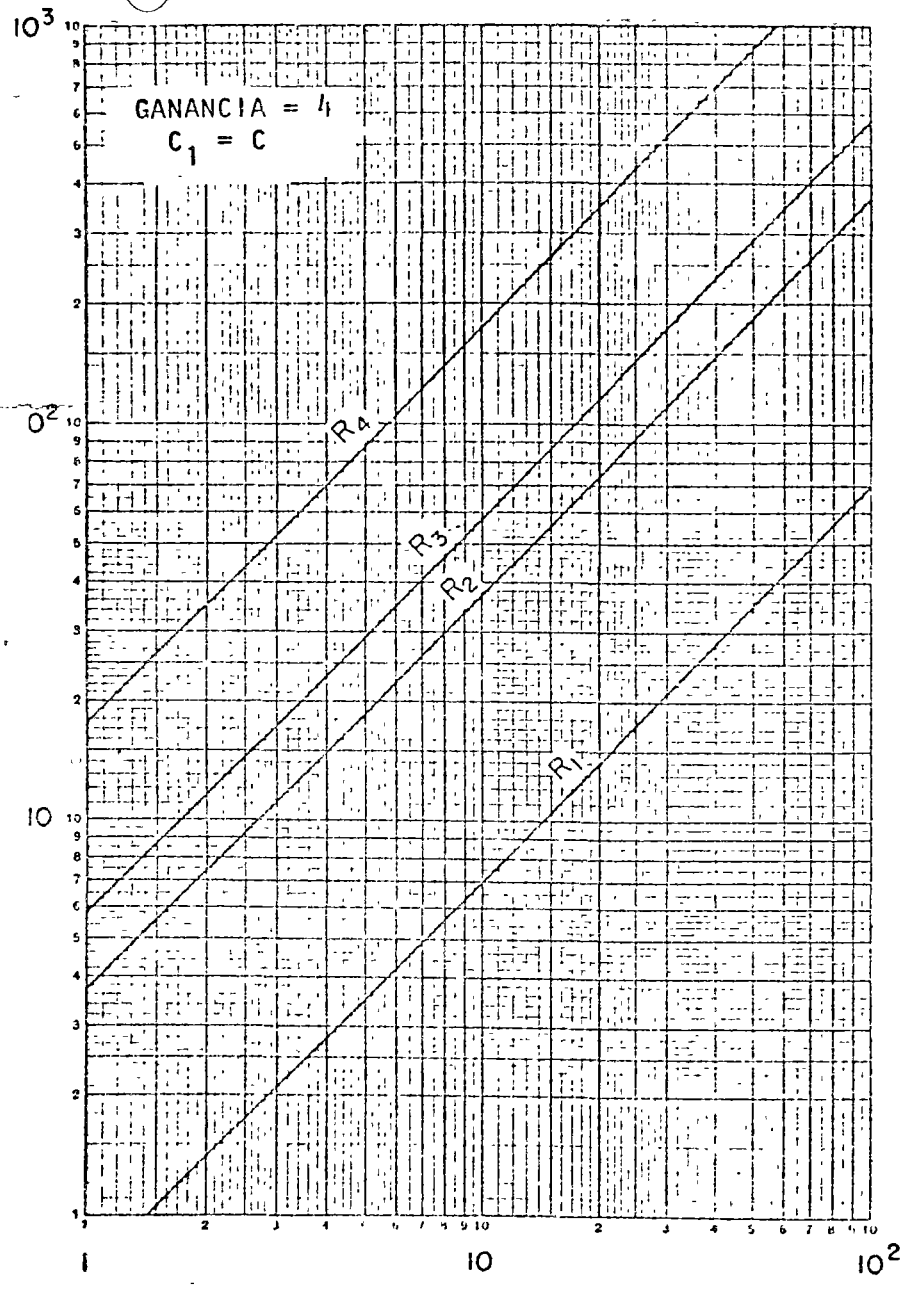
GRAFICA PARA DETERMINA EL PARAMETRO K PARA fc COMPRENDIDA ENTRE 10^4 y 10^6 Hz

Fig. 2c



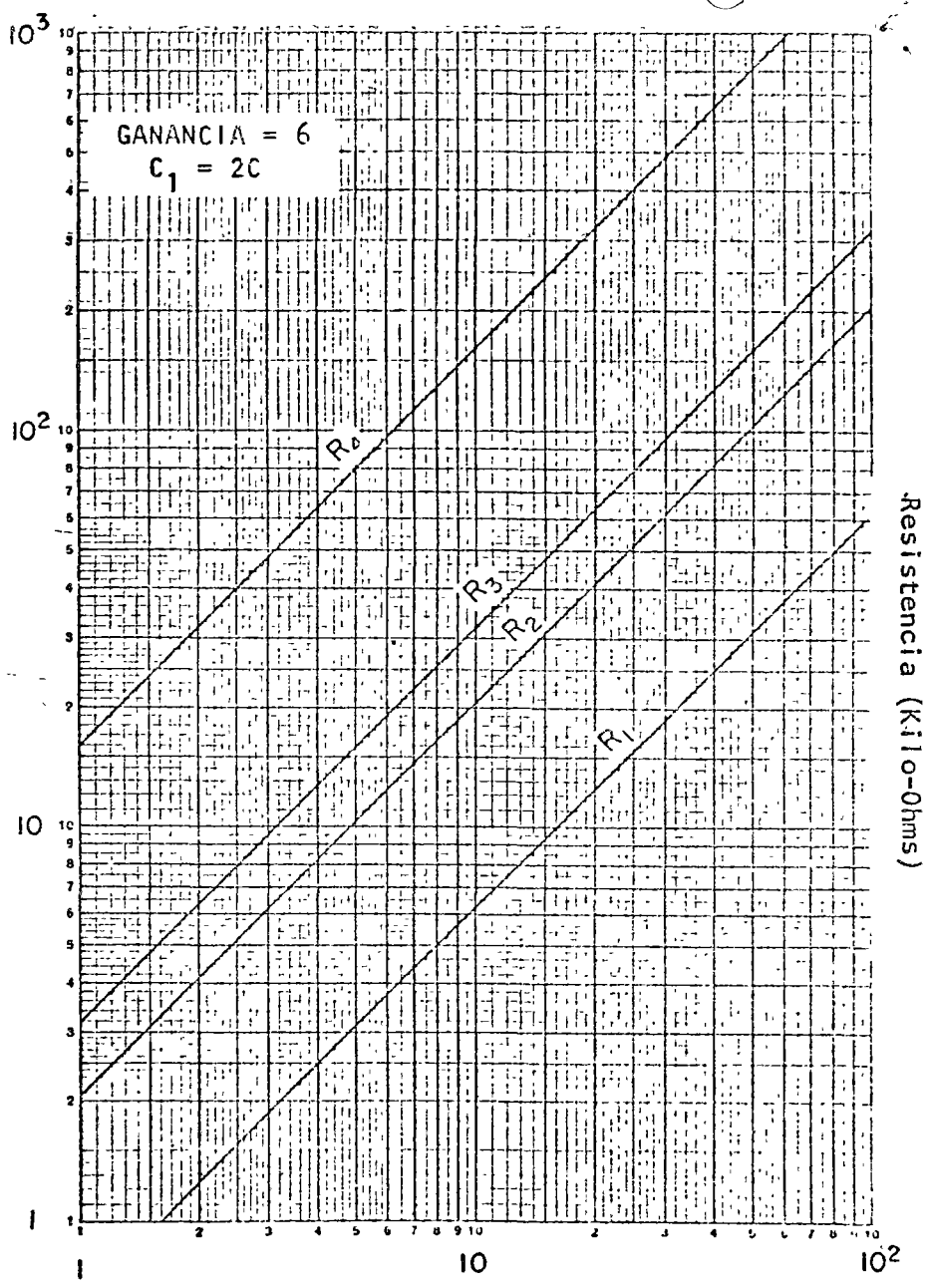
GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2, R_3 y R_4

Fig. 3a



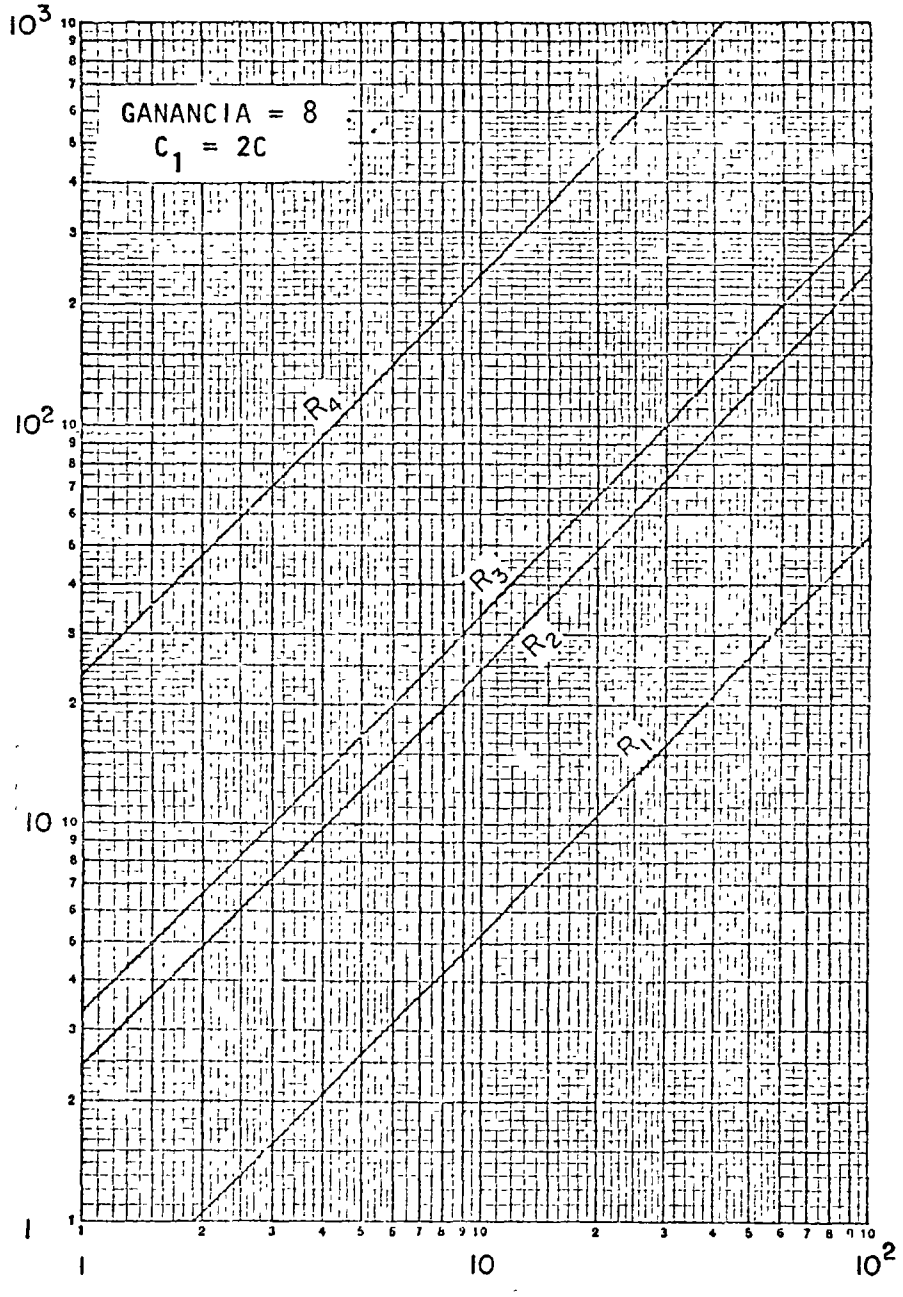
GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2, R_3 y R_4

Fig. 3b



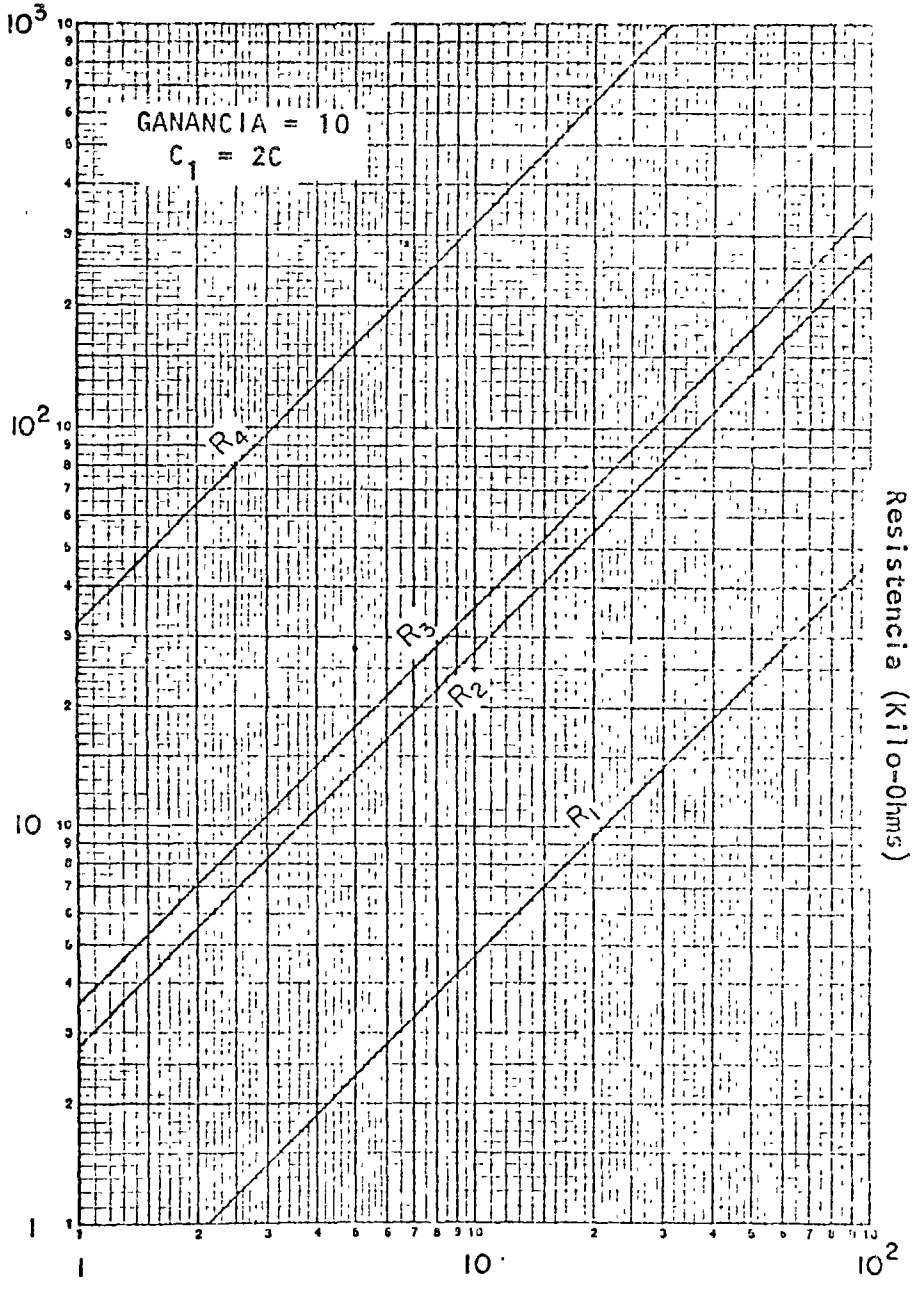
GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2, R_3 y R_4

Fig. 3c



GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2, R_3 y R_4

Fig. 3d



GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2, R_3 y R_4

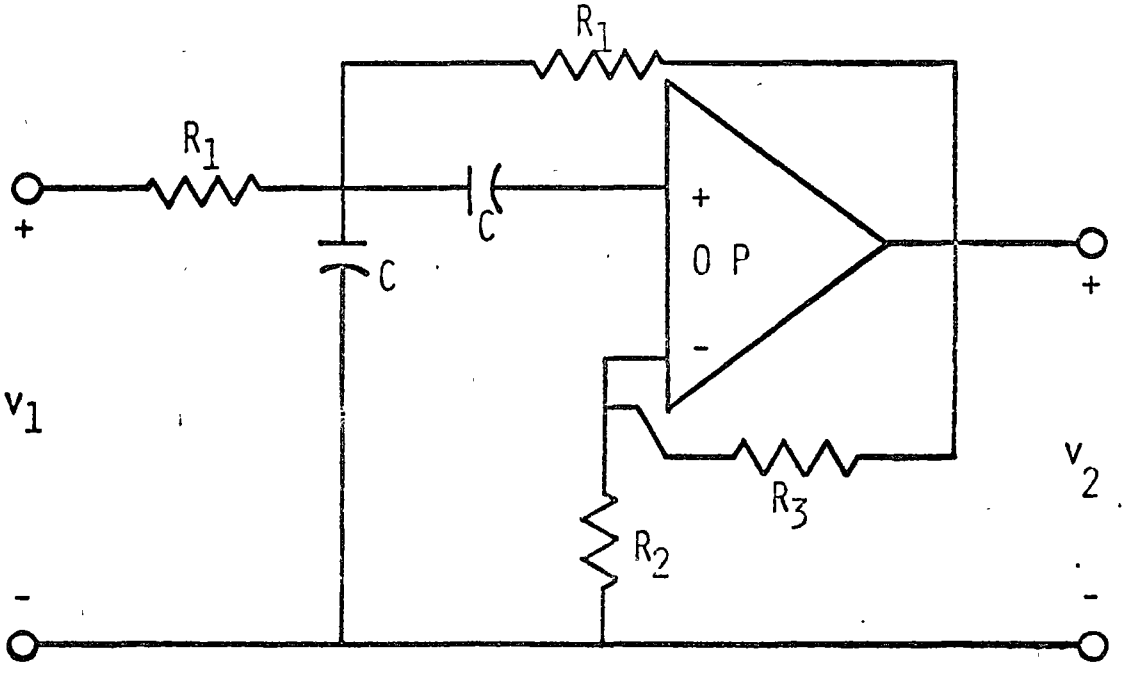
Fig. 3e

1.b.- Diseño gráfico de un filtro paso banda de segundo orden

Función de transferencia:

$$\frac{V_2(s)}{V_1(s)} = \frac{KS}{s^2 + BS + WO^2} \qquad \text{Ganancia} = \frac{k}{B}$$

El circuito empleado para la realización del filtro mencionado anteriormente se muestra en la figura 4.



CIRCUITO PROTOTIPO DE UN FILTRO PASO BANDA DE SEGUNDO ORDEN

FIG. 4

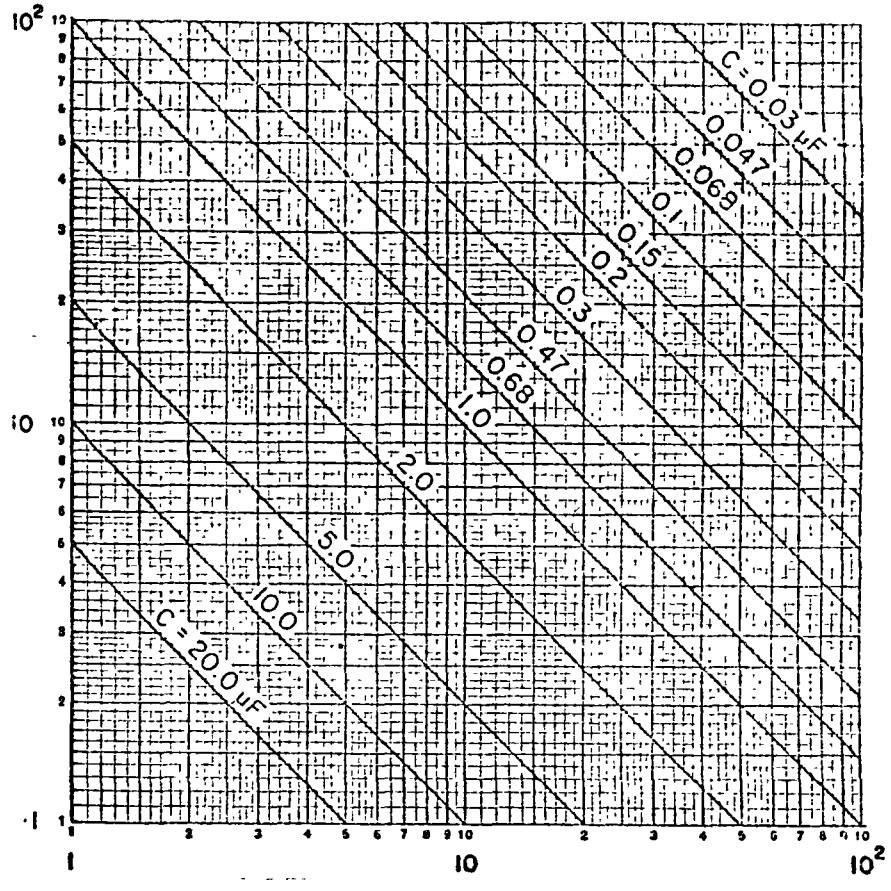
Pasos a seguir en el diseño:

a) Seleccione un valor para la capacitancia C y determine el valor del parametro K a partir de la figura 5a, 5b ó 5c según sea el valor de la frecuencia fo deseada.

b) Usando el valor de K obtenido anteriormente determine el valor de los restantes elementos del circuito usando la figura 6a, 6b ó 6c, según sea el valor de Q (ó ancho de banda) deseado.

c) Construya el filtro y complete la tabla siguiente. Tome AB = 0.32fo, G = 21.7 y fo = 80 Hz.

f (Hz)	v_2 (Volts)	v_1 (Volts)	v_2/v_1
20			
40			
60			
80			
100			
200			
400			
600			
800			
1000			

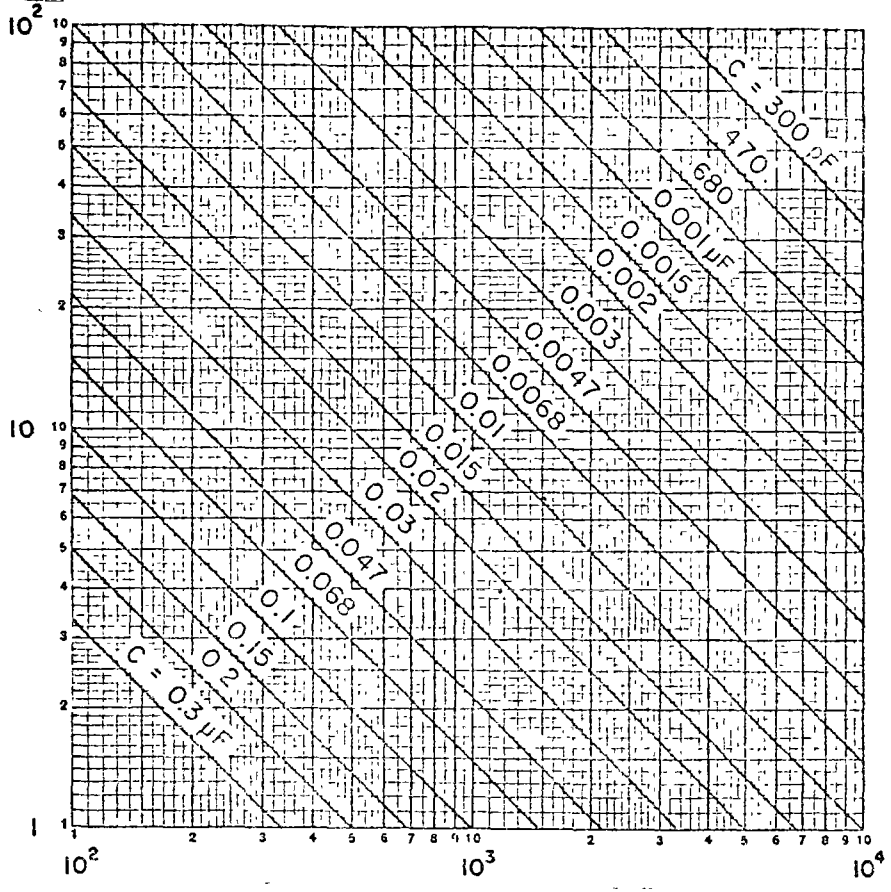


Parámetro K

Frecuencia Central fo

GRAFICA PARA DETERMINAR EL PARAMETRO K PARA fo COMPRENDIDA ENTRE 1 y 10^2 Hz

Fig. 5a

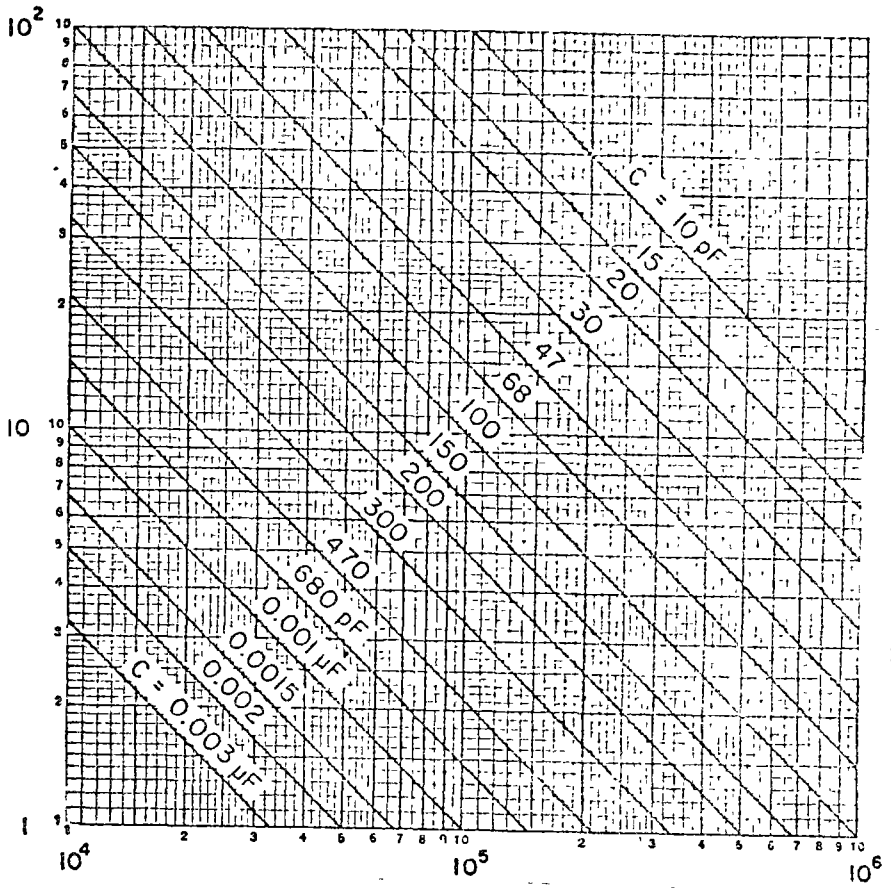


Parámetro K

Frecuencia Central fo

GRAFICA PARA DETERMINAR EL PARAMETRO K PARA fo
COMPRENDIDA ENTRE 10^2 y 10^4 Hz

Fig. 5b

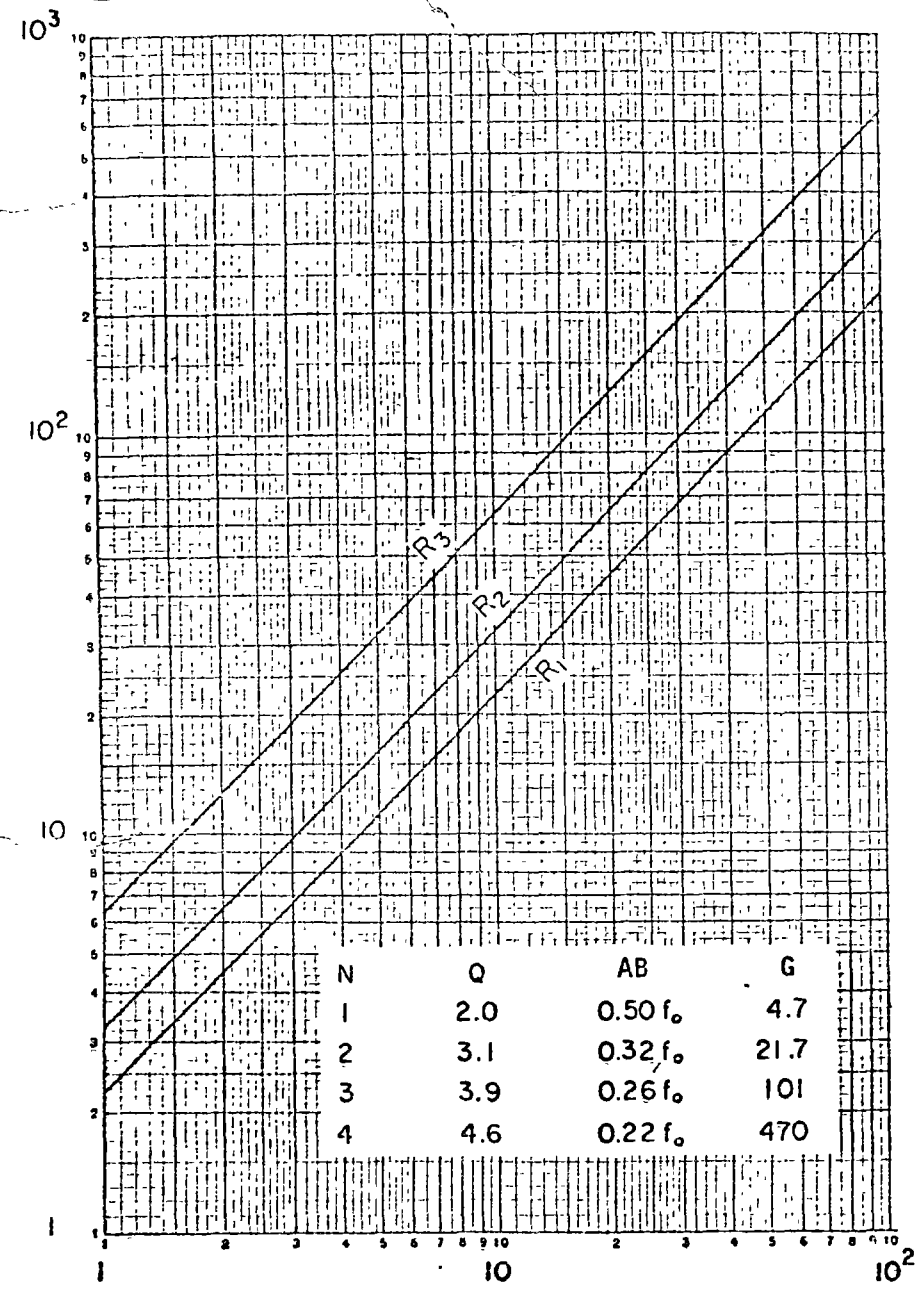


Parametro K

Frecuencia Central fo

GRAFICA PARA DETERMINAR EL PARAMETRO K PARA fo
COMPRENDIDA ENTRE 10^4 y 10^6 Hz

Fig. 5c



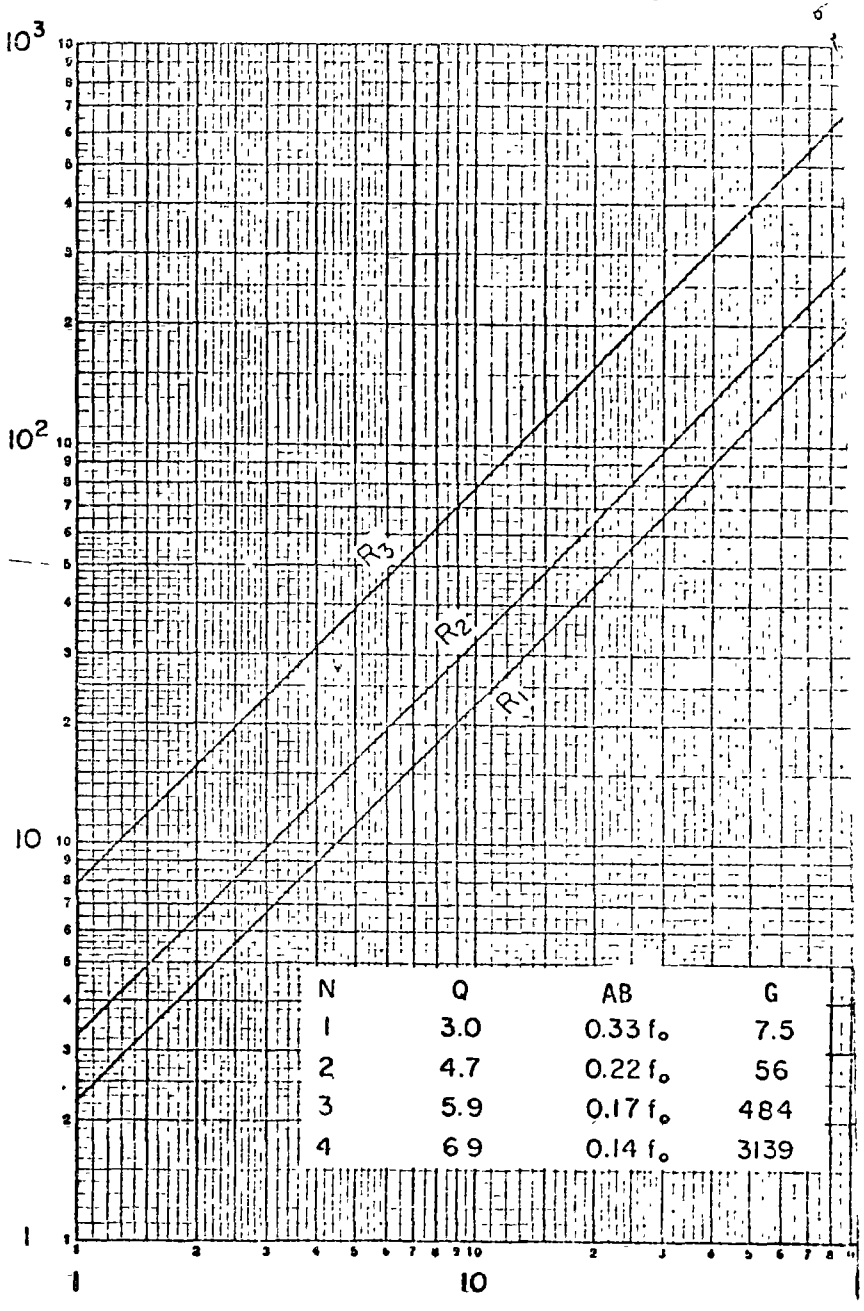
N	Q	AB	G
1	2.0	0.50 f_o	4.7
2	3.1	0.32 f_o	21.7
3	3.9	0.26 f_o	101
4	4.6	0.22 f_o	470

Parametro K

GRAFICA PARA DETERMINAP LOS VALORES DE LAS RESISTENCIAS R_1, R_2 y R_3

Fig. 6a

Resistencia (Kilo-Ohms)

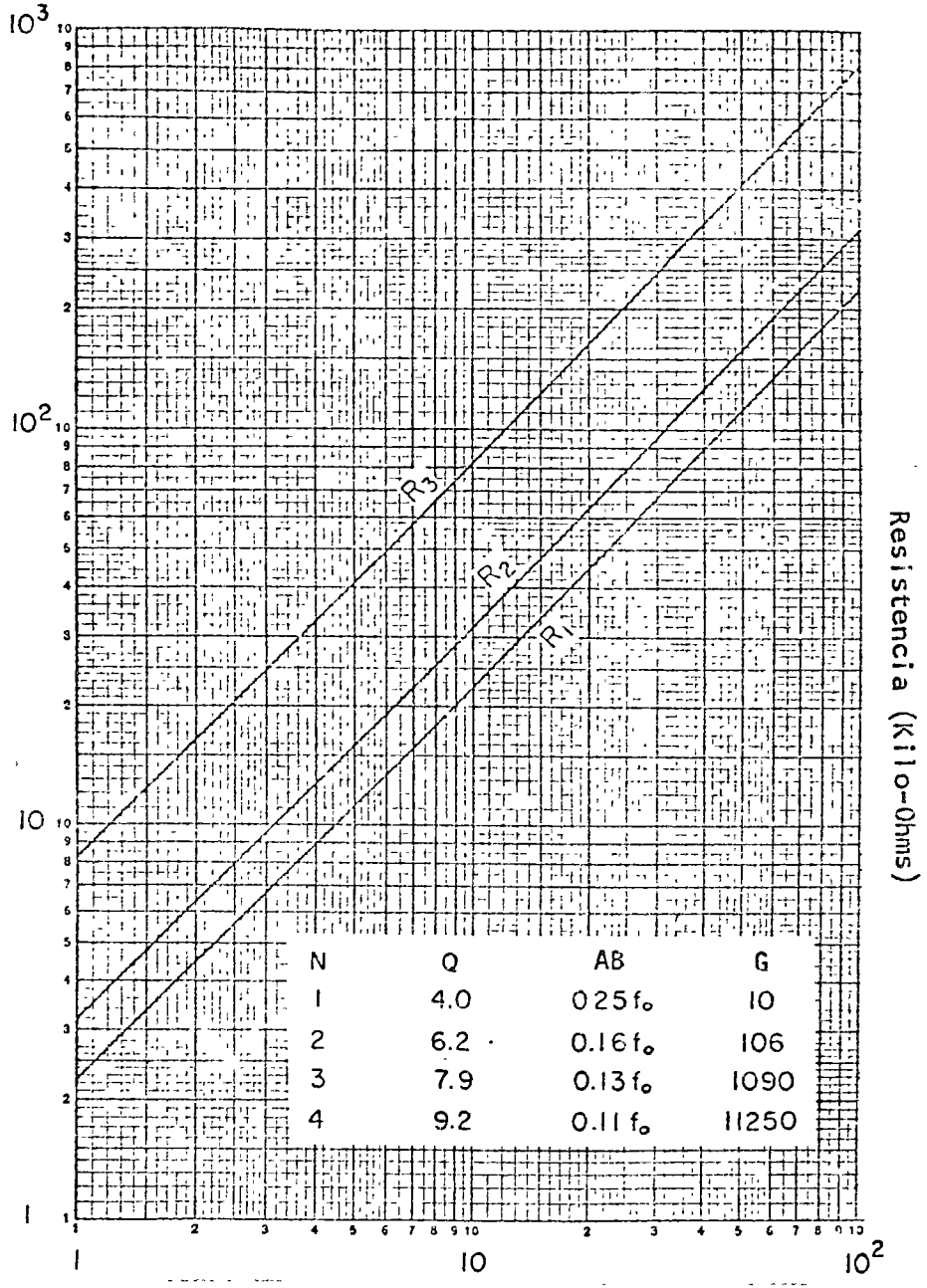


N	Q	AB	G
1	3.0	0.33 f_o	7.5
2	4.7	0.22 f_o	56
3	5.9	0.17 f_o	484
4	6 9	0.14 f_o	3139

Parametro K

GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2 y R_3

Fig. 6b



N	Q	AB	G
1	4.0	025 f_o	10
2	6.2	0.16 f_o	106
3	7.9	0.13 f_o	1090
4	9.2	0.11 f_o	11250

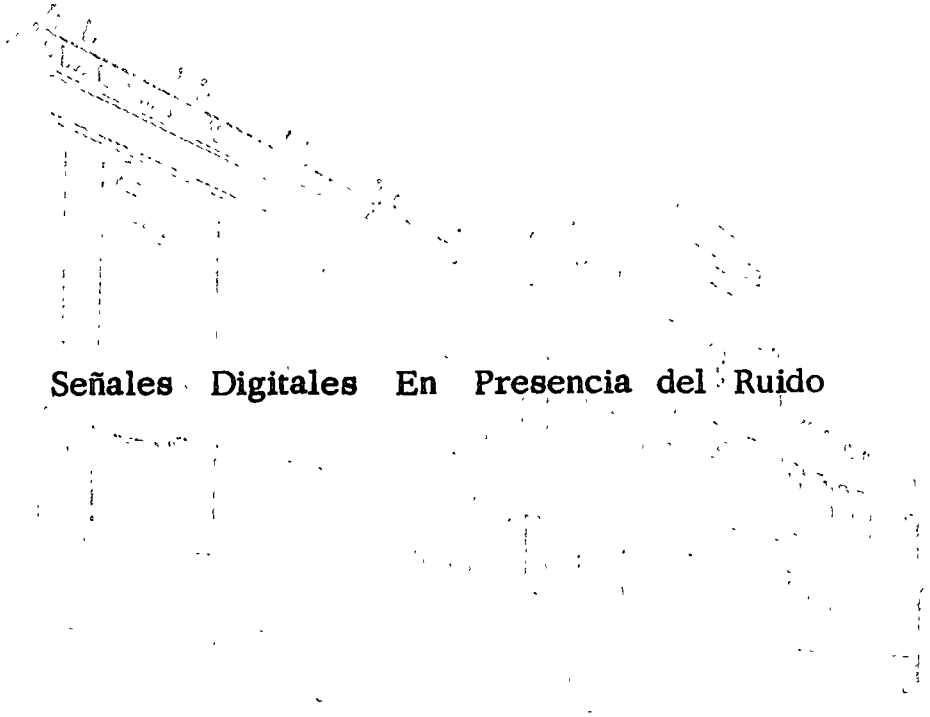
GRAFICA PARA DETERMINAR LOS VALORES DE LAS RESISTENCIAS R_1, R_2 y R_3

Fig. 6c

NOTAS

centro de educación continua
división de estudios superiores
facultad de ingeniería, unam

LA ELECTRONICA EN LAS COMUNICACIONES



Señales Digitales En Presencia del Ruido

M.en I. Federico Kuhlmann R.

C O D I F I C A C I O N Y D E C O D I F I C A C I O N

Federico Kuhlmann R.

I N D I C E

CAPITULO I. PROLOGO

PROLOGO

La presente exposición está dirigida a alumnos que cursan la materia de Comunicaciones II.

Siguiendo la secuencia lógica, los estudiantes deben estar familiarizados con los temas de las comunicaciones mencionados a continuación, para que el objetivo del tema a exponer esté claramente definido:

- Sistemas de modulación analógica con señales continuas
- Sistemas de modulación analógica con pulsos
- Sistemas digitales
- Origen y efecto del ruido

El objetivo de la sección "Codificación y decodificación", enmarcada en el temario del segundo curso de Comunicaciones

es el siguiente:

"Mostrar al alumno técnicas para proteger información digital transmitida a través de un canal ruidoso, contra el ruido aditivo del canal"

Se propone la siguiente meta:

"El alumno debe ser capaz de: determinar el tipo de código a utilizar y la protección de la cual se proveerá la información y diseñar los circuitos electrónicos para la implementación del código seleccionado, de acuerdo a la probabilidad de error del canal de transmisión".

Para alcanzar la meta y cumplir el objetivo propuestos se analizarán debidamente dos técnicas de protección:

- CODIGOS DE BLOQUE
- CODIGOS CONVOLUCIONALES

Debe enfatizarse que los codificadores (o decodificadores) están enmarcados dentro del codificador (o decodificadores) del canal; no se analizarán los moduladores o demoduladores de RF, que también son parte del codificador del canal.

CAPITULO II. CODIGOS DE BLOQUE

2. CODIGOS DE BLOQUE

2.1 Introducción

En este capítulo se mostrará una técnica de codificación para información binaria basada en agregar dígitos redundantes a la secuencia de información que forma una palabra. Utilizando argumentos de las Teorías de Información y Probabilidad, es fácilmente demostrable que el contenido de información no se altera con éstos dígitos y además que con los dígitos redundantes disminuye la probabilidad de error en la secuencia de dígitos binarios transmitida. Este tipo de códigos protege palabras utilizando la idea central de verificación de paridad. Esta está basada en la convención que, si una palabra tiene un número impar de unos, se le agrega al final otro uno; en caso contrario, se le agrega un cero. Es debido a este procesamiento, por palabras, que se les

llama a estos códigos Códigos de Bloque.

Entre las ventajas que presentan éstos códigos se pueden mencionar las siguientes:

- pueden tanto detectar como corregir errores
- se puede agregar cualquier número de dígitos redundantes; la capacidad de detección y corrección de errores depende de este número de dígitos redundantes
- son fácilmente realizables.

Evidentemente el código a utilizar depende del canal a través del cual se enviará la información. Para trasmitir por un canal muy ruidoso se necesita mucha protección para la información (o sea, muchos dígitos redundantes); para trasmitir por un canal con probabilidad de error (por dígito) muy baja, se necesitan menos dígitos redundantes para obtener en promedio el mismo número de errores, por secuencia de palabras, que en el caso anterior.
La idea central de este capítulo es mostrar la estructura básica y la forma de construir los códigos de bloque.

2.2 Definiciones

Sea $\underline{u} = (u_1, u_2, \ldots, u_n)$ un vector de información (o mensaje): al vector

$$\underline{x} = (\delta_e^{(1)}(\underline{u}),\ \delta_e^{(2)}(\underline{u}),\ \ldots,\ \delta_e^{(n)}(\underline{u}))$$

se le llamará palabra codificada o palabra trasmitida. Al conjunto de vectores $\underline{x}$ se le llamará código y se dirá que $\underline{x}$ es una palabra del código.

El conjunto $\{\delta_e^{(i)}(u)\}_{i=1}^{n}$ representa n combinaciones lineales de las n componentes de $\underline{u}$; no tienen que ser n combinaciones diferentes.

Si la palabra transmitida tiene n dígitos donde

$$n = n + m$$

entonces los últimos $m = n-n$ dígitos se llaman dígitos redundantes; los primeros n dígitos son los dígitos de información.

Defínase la suma en aritmética módulo 2 (mod-2) de la siguiente forma

$$0 \oplus 1 = 0 \quad 0 \oplus 0 = 0$$
$$1 \oplus 0 = 0 \quad 0 \oplus 1 = 1$$

Obsérvese que cambiar uno o más dígitos de una palabra codificada $\underline{x}$ es equivalente a sumarle (mod-2) a $\underline{x}$ un vector $\underline{z}$ con unos en las posiciones en que se cambiaron los dígitos de $\underline{x}$ y ceros en las demás. Por ejemplo, sea

$$\underline{x} = (1\ 0\ 1\ 1\ 0\ 0\ 1\ 0)$$

llámese $\underline{y}$ al vector $\underline{x}$ con uno o varios dígitos alterados •

$$\underline{y} = (1\ 1\ 0\ 1\ 0\ 1\ 1\ 0)$$

Entonces el vector $\underline{z}$ que satisface $\underline{x} = \underline{y} \oplus \underline{z}$ es

$$\underline{z} = (0\ 1\ 1\ 0\ 0\ 1\ 0\ 0)$$

Utilizando estas propiedades se llamará a $\underline{z}$ vector de errores y a $\underline{y}$ palabra recibida. Nótese que si

$$\underline{z} = \underline{0}$$

($\underline{0}$ es un vector de ceros) para todas las palabras transmitidas entonces se puede concluir que el canal de trasmisión no introduce errores y además

$$\underline{x} = \underline{y}$$

o sea, que la palabra recibida es igual a la transmitida.

Nótese que $\underline{y} = \underline{x} \oplus \underline{z}$

o equivalentemente $\underline{z} = x \oplus \underline{y}$

Al número de dígitos diferentes de cero en una secuencia se le llamará peso de la secuencia; al mínimo número de dígitos diferentes de cero en las sumas (mod-2) de dos palabras cuales

quiera de un código se le llamará distancia del código.

Un código que genera palabras de longitud r a partir de mensajes de longitud n se llama código (r,n).

En álgebra mod-2 son válidas las leyes asociativa, distributiva y conmutativa de la aritmética.

2.3 Construcción de los códigos

2.3.1 Codificación

Como se mencionó anteriormente, las palabras del código (r,n) se forman a partir de combinaciones lineales de los elementos de $\underline{u}$; estas pueden ser descritas a través de un conjunto de ecuaciones de la forma

$$x_i = \sum_{j=1}^{n} u_j \, g_{ji} \qquad 1 \leq i \leq r \qquad (1)$$

donde

x_i es la i-ésima componente de $\underline{x}$

$\sum_{\{\alpha\}}$ es la sumatoria mod-2 sobre el conjunto de índices $\{\alpha\}$

$\{g_{ij}\}_{\substack{1 \leq j \leq r \\ 1 \leq i \leq n}}$ representa un conjunto de dígitos binarios arbitrarios pero fijos

Se hablará de un código sistemático (r,n) si

$$g_{ji} = \delta_{ji} \qquad 1 \leq j \leq n$$
$$1 \leq i \leq n$$

donde δ_{ji} es la función δ de Kronecker.

Obviamente (1) representa un conjunto de ecuaciones lineales; estas pueden ser escritas matricialmente

$$\underline{x} = \underline{u}\, G \tag{2}$$

G es una matriz de dimensión $(n \times r)$ cuyos elementos son los números g_{ji} del conjunto descrito anteriormente.

Esto es

$$G = \begin{bmatrix} g_{11} & g_{12} & \cdots & g_{1r} \\ g_{21} & g_{22} & \cdots & g_{2r} \\ \vdots & \vdots & & \vdots \\ g_{n1} & \cdots & & g_{nr} \end{bmatrix} \tag{3}$$

y si el código es sistemático

$$G = \begin{bmatrix} 1 & 0 & \cdots & 0 & g_{1,n+1} & \cdots & g_{1,r} \\ 0 & 1 & \cdots & 0 & g_{2,n+1} & \cdots & g_{2,r} \\ \vdots & \vdots & & \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & 1 & g_{n,n+1} & \cdots & g_{n,r} \end{bmatrix} \tag{4}$$

lo cual puede ser escrito como

$$G = \left[I_n \;\vdots\; G' \right] \qquad (5)$$

donde I_n es la matriz identidad de dimension n.

Debido a que, a través de la ecuación (2) se generan las palabras del código, a la matriz G se le llama matriz generadora.

2.3.2 Decodificación

Por simplificar matemáticamente el proceso de decodificación se utilizarán códigos sistemáticos.

La ecuación (1), para un código sistemático, puede ser expresada como

$$x_i = u_i \qquad 1 \le i \le n \qquad (6)$$

$$x_i = \sum_{j=1}^{n} g_{ji}\, u_j \qquad n < i \le r \qquad (7)$$

y substituyendo (6) en (7)

$$x_i = \sum_{j=1}^{n} g_{ji}\, x_j \qquad n < i \le r \qquad (8)$$

o similarmente

$$\sum_{j=1}^{n} g_{ji} \, x_j \oplus x_i = 0 \qquad n < i \leq r \qquad (9)$$

La ecuación (9) puede ser desarrollada y escrita en forma matricial quedando

$$(x_1 \; x_2 \; - \; - \; - \; x_n) \begin{bmatrix} g_{1,n+1} & g_{1,n+2} & \cdots & g_{1,r} \\ g_{2,n+1} & g_{2,n+2} & \cdots & g_{2,r} \\ \vdots & & & \\ g_{n,n+1} & g_{n,n+2} & \cdots & g_{n,r} \\ \hline 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & \vdots \\ \vdots & \vdots & 1 & \vdots \\ 0 & \cdots & \cdots & 1 \end{bmatrix} = \underline{0}$$

o equivalentemente

$$\underline{x} \begin{bmatrix} G' \\ \hline I_m \end{bmatrix} = \underline{0} \qquad (10)$$

Si se define la matriz H por medio de

$$H = \begin{bmatrix} G' \\ \hline I_m \end{bmatrix} \qquad (11)$$

Entonces (10) se transforma en

$$\underline{x} \; H = \underline{0} \qquad (12)$$

Es evidente que si una palabra se genera a partir de (2), es-

ta debe satisfacer (12); por otro lado, una palabra que satisface (12) debe haber sido generada por medio de (2).

Es importante hacer notar que el conjunto de palabras de un código de bloque es mayor que el número de posible mensajes a codificar; si se codifican 2^n mensajes de longitud n con un código (n,n) donde $n>n$ entonces evidentemente $2^n>2^n$; esto significa que existen secuencias de longitud n que no pertenecen al código (n,n); se tratará que éstas secuencias sean precisamente la suma de palabras transmitidas y vectores de error.

De aquí se puede concluir que los elementos de la matriz generadora deben ser fijados de tal forma que, si se desea corregir errores de orden ℓ (los vectores de error tienen peso ℓ), la distancia entre la palabra recibida y cualquier palabra del código excepto la transmitida debe ser mayor que la distancia entre la palabra recibida y la transmitida, o sea, mayor que ℓ. Este criterio se llama criterio de máxima similitud.

Como se recordará $$\underline{y} = \underline{x} \oplus \underline{z} \qquad (13)$$

Pero si $\underline{y}$ no pertenece al código

$$\underline{y} H \neq \underline{0} \qquad (14)$$

La ecuación (14) encierra la idea básica para la detección de

errores; la ecuación (13) se utilizará para su corrección.

Defínase el síndrome $\underline{S}$ en la siguiente forma

$$\underline{S} = \underline{y}\, H \qquad (15)$$

De lo anterior se concluye que si $\underline{S} = \underline{0}$ entonces $\underline{y}$ es una palabra del código; si $\underline{S} \neq \underline{0}$ entonces $\underline{y}$ no pertenece al código y la palabra transmitida $\underline{x}$ fue alterada por el vector de error $\underline{z}$ (debido evidentemente al ruido del canal). Esto es

$$\underline{y} = \underline{x} \oplus \underline{z}$$

resultando el síndrome

$$\underline{S} = (\underline{x} \oplus \underline{z})\, H = \underline{x}\, H \oplus \underline{z}\, H \qquad (16$$

y debido a la ecuación (12)

$$\underline{S} = \underline{z}\, H \neq \underline{0} \qquad (17)$$

porque $\underline{z}$ no pertenece al código que tiene una distancia mayor que cualquier vector de error. (Se supone que el canal tiene probabilidad no nula de error por dígito; sin embargo la probabilidad de alterar d dígitos de una palabra, que resultaría en otra palabra del código, es insignificante).

El síndrome es un vector de dimensión $m = n-k$ o sea que exis-

ten sólo 2^m síndromes diferentes; si se asocia a cada posible síndrome un vector de error del conjunto de posibles errores (que tiene 2^n elementos), una vez conocido el síndrome se podrá determinar la secuencia de error que probablemente lo originó. Por tanto, los errores que se escojan deberán ser los de mayor probabilidad de ocurrencia.

Supóngase que el vector de error $\underline{z}_1$ tiene alta probabilidad de ocurrencia; asóciesele el síndrome $\underline{S}_1$. La palabra transmitida es $\underline{x}_1$. La recibida, evidentemente, $\underline{y}_1 = \underline{x}_1 \oplus \underline{z}_1$. A partir de $\underline{y}_1$ se encuentra $\underline{S}_1$ y de éste, $\underline{z}_1$. En esta forma se determina finalmente $\underline{x}_1 = \underline{y}_1 \oplus \underline{z}_1$. Por las propiedades de detección de la matriz H a esta se le llama matriz de verificación.

2.3.3 Ejemplo

Se desea codificar mensajes binarios de 3 dígitos en forma sistemática. El canal de transmisión requiere que se corrijan por lo menos todos los errores de peso unitario (errores sencillos), se supone además que todos los errores depeso 2 tienen igual probabilidad de ocurrencia.

Solución

El número de mensajes es $2^3 = 8$. Como el código debe corregir todos los errores sencillos y éstos pueden aparecer en cual-

quier posición se necesita un número mínimo de $(4+m)$ síndromes (m = número de dígitos redundantes).

Por tanto se agregarán 3 dígitos redundantes para tener en total 6 dígitos por palabra y 8 diferentes síndromes.

Como H debe tener todos sus renglones difererentes para que al multiplicar por cada uno de los errores sencillos se obtengan síndromes distintos, se iniciará el diseño del código con esta matriz cuya estructura está dada por (11)

$$H = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ - & - & - \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} G' \\ - - \\ I_3 \end{bmatrix}$$

$$G = \left[I_3 \;\vdots\; G' \right] = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

A partir de G se pueden determinar las funciones

$$\{ \delta_e^{(i)} \}_{i=1}^{6}$$

Estas son

$$x_1 = \delta_e^{(1)}(\underline{u}) = u_1$$

$$x_2 = \delta_e^{(2)}(\underline{u}) = u_2$$

$$x_3 = \delta_e^{(3)}(\underline{u}) = u_3$$

$$x_4 = \delta_e^{(4)}(\underline{u}) = u_1 \oplus u_3$$

$$x_5 = \delta_e^{(5)}(\underline{u}) = u_1 \oplus u_2$$

$$x_6 = \delta_e^{(6)}(\underline{u}) = u_2 \oplus u_3$$

El siguiente paso es asignar un síndrome a cada error probable, a través de una tabla de decodificación; de acuerdo al planteamiento, los errores más probables son los más sencillos.

TABLA DE DECODIFICACION

Síndrome $\underline{S}$	Vector de errores $\underline{z}$
0 0 0	0 0 0 0 0 0
0 0 0	0 0 0 0 0 1
0 1 0	0 0 0 0 1 0
1 0 0	0 0 0 1 0 0
1 0 1	0 0 1 0 0 0
0 1 1	0 1 0 0 0 0
1 1 0	1 0 0 0 0 0

Debido a que todos los errores de peso 2 son equiprobables se escogió arbitrariamente uno cuyo síndrome fuera el que faltaba en la tabla.

Así, si se recibe $\underline{y} = (1\ 0\ 1\ 0\ 1\ 0)$

entonces $\underline{S} = (0\ 0\ 1)$

y $\underline{z} = (0\ 0\ 0\ 0\ 0\ 1)$

por lo cual $\underline{x} = y \oplus z = (1\ 0\ 1\ 0\ 1\ 1)$

y $\underline{u} = (1\ 0\ 1)$

Este código detecta y corrige todos los errores sencillos y un error doble.

2.3.4 Realización

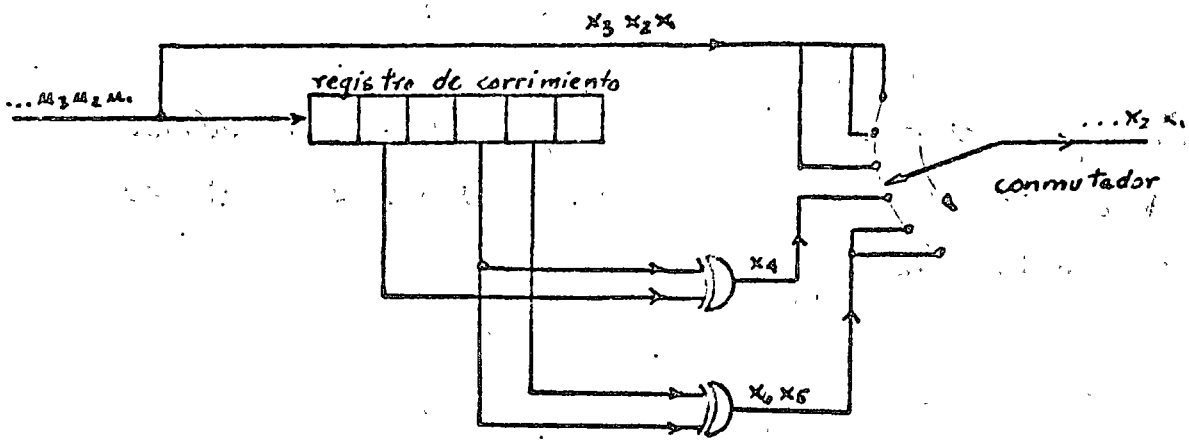
Para la realización del código (6,3) bajo análisis no se requieren más que los siguientes elementos activos:

registrosde corrimiento

compuertas OR-exclusivo

reloj

Esquemáticamente se ilustra a continuación el codificador



CAPITULO III. CODIGOS CONVOLUCIONALES

3. CODIGOS CONVOLUCIONALES

3.1 Introducción

Debido a que la información digital no siempre está estructurada en forma de palabras (como en PCM), es necesario estudiar otro tipo de códigos que permitan la protección de la información en forma serial (tal y como se obtendría a partir de un Modulador Delta).

Se protegerá la información dígito a dígito intercalando en la secuencia de información dígitos redundantes. A un código convolucional que contiene k dígitos de chequeo por cada n dígitos de información se le llamará código convolucional (k,n).

3.2 Definiciones, codificación y decodificación.

Sea $\underline{u} = (u_1, u_2, \ldots)$ una secuencia de dígitos de información (mensaje).

A la secuencia

$$\underline{x} = (x_{11}, x_{12}, x_{13}, \ldots, x_{1k}, x_{21}, \ldots x_{2k} \ldots x_{31} \ldots)$$

se le llama secuencia codificada o secuencia transmitida; x_{ij} es generado a través de combinaciones lineales de los ℓ dígitos anteriores a u_{i+1}.

Esto es

$$x_{ij} = \delta_c^{(j)} (u_{i-1-e}, \ldots, u_{i-1})$$

donde $\delta_c^{(j)}(\,,\,,\,,\ldots)$ es una combinación lineal de los argumentos. A la secuencia

$$\underline{y} = (y_{11}, y_{12}, y_{13}, \ldots, y_{1k}, y_{21} \ldots y_{2k} \ldots)$$

se le llama secuencia recibida;

es evidente que si el canal de transmisión no tiene ruido entonces

$$\underline{x} = \underline{y} \tag{19}$$

Por otra parte, si el canal tiene ruido y el código se diseña en forma adecuada a partir de $\underline{y}$ se obtiene la secuencia $\underline{t}$ tal que

$$\underline{u} = \underline{t} \tag{20}$$

donde a $\underline{t}$ se le llamará secuencia decodificada.

La secuencia decodificada $\underline{t}$ se obtiene en la siguiente forma

$$\underline{t} = (t_1, t_2, \ldots)$$

donde

$$t_\alpha = g_\lambda^{(\beta)} (y_{\alpha-e,1}, \ldots y_{\alpha-e,j}, \ldots y_{\alpha,1} \ldots y_{\alpha,j}) \tag{21}$$

y $g_\lambda^{(\beta)}(\cdot)$ es una función lógica de los argumentos.

Se ilustrará por medio de un ejemplo la codificación y decodificación con este tipo de códigos.

3.3 Ejemplo

Se desea transmitir una secuencia de información

$$\underline{u} = (1\ 0\ 1\ 1\ 0\ \ldots\ldots)$$

protegida por medio de un código convolucional (2,1).

El canal tiene una probabilidad de error tal que

$$P(\text{3 errores en 3 dígitos}) << P(\text{2 errores en 3 dígitos}) << P(\text{1 error cada 3 dígitos})$$

Solución

Una posible codificación es

$$x_{i1} = u_i = x_{i2}$$

resultando la secuencia transmitida

$$\underline{x} = (u_1, u_1, u_1, u_2, u_2, u_2, \ldots\ldots)$$

o sea

$$\underline{x} = (1\ 1\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 0\ 0\ 1\ 1\ 1\ \ldots\ldots)$$

La decodificación y corrección se efectúan en la siguiente forma

$$t_\alpha = \begin{cases} y_{\alpha 1} & \text{si} \quad y_{\alpha 1} = y_{\alpha 2} \\ y_{\alpha 2} & \text{si} \quad y_{\alpha 2} = y_{\alpha 3} \\ y_{\alpha 3} & \text{si} \quad y_{\alpha 3} = y_{\alpha 1} \end{cases} \qquad (22$$

La relación (22) es precisamente la función lógica mencionada en (21)

Supóngase que la secuencia recibida es

$$\underline{y} = (1\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 1\ 1\ 1\ 1\ 0\ 0\ 1\ \ldots\ldots)$$

Usando t_α como se definió en (22) resulta que

$$\underline{t} = (1\ 1\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 1\ 0\ 0\ 0\ \ldots\ldots)$$

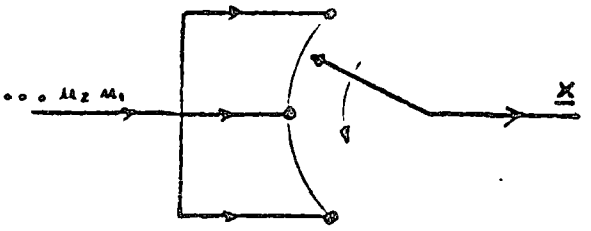
la cual es igual al mensaje.

El código del ejemplo anterior es apropiado para el canal descrito en las hipótesis; si fuese muy probable la aparición de dos errores en 3 dígitos consecutivos, éste código obviamente podría provocar que $\underline{t} \neq \underline{u}$ con una probabilidad considerable.

3.4 Realización

El codificador puede ser realizado con el siguiente circui-

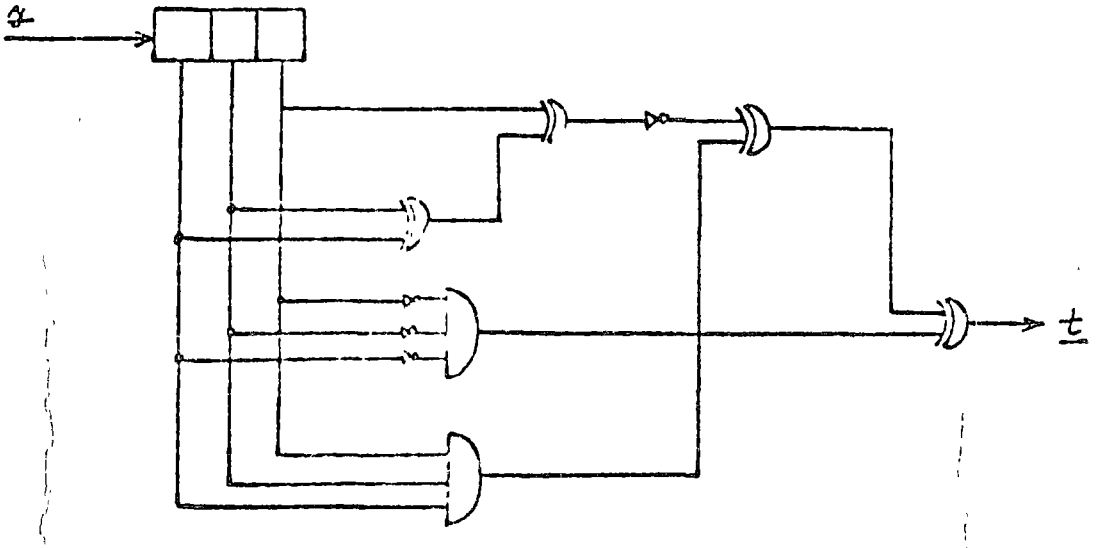
to:



Un mismo dígito es alimentado al canal de transmisión 3 veces para que 3 dígitos consecutivos de $\underline{x}$ sean iguales.

La frecuencia del conmutador debe ser 3 veces mayor que (duración de un dígito de $\underline{u}$)$^{-1}$

La decodificación puede ser realizada con el circuito mostrado a continuación:



Fácilmente se puede demostrar que el circuito mostrado decodifica correctamente de acuerdo a la tabla

$y_{\alpha,3}$	$y_{\alpha,2}$	$y_{\alpha,1}$	t_α
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

La duración del dígito t_α es tres veces mayor que la duración de cualquier dígito de $\underline{y}$.

CAPITULO IV. CONCLUSION

4. CONCLUSION

Finalmente es importante mencionar que los dos tipos de códigos analizados son elementos del conjunto de códigos correctores; existen una infinidad de éstos, con las estructuras más variadas y complejas que uno pueda imaginar.

Sin embargo, para fines didácticos, el análisis de los códigos de bloque y los convolucionales es suficiente para familiarizar al estudiante con la posibilidad de proteger la información y para motivar a estudiantes interesados.

Se ha demostrado que fácilmente se puede proteger la información digital contra ruido en un canal de transmisión.

Esta información puede ser codificada tanto cuando está dis

ponible en forma de palabras como cuando es una secuenci continua de dígitos, sin estructura alguna.

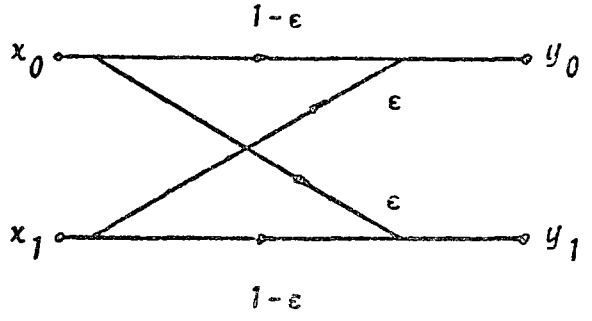
Para complementar la teoría se ha desarrollado en el laboratorio de Comunicaciones un circuito codificador y uno de codificador de códigos de bloque ambos con lógica TTL.

Deben diseñarse un codificador y un decodificador convolucionales para poderlos utilizar en serie con el Modulador Delta que está siendo terminado.

APENDICE. CANAL BINARIO SIMETRICO

CANAL BINARIO SIMETRICO (BSC)

Un modelo matemático de un canal de transmisión frecuentemente utilizado es el representado a continuación



A ε se le llama probabilidad de transición y es precisamente la probabilidad de error en un dígito transmitido, o sea

$$\varepsilon = P(y_1|x_0) = P(y_0|x_1) < \frac{1}{2}$$

Supóngase que la información digital proviene de una fuente discreta sin memoria, o sea que se satisface

$$P(x_i, x_{i+1}) = P(x_i)P(x_{i+1})$$

y que además

$$P(x_0) = P(x_1) = \frac{1}{2}$$

Entonces, para el ejemplo del capítulo 2, la probabilidad de error en el mensaje decodificado es

$$P(e) = 1 - P\ (no\ error) =$$

$$= 1 - (1-\varepsilon)^6 - 6\ (1-\varepsilon)^5 - \varepsilon^2(1-\varepsilon)^4 \qquad (23)$$

lo cual está basado precisamente en la corrección de todos los errores sencillos y uno doble.

Si no se codificaran los mensajes, entonces

$$P(e) = 1 - P(no\ error) = 1-(1-\varepsilon)^6 \qquad (24)$$

Evidentemente, la probabilidad de error es menor cuando se codifica la información, debido a que

$$6\varepsilon(1-\varepsilon)^5 + \varepsilon^2\ (1-\varepsilon)^4 > 0$$

Para el ejemplo del Apéndice 3, si se codifica, se obtiene una probabilidad de error en el mensaje decodificado dada por

$$P(e) = 1 - P\ (no\ error) = 1 - (1-\varepsilon)^3 - 3\ (1-\varepsilon)^2 \qquad (25)$$

y si no se codifica

$$P(e) = 1 - P(no\ error) = 1-(1-\varepsilon)^3$$

y como $3\varepsilon(1-\varepsilon)^2 > 0$ se concluye también que la codificación disminuye la probabilidad de error por dígito del mensaje.

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LA ELECTRONICA EN LAS COMUNICACIONES

APLICACION A LAS COMUNICACIONES ANALOGICAS

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AGOSTO DE 1976.

CAPITULO II

2. APLICACION A LAS COMUNICACIONES ANALOGICAS

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2. APLICACION A LAS COMUNICACIONES ANALOGICAS

Las técnicas de trasmisión de señales se llevan a la práctica, casi en su totalidad, con circuitos electrónicos; tanto en el caso de las comunicaciones analógicas, como en las digitales, debido principalmente a que son estos circuitos los que más fácilmente permiten realizar los procesos de modulación y demodulación, al mismo tiempo que dan gran confiabilidad al sistema.

En el caso de los sistemas de modulación análogos, se debe introducir la información m(t) en una portadora p(t) de la forma

$$p(t) = A_p \cos(\omega_o t + \emptyset) \qquad (2.1)$$

La señal p(t), que cumple con la función de adaptar la información al canal de trasmisión, puede transportarla si ésta se incluye de alguna manera en p(t) haciendo variar uno o varios de sus parámetros en forma proporcional a m(t).

La señal de voltaje m(t) se introduce en p(t) si se varía la amplitud A_p o el ángulo $\omega_o t + \emptyset$ de esta última. Cuando lo que varía es A_p, los sistemas se modulación se denominan lineales, por el comportamiento de los espectros de frecuencia; mientras que si lo que varía es el ángulo, se denominan angulares. Ejemplos típicos de los sistemas lineales son la Amplitud Modulada (AM) y la Doble Banda Lateral (DSB); y de los sistemas angulares la Frecuencia Modulada (FM) y la Fase Modulada (PM). Estos son los sistemas de modulación que se analizarán a continuación.

2.1 Moduladores Lineales

El principal problema de la Ingeniería de Comunicaciones es establecer contacto entre dos puntos con el fin de intercambiar información. Esto se realiza por medio de la trasmisión de mensajes a través del espacio o por medio de una línea de trasmisión. Evidentemente, es deseable que este proceso se lleve a cabo dentro de ciertos márgenes de diseño que comprenden básicamente la recepción confiable, la adaptación adecuada de la información al medio (canal), el costo del sistema y la complejidad del mismo.

Al adaptar el mensaje al canal de trasmisión, deben considerarse las características, tanto de la información como del medio, para decidir la técnica a emplear. Cuando se trata de información de baja frecuencia (p. ej. audio) a enviarse a través del espacio, hay dos problemas fundamentales que deben resolverse: la propagación de estas frecuencias y la interferencia que podría haber con otras comunicaciones. Ambos problemas se resuelven mediante la selección de un intervalo adecuado de frecuencias que presente las características de propagación requeridas por el caso y se procede a situar, mediante la modulación, el espectro de la información en dicho intervalo. La técnica mas empleada para este efecto es la Modulación en Amplitud (AM), debido a la sencillez con que se realizan los circuitos moduladores y demoduladores encargados de desplazar el espectro de m(t) al intervalo de frecuencias elegido. Por otra parte, la técnica de Doble Banda Lateral (DSB) tiene la ventaja de que toda la potencia de la señal resultante se emplea en las componentes debidas a la información. Así, si se de

fine la eficiencia $\mathcal{E}$ como

$$\mathcal{E} = \frac{\text{potencia de las componentes debidas a } m(t)}{\text{potencia total}} 100\% \qquad (2.2)$$

se observa que para DSB $\mathcal{E} = 100\%$. Sin embargo, esta eficiencia solo se consigue con una mayor complejidad de los circuitos moduladores y demoduladores.

2.1.1 Modulación de Amplitud (AM)

El diagrama de bloques de la Fig. 2.1 muestra el proceso de modulación de AM, el que consiste básicamente en la obtención de la señal

$$g_{AM}(t) = A_p(K + m(t)) \cos\omega_o t \qquad (2.3)$$

donde K es un voltaje constante que se agrega a m(t) y A_p es el valor relativo de la portadora p(t). En la ecuación (2.3) se observa que la amplitud de la portadora se hace variar alrededor de K de acuerdo a m(t). En AM se exige que $K \geq \max(|m(t)|)$, de manera que el término amplitud cumple con

$$A_p(K + m(t)) \geq 0 \qquad (2.4)$$

Se define el índice de modulación a, por medio de la relación que existe en un momento dado entre K y $|\max(\, m(t)\,)|$

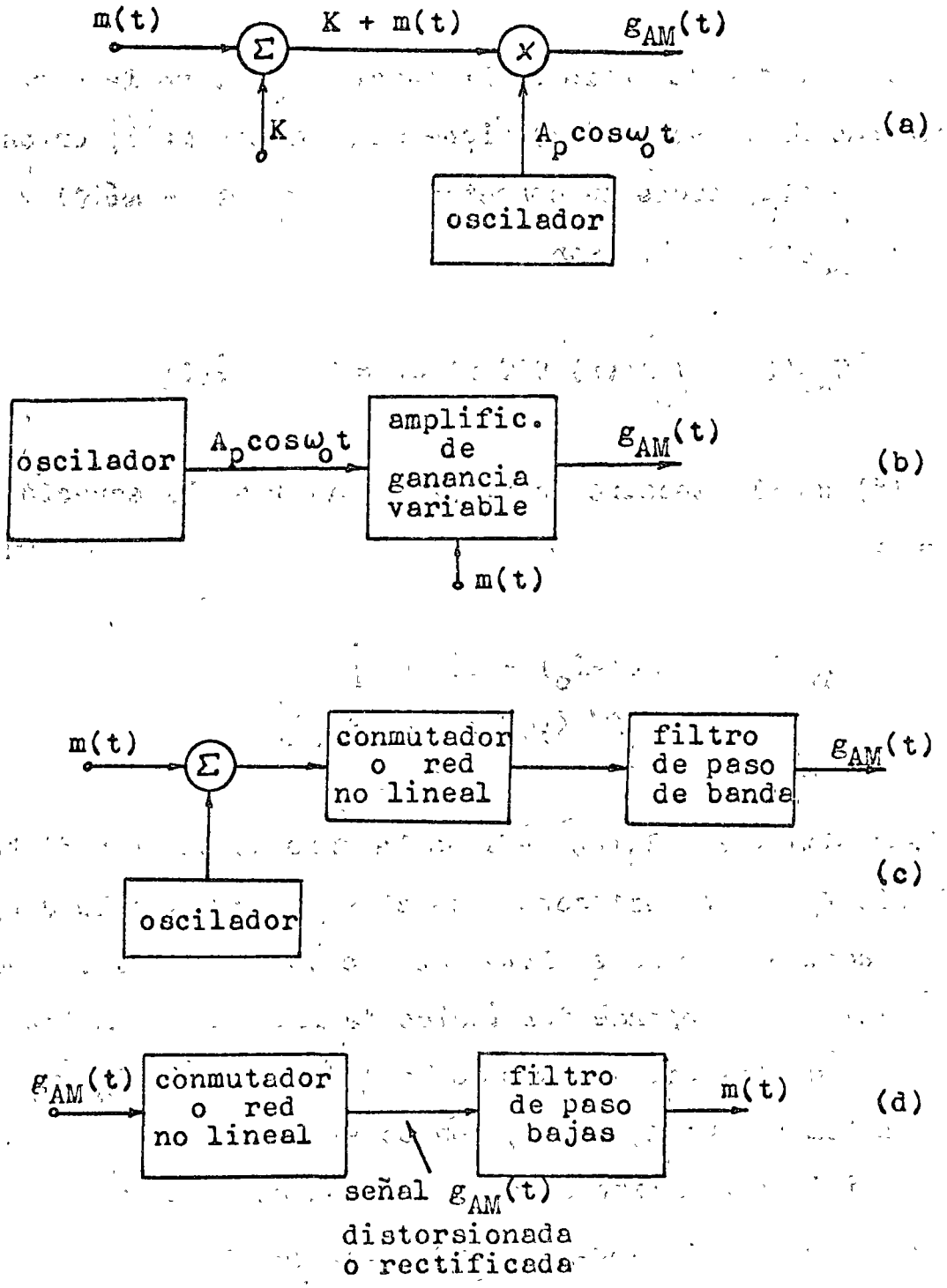

Fig. 2.1 La modulación en amplitud a) El proceso de modulación, b) amplificador modulador de ganancia variable, c) modulador no lineal, d) el proceso de demodulación.

$$a = \frac{|\max(\ m(t)\ )|}{K} 100\% \qquad (2.5)$$

Respecto del espectro de la señal $g_{AM}(t)$, en la Fig. 2.2 se aprecia que si la señal m(t) tiene un espectro M(f), entonces m'(t) = K + m(t) tiene un espectro M'(f) = M(f) + Kδ(f) y el de la señal $g_{AM}(t)$ resulta ser

$$G_{AM}(f) = \int_{-\infty}^{\infty} M'(x)\ P(f-x)\ dx = M'(f)*P(f) \qquad (2.6)$$

donde P(f) es el espectro de p(t). A partir de la ecuación (2.6), se tiene*

$$G_{AM}(f) = \frac{1}{2}\left[M(f-f_o) + M(f+f_o)\right] + \frac{K}{2}\left[\delta(f-f_o) + \delta(f+f_o)\right] \qquad (2.7)$$

Este último resultado refleja la traslación de M(f) hasta la frecuencia f_o de la portadora, más el espectro de ella, P(f). Debe notarse, además, que la amplitud de los espectros desplazados $M(f-f_o)$ y $M(f+f_o)$ depende del índice de modulación, mientras que la amplitud de los componentes de la portadora $\delta(f-f_o)$ y $\delta(f+f_o)$ depende solamente de K, o sea, son constantes.

La eficiencia máxima de este sistema se tiene para $|\max[m(t)]|$ = K, lo que significa para m(t) senoidal que $\mathcal{E}$ = 33.3%

*Se ha tomado $P(f) = \delta(f-f_o) + \delta(f+f_o)$, o sea, $A_p = 1$

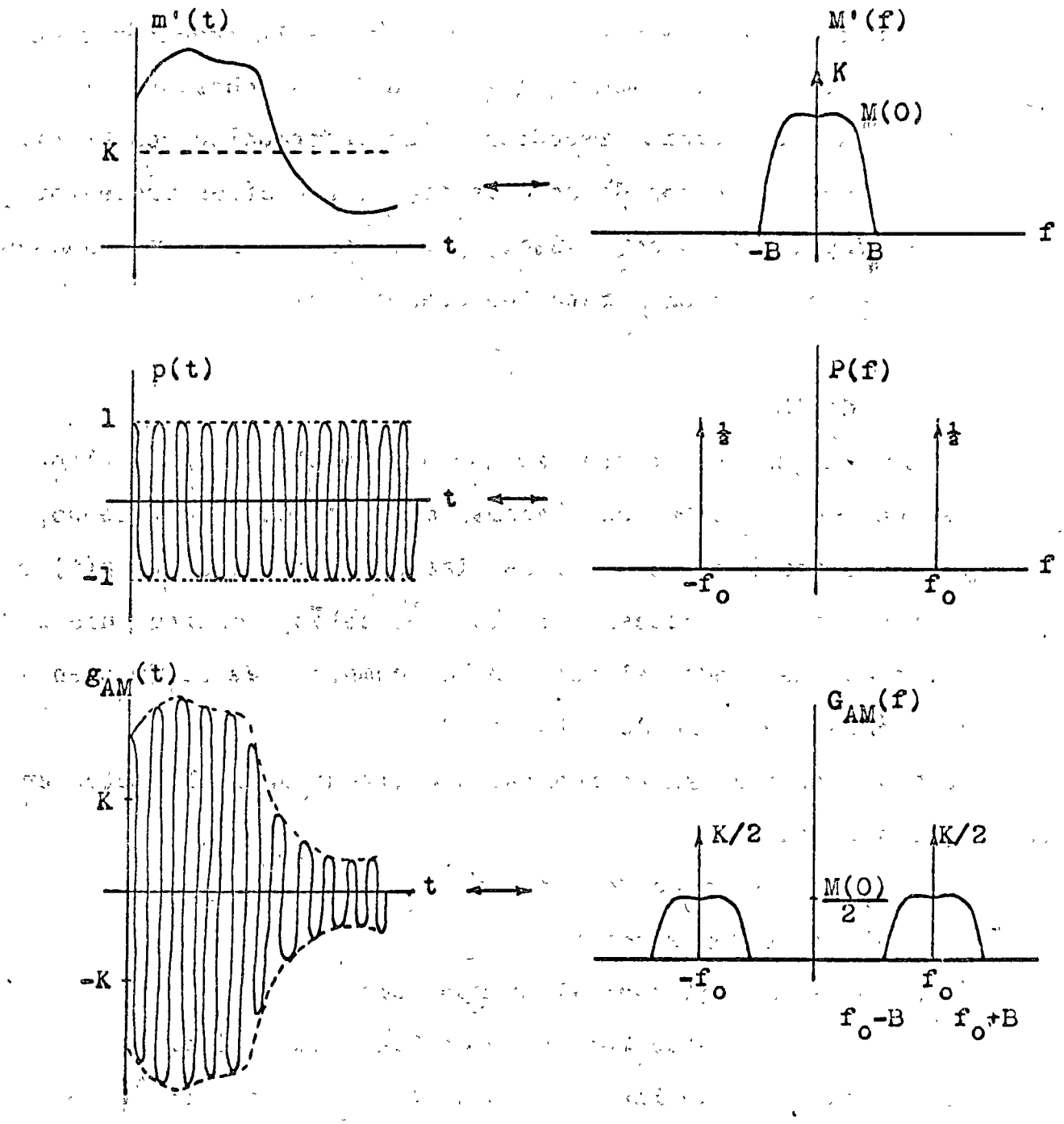

Fig. 2.2 Las señales y sus espectros en la modulación de AM a) Señal moduladora (información), b) portadora, c) señal de AM resultante.

Por otra parte, el proceso de demodulación de AM (denominado detección), es simple debido a que la forma de la envolvente de la señal $g_{AM}(t)$ es exactamente igual a la de la señal m(t) (ver Fig. 2.2), lo que permite reconstruir la información con un circuito no lineal (detector de envolvente), o con otros procedimientos que se analizarán a continuación, pero que no son muy comunes (detector de conmutación y detector cuadrático).

Moduladores de AM

La traslación de frecuencias que debe realizar un modulador se consigue con circuitos no lineales o variables en el tiempo, los que al distorcionar o modificar las señales portadora p(t) e información m(t), introducen armónicas de éstas, consiguiendo en esta forma que se pueda seleccionar los componentes de frecuencia necesarios por medio de filtros.

La modulación de AM se realiza con circuitos no lineales en los siguientes casos

a) Modulador de Conmutación

b) Modulador Cuadrático

y con circuitos variables en el tiempo como

c) Amplificador Modulador de Ganancia Variable

La demodulación de las señales de AM se realiza en forma similar con los siguientes circuitos no lineales

a) Demodulador de Envolvente

b) Demodulador de Conmutación

c) Demodulador Cuadrático

Amplificador Modulador de Ganancia Variable y
Demodulador de Envolvente.

Estos son los métodos más usados para efectuar los procesos de modulación y demodulación de AM. La Fig. 2.3 muestra el diagrama de un amplificador de ganancia variable típico, en el que la ganancia A es función de la información m(t). Entonces, si se tiene que A(t) = K + m(t), la señal de salida es

$$g_{AM}(t) = A_p(K + m(t)) \cos\omega_o t \qquad (2.8)$$

ecuación que corresponde con (2.3).

El amplificador de ganancia variable puede implementarse con una válvula de vacío o con otros dispositivos electrónicos, como se aprecia en la Fig. 2.3, procurando que la señal m(t) introduzca una variación en la polarización del circuito. Esto provocará que la ganancia del amplificador varíe de acuerdo a m(t). En la práctica no es indispensable que A(t) sea exactamente igual a K + m(t), ya que cualquier distorsión que se presente puede eliminarse con un circuito sintonizado de salida.

Cabe destacar que estos moduladores se transforman en simples amplificadores si se elimina la señal m(t) (p. ej. cuando el índice de modulación a = 0), lo que implica que estos circuitos tienen la ventaja de amplificar la señal. Sin embargo, debido a que la variación que produce la polarización en los parámetros μ o β del dispositivo activo en cuestión, este tipo de modulador no permite índices de modulación muy elevados. Este inconveniente se

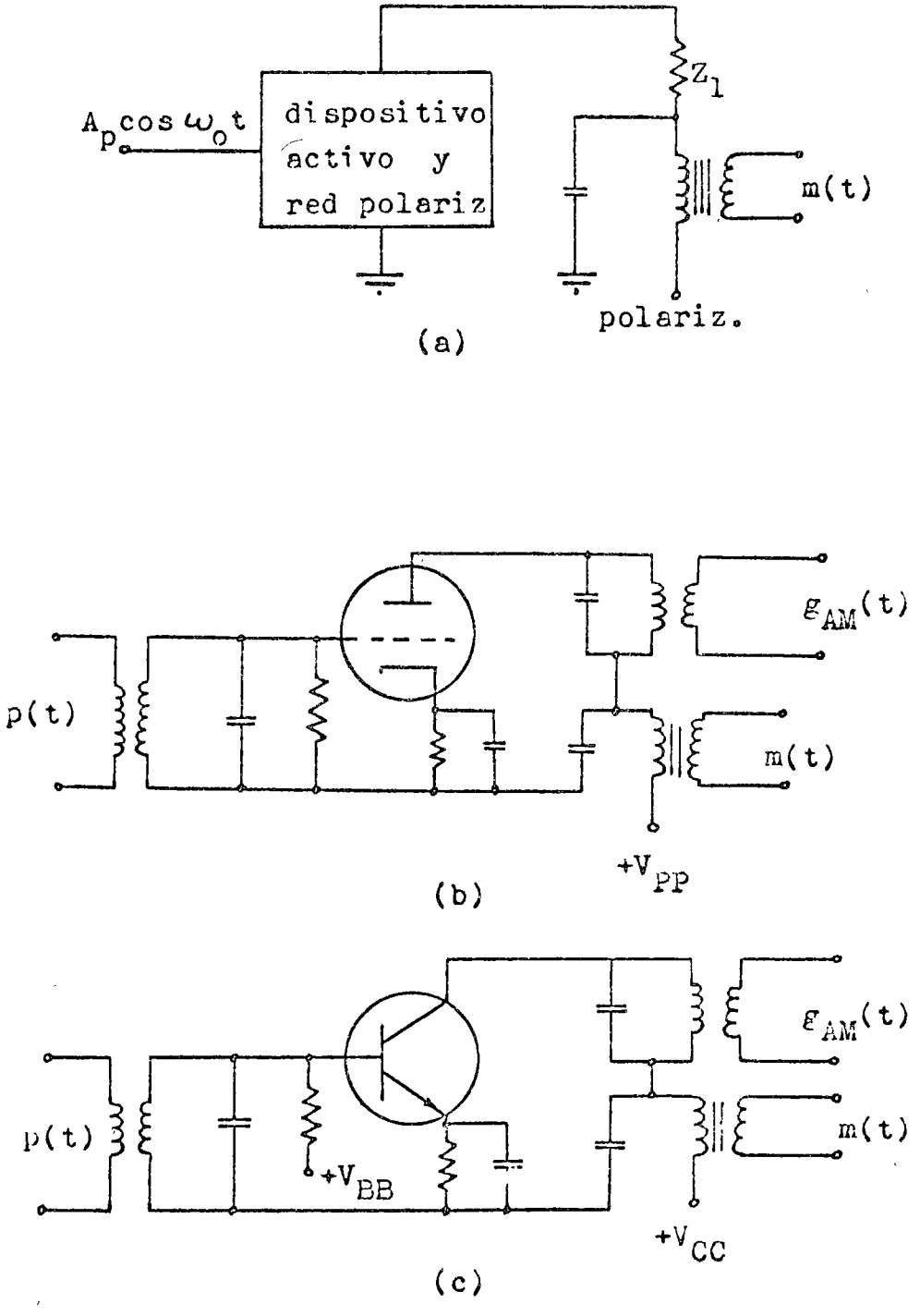

Fig. 2.3 Modulador amplificador de ganancia variable. a) Diagrama típico, b) modulador con triodo, c) modulador con transistor.

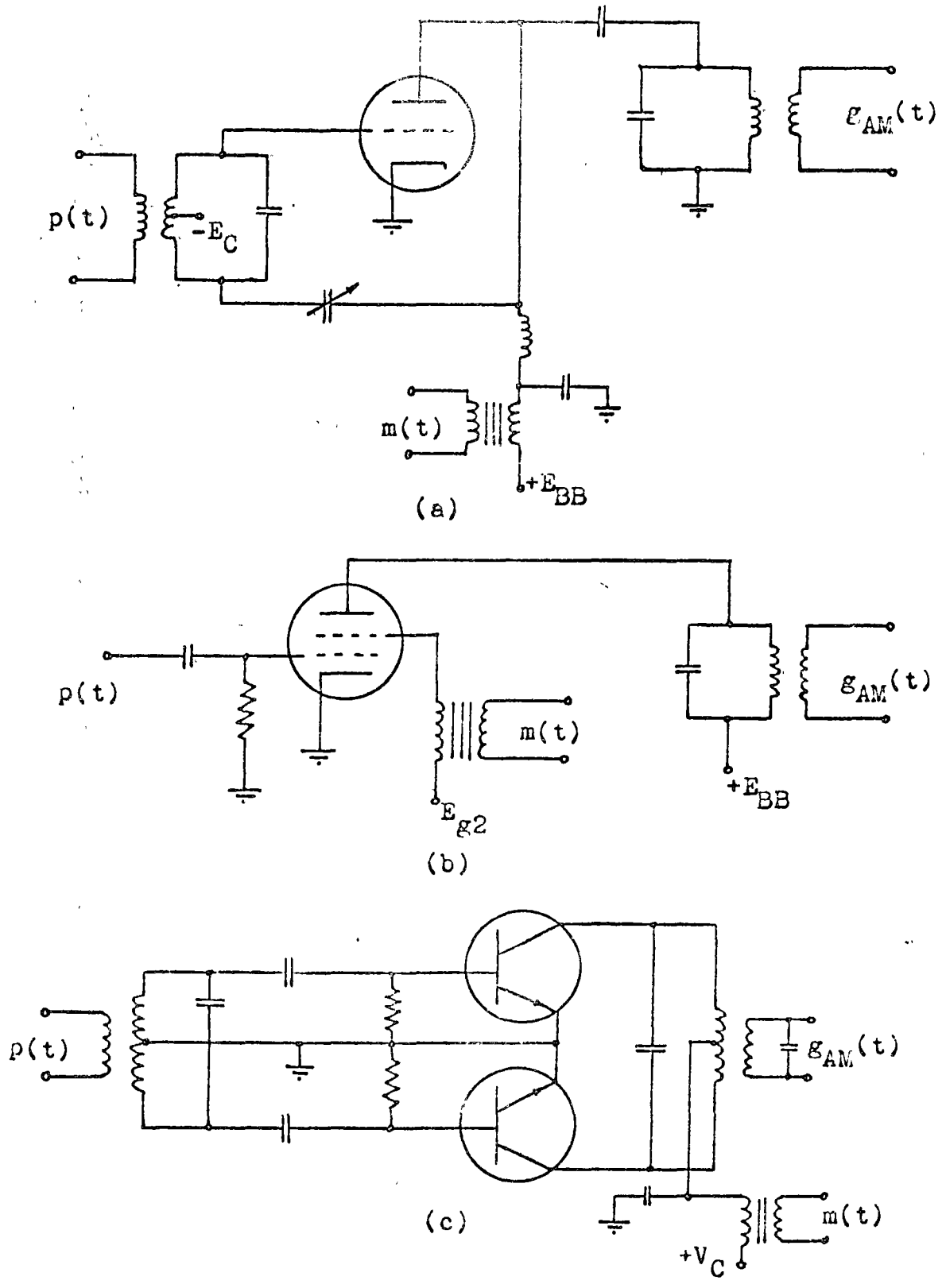

Fig. 2.4 a)Amplificador clase C con triodo modulado en placa, b) Amplificador clase C con tetrodo modulado en pantalla, c) Amplificador transistorizado clase C modulado en colector.

remedia si se utiliza amplificadores no lineales del tipo clase C, con lo que se gana eficiencia en la conversión de potencia y se pueden obtener índices de modulación mayores. La Fig. 2.4 muestra algunos de estos moduladores.

En cuanto a la demodulación, el circuito de la Fig. 2.5 muestra el denominado demodulador de envolvente. En esta figura se aprecia claramente la operación, la que consiste básicamente en la reconstrucción de la información a partir de los pulsos rectificados por el diodo. Para óptima operación se requiere que la frecuencia de la portadora sea muy superior a la frecuencia máxima de la información (lo que ocurre generalmente en la práctica) y que la constante de tiempo RC sea adecuadamente elegida. Como se aprecia en la Fig. 2.5, un valor alto de dicha constante produce una distorsión en m(t), mientras que un valor pequeño no permite una adecuada demodulación.

Moduladores de Conmutación

Uno o una red de diodos rectificadores pueden utilizarse para producir la modulación o la demodulación de una señal de AM. La característica no lineal de los diodos permite la generación de armónicas de la mezcla de señales portadora y moduladora, con lo que se produce el traslado en frecuencia de m(t).

En la Fig. 2.6 se observa un modulador con un simple diodo, cuyo funcionamiento se explica fácilmente al considerar que el diodo produce una conmutación a la frecuencia de la portadora, o sea, es un interruptor que se abre cuando $p(t) < 0$ y se cierra cuando $p(t) > 0$. esto equivale a multiplicar la suma $m(t) + p(t)$

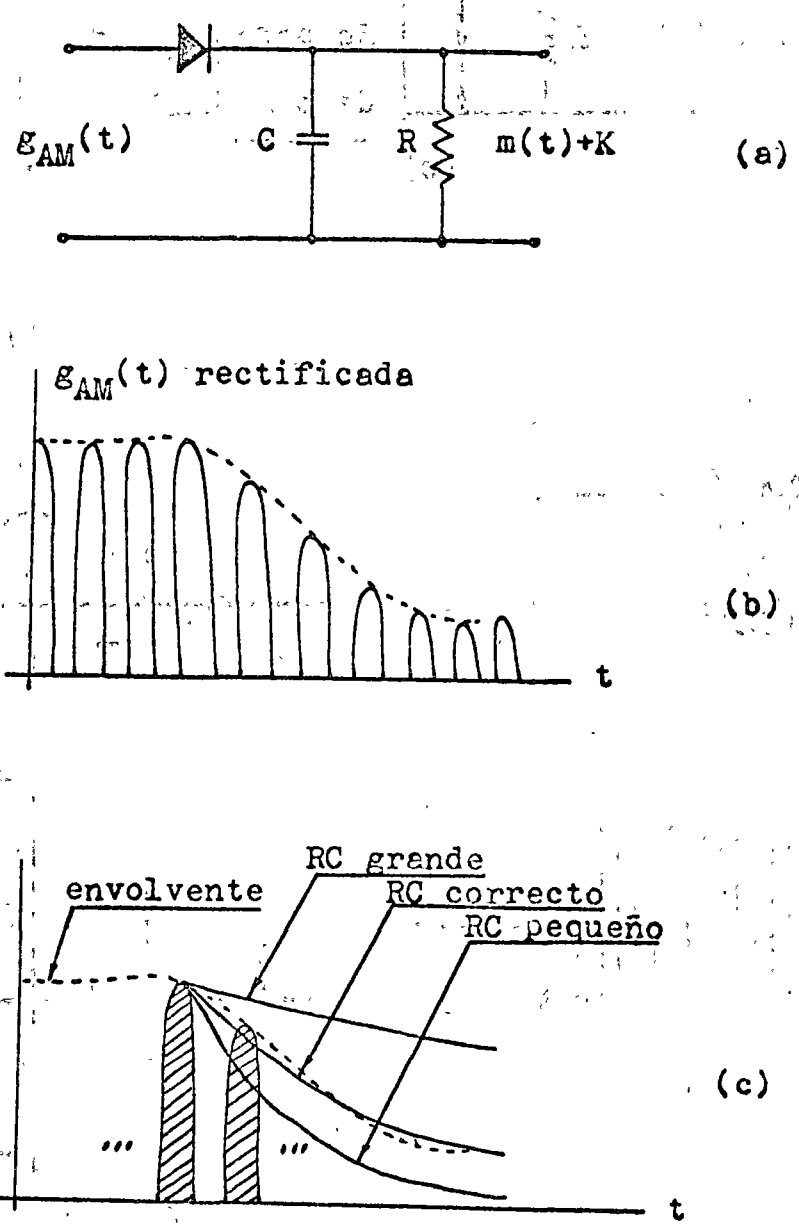

Fig. 2.5 Detector de envolvente a) Circuito, b) forma de onda, c) efecto de la constante de tiempo RC en la reconstrucción de la señal m(t).

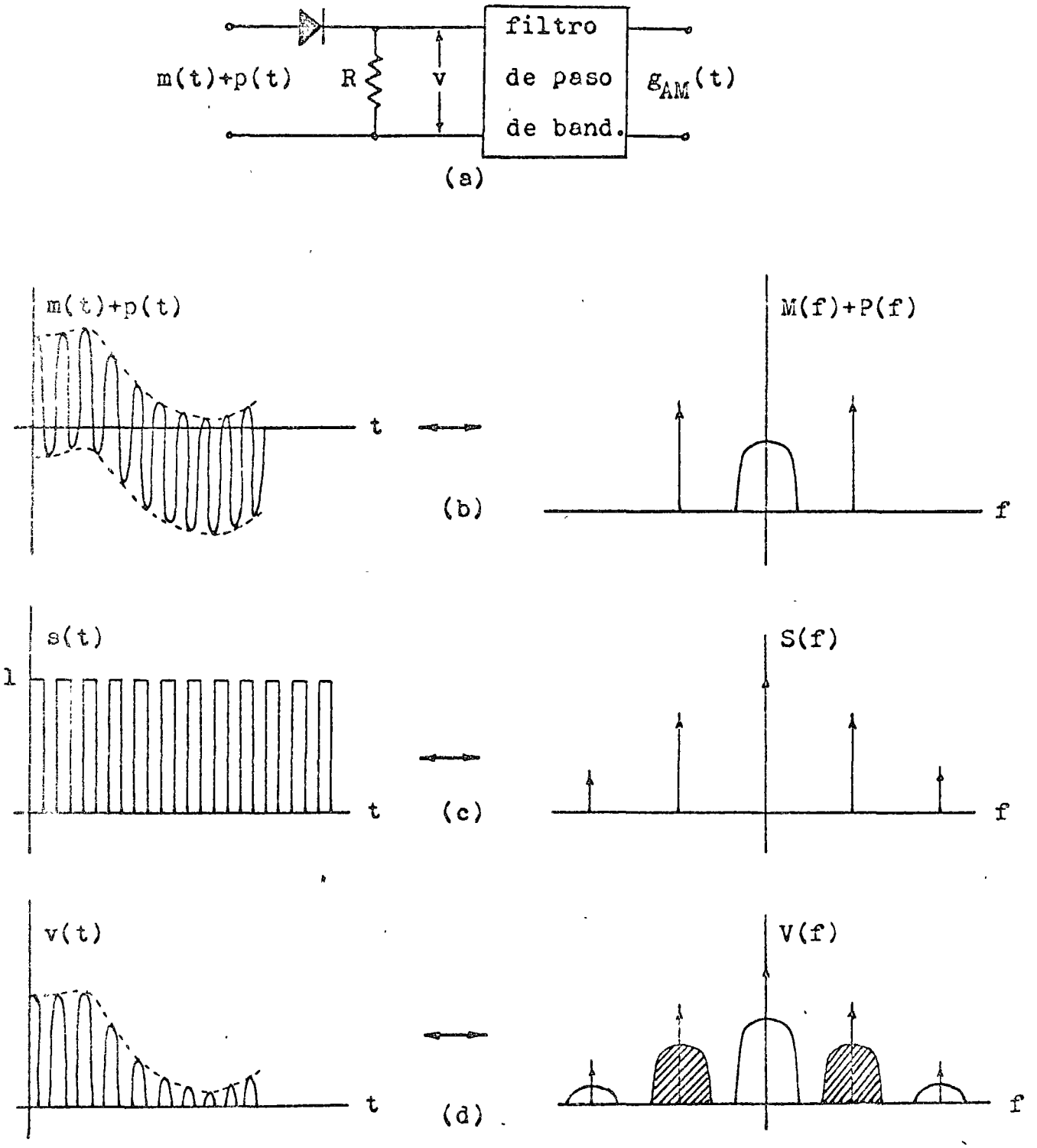

Fig. 2.6 Modulador de conmutación con diodo. a) Circuito, b) portadora, moduladora y espectro de ambas, c) la señal de conmutación, d) señal resultante y espectro.

por una señal cuadrada de frecuencia igual a la de p(t) y que oscila entre 0 y 1. El espectro de la señal resultante contiene una portadora y dos bandas laterales, las que se separan del resto mediante un filtro de paso de banda.

Modulador Cuadrático

Si se dispone de una red no lineal cuya característica pueda describirse aproximadamente en la forma (ver Fig. 2.7)

$$y(t) = a\,x(t) + b\,x^2(t) \qquad (2.9)$$

se tendrá un dispositivo que producirá armónicas de la señal de entrada x(t). Si se considera que

$$x(t) = m(t) + p(t) \qquad (2.10)$$

entonces

$$y(t) = \frac{b}{2} + am(t) + bm^2(t) + \left[a + 2bm(t)\right]\cos\omega_0 t + \frac{b}{2}\cos 2\omega_0 t \qquad (2.11)$$

Esta última ecuación contiene la señal de AM dada por el cuarto término*

$$g_{AM}(t) = 2b\left(\frac{a}{2b} + m(t)\right)\cos\omega_0 t \qquad (2.12)$$

*Hay que hacer notar que, como a/2b puede ser una constante pequeña, se tiene un mejor resultado si se agrega una constante K a la ecuación (2.10)

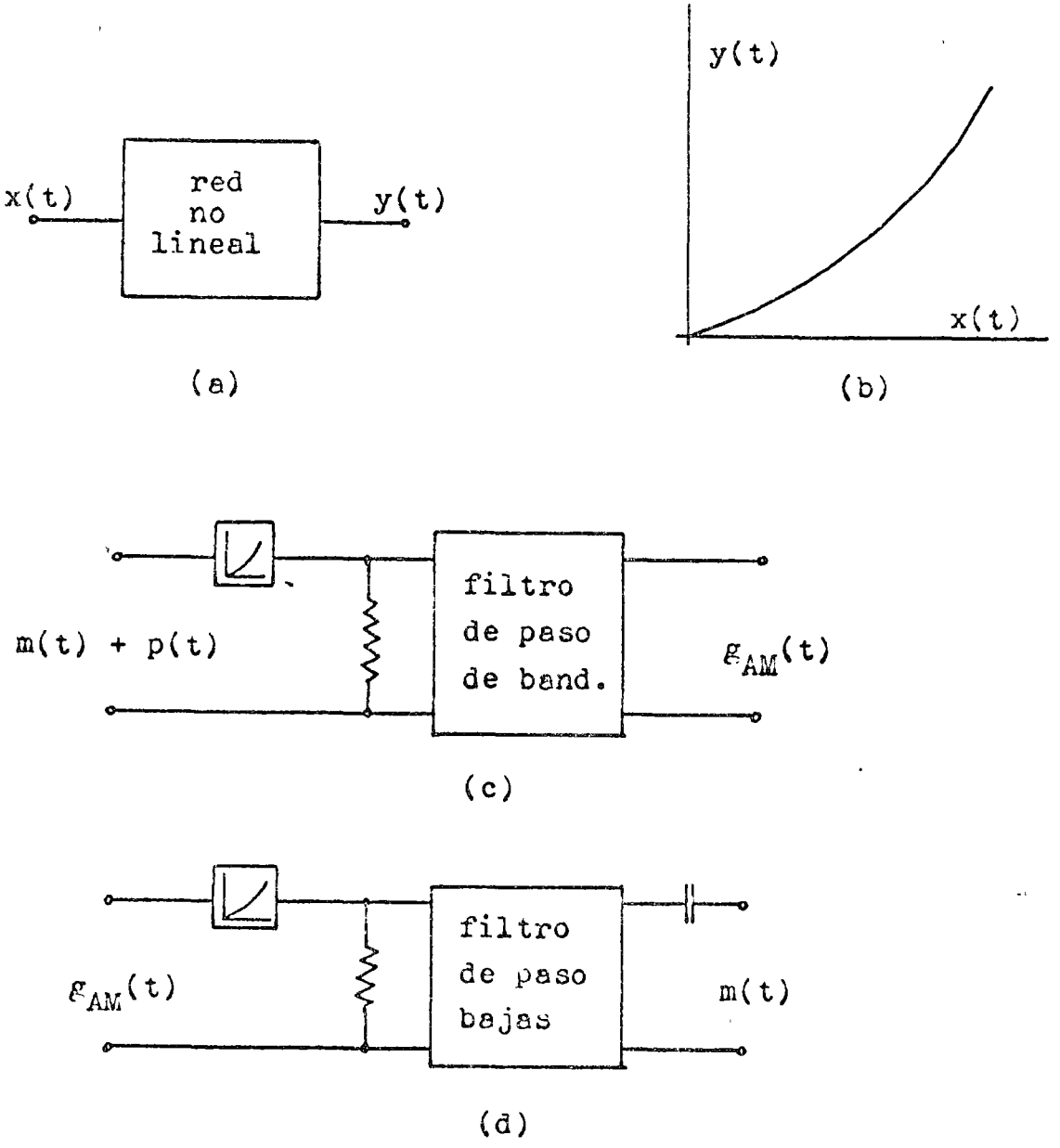

Fig. 2.7 Modulación cuadrática a) Sistema no lineal, b) característica, c) modulador cuadrático, d) demodulador cuadrático.

Los demás términos de la ecuación (2.11) se eliminan con un filtro de paso de banda.

Puede demostrarse fácilmente que el circuito cuadrático puede usarse como demodulador bajo ciertas condiciones que implican una eficiencia más pobre, por lo que su uso es muy restringido.

Por otra parte, como cualquier red no lineal permite realizar este tipo de modulador, un problema interesante es encontrar el dispositivo que permita un máximo aprovechamiento de los niveles de potencia de entrada y salida.

2.1.2 Doble Banda Lateral (DSB)

La baja eficiencia de AM implica que gran parte de la potencia de la señal modulada no sea aprovechable, lo que constituye un desperdicio. Una manera de mejorar esta situación es por medio de la modulación en doble banda lateral, ya que en este caso la señal modulada no tiene componentes de la portadora. La Fig. 2.8 muestra como se realiza la modulación y demodulación en DSB, la que consiste básicamente en un sistema de AM que no cumple con la ecuación (2.4), ya que se tiene K=0, o sea,

$$g_{DSB}(t) = A_p m(t)\cos\omega_o t \qquad (2.13)$$

Esta vez resulta que la eficiencia es de 100%, según la ecuación (2.5) y debido a que $g_{DSB}(t)$ es directamente proporcional a m(t). Además, el espectro de la señal modulada está dado por

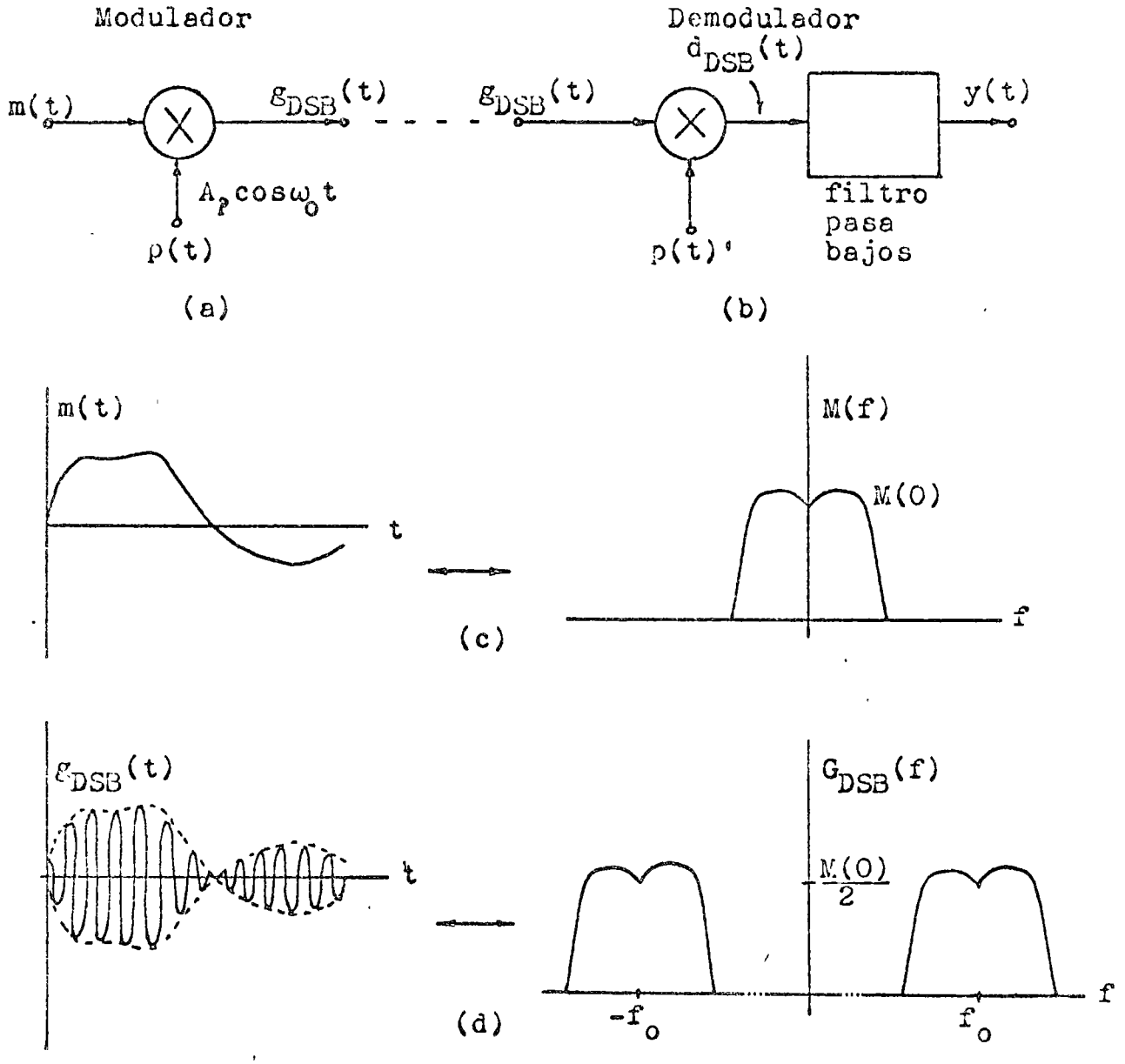

Fig. 2.8 Modulación y demodulación en DSB a)Modulación, b) demodulación, c) señal y espectro de m(t), d) señal y espectro de DSB.

$$G_{DSB}(f) = \int_{-\infty}^{\infty} M(x)\ P(f-x)dx = M(f)*P(f) \qquad (2.14)$$

de donde se obtiene*

$$G_{DSB}(f) = \tfrac{1}{2}\left[M(f-f_o) + M(f+f_o)\right] \qquad (2.15)$$

Debe notarse que esta última ecuación puede deducirse de (2.7) si se toma K = 0, con lo cual resulta obvio que la modulación en DSB no es otra cosa que la misma modulación en AM con la portadora suprimida.

En cuanto a la demodulación debe destacarse que, debido a que la señal envolvente puede hacerse negativa, no puede utilizarse el simple proceso del demodulador de envolvente para recuperar la información, sino que es preciso recurrir nuevamente a la multiplicación para realizar el desplazamiento hacia las bajas frecuencias de los espectros trasladados de la ecuación (2.15). Además, la Fig. 2.8 indica que se debe conocer la portadora en el receptor en el momento de efectuar la demodulación. Así, si p(t)' esta dada por

$$p(t)' = 2\cos(\omega_o t + \phi(t)) \qquad (2.16)$$

entonces

$$d_{DSB}(t) = m(t)\cos\phi(t) + m(t)\cos(2\omega_o t + \phi(t)) \qquad (2.17)$$

*$A_p = 1$

de donde se obtiene a la salida del filtro, si los dos espectros componentes de (2.17) no se traslapan,

$$y(t) = m(t)\cos \phi(t) \qquad (2.18)$$

Si $\phi(t)$ es una constante, el efecto del error de fase es una atenuación de la señal $m(t)$. Esto no constituye una distorsión, sin embargo, en los sistemas reales $\phi(t)$ es variable en el tiempo en una forma desconocida y aleatoria, lo que significa que la señal de salida se distorsiona seriamente.

Esta dificultad del sistema de modulación DSB exige que en el receptor esté presente la portadora para que la demodulación pueda llevarse a cabo en forma síncrona o coherente. Hay básicamente dos maneras de obtener la señal $p(t)$ en el receptor; una, es enviando junto con $g_{DSB}(t)$ una portadora de baja potencia, la que puede aislarse antes de demodular mediante un filtro de paso de banda muy estrecho, y la otra consiste en elevar al cuadrado la señal de DSB recibida, entonces

$$g^2_{DSB}(t) = \tfrac{1}{2}m^2(t) + \tfrac{1}{2}m^2(t)\cos 2\omega_o t \qquad (2.19)$$

El segundo término de (2.19) contiene una componente discreta en $2\omega_o$, (ya que $m^2(t)$ tiene una componente continua), la que puede extraerse del espectro de $g^2_{DSB}(t)$ mediante un filtro estrecho de paso de banda y usarse para demodular si se divide en frecuencia por dos

Moduladores de DSB

La señal de DSB puede conseguirse en la práctica por metodos similares a los de AM, sin embargo, debe procurarse que la portadora sea efectivamente suprimida. Este tipo de moduladores (y de moduladores) se denominan balanceados debido a que un apropiado balance del circuito permite minimizar el contenido de portadora de la señal resultante.

Los moduladores de DSB pueden clasificarse en

a) Moduladores de conmutación

b) Moduladores cuadráticos.

Estos circuitos permiten realizar también la demodulación, si a la entrada se introduce la señal $g_{DSB}(t)$. Sin embargo este proceso puede llevarse a efecto por medio del método de reinserción de portadora, que consiste básicamente en agregar el término que falta en la ecuación (2.13) para transformar la señal de DSB en una de AM y demodular con un detector de envolvente. Un método más elaborado, denominado Lazo de Amarre de Fase (PLL) de Costas, será analizado más adelante.

Moduladores de Conmutación

Este tipo de moduladores se implementa en la forma de un modulador balanceado que produce el efecto de una multiplicación entre la información y una señal cuadrada de frecuencia ω_o. Este resultado se obtiene por medio de diodos que conducen o se cortan gobernados por la frecuencia de la portadora p(t). En la Fig. 2.9 se aprecia un circuito puente de diodos que permite o impide la conducción entre los puntos a y b, de acuerdo a la señal p(t). Es

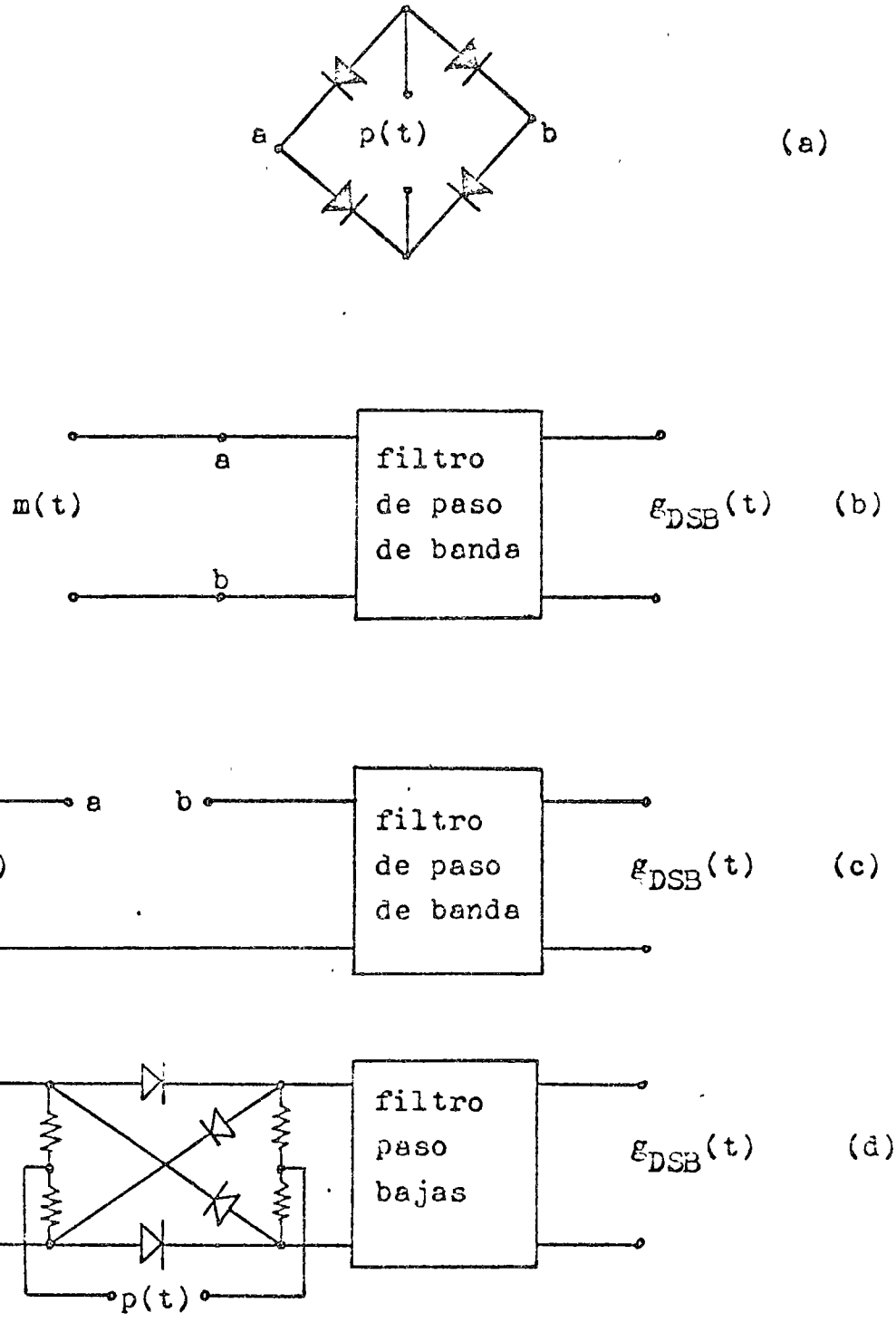

Fig. 2.9 Moduladores y demoduladores balanceados de DSB a) Circuito conmutador, b) Modulador paralelo, c) Modulador serie, d) Modulador doble balanceado.

te circuito genera la referida multiplicación si se sitúa adecuadamente en serie o en paralelo con la información, segun se observa en esta misma figura.

La multiplicación de la información con la señal cuadrada genera una serie de armónicas que se eliminan con un filtro de paso de banda adecuado. Ya que la señal cuadrada contiene una componente en ω_o y armonicas en $n\omega_o$, el efecto de la multiplicación es producir una señal de DSB centrada en cada una de estas frecuencias.

El modulador de la Fig. 2.9 (d) difiere de los anteriores en el hecho que en aquéllos la señal cuadrada varía entre 0 y 1, mientras que en este último lo hace entre +1 y -1. En esta forma, el espectro de la señal resultante no contiene componentes de m(t), por lo que un filtro pasabajas es suficiente para aislar $g_{DSB}(t)$.

Moduladores cuadráticos

Puesto que un modulador cuadrático permite obtener AM, es fácil suponer que balanceando este tipo de moduladores puede eliminarse la componente de portadora del espectro resultante, con lo que la señal de DSB se obtiene en la salida. Un modulador típico aparece en la Fig. 2.10 y su funcionamiento consiste básicamente en que las componentes de p(t) de ambas ramas tienden a cancelarse, mientras que las componentes de las bandas laterales se refuerzan. Cuando este circuito se balancea adecuadamente su salida es $g_{DSB}(t)$.

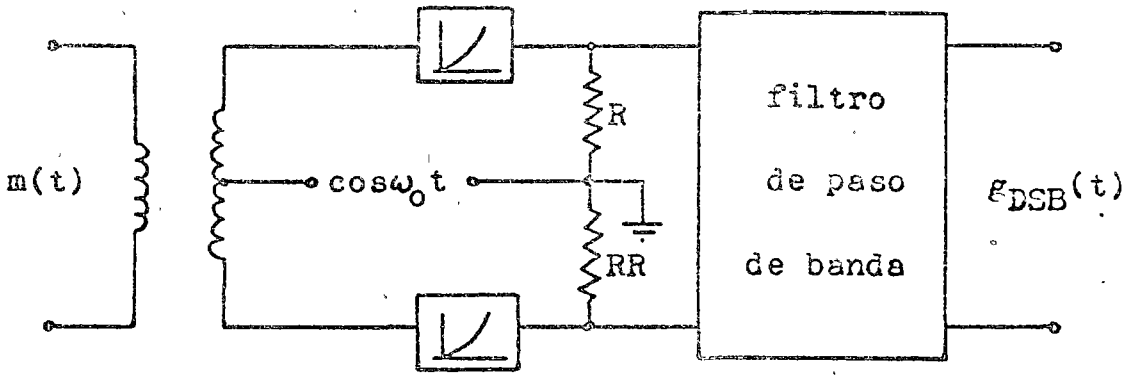

Fig. 2.10 Modulador cuadrático balanceado

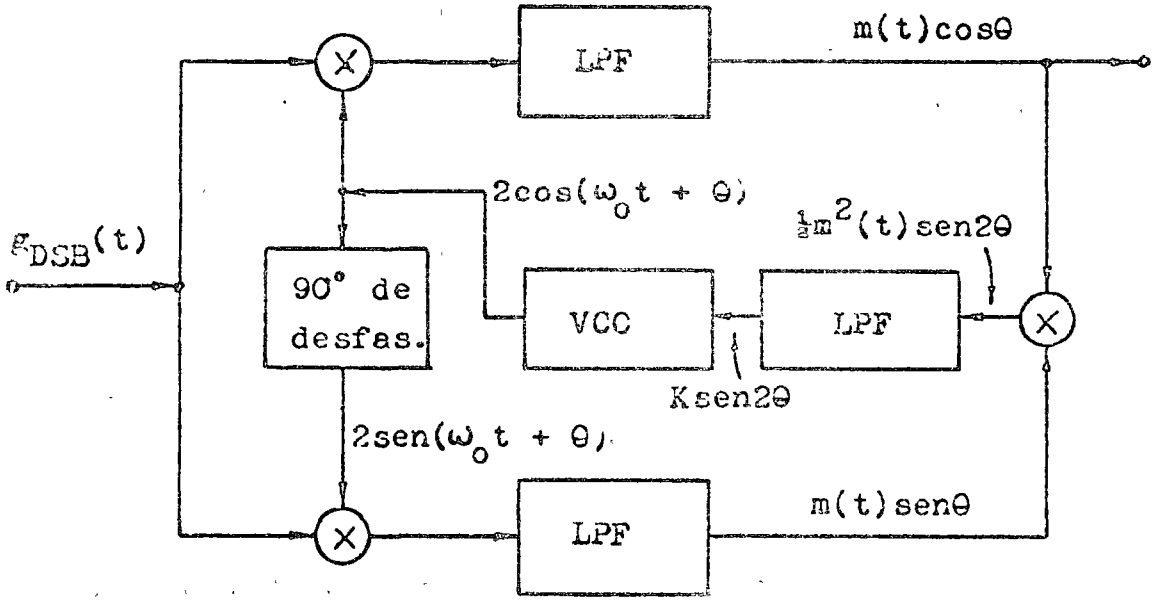

Fig. 2.11 El demodulador PLL de Costas. LPF = Filtro de paso bajas. VCO = Oscilador controlado por voltaje.

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Moduladores cuadráticos

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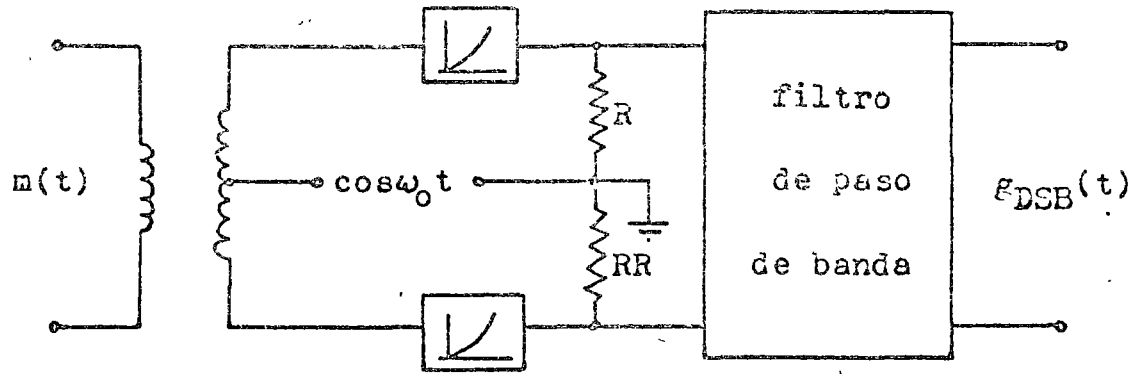


Fig. 2.10 Modulador cuadrático balanceado

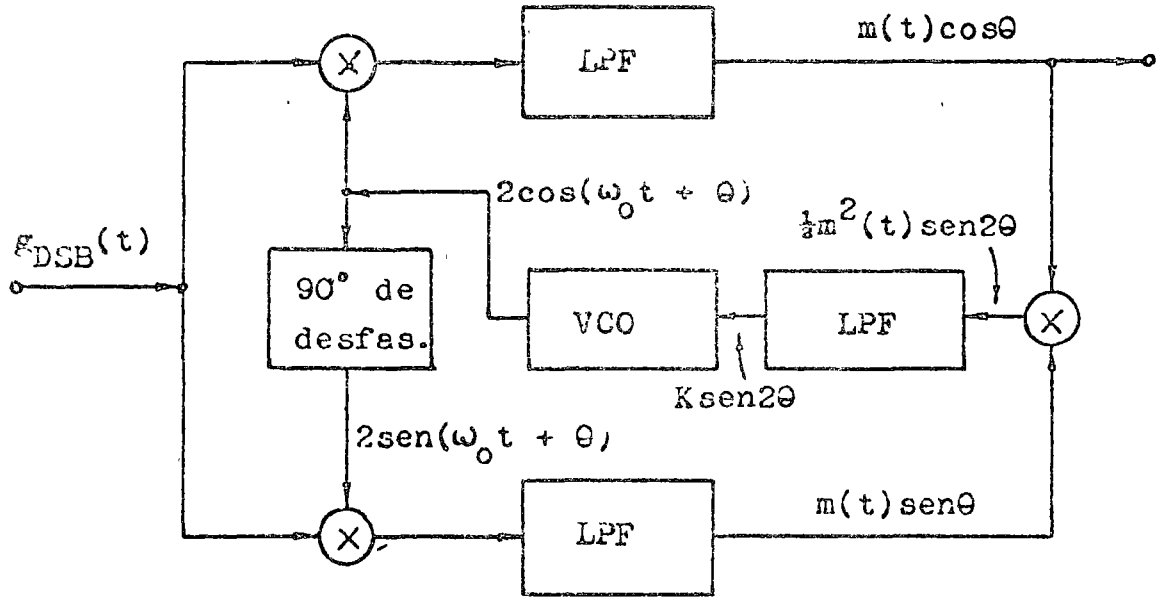


Fig. 2.11 El demodulador PLL de Costas. LPF = Filtro de paso bajas. VCO = Oscilador controlado por voltaje.

La Reinserción de Portadora y otros Métodos

Es evidente que si a la ecuación (2.13) se le agrega el término $A_p K \cos\omega_o t$, se obtiene la ecuación (2.3) que puede demodularse con los detectores conocidos de AM. En este caso, debe cuidarse la obtención de la señal portadora mediante alguno de los métodos ya mencionados y que cumpla con los requisitos de amplitud (ecuación (2.4)) y fase, para que la señal de AM generada pueda detectarse sin distorsión. Este método se denomina demodulación con reinserción de portadora.

Otro método es el que muestra la Fig. 2.11 y se denomina demodulador Lazo de Amarre de Fase de Costas. En este caso se obtiene la señal m(t) para un valor pequeño de Ø. El diagrama de bloques permite conocer las señales en cada punto a partir de la entrada del demodulador y la salida del oscilador controlado por voltaje (VCO).

2.2 Moduladores Angulares

La información m(t) puede incluirse también en el angulo $\theta = \omega_o t + \phi$ de la señal de la ecuación (2.1) en forma analógica y proporcional. En esta forma, se tiene dos posibilidades para realizar esta operación; una, es variando de acuerdo a m(t) la frecuencia ω_o, y la otra es realizando dicha variacion en la fase ϕ. Así, se producen los dos tipos más comunes de modulación angular: Frecuencia Modulada (FM) y Fase Modulada (PM). Durante estos dos procesos, la amplitud de la portadora permanece constante, mientras que el ángulo instantáneo de la portadora es

$$\theta_i(t) = \omega_o t + \phi(t), \qquad \omega_o \text{ constante} \tag{2.20}$$

y la frecuencia instantánea

$$_i(t) = \frac{d}{dt}\theta_i = \omega_o + \frac{d}{dt}\phi, \qquad \omega_o \text{ constante} \tag{2.21}$$

Según estos dos últimos resultados, la variación instantánea de fase y frecuencia en forma proporcional a m(t) puede efectuarse mediante los parámetros desviación de fase y desviación de frecuencia en la siguiente forma

$$\phi(t) = k_p m(t) \tag{2.22a}$$

$$\frac{d}{dt}\phi = k_f m(t) \tag{2.22b}$$

donde k_p y k_f son las constantes de desviación de fase y frecuen-

cia, respectivamente. Según lo anterior, las señales moduladas están dadas por

$$g_{PM}(t) = A_p \cos\left[\omega_o t + k_p m(t)\right] \qquad (2.23a)$$

$$g_{FM}(t) = A_p \cos\left[\omega_o t + k_f \int m(t)dt\right] \qquad (2.23b)$$

Debe notarse que la integral no tiene límites debido a que la condición inicial de fase no es importante. Por otra parte, en las ec. (2.23) se aprecia que, ya sea que se module en fase o en frecuencia, el resultado siempre puede interpretarse como una variación de $\phi(t)$ en forma proporcional a $m(t)$ o a la integral de $m(t)$. Esto permite concebir que aunque se trata de dos sistemas diferentes, existe una importante similitud entre ambos.

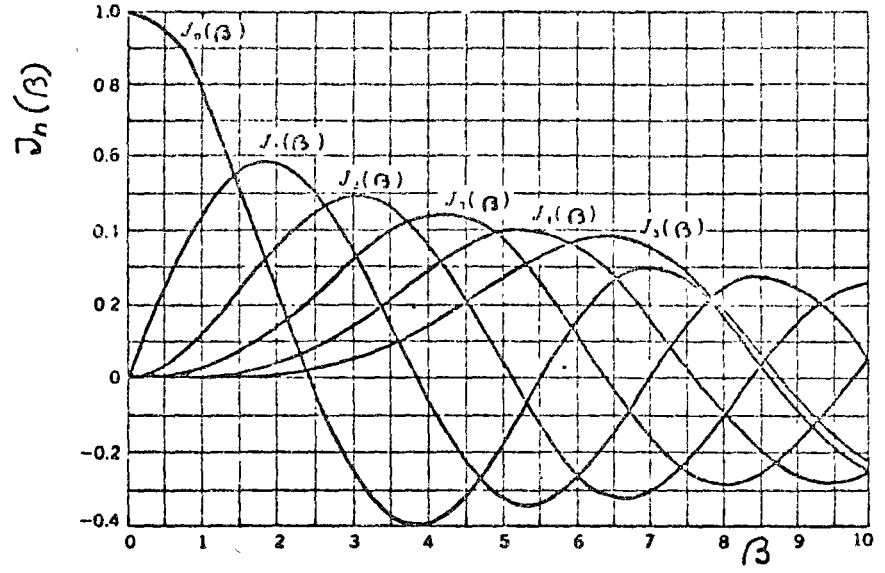
Espectro de la Señal Modulada en Angulo

Obtener el espectro de una señal de FM o PM cualquiera es normalmente un problema difícil, sin embargo, puede realizarse una evaluación interesante si se considera una moduladora senoidal. Se tomará para PM, $m(t) = k_p \operatorname{sen} \omega_o t$ y para FM, $m(t) = k_f \cos\omega_o t$ definiendo $\beta_{PM} = k_p$ y $\beta_{FM} = k_f/\omega_m$, se tiene

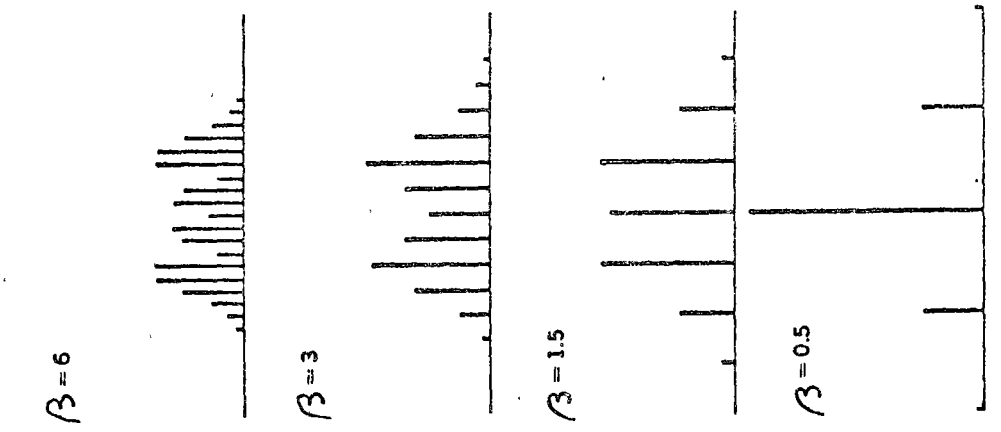
$$g(t) = A_p \cos\left[\omega_o t + \beta \operatorname{sen} \omega_m t\right] \qquad (2.24)$$

Esta expresión puede descomponerse en la siguiente forma

$$g(t) = A_p \sum_{n=-\infty}^{\infty} J_n(\beta) \cos(\omega_o + n\omega_m t) \qquad (2.25)$$



(a)



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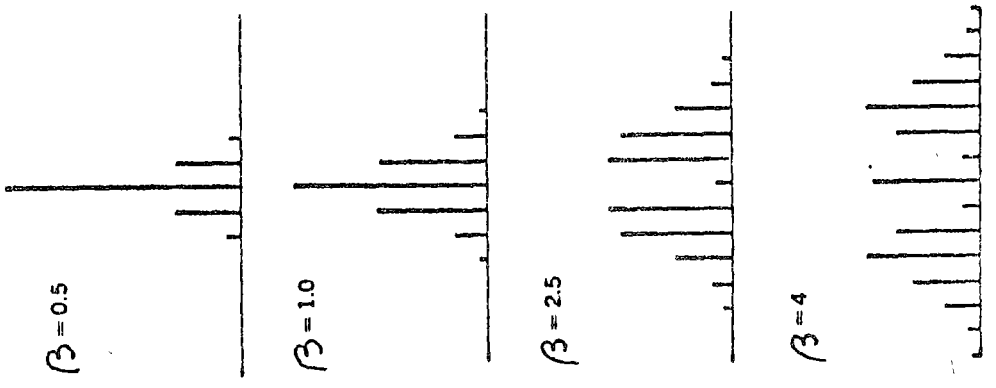


(c)

Fig. 2.12 a) Funciones de Bessel, b) espectro de FM con desviación máxima constante y frecuencia de modulación (ω_m) variable, c) espectro de FM con desviación máxima variable y ω_m constante. Estos dos últimos efectos se ilustran para diferentes índices de modulación, β.

donde $J_n(\beta)$ son las funciones de Bessel de primera clase y orden n, las que aparecen en la Fig. 2.12.

La ecuación (2.25) indica que existen infinitas bandas laterales para una moduladora senoidal, separadas de la portadora por un número entero de veces la frecuencia de la moduladora, ω_m. La amplitud de estas bandas laterales determinará el ancho de banda BW, de la señal resultante (ya que los $J_n(\beta)$ tienden a cero cuando n tiende a infinito), pero como dicha amplitud esta dada precisamente por $J_n(\beta)$, el ancho de banda será una función de β. Cabe hacer notar que para una señal de FM el ancho de banda se mantiene aproximadamente constante, ya que si en la ecuación (2.25) se incrementa ω_m, el espaciamiento de las bandas laterales aumenta al mismo tiempo que β disminuye. Este efecto no se produce en PM, ya que β_{PM} es constante y el espaciamiento producido por un incremento de ω_m hace aumentar efectivamente el ancho de banda mínimo necesario.

Una regla generalmente aceptada para determinar BW en una señal de FM es la conocida como regla de Carson

$$BW = 2(\beta + 1)\omega_m \qquad (2.26)$$

Esta expresión es válida solo para la modulación senoidal, ya que $\beta = k_f/\omega_m$ esta definido para este tipo de señales, sin embargo su validez puede extenderse a señales arbitrarias al definir la razón de desviación, D, en la siguiente forma

$$D = \frac{\text{máxima desviación en frecuencia}}{\text{ancho de banda de } m(t) = B} \qquad (2.27)$$

y entonces se tiene

$$BW = 2(D + 1)\, B \qquad (2.28)$$

Nótese que si $D \ll 1$, el ancho de banda $BW = 2B$ y la señal se denomina FM de banda angosta. Por otra parte, si $D \gg 1$, la señal se llama FM de banda ancha y $BW = 2DB$.

El análisis espectral realizado para la modulación angular, considera que la señal m(t) es solamente una senoidal. Si se toma m(t) como una suma ponderada de señales senoidales puede encontrarse que el resultado contiene las bandas laterales generadas por cada una de las senoidales componentes de la suma, más todas las combinaciones posibles entre ellas (o sea, las frecuencias dadas por $\omega_o + n_1\omega_1 + n_2\omega_2 + \ldots$, con $n_1, n_2, \ldots$ enteros). Este fenómeno de generación de bandas laterales por combinación o cruce es exclusivo de la modulación angular, motivo por el cual se dice que esta modulación es no lineal.

2.2.1 Frecuencia Modulada (FM)

La señal de Frecuencia Modulada está dada por la ecuación (2.23b) y puede notarse que aunque en ella se ha hecho variar con m(t) la frecuencia, el resultado es una variación en la fase con la integral de m(t). Esta propiedad permite obtener las dos seña-

les de la ecuación (2.23) con el mismo modulador y demodularlas en la misma forma, siempre y cuando se realicen previamente las operaciones de integrar o diferenciar. Por esto se hará incapié en los sistemas de FM, que por las razones ya vistas del ancho de banda es la más utilizada.

Moduladores de FM

Debido a que en FM la fase de la señal es $k_p \int m(t)\, dt$ y en PM, $k_p\, m(t)$, según las ecuaciones (2.23), la relación que existe entre estos dos tipos de modulacion es muy estrecho. Si se integra la información y se modula en fase, el resultado es una modulación en frecuencia; por el contrario, si se diferencia la señal m(t) y posteriormente se modula en frecuencia, el resultado es una señal modulada en fase.

Esta razón permite generar FM de dos maneras fundamentales

a) Modulación directa,

b) Modulación indirecta.

La primera de ellas consiste en variar, de acuerdo a m(t), uno de los parámetros de los circuitos sintonizados que se utilizan en un oscilador, por ejemplo, si L y C son la inductancia y la capacidad del circuito, la frecuencia de resonancia ω_r es

$$\omega_r = \frac{1}{\sqrt{LC}} \qquad (2\text{-}29)$$

entonces, una pequeña variación en L ó C produce una variación aproximadamente lineal en ω_r y por tanto en la frecuencia de oscilación del oscilador.

Algunos moduladores de este tipo son

i) De diodo varactor,

ii) De reactor saturable,

iii) De reactancia (transistor o válvula de vacio)

La segunda manera de generar FM consiste en integrar la información y posteriormente modular en fase.

En cuanto a los demoduladores, éstos producen una salida proporcional a la frecuencia de la señal de FM, con lo que transforman FM en AM. Este tipo de demoduladores se denominan discriminadores y su funcionamiento se explica fácilmente si se considera que son circuitos con una característica muy lineal alrededor de la frecuencia ω_o y con una pendiente mayor que cero. Un dispositivo de esta naturaleza se observa en la Fig. 2.13.

Otros demoduladores son el discriminador Lazo de Amarre de Fase (PLL), cuya principal característica es su eficiencia bajo condiciones de señal débil, y el discriminador de promedio de pulso, cuya función es convertir la señal de FM en un tren de pulsos de duración constante y período dependiente de la frecuencia instantánea de $g_{FM}(t)$. Evidentemente, el promedio de estos pulsos es la información m(t).

El discriminador PLL aparece en la Fig. 2.14, donde se observa que el detector de fase determina la señal error de fase entre la entrada y la salida del VCO. Esta señal, después de ser amplificada y filtrada tiende a reducir el error al variar la frecuencia del VCO. Puesto que este error de fase es producto de la modu

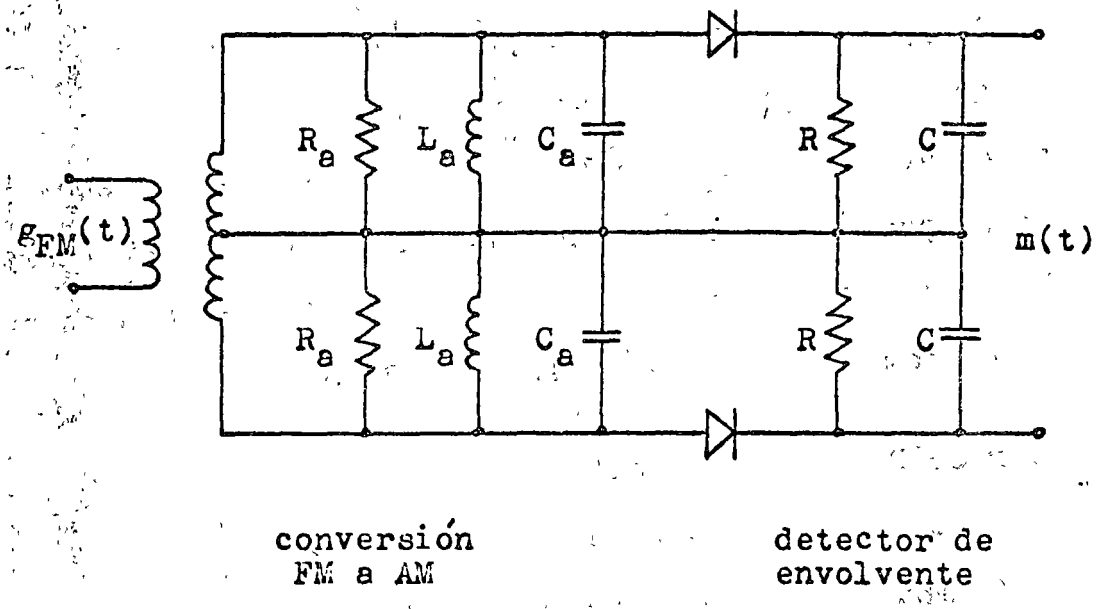


Fig. 2.13 Discriminador por conversión de FM a AM. Este demodulador es balanceado, de modo que la salida del circuito superior e inferior se refuerzan en la salida.

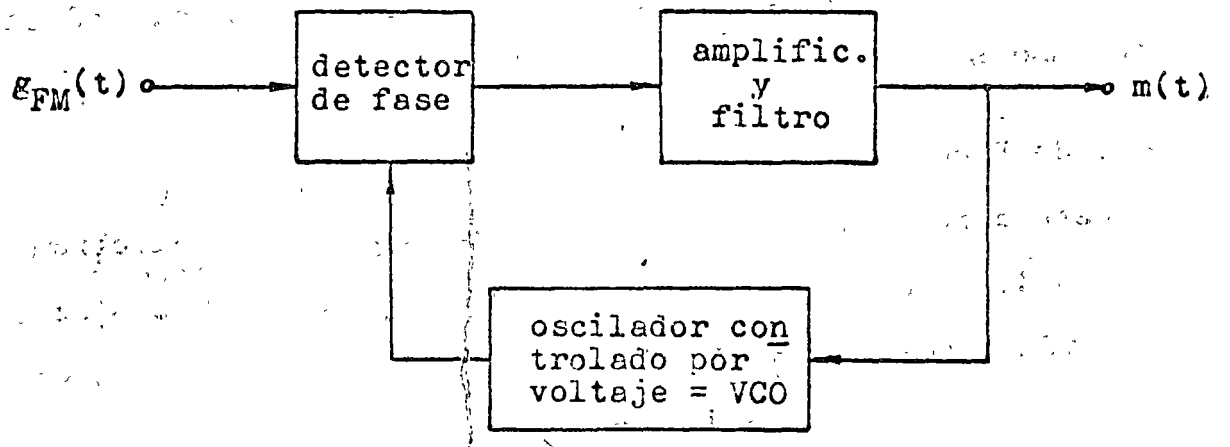


Fig. 2.14 Discriminador de Lazo de Amarre de Fase (PLL)

lación, la salida del filtro es m(t).

Modulador de Diodo Varactor

La variación de capacidad que se mencionara anteriormente, se consigue en la práctica con un diodo varactor, el cual tiene una capacidad que depende del voltaje entre sus extremos. Así, la señal m(t) producirá variaciones en la capacidad intrínsica del diodo, la que puede aprovecharse para modificar la sintonía de un oscilador, como se muestra en la Fig. 2.15.

Modulador de Reactor Saturable

Así como la señal m(t) modifica la capacidad del diodo varactor, puede modificarse la inductancia de un reactor saturable, lo que permite producir una variación similar en la inductancia del circuito sintonizado del oscilador, como se indica en la Fig. 2.16. Esta forma de generar FM permite obtener desviaciones de frecuencia máxima grandes, lo que no se logra con los otros moduladores mencionados.

Modulador de Reactancia

En este caso se utiliza la propiedad que tienen los circuitos activos de presentar una [illegible] variable entre sus extremos de salida y que depende [illegible] de entrada m(t). En esta forma, es fácil producir variaciones [illegible] la frecuencia de oscilación de un oscilador. La Fig. 2.17 muestra un modulador de este tipo con transistores, en el que la reactancia es del tipo capacitivo. Naturalmente que es factible conseguir impedancias de salida inductivas, dependiendo del tipo de elemento que se sitúe entre co-

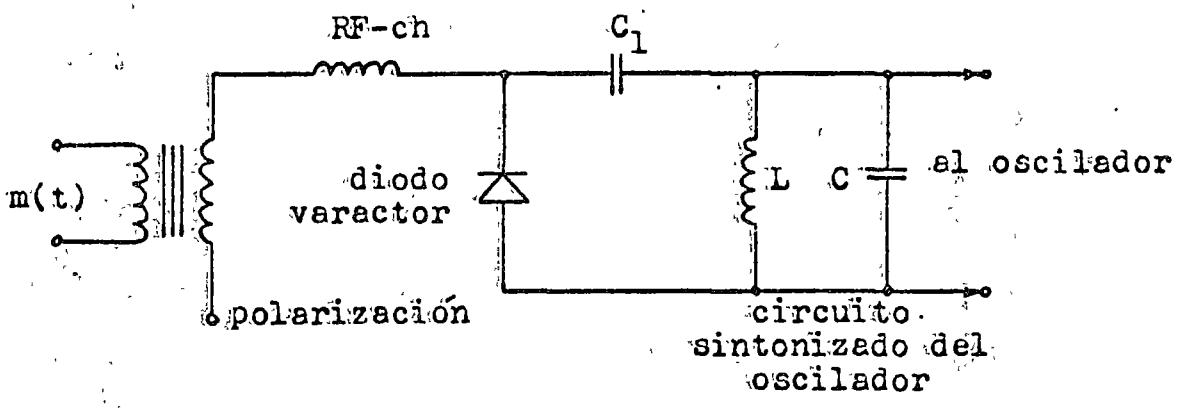


Fig. 2.15 Modulador de FM de diodo varactor.

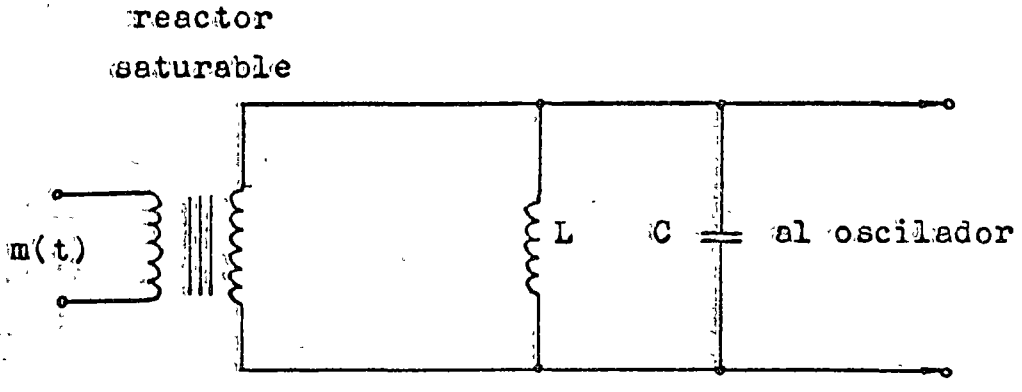


Fig. 2.16 Modulador de FM de reactor saturable

lector y base (o grilla y placa).

Cabe destacar que con este modulador y el que utiliza diodo varactor sólo se consigue FM de banda angosta, por lo que es preciso, si se desea, producir FM de banda ancha con un conversor de banda ancha, el que se analizará mas adelante.

2.2.2 Fase Modulada (PM)

Como ya se viera, la señal de PM dada por el ecuación (2.23a) no tiene un espectro que se mantenga constante como la de FM, sino que depende de la frecuencia de la señal moduladora y especialmente de las máximas componentes de ésta. Por esta razón, su uso no está muy extendido y por lo general sólo se utiliza para generar FM por el método indirecto, que ya se mencionara.

Un diagrama de bloques de este método aparece en la Fig. 2.18, donde se supone que la señal de PM es de banda angosta y que es necesario transformarla en FM de banda ancha. Puede notarse que la modulación se realiza con una portadora ya generada, en contraste con los métodos de generación de FM directos, en los cuales se modula sobre el oscilador. Por esta razón, el método indirecto de modulación de FM tiene una gran estabilidad en la señal producida, En otras palabras, las variaciones naturales en la frecuencia de los osciladores sintonizados producidas por los componentes se evitan si la portadora se genera con un oscilador de cristal. De otro modo, se requiere un circuito especial para estabilizar la señal generada.

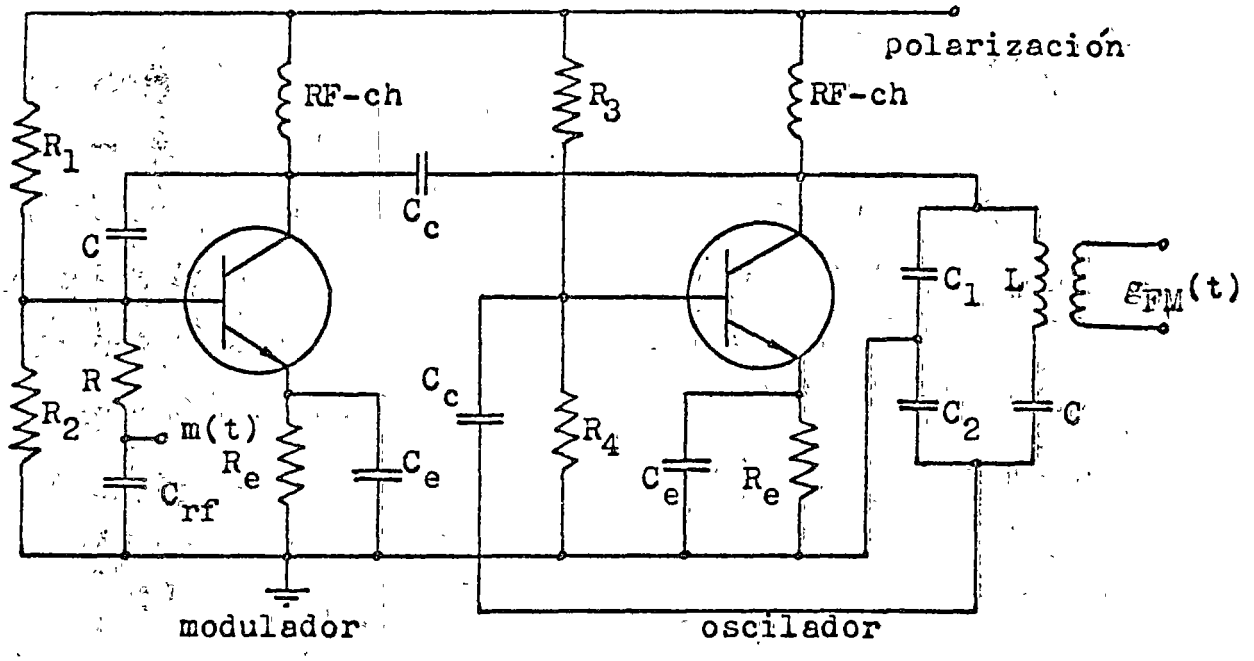


Fig. 2.17 Circuito transistorizado de un modulador de reactancia. Se compone de dos secciones: el modulador y el oscilador. Se muestran los componentes de acoplamiento y polarización.

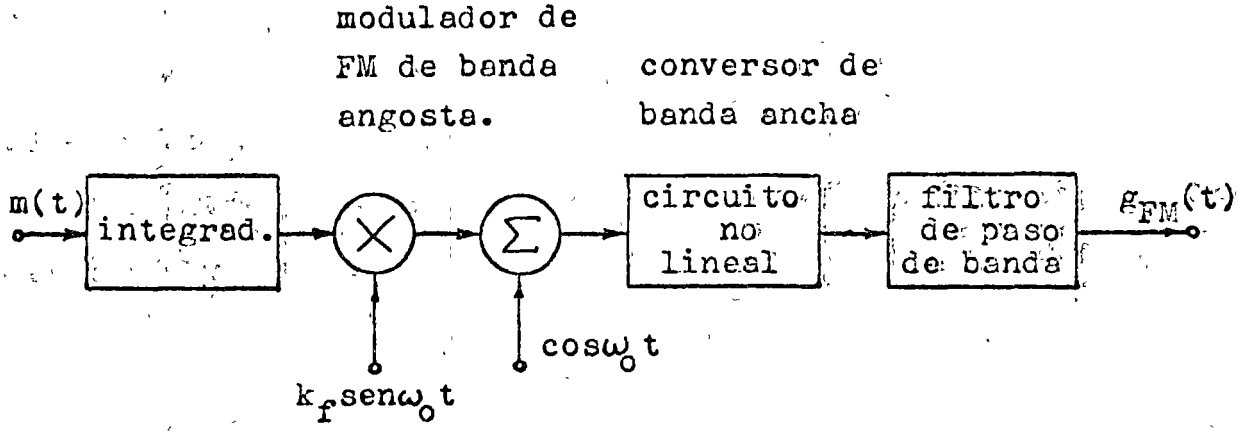


Fig. 2.18 Modulador de FM indirecto. Se emplea un modulador de fase y un conversor de banda ancha. La señal m(t) se integra previamente.

Conversión a Banda Ancha

Cuando se genera FM en forma indirecta y se produce PM de banda angosta, suele ser necesario alterar la señal obtenida para que el índice de modulación sea mayor y la desviación máxima de frecuencia sea la adecuada. Una forma de producir esta conversión a banda ancha es mediante una red no lineal que produzca el efecto de la multiplicación del ángulo de la portadora por un número entero. Las otras armónicas que aparecen en el proceso deben eliminarse con filtros pasabanda adecuados. Debido a que la multiplicación que se consigue afecta a todo el ángulo de la portadora, y por tanto, a la frecuencia; la señal de entrada debe ser una subarmónica de la señal de salida, o sea,

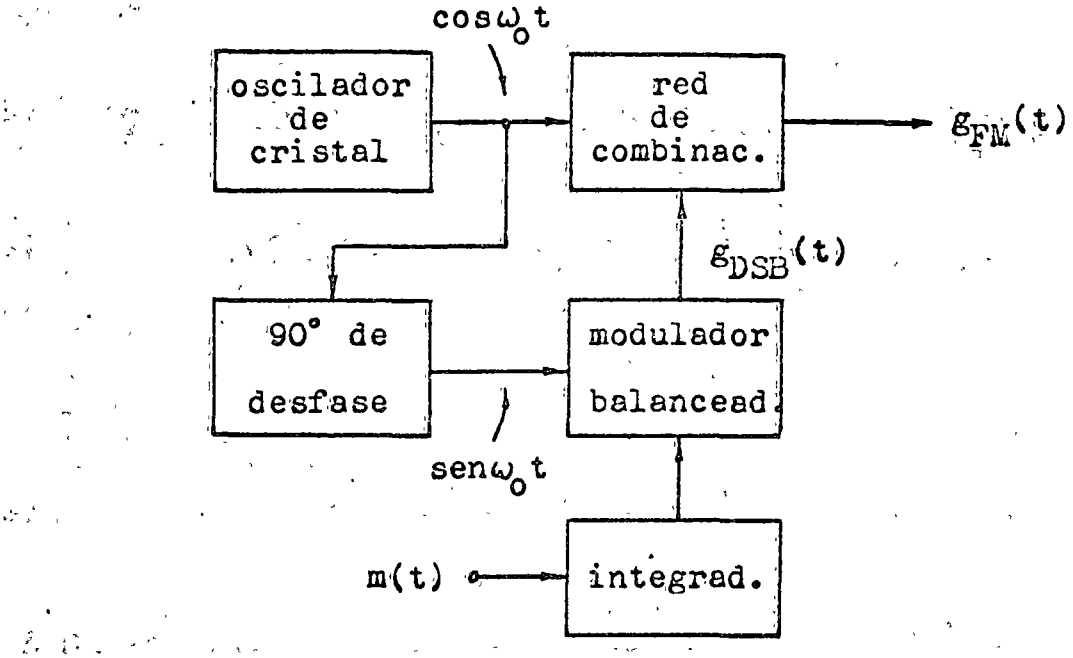
$$g_{in}(t) = A_p \cos\left(\frac{\omega_o}{n} t + k_f \int m(t)\, dt\right) \qquad (2.30)$$

$$g_{out}(t) = A_p \cos\left(\omega_o t + n k_f \int m(t)\, dt\right) \qquad (2.31)$$

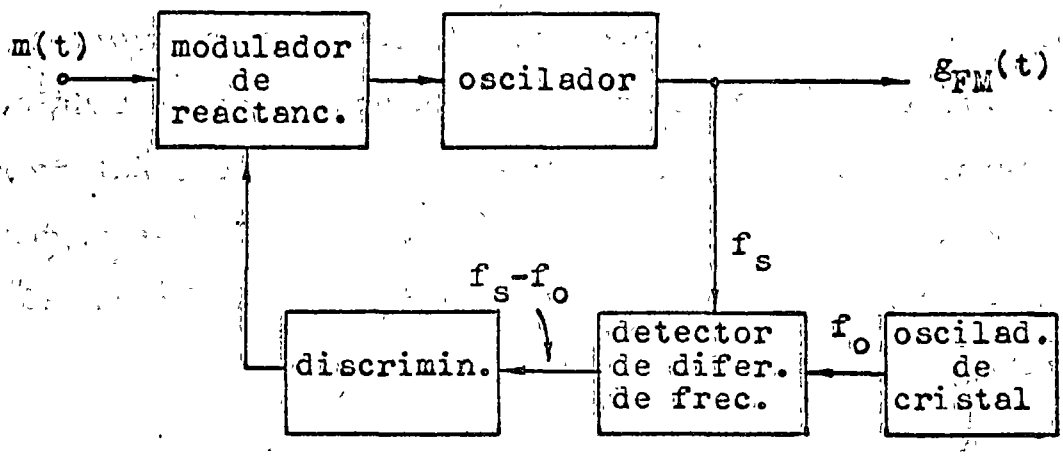
Esta última señal es de una frecuencia tan estable como lo es la frecuencia de entrada ω_o/n y su desviación en frecuencia es n veces mayor, o sea, para un n mayor que determinado valor la ecuación (2.31) describe una señal FM de banda ancha.

Modulador de Armstrong

El diagrama de bloques de este modulador aparece en la Fig. 2.19 y su funcionamiento está basado en la modulación indirecta de FM, ya que se trata en realidad de un modulador de fase.



(a)



(b)

Fig. 2.19 a)Modulador de FM de Armstrong, b) Modulador de FM de reactancia con lazo de realimentación y oscilador de cristal estabilizadores de frecuencia.

En la señal de PM de la ecuación (2.23) se tiene modulación de banda angosta si $k_p m(t)$ $\left[o\ k_f \int m(t)dt \right]$ es mucho menor que 1 para todo t. En este caso, la ecuación (2.23) puede escribirse

$$g_{FM}(t) = \mathrm{Re}\left[A_p \exp(j\omega_o + jk_f \int m(t)dt)\right] \qquad (2.32)$$

$$g_{FM}(t) = \mathrm{Re}\left[A_p \left(1 + jk_f \int m(t)dt\right) \exp(j\omega_o)\right] \qquad (2.33)$$

de donde

$$g_{FM}(t) = A_p\left[\cos\omega_o t - k_f \int m(t)dt\ \mathrm{sen}\omega_o t\right] \qquad (2.34)$$

En esta última ecuación se observa que la señal de FM de banda angosta obtenida contiene una componente de la portadora y un par de bandas laterales (DSB) con la portadora $\cos\omega_o t$ desfasada 90 grados. Este es el principio que utiliza el modulador de Armstrong para obtener PM, pero debido a que la señal moduladora es la integral de m(t), la señal resultante es una señal de FM.

Finalmente cabe hacer notar que la señal de banda angosta que se ha obtenido puede ser convertida a banda ancha por el método ya mencionado.

2.3 Multicanalización en Frecuencia (FDM)

La propiedad de traslado lineal del espectro de frecuencia de una señal dada, ya analizado en 2.1, permite deducir que espectros trasladados por diferentes señales portadoras no producirán interferencia entre ellos y aunque estén mezclados en el tiempo, pueden ser separados mediante filtros adecuados en el receptor. Un sistema como el mencionado se utiliza para trasmitir por un canal un gran número de señales de banda limitada. Esta situación es típica en telefonía, donde se tiene una gran cantidad de señales similares, las que deben ser trasmitidas ya sea por líneas de trasmisión o por el espacio.

El diagrama de bloques de un sistema de FDM se muestra en la Fig. 2.20, donde las señales individuales se modulan en AM. Evidentemente, este sistema tiene las desventajas propias de este tipo de modulación en lo referente a eficiencia. Esta situación se mejora notablemente si se modula cada señal con DSB, como se indica en la Fig. 2.20e, donde los espectros modulados no contienen componentes de las portadoras. Por último, en la figura 2.20f se observa el resultado de filtrar una de las bandas laterales de las señales de DSB. En este caso, se tiene solo una banda lateral por cada señal con lo que el ancho de banda mínimo requerido es la mitad del anterior. Este sistema de modulación se conoce como Banda Lateral Unica (SSB), y su utilización en sistemas FDM permite obtener ancho de banda mínimo con máxima eficiencia.

Banda Lateral Unica (SSB)

El uso de este metodo de modulación no esta restringido a

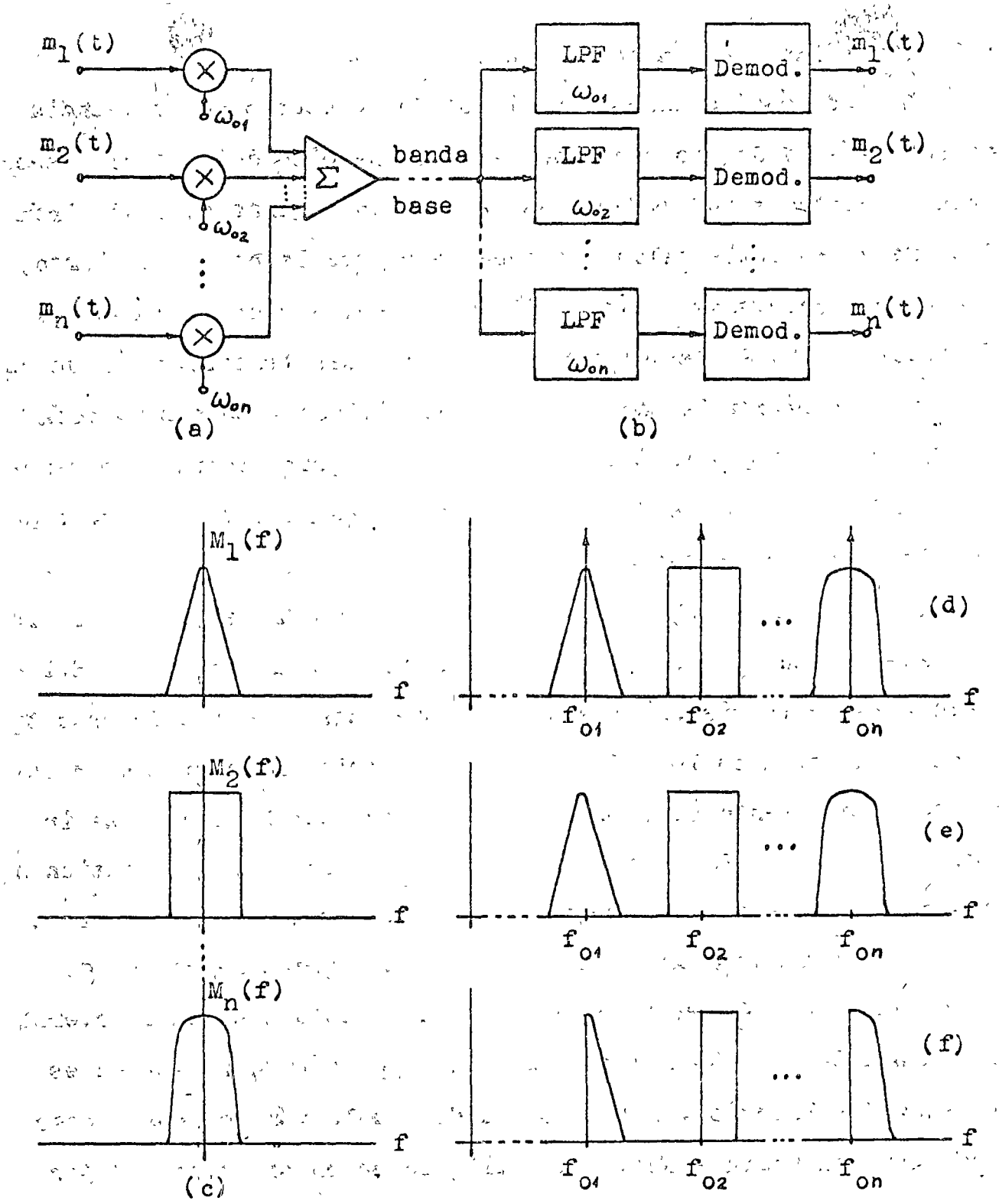


Fig. 2.20 El sistema de multicanalización por división de frecuencia. a) Modulación, b) demodulación, c) espectros de las señales componentes, d) espectro de FDM/AM, e) espectro de FDM/DSB, f) espectro de FDM/SSB.

FDM, sino que su aplicación es extensiva a todos los casos en que la eficiencia y/o el ancho de banda sean importantes. Como ya se viera, la señal de SSB puede obtenerse a partir de DSB mediante un filtro muy selectivo de paso de banda que pueda aislar adecuadamente la banda (superior o inferior) deseada, aunque existen otros métodos para generar SSB.

En cuanto a la demodulación de las señales de SSB, se obtienen buenos resultados con los mismos demoduladores coherentes utilizados en DSB.

2.4 Referencias

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PRACTICA II

OBjetivo: Verificar en la práctica aspectos de la teoría de modulación de frecuencia.

1.- Modulación.

La modulación de la frecuencia se realiza por medio de un oscilador controlado por voltaje, donde la señal de control es la mpdulante.

2.- Demodulación.

Este proceso puede ser realizado por medio de un demodulador de fase síncrona o PLL, cuyo diagrama de bloques es mostrado en la figura 1.

La salida del detector de fase después de pasar por el amplificador y filtro se supone proporcional al error entre la fase de la señal de entrada y la fase de la señal del oscilador controlado por voltaje (VCO), la salida del amplificador y filtro cambiará la frecuencia del VCO de tal manera que el error de fase tiende a 0, por lo que esta señal tendrá que ser proporcional a m(t).

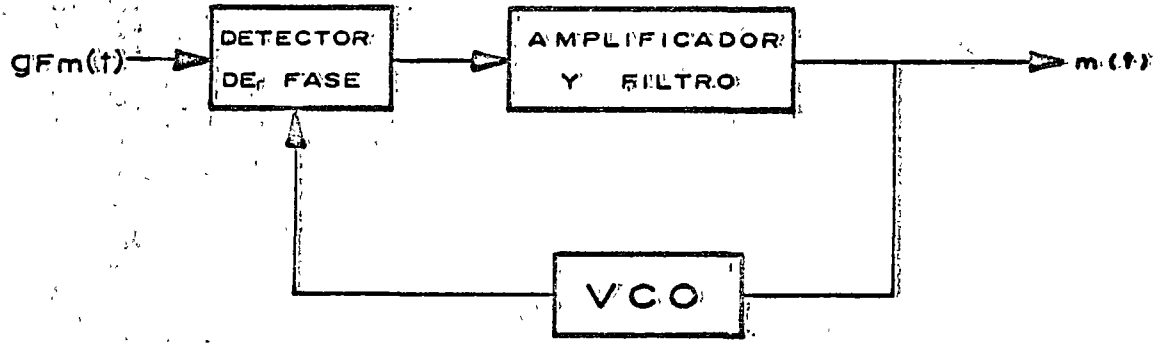

Figura 1 .Demodulador de fase síncrona (PLL)

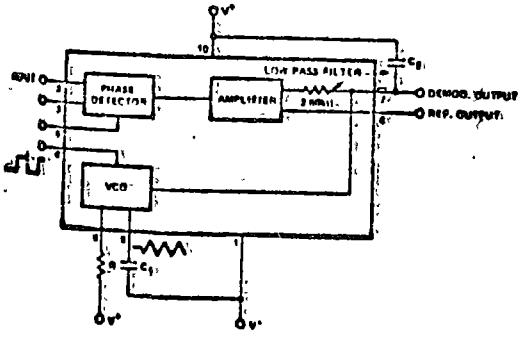

Figura 2 .Diagrama de bloques.

La figura 2 muestra un demodulador de fase síncrona.

3.- Experimentos.

3.1 Usando un modulador y un generador de funciones, module la frecuencia de una señal senoidal portadora de frecuencia 1KHZ y amplitud - - - 3 Vp.p. con una señal senoidal de frecuencia 100HZ y amplitud 3 Vp.p. Obsérvese la señal modulada en el osciloscopio y en el analizador de espectro.

3.2 Repetir 3.1 usando una señal modulante tringular.

3.3 Empezando en 0 volts aumente la amplitud de una señal senoidal - modulante hasta que desaparesca la componente en la frecuencia f_c de la señal modulada; en ese momento $B_f = 2.4$, calcule K_f.

3.4 Polarizante el PLL con $\pm$ 5 volts haga que la frecuencia del oscilador (VCO) del PLL sea 50 KHZ.

3.5 Use una señal portadora senoidal de frecuencia 50 KHZ y amplitud 1 Vp.p. y una señal modulante senoidal de frecuencia 700 HZ y aplitud - - - 1 Vp.p.

3.6 Conecte la señal modulada al PLL y observe en el osciloscopio — tanto la señal modulante como la demodulada obtenida del PLL.

3.7 Repita 3.5 con una señal modulante tringular de frecuencia igual a 100 HZ.

PRACTICA III

MODULACION POR AMPLITUD DE PULSO (PAM) Y TEORIA DEL MUESTREO

MODULACION POR DURACION DE PULSO (PDM)

Objetivo: Verificar en la práctica la validez de la teoría del muestreo y mostrar dos de las formas de modulación por pulsos PAM y PDM.

1.a. Modulación por amplitud de pulso y teoría del muestreo

Instrumentos: Osciloscopio, Analizador de espectros, circuitos impresos de PAM, PDM y filtros pasobajas.

Teorema del muestreo: es posible recuperar completamente una señal de banda limitada que no tenga componentes de frecuencia arriba de B hz., siempre y cuando esta señal haya sido muestreada con una frecuencia de por lo menos 2B Hz.

Recuperación: la reconstrucción de la señal se lleva a cabo pasando la señal muestreada a través de un filtro pasobajas cuya frecuencia de corte sea mayor que B Hz., pero menor que f_o-BHz, donde f_o es la frecuencia de muestreo. Las figuras 1-a, 1-b y 1-c ilustran los espectros de amplitud de la señal original, de la señal muestreada y las condiciones del filtro, respectivamente.

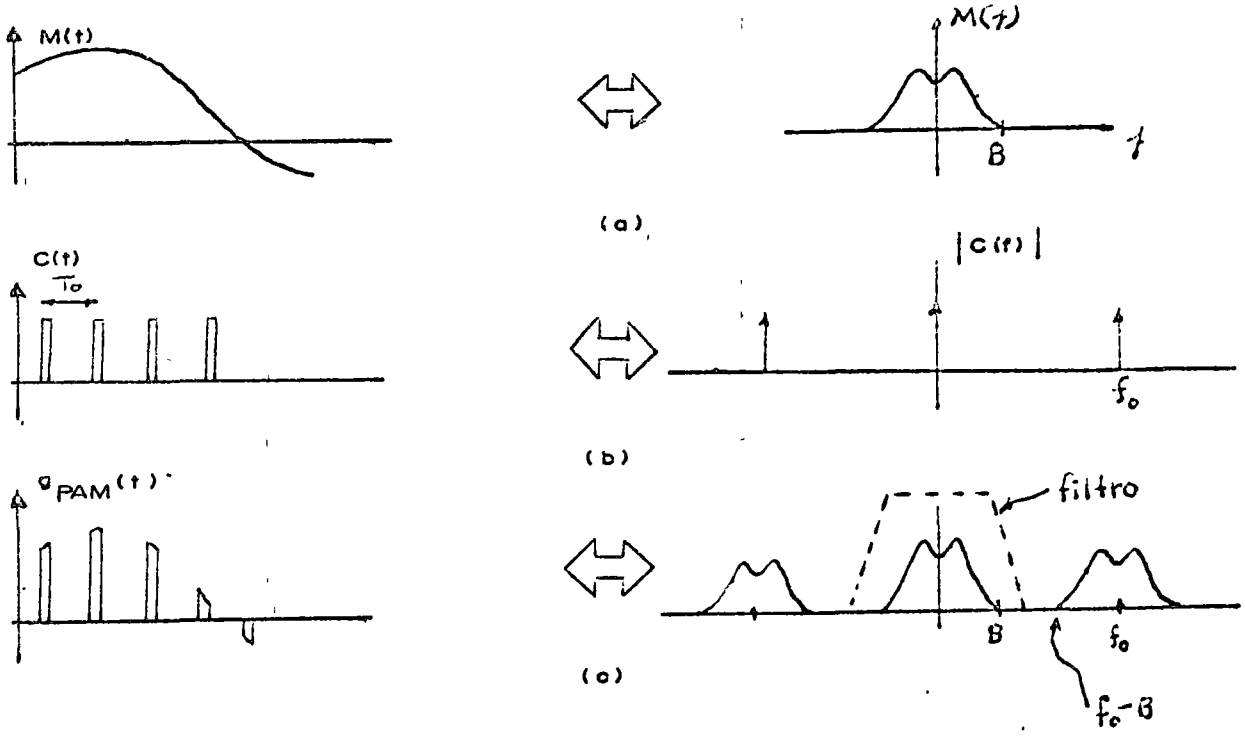

Fig. 1 Modulación por amplitud de pulso en el dominio del tiempo y la frecuencia.

La modulación por amplitud de pulso se puede interpretar a partir de la teoría del muestreo en donde un tren de pulsos es modulado por una señal $m(t)$, lo cual equivale a tomar muestras de la señal cada vez que ocurre un pulso, pudiéndose aplicar el Teorema del Muestreo.

Desarrollo de la práctica:

a) Por medio del generador de funciones, obtenga una señal senoidal de 1 khz. y obsérvela en el osciloscopio.

b) Introduzca esta señal en el analizador y vea si el espectro contiene 2 impulsos aplicados en $f = \pm 1$ khz.

c) Alimente el muestreador con la senoide y observe la salida en el osciloscopio. Calcule la frecuencia de muestreo.

d) Observe el espectro de amplitud de la señal muestreada. Verifique que coincide con los cálculos teóricos. ¿qué frecuencia de corte deberá tener el filtro de reconstrucción?

e) Recupere la señal introduciéndola al filtro pasabajas y comparela con la señal original ¿ Existe distorsión?

f) Haga el experimento de nuevo, variando la frecuencia de la senoide ¿qué sucede si la frecuencia de muestreo es menor que dos veces la frecuencia de la senoide?

1.b. Modulación por duración de pulso.

Teoría: Así como en PAM la información está contenida en la amplitud de cada pulso, en el caso de PDM, la información (señal moduladora) está contenida en la duración de los pulsos, siendo ésta proporcional a la amplitud de la señal moduladora.

Una forma mediante la cual se puede realizar la modulación por duración de pulso es la siguiente: a la señal moduladora se le añade una componente de directa con el fin de hacer factible su comparación con una onda diente de sierra que debe tener una frecuencia de por lo menos el doble de la moduladora $m(t)$. (Teorema de Nyquist).

En la fig. 2 se muestra el diagrama electrónico del modulador; la señal diente de sierra se obtiene mediante un sencillo circuito que emplea un transistor UJT.

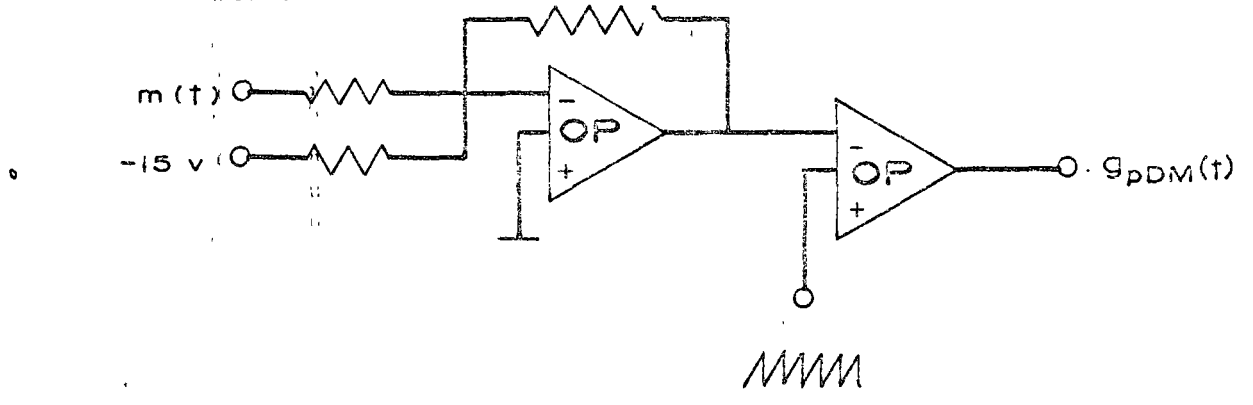

Fig. 2 Modulador por duración de pulso

Desarrollo: (a) observar la señal $G_{PDM}(t)$ y verificar la coincidencia de la amplitud de la señal $m(t)$ con el ancho de los pulsos. Hallar la frecuencia de muestreo. ($m(t) = A\text{sen } 2\pi f_m(t)$). Ver fig. 3

(b) Observe el espectro de la señal modulada el cual muestra un gran parecido con el de FM, pero aparece una componente a la frecuencia de la señal moduladora $m(t)$. Ver la fig. 4

(c) Recuperación: la recuperación puede hacerse mediante un filtro pasabajas. Ver figura 4

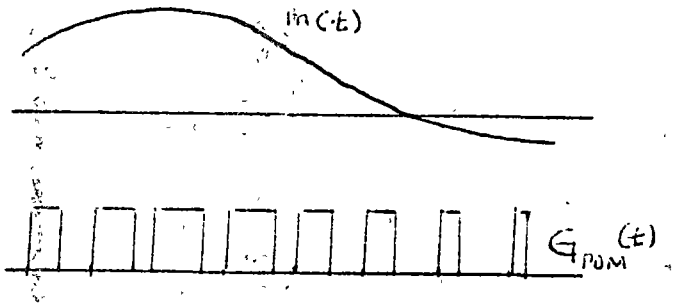

FIG 3. SEÑAL MODULADORA Y SEÑAL MODULADA POR PDM.

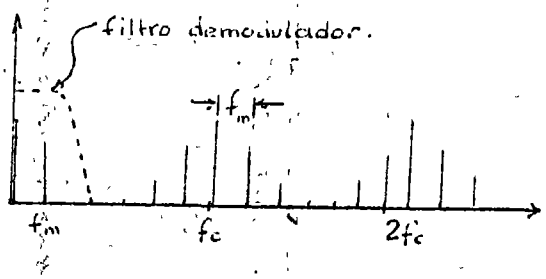

FIG 4. ESPECTRO DEL PDM Y RECUPERACION.

CAPITULO III

APLICACION A LAS COMUNICACIONES DIGITALES

Dr. Jorge Valerdi Caram*

3.1 MODULACION POR PULSOS

Como se ha demostrado en capítulos anteriores, los amplificadores operacionales pueden ser usados como generadores de onda, multiplicadores, amplificadores lineales o no lineales, etc., y es de esperarse que también se les pueda considerar como moduladores y/o demoduladores de señales de pulsos. Estas últimas funciones pueden implementarse combinando integradores, multiplicadores, comparadores y compuertas de precisión. A continuación se considerarán diferentes tipos de modulación por pulsos, los cuales se pueden implementar como se mostrará, con amplificadores operacionales.

Los tipos más comunes de modulación por pulsos, se muestran en la Fig. 3.1.1 y son:

- modulación por amplitud de pulsos (MAP)
- modulación por duración de pulsos (MDP)
- modulación por posición de pulsos (MPP)

3.1.1. MODULACIÓN POR AMPLITUD DE PULSOS

El método mas directo para realizar la modulación por amplitud de pulsos (MAP), es utilizando un multiplicador analógico. Sin embargo, como la portadora es un tren de pulsos, la implementación de dicho modulador puede ser más fácil utilizando un circuito de control para encendido y apagado de la señal analógica de entrada.

Una compuerta de un transistor y un amplificador operacional para realizar

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MAP se muestra en la Fig. 3.1.2. En este circuito, el tren de pulsos e_c conmuta al transistor Q_1 entre los estados de encendido y apagado (saturación y corte). El voltaje de modulación e_M es siempre negativo y varía de 0 a 10v. Cuando e_c = 10v, Q_1 es polarizado a corte y la salida e_o, es igual a $(-e_M - V_B)$. Cuando e_c cambia de estado (a un valor aproximadamente de 0v.), Q_1 es polarizado a saturación por medio de la resistencia de 33 kΩ hacia la fuente de -15 v. Entonces e_o sería igual a $-V_B-2V_{CE(sat.)}$, es decir,

$$e_o = \begin{cases} -e_M - V_B \\ -V_B - 2V_{CE(Sat.)} \end{cases}$$

El voltaje $V_{CE\ (Sat.)}$ puede hacerse muy pequeño escogiendo un transistor que tenga un valor bajo de este voltaje de saturación colector-emisor, (los valores típicos oscilan entre 20 y 200 mV para transistores de conmutación), y haciendo la resistencia $R_1/2$ bastante alta. Un transistor de efecto de campo puede utilizarse en lugar del transistor bipolar, sí así se desea. El voltaje de desviación en el estado de conducción será menor, pero el efecto capacitivo de alimentación de los transientes de conmutación puede empeorar.

Otro método para realizar MAP se puede implementar por medio de diodos, como se ilustra en la Fig. 3.1.3. No obstante un puente de diodos se puede utilizar para realizar la conmutación, la exactitud dependería de las características de los diodos. Sin embargo, un circuito rectificador de precisión como el de la Fig. 3.1.3 provee mejor exactitud y mayor rango dinámico.

Para la explicación de dicha figura, supóngase que e_c es un tren de pulsos que varía entre 0 y 10 v. El voltaje de modulación e_M es simétrico y varía entre $\pm$ 4 v. El amplificador A_1 tiene dos posibles salidas:

$$e_1 = \begin{cases} (-e_c - e_M - V_B) & \text{si:} \quad (-e_c - e_M - V_B) < 0 \\ 0 & \qquad\quad (-e_c - e_M - V_B) > 0 \end{cases}$$

El amplificador A_2 tiene también dos posibles salidas:

$$e_o = \begin{cases} -e_c-(-e_c-e_M-V_B) = e_M + V_B & \text{si: } e_1 < 0 \\ -e_c & e_1 = 0 \end{cases}$$

Si E_H es más positivo que $|e_m - V_B|$, entonces e_1 tendrá valores negativos y la salida será $(e_M + V_B)$. Si $(e_M + V_B) < 0$, entonces $e_1 = 0$ cuando e_c es $\cong 0$ y la salida será igual a cero. El voltaje de polarización V_B está ajustado a -5v. para el ejemplo mostrado.

3.1.2 MODULACION POR DURACION DE PULSOS

La generación de MDP puede ser como se indica en el sistema conceptual de la Fig. 3.1.4. Nótese que en este sistema se hace uso de la salida de un modulador por amplitud de pulsos (MAP), la cual es sumada a una señal triangular para producir la señal 3.1.4 (d). ESta señal, a su vez, es pasada a través de un amplificador de ventana para producir la modulación por duración de pulsos 3.1.4 (e). Este amplificador de ventana debe ser capaz de dar un pulso de salida cuya duración será proporcional al tiempo que la señal de entrada 3.1.4(d) esté dentro de la ventana de voltaje determinada por dicho amplificador.

Entonces, se obtiene que la salida $g_{PDM}(t)$ es un tren de pulsos cuya duración es proporcional al valor de la señal moduladora, y de período constante.

Como ejemplo de un circuito conversor de voltaje a duración de pulso se muestra la Fig. 3.1.5. Si la portadora es senoidal, ésta es amplificada y cortada hasta formar una onda cuadrada, y luego convertida a una onda triangular por medio de un integrador. La señal moduladora de entrada controla la polarización de la onda triangular y modula el ancho del pulso alrededor de la condición de 50% en su ciclo de trabajo. El ancho de pulso T_1 está dado por

$$T_1 = \frac{10 + e_m}{20} T_c$$

donde $-10 \leq e_m \leq 0$

Otro ejemplo de un convertidor de voltaje a duración de pulso, es haciendo uso de un integrador conmutado para obtener un modulador muy lineal y además estable, como el de la Fig. 3.1.6.

Se debe tener un tren de pulsos el cual provee una señal de control de tiempo, para así obtener un tren de pulsos sincronizado con los pulsos de entrada con una duración que será función lineal del voltaje de entrada. Los valores V_R, C_1 y R_1 en el circuito deben de seleccionarse de tal manera que cumplan con el rango dinámico deseado y la repetición de los pulsos (el período). Por ejemplo, si la frecuencia de los pulsos de entrada es de 1 KH_z y el voltaje de entrada varía de 0.1 a 10 v., y V_R es + 10v, entonces

$$0.01\ R_1C_1 < T_p < R_1C_1$$

donde T_p es la duración o ancho del pulso y debe ser menor que el período T_c para evitar ambiguedades. Consecuentemente R_1C_1 debe ser menor que T_c.

Si R_1C_1 es igual a 0.9 T_c, entonces R_1C_1 = 0.9 m seg., y si C_1 = 0.01μf entonces R_1 = 90 KΩ. Se tiene que con los valores anteriores T_p = 0.09 e_1 mseg., el ciclo de trabajo es T_p/T_c = 0.09 e_1.

3.1.3 MODULACION POR POSICION DE PULSOS

Existe una relación muy estrecha entre modulación por posición (MPP) y modulación por duración de pulsos, la cual se puede apreciar en la Fig. 3.1.7 en donde se muestra la generación de MPP a partir de MDP.

Teniendo los pulsos controlados por duración, se diferencia la señal y después de rectificarla e invertirla, se obtiene un tren de impulsos cuya posición es proporcional a la amplitud de la señal moduladora. Este tren de impulsos dispara a un multivibrador monostable originando pulsos angostos modulados por posición.

3.2. MODULACION POR PULSOS CODIFICADOS

La modulación por pulsos codificados es un método de modulación en el cual una señal analógica contínua es transmitida en un modo digital equivalente. La base del funcionamiento de esta modulación codificada es la conversión de esa señal analógica, por medio de muestras a un código binario. Estas muestras de la señal analógica deben ser tomadas de acuerdo al teorema del muestreo que dice:

> Si una señal limitada en ancho de banda, es muestreada a intervalos regulares de tiempo y a una razón constante de dos veces o más, que la frecuencia mas alta contenida en la señal, entonces la muestra tomada contiene toda la información de la señal original. Esta señal original puede ser reconstruída utilizando un filtro paso bajas.

Como un ejemplo del teorema de muestreo, se puede mencionar que un canal de voz de 4 KHz de ancho de banda, tendría que ser muestreado a una razón mínima de 8 000 muestras por segundo.

Para desarrollar una señal PCM a partir de una o varias señales analógicas, se requieren tres pasos: Muestreo, Cuantización y Codificación. El resultado es una señal binaria secuencial, es decir, una secuencia de bits, que pueden o no ser aplicados a una línea de comunicación sin pasos adicionales de modulación.

Aquí se está suponiendo que la forma más simple de transmisión digital es la binaria, donde un elemento de información es asignado a una de las dos posibilidades existentes. Así mismo existe un sistema en números que se ha basado en dos valores, los cuales por convención han sido asignados los símbolos 1 y 0. Este es entonces el sistema binario y su base numérica es 2. El elemento de información básica del sistema binario se reconoce como bit, que es una palabra compuesta del inglés: BInary digiT. El bit entonces puede tomar los valores 1 ó 0. Un número discreto de bits pueden identificar un elemento de información y a este conjunto de bits se le conoce como un carácter.

Una de las principales ventajas de la transmisión digital es que las señales pueden ser regeneradas en puntos intermedios sobre los enlaces comprendidos en la transmisión. Por otro lado el precio que se paga por esta característica es el incremento en ancho de banda requerido por PCM. Sistemas prácticos han demostrado requerir 16 veces el ancho de banda de su equivalente analógico (por ejemplo, un canal que conduce señales de voz de 4 KHz requiere 16 x 4, ó 64 KHz, cuando se transmite por PCM). La regeneración de una señal digital se simplifica y es particularmente efectiva cuando la señal de la línea es binaria, ya sea neutral, polar, o bipolar.

La transmisión binaria también tolera niveles de ruido más altos (es decir, razones de señal a ruido más degradados) cuando se compara con su equivalente ananlógico. Este aspecto, además de la capacidad de regeneración, es un paso importante en la ingeniería de transmisión de señales. La regeneración que se lleva a cabo en cada repetidor, por definición, origina una nueva señal digital; por lo tanto, el ruido como se conoce tradicionalmente, no es acumulativo. Sin embargo, existe un ruido equivalente en sistemas de PCM el cual es generado en el proceso de modulación-demodulación. Esta es la distorsión por cuantización, y el receptor puede confundirlo con el ruido térmico.

Concerniente al ruido térmico de intermodulación, se puede comparar un enlace de 2 500 Km. de un sistema analógico que utiliza FDM ya sea sobre cable o radio, con un sistema de PCM equivalente que transmite sobre los mismos medios:

	FDM/radio/cable	PCM/radio/cable
Multiplex	2 500 pWp	130 pWp equiv.
Radio/cable	7 500 pWp	0 pWp
	10 000 pWp	130 pWp equiv.

donde se aprecia que el enlace PCM no es dependiente de la longitud de recorrido del sistema.

La razón de error es otro factor importante. Si se puede mantener una razón de error en la porción digital del sistema de 1×10^{-5}, la señal será todavía

intelegible. Un tercer factor de importancia en los sistemas de transmisión PCM en cable, es la interferencia cruzada de un sistema hacia otro o de la trayectoria de transmisión sobre la de recepción dentro del mismo paquete de cables.

A continuación se presentará el material básico que muestra los problemas existentes en las diferentes etapas de los sistemas PCM.

3.2.1 MUESTREO

Si se toma en cuenta el teorema de muestreo mencionado anteriormente, sobre el envío de información telefónica que comprende las frecuencias de 300-3400 Hz de acuerdo con la convención del CCITT (originando un ancho de banda de 3 100 Hz), y se muestrea a una razón de 8 000 muestras por segundo, se ha cumplido con el teorema de Nyquist y es de esperarse que toda la información original pueda recuperarse en su forma analógica. Para lo anterior, una muestra es tomada cada 1/8 000 segundos, es decir, cada 125 microsegundos.

Otro ejemplo puede ser un canal de alta fidelidad de 15KHz. En este caso la razón de muestreo mas baja que se podría tomar, es de 30 000 muestras por segundo. Entonces las muestras serían tomadas intervalos de 1/30 000 segundos, es decir espaciadas a 33.3 microsegundos.

Un sistema PCM práctico comprende multiplexaje por división de tiempo, con una excepción (SPADE). El muestreo en estos casos no comprende únicamente un canal de voz, sino varios. En la práctica un sistema normal comprende 24 canales de voz; otros consideran 32 canales. El resultado del muestreo múltiple es una señal de tipo PAM. En la figura 3.2.1 se muestra el caso de 3 señales analógicas muestreadas y sus formas PAM de entrada al cuantizador-codificador.

Si el canal de voz nominal de 4 KHz debe ser muestreado 8 000 veces por segundo, y un grupo de 24 canales de voz similares deben ser muestreados secuencialmente para intercalarlos, formando una onda PAM de multicanal, esto puede ser realizado a través de compuertas. Si se abre la compuerta por un período de 3.25 microsegundos para cada canal de voz a ser muestreado en forma sucesiva del

1 al 24, esta secuencia completa puede ser realizada en un período de 125 micros-gundos ($1 \times 10^6/8\ 000$). A este período de 125 microsegundos se le conoce como un marco, y dentro de este marco todos los 24 canales son muestreados una vez, en forma sucesiva.

3.2.2 CUANTIZACION

El siguiente paso en el proceso de formar una secuencia de bits PCM, es asignar un código binario a cada muestra conforme se presenta al codificador. Hay que recordar que un código binario de 4 elementos discretos (un código de nivel 4) codificará 24 significados distintos y separados diferentes caracteres, los cuales no son suficientes para un alfabeto de 26 letras; un código de 5 niveles suministraría 32 caracteres. El código ASCII es básicamente un código de 7 niveles que permite 128 significados discretos para cada combinación de código. Un código de 8 niveles permitiría 256 posibilidades.

Otro concepto que debe tenerse en mente es que los anchos de banda están relacionados con la razón de información, es decir, el número de bits por segundo transmitidos. El objetivo es mantener algún control sobre la cantidad de ancho de banda necesaria. Por lo tanto debe de limitarse la longitud del código, es decir, el número de niveles.

Hasta ahora un número infinito de niveles de amplitud se presenta al codificador, y la excursión de la onda PAM es entre 0 y 1 volt; se puede uno preguntar, cuántos valores discretos se encuentran entre 0 y 1? Todos los valores deben ser considerados, aún el de 0.0176487892 volts.

El rango de intensidad de las señales de voz que son enviados por canales telefónicos analógicos es del orden de 60 dB. El rango 0-1 volts de la etapa PAM en la entrada del codificador puede representar el rango de 60 dB. Más aún el codificador no puede suministrar un código de longitud infinita (por ejemplo un número infinito de niveles codificados) para satisfacer cada nivel en el rango de los 60 dB. La clave es asignar niveles discretos de -1 pasando por 0 a +1.

La asignación de valores discretos a las muestras PAM se llama cuantizac.ón.

Para citar un ejemplo consideremos la figura 3.2.2 donde existen 16 niveles cuánticos entre -1 y +1 volts y están codificadors como sigue;

0	0000	8	1000
1	0001	9	1001
2	0010	10	1010
3	0011	11	1011
4	0100	12	1100
5	0101	13	1101
6	0110	14	1110
7	0111	15	1111

Un análisis de la figura 3.2.2 muestra que el paso 12 es utilizado dos veces. En ninguna de las ocasiones que es utilizado toma los valores reales de la senoidal analogica, sino que toma valores redondeados. Estos valores redondeados se muestran con línea punteada en la misma figura. Las líneas punteadas horizontales muestran el punto donde el cambio cuántico excede hacia el siguiente nivel superior o inferior; ya sea que la señal senoidal esté arriba o abajo de ese valor. Si se toma el paso 14 en la curva, como otro ejemplo, la parte que va cayendo de su máximo le es asignada a dos valores de 14 en forma consecutiva. Para el primero, la curva está arriba de 14 y para el segundo está abajo; este error en el caso del 14, del valor cuántico al valor verdadero, se le conoce como distorsión cuántica. Esta distorsión es la fuente principal de imperfección en los sistemas PCM.

Si se mantiene el rango de 1 a -1 y se dobla el número de pasos cuánticos de 16 a 32 se podría identificar un mejoramiento en la distorsión de cuantización. Para apreciar este mejoramiento se debe determinar el incremento de los pasos en milivolts, para cada caso; en el primero, el rango total de 2000 milivolts sería dividido en 32 pasos, es decir 187.5 milivolts por paso, el segundo caso tendría 2 000/64, es decir, 93.7 milivolts por paso.

Para el caso de los 32 pasos, el error de cuantización mas grande ocurriría cuando una señal de entrada al ser cuantizada, se encuentre a la mitad del nivel de uno de los pasos, o en este caso a 93.7 milivoltas arriba o abajo del

nivel de cuantización más cercano. Cuando se tienen 64 pasos, el error máximo ocurriría igualmente a la mitad del nivel, es decir, a los 46.8 milivolts. El mejoramiento en decibeles, al doblar el número de pasos de cuantización es:

$$20 \log\left(\frac{97.7}{46.8}\right) = 20 \log 2$$
$$= 6 \text{ dB aprox.}$$

Lo anterior es válido únicamente para cuantización lineal. Entonces, el incrementar el número de pasos de cuantización para un rango de valores fijo reduce la distorsión de cuantización en forma proporcional. En experimentos prácticos, se ha encontrado que si se suministra un sistema de 2 048 pasos de cuantización uniformes, se alcanza una calidad de señal suficientemente aceptable.

Para un sistema de 2 048 pasos de cuantización, se requeriría que el codificador suministrara para cada paso cuántico se asignara un carácter o significado, lo que requiere un código de 11 elementos, es decir:

$$2^n = 2\,048 \quad (n=11)$$

Con una razón de muestreo de 8 000 muestras por segundo por canal de voz, la razón de información binaria por canal será de 88 000 bits por segundo. Considérese que el ancho de banda equivalente es una función de la razón o velocidad de la información; el deseo de reducir esta figura es claramente obvia.

3.2.3 CODIFICACION

Se ha observado que los sistemas PCM mas comunes utilizan códigos binarios de 7 y de 8 niveles, es decir:

$$2^7 = 128 \text{ pasos cuánticos}$$
$$2^8 = 256 \text{ pasos cuánticos.}$$

El objetivo que se persigue al codificar es el de reducir el error debido al ruido. Esto se hace representando a la amplitud de PAM como un número

binario y enviando una serie de pulsos de amplitud máxima (unos) y espacios (ceros) para representar al número binario, como se puede apreciar en la figura 3.2.3. Se supone que en el detector se conoce donde comienza y termina cada número binario es decir, se presupone sincronía.

El uso de la codificación para transmitir PAM cuantizado, resulta entonces en una señal de PCM. Este tipo de modulación de pulsos es adecuado para la transmisión de señales en la presencia de ruido muy intenso, ya que el proceso de detección consiste en hacer una decisión relativamente fácil de presencia o ausencia del pulso durante un intervalo de tiempo.

El costo de este mejoramiento en los sistemas PCM relativo a PAM, es el ancho de banda. En lugar de determinar ahora la amplitud de un pulso, se tiene que determinar si el pulso que se transmitió fue un 1 ó un 0.

Para obtener una estimación ideal del ancho de banda requerido en PCM, se puede considerar el argumento de que un número binario de n dígitos se puede utilizar para especificar 2^n niveles diferentes. Para determinar este ancho de banda se debe conocer el número de niveles cuánticos decididos para el sistema. Se concluirá entonces que el ancho de banda para transmitir este tipo de señales es n veces mayor que el que se requiere para transmitir la señal moduladora original, es decir:

$$\frac{1}{2xB} = \frac{1}{2nf_m} \qquad \text{ó}$$

$$B = nf_m$$

MODULACION DELTA

Este tipo de modulación es una técnica por la cual una señal analógica puede ser codificada en dígitos binarios. Entonces DM es un sistema PCM. Se restringirá sin embargo, el nombre PCM a la técnica de codificación descrita anteriormente. DM tiene el mérito de que los circuitos electrónicos requeridos para la modulación en el transmisor, y particularmente para la demodulación en el receptor, son sustancialmente más simples que los circuitos correspondientes requeridos en PCM.

Un sistema de modulación Delta se muestra en el bloque de la figura 3.2.4. El generador de pulsos siministra un tren regularmente recurrentes de $p(t)$ con amplitud y polaridad fija. Para simplificar la explicación se supondrá que estos pulsos son arbitrariamente angostos pero aún así, de área finita. El modulador recibe estos pulsos $p_i(t)$ así como una señal $\Delta(t)$. La salida del modulador $p_o(t)$ es el tren de pulsos de entrada multiplicado por +1 ó por -1, dependiendo de la polaridad de $\Delta(t)$ únicamente. Si $\Delta(t)$ es positiva cuando $p_i(t)$ ocurre, la multiplicación es por +1 y si es negativa, será por -1.

La forma de onda $p_o(t)$ es aplicada a un integrador cuya salida se le ha designado $\tilde{m}(t)$. Como se verá, $\tilde{m}(t)$ es una proximación de la señal de entrada $m(t)$. Estas dos señales son comparadas en un amplificador diferencial cuya salida está dada por:

$$\Delta(t) = m(t) - \tilde{m}(t)$$

La operación de este modulador se puede explicar también con las formas de onda mostradas en la figura 3.2.5. En esta figura, $t = 0$ ha sido seleccionada para ocurrir a la mitad de los pulsos. Los valores iniciales de $m(t)$ y $\tilde{m}(t)$ han sido seleccionados en forma arbitraria. En el tiempo t_1 del primer pulso, sucede que $m(t)$ es mayor que $\tilde{m}(t)$. Por lo tanto, el pulso de salida del modulador es positivo. La respuesta del integrador a este pulso, es una función escalón; en el tiempo t_2, $\Delta(t) = m(t) - \tilde{m}(t)$ es aún positiva, con la resultante de que $m(t)$ es una función escalón positiva, una vez más. Las formas de onda $\tilde{m}(t)$ continúan su progresión en forma de escalón hacia $m(t)$ hasta el cuarto pulso, en donde se detecta una igualdad.

Entonces inmediatamente después del primer pulso, $\Delta(t)$ es negativa, y el siguiente pulso en la salida del modulador es de polaridad negativa. La primera parte $m(t)$ ha sido indicada sin variación de tiempo, para mostrar el acercamiento transiente inicial de $\tilde{m}(t)$ hacia $m(t)$, y para ilustrar también el seguimiento de $\tilde{m}(t)$ cuando $m(t)$ no varía.

La señal que es transmitida a través del canal de comunicaciones es la forma de onda de pulsos de $p_o(t)$. En la práctica cada pulso es de duración finita,

para aumentar la energía en el bit transmitido. Se observa que al transmitir $p_o(t)$, se transmite en forma codificada, no el nivel de la señal misma, sino la información sobre la diferencia entre la forma de onda m(t) y su aproximación $\tilde{m}(t)$. De ahí el que se derive el nombre de la modulación Delta.

El cuantizador mostrado en la figura 3.2.4 sirve para realizar, en principio, la misma función hecha por el receptor en un sistema PCM. Es de esperarse que si el ruido que se añade a la señal en un canal de comunicaciones no es demasiado grande, el cuantizador siempre será capaz de distinguir un pulso positivo de uno negativo.

El tren de pulsos de la figura anterior es el que se suministra entonces al receptor. Se podrá consecuentemente reconstruir la forma de onda $\tilde{m}(t)$ utilizando un integrador, al igual que en el transmisor. Seguido del integrador se coloca un filtro paso-bajas para suprimir las fluctuaciones indeseables en $\tilde{m}(t)$ y alizar al señal de manera que siga en una manera mas o menos bien comportada, la forma original de m(t). Sin embargo, se reconoce que un filtro paso-bajas proporcionará por sí mismo una medida aproximada de la integración. Entonces se puede obviar el integrador en el receptor y depender del filtro únicamente; su salida será $\hat{m}(t)$, que difiere de entrada del transmisor m(t), solamente debido a los efectos de la aproximación en forma escalonada de la modulación Delta y los errores hechos por el cuantizador del receptor debido al ruido.

Entonces el aspecto escencial de un sistema DM es que transmite información sobre la señal de diferencia. Nótese que esta señal está disponible a la salida del amplificador diferencial de la figura 3.2.4. En este sistema no se transmite $\Delta(t)$ sino únicamente su polaridad, determinada en cada tiempo de muestreo. Se puede también, si así se desea, transmitir $\Delta(t)$. Entonces suponiendo que $\Delta(t)$ fuera aplicada como la señal de entrada a un sistema PCM, este sistema sería identificado como Delta - PCM o simplemente DPCM.

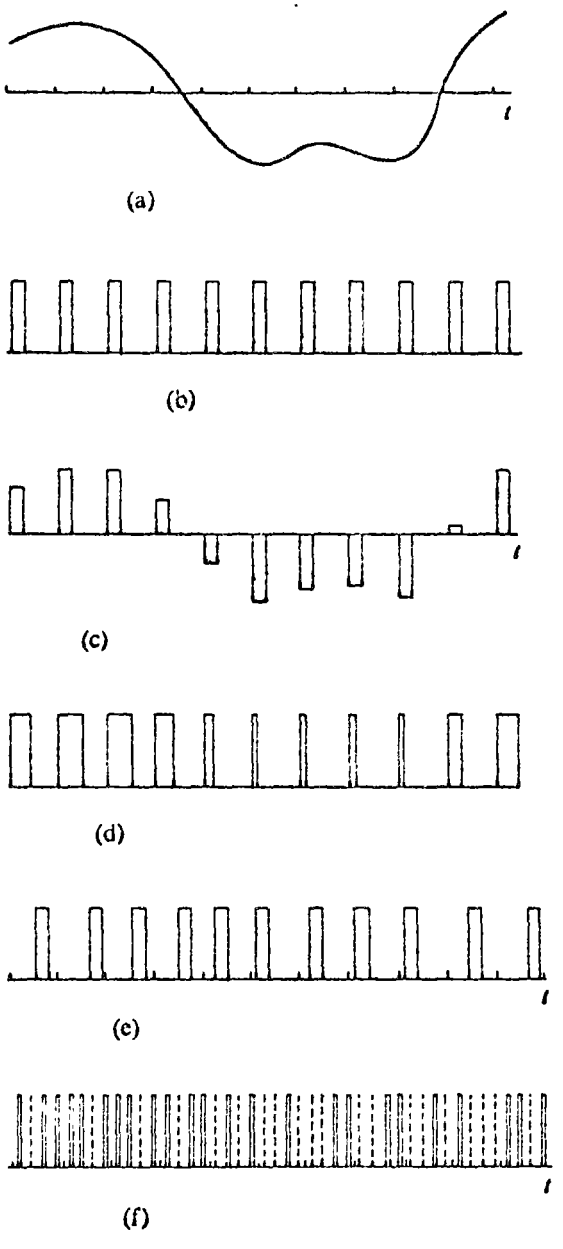


FIG. 3.1.1 TIPOS DE MODULACION POR PULSOS

(a) Señal Moduladora

(b) Portadora

(c) Modulación por Amplitud de Pulsos (MAP)

(d) Modulación por Duración de Pulsos (MDP)

(e) Modulación por Posición de Pulsos (MPP)

(f) Modulación por Pulsos Codificados (MPC ó MIC)

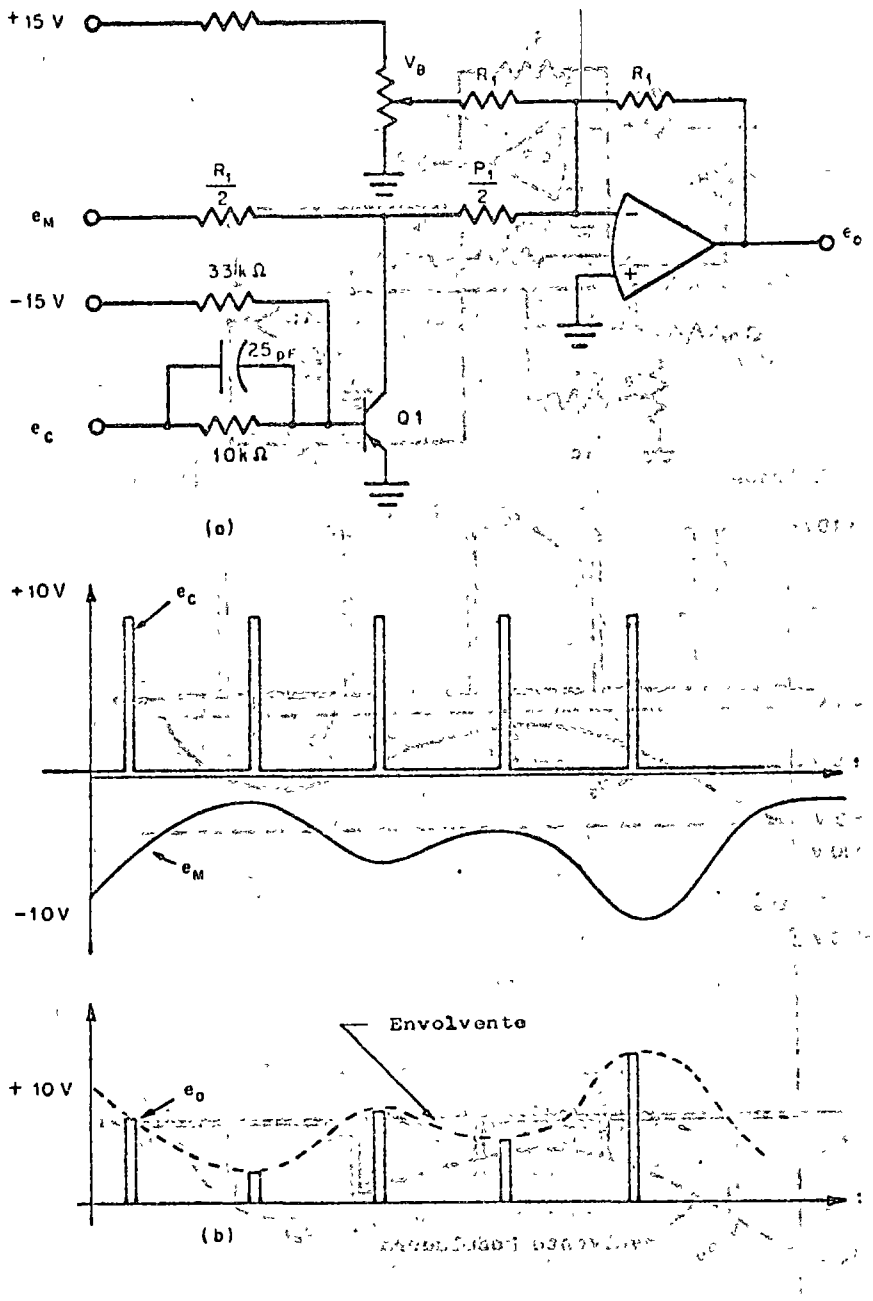


FIG. 3.1.2 MODULACION POR AMPLITUD DE PULSOS

(a) MAP utilizando un transistor como compuerta

(b) Formas de onda

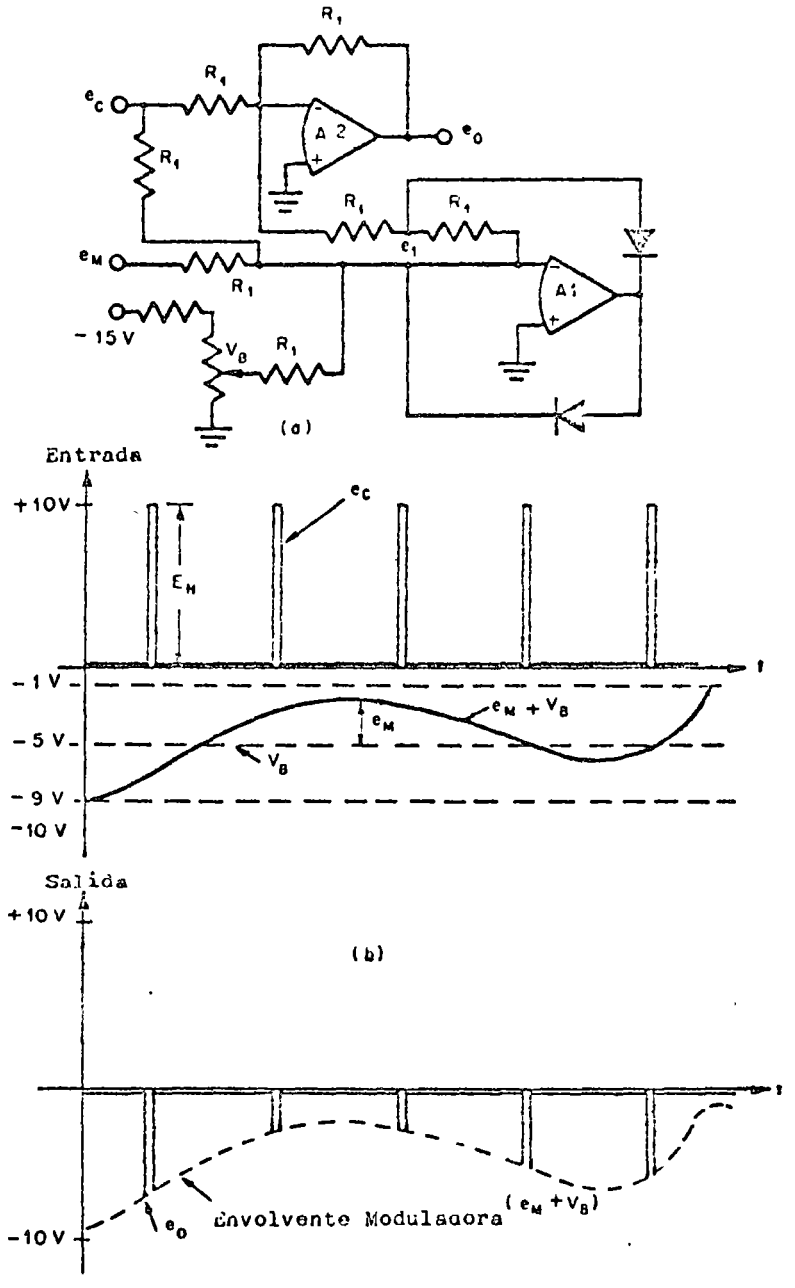


FIG. 3.1.3 MODULADOR POR AMPLITUD DE PULSOS

(a) Diagrama

(b) Formas de Onda

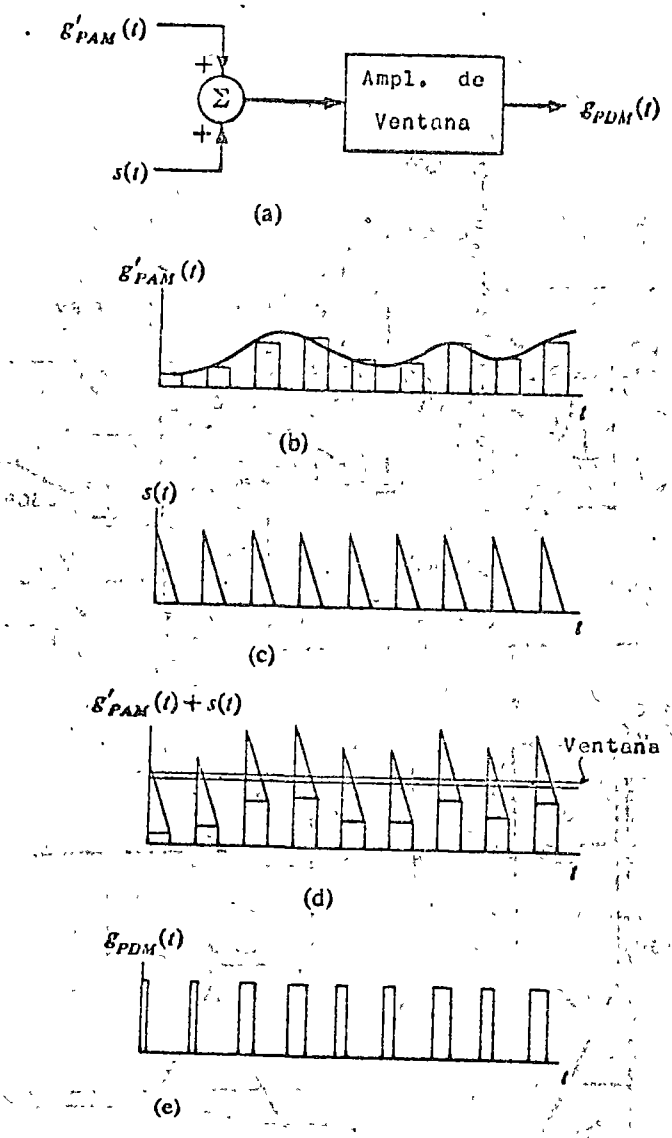


FIG. 3.1.4 GENERACION DE MDP

(a) Sistema Conceptual
(b) Señal MAP
(c) Señal Triangular
(d) Ventana
(e) Señal MDP (ventana amplificada)

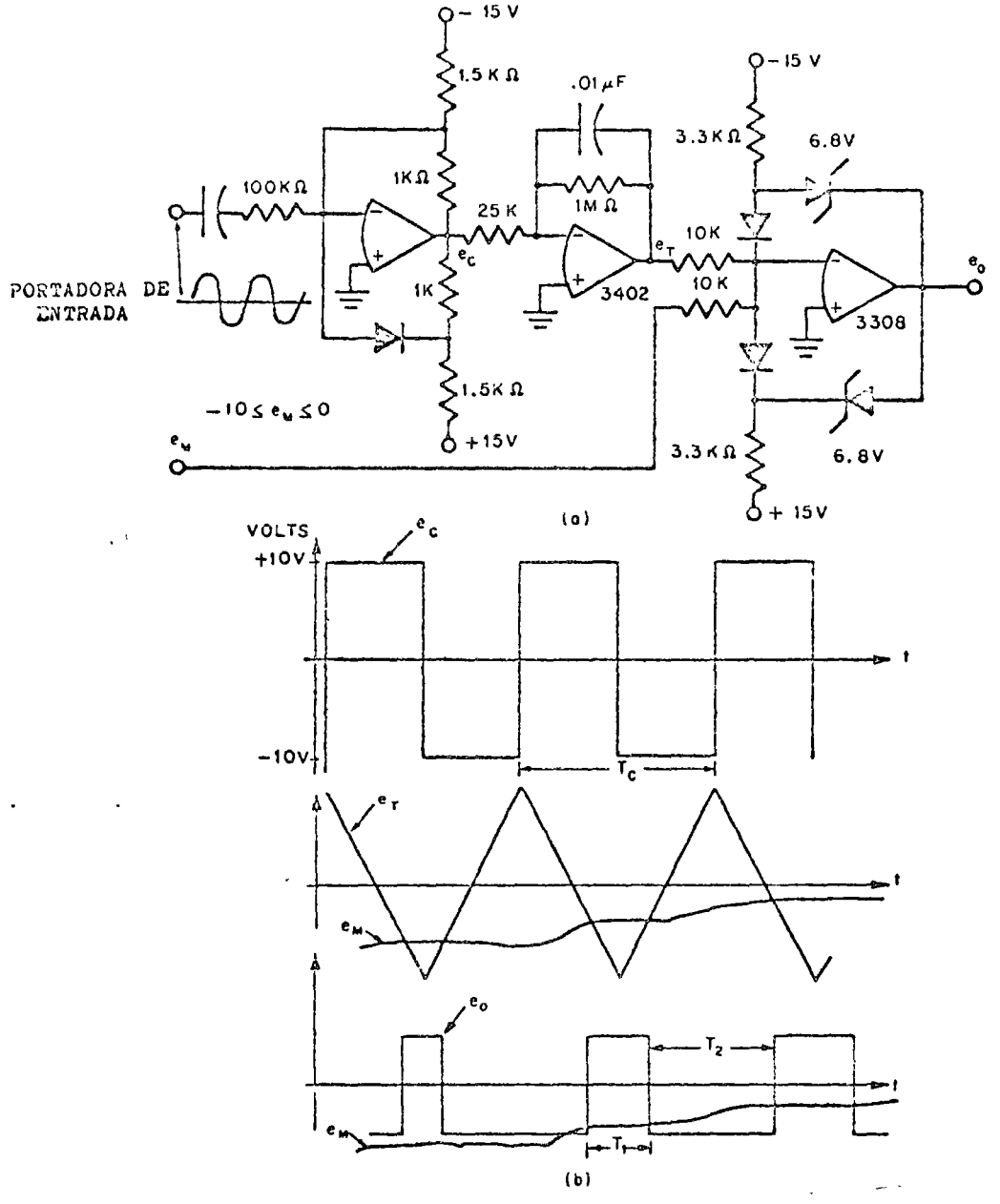


FIG. 3.1.5 MODULADOR POR DURACION DE PULSOS

(a) Diagrama

(b) Formas de Onda

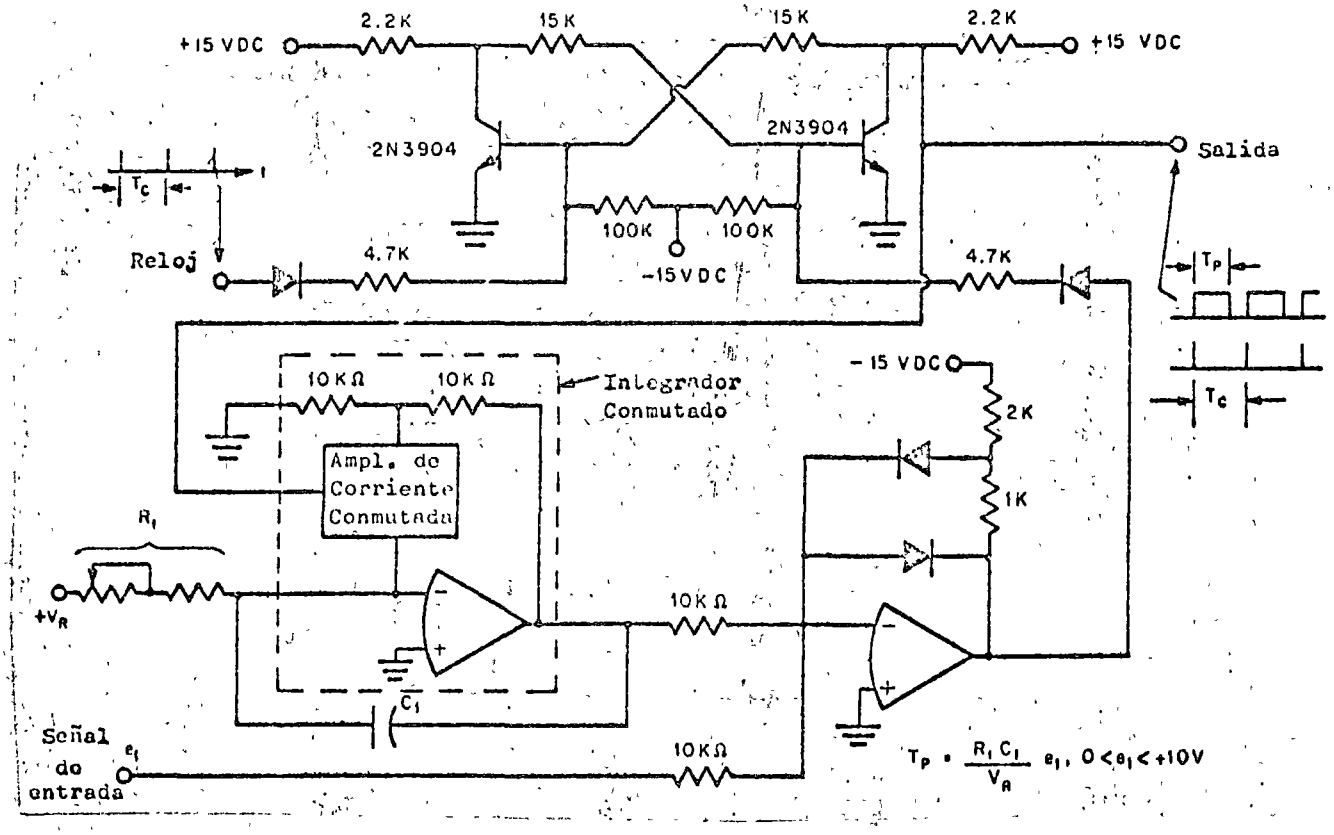


FIG. 3.1.6 DIAGRAMA SIMPLIFICADO DE UN CONVERSOR DE VOLTAJE A DURACION DE PULSOS

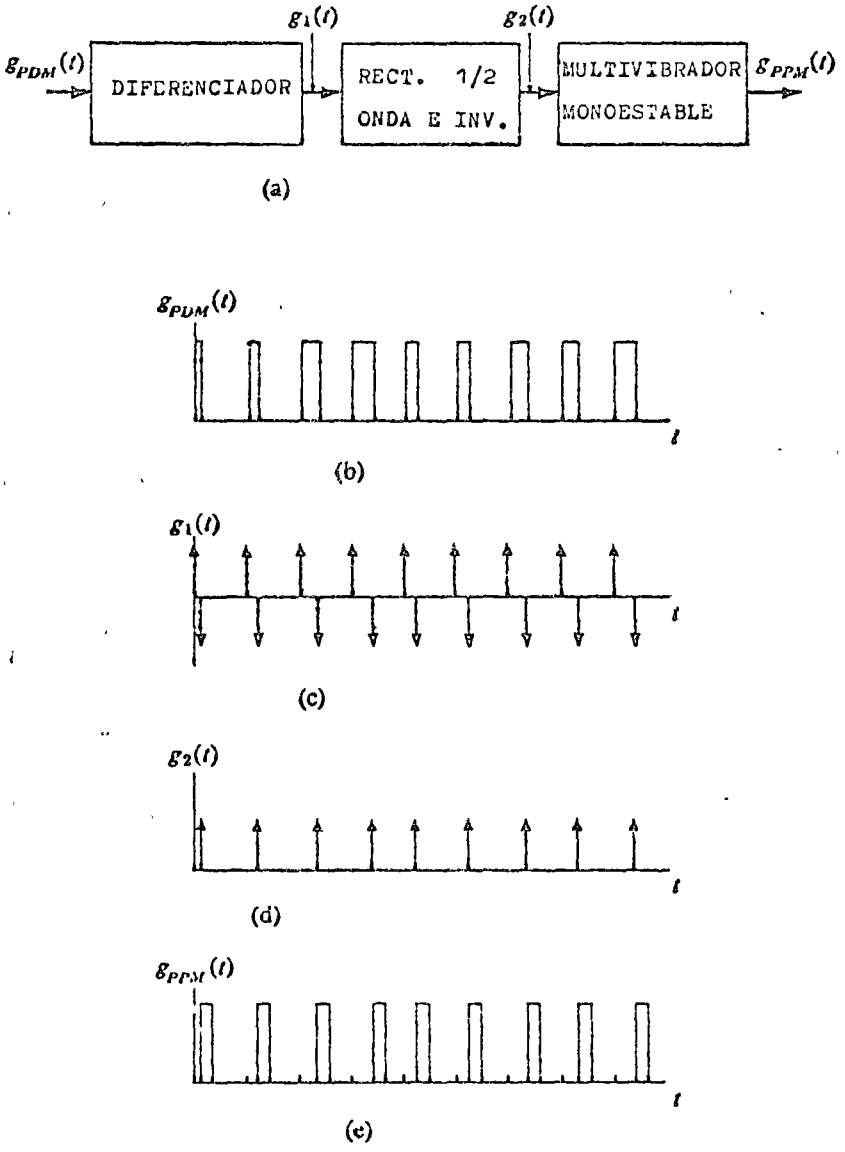


FIG. 3.1.7 GENERACION DE MPP

(a) Conversión MDP-MPP
(b) Señal MDP
(c) Señal Diferenciada
(d) Señal Rectificada e invertida
(e) Señal MPP

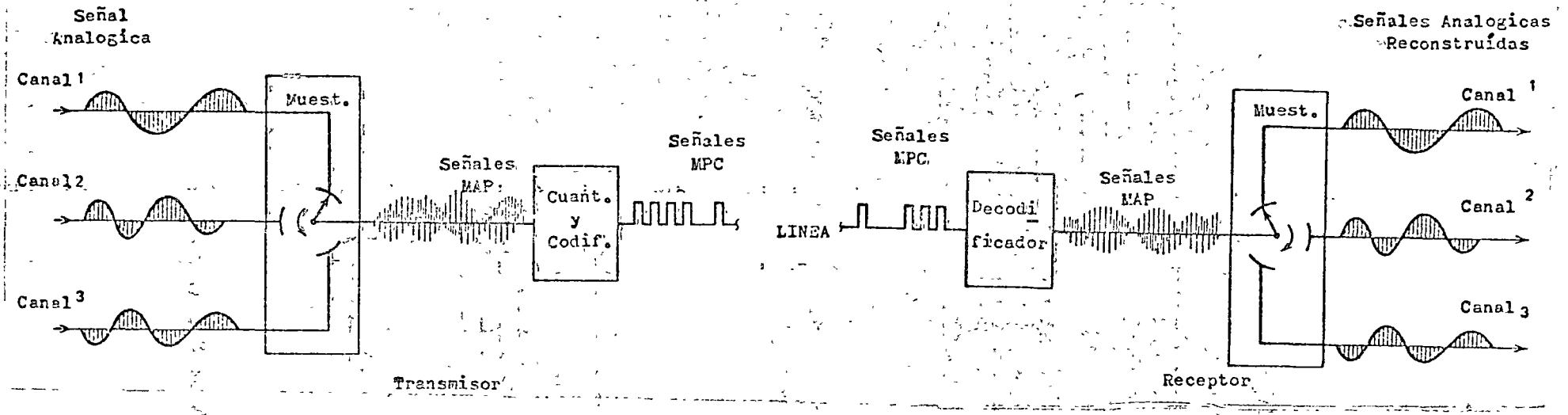
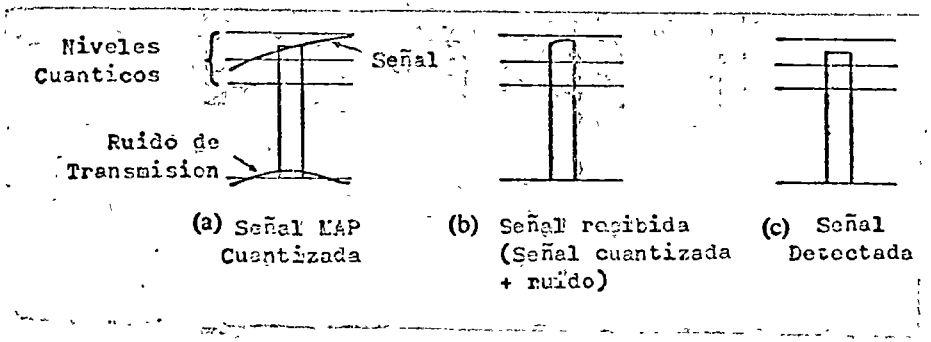
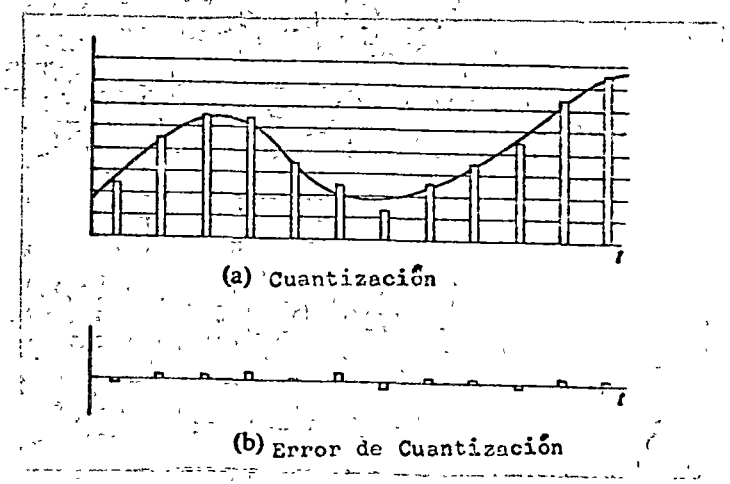


FIG. 3.2.1 SISTEMA SIMPLIFICADO MAP - MIC



3.2.1a INMUNIDAD DE MAP CUANTIZADO AL RUIDO DE NIVELES BAJOS



3.2.1b MAP CUANTIZADO

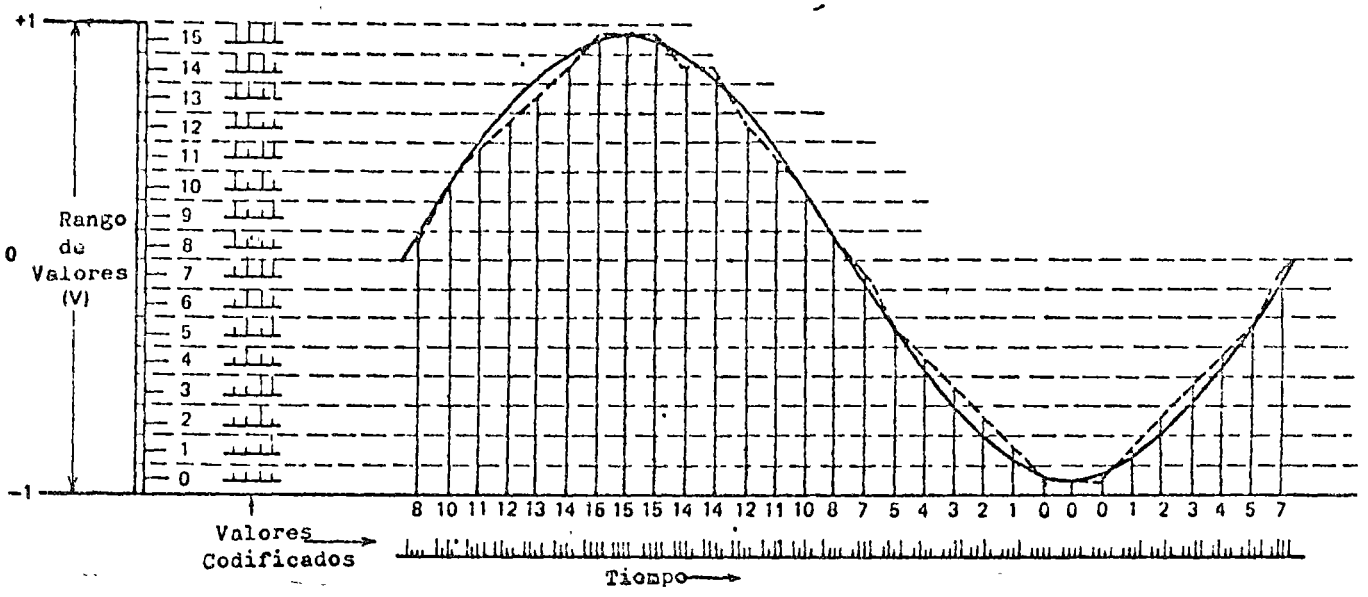


FIG. 3.2.2 CUANTIZACION Y CODIFICACION RESULTANTE UTILIZANDO 16 PASOS CUANTICOS

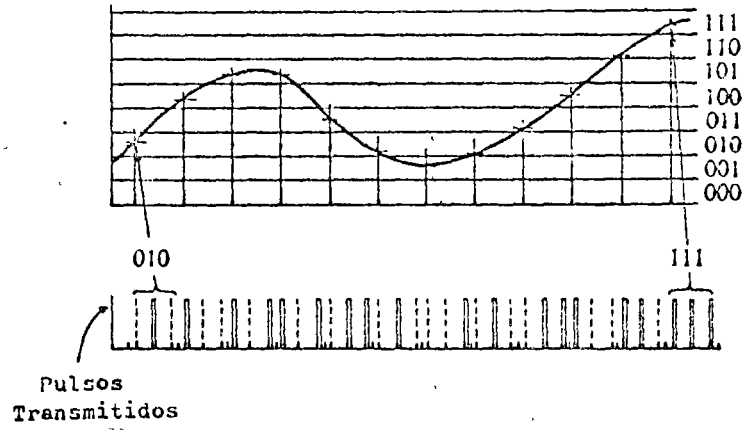


FIG. 3.2.3 FORMACION DE MIC (PCM)

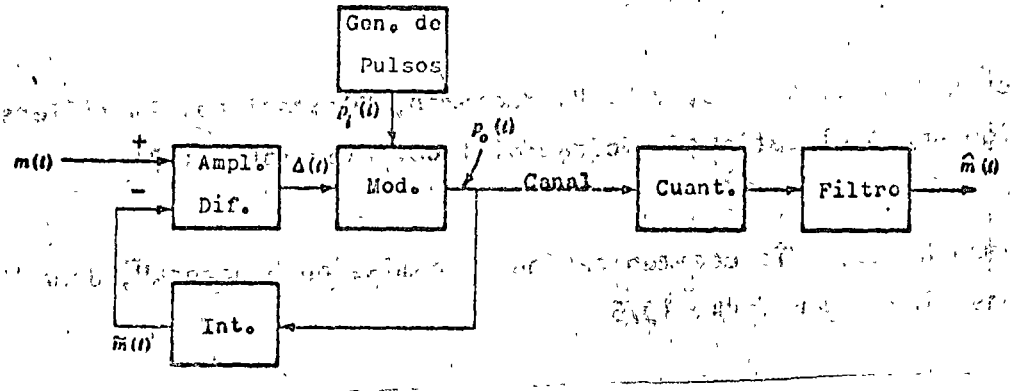


FIG. 3.2.4 SISTEMA DE MODULACION DELTA

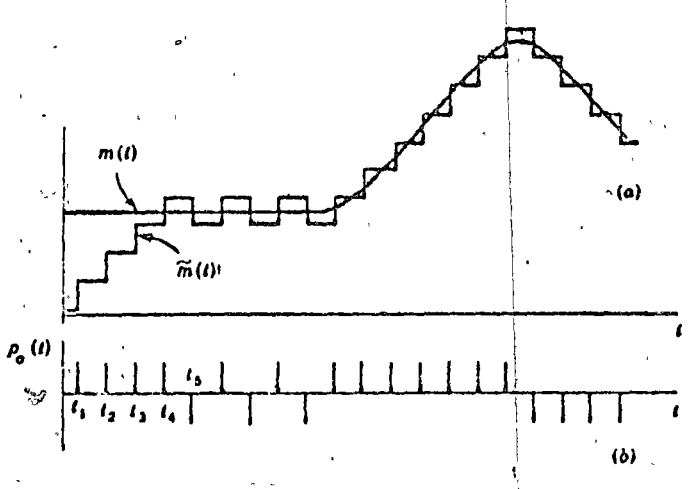


FIG. 3.2.5 FORMAS DE ONDA DE UN SISTEMA MD

(a) La señal m(t) y su aproximación m(t)

(b) El tren de Pulsos Transmitido

R E F E R E N C I A S

- Taub, H. y D. L. Schilling, "Principles of Communication Systems", McGraw-Hill, Kogakusha, Ltd., 1971.

- Tobey G., J. G. Graeme, y L. P. Huelsman, "Operational Amplifiers: Design and Applications", McGraw-Hill Co., New York, 1971

- Freeman R. L., "Telecommunication Transmission Handbook", John Willey & Sons, Inc., New York, 1975

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- Simpson R. S. y R. C. Houts, "Fundamentals of Analog and Digital Communication Systems", Allyn & Bacon, Boston, 1971.

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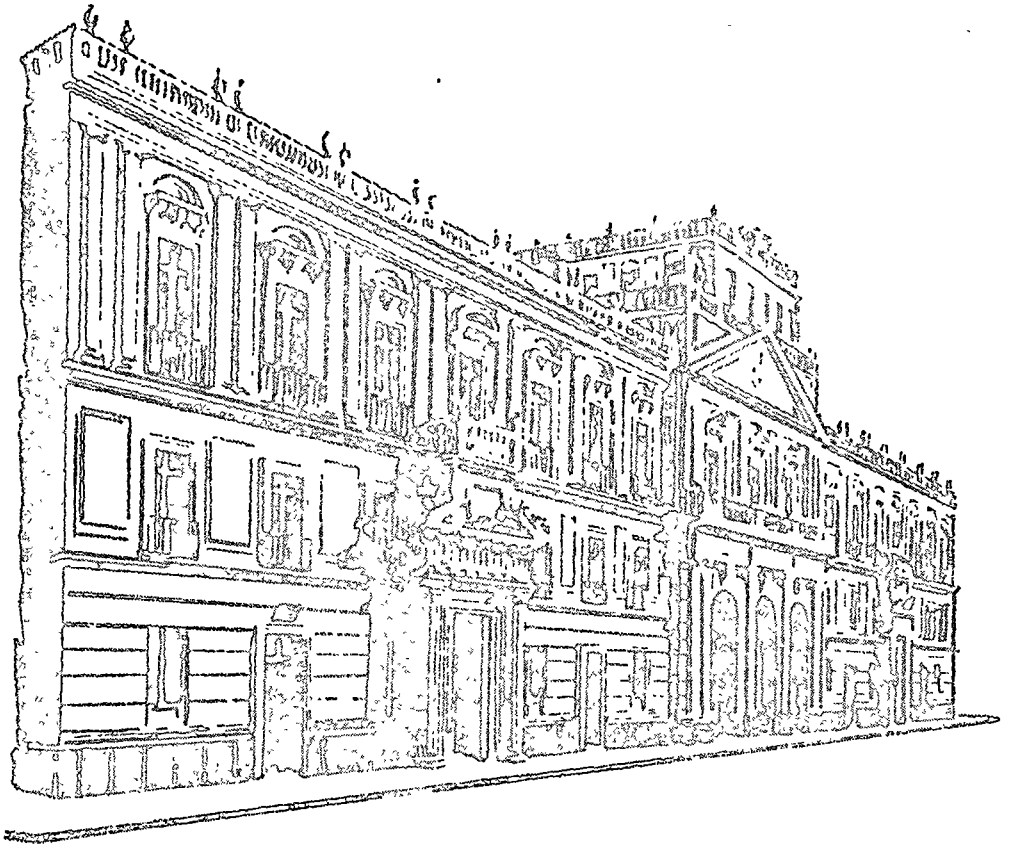
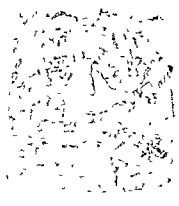
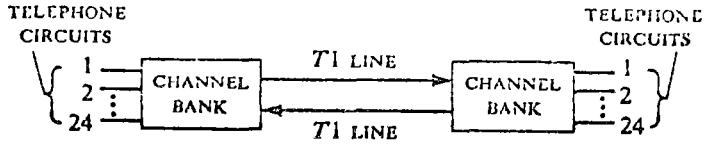


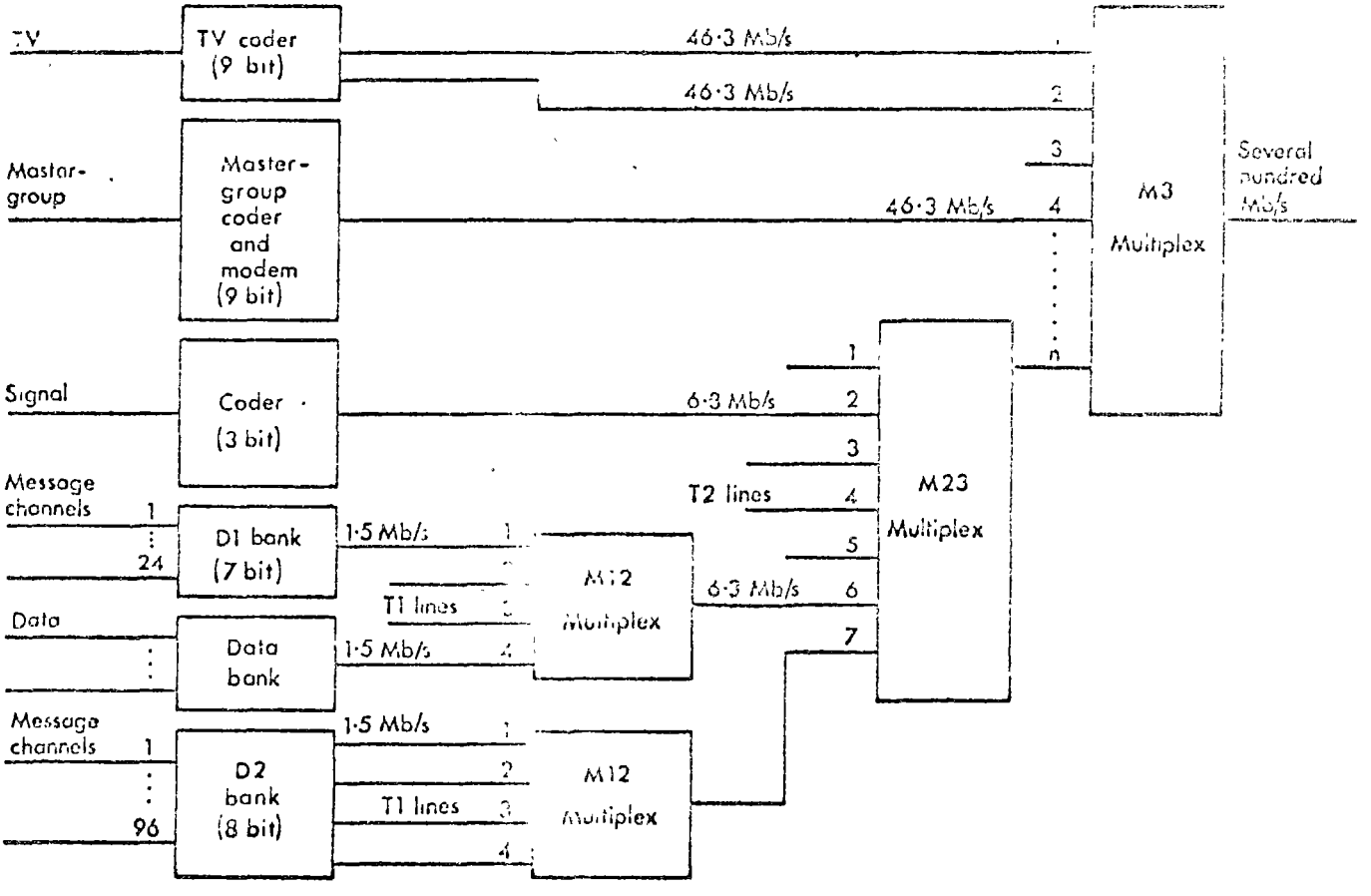
DR. JORGE VALERDI CARAM

AGOSTO DE 1976.

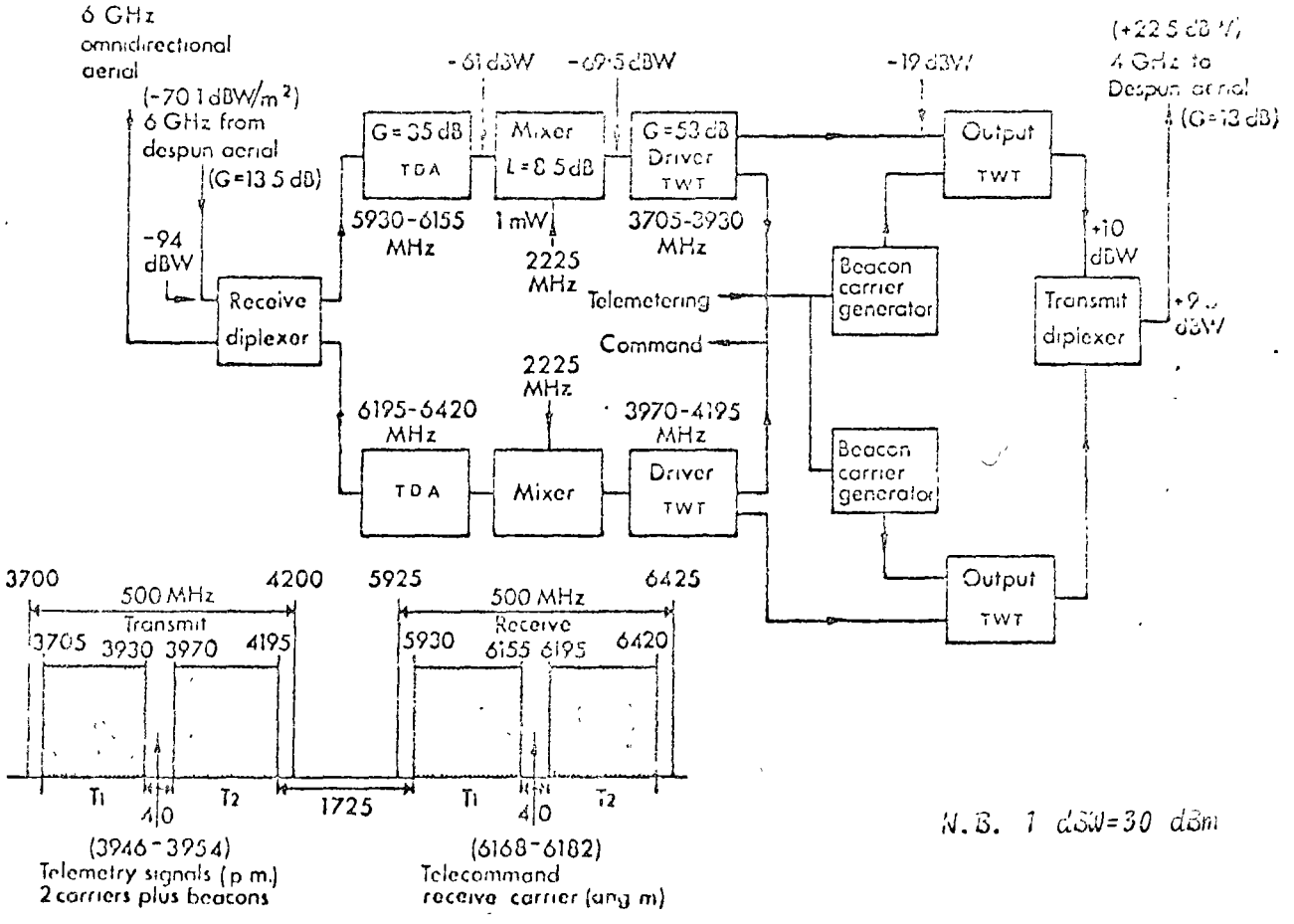




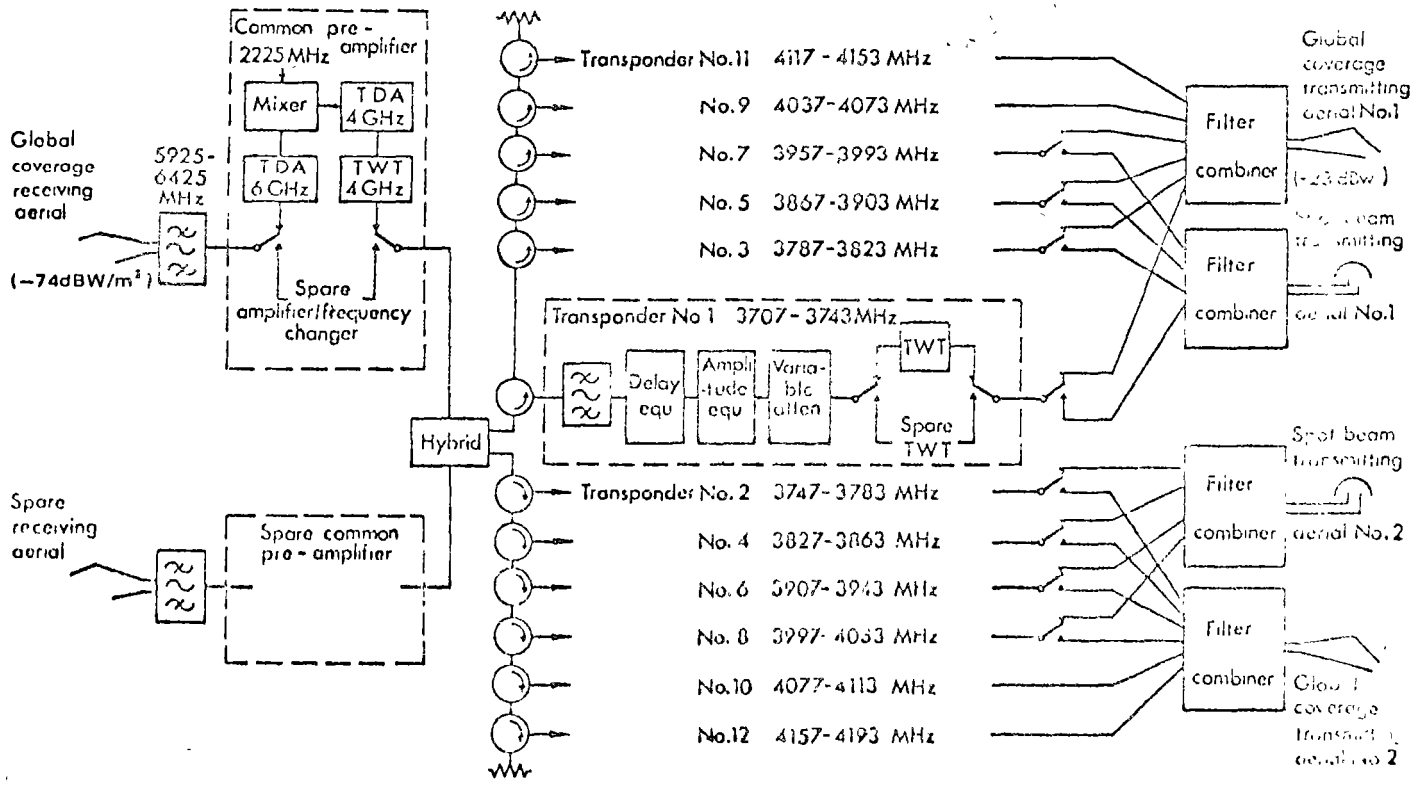
Sistema de Portadoras T1



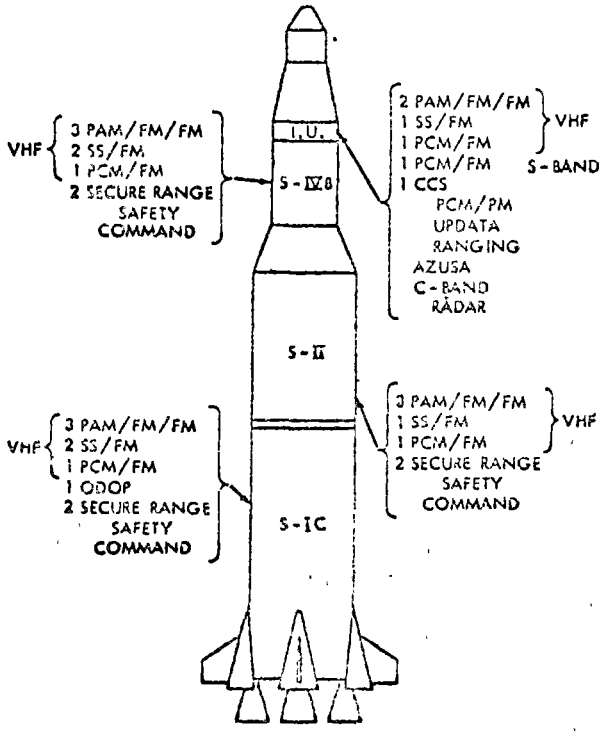
Jerarquía Digital Del Sistema BELL



Sub-sistema del Satelite de Comunicaciones
INTELSAT III



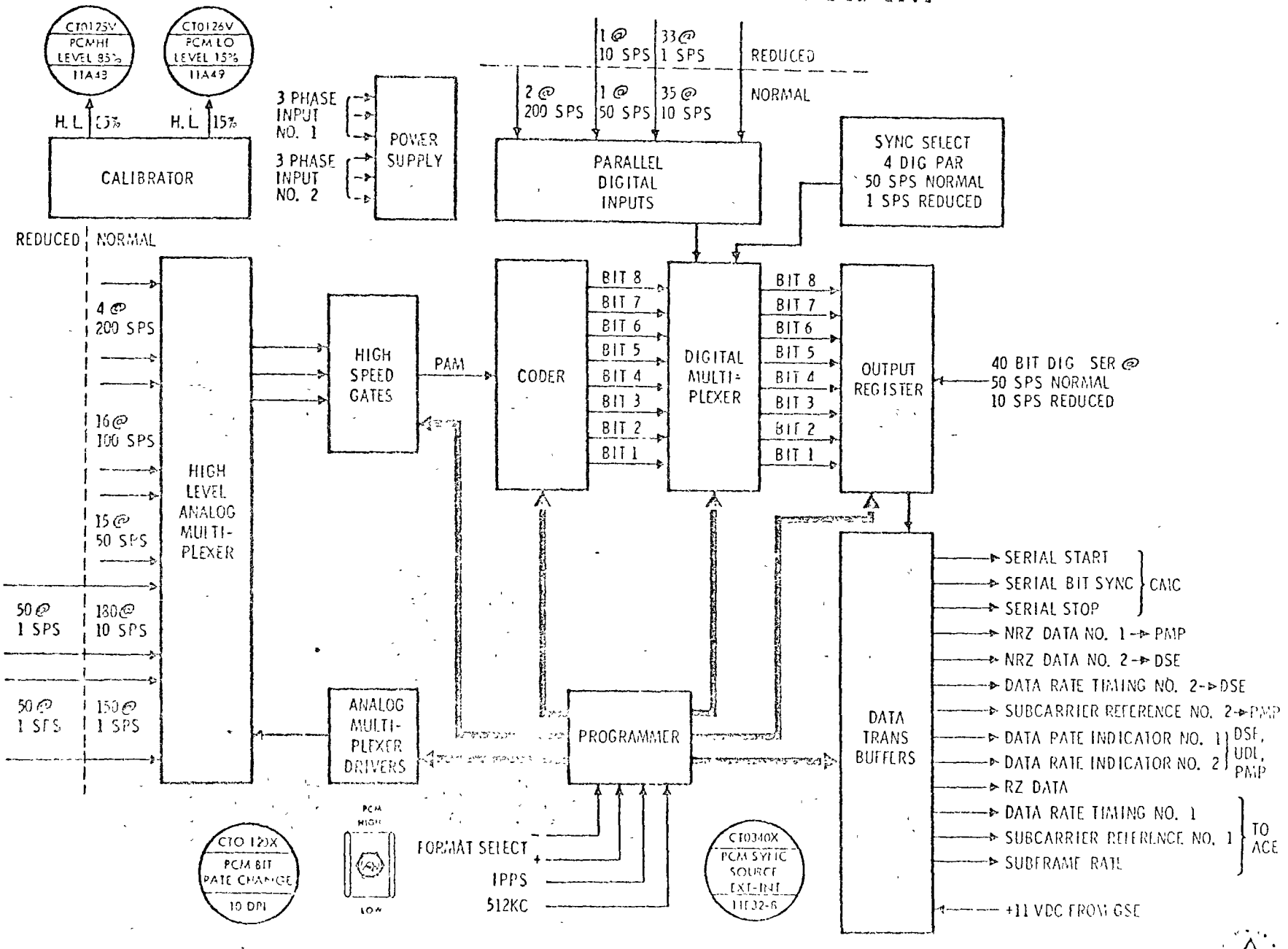
Sub-sistema del Satelite de Comunicaciones INTELSAT IV



Sistema de Instrumentacion del SATURNO V

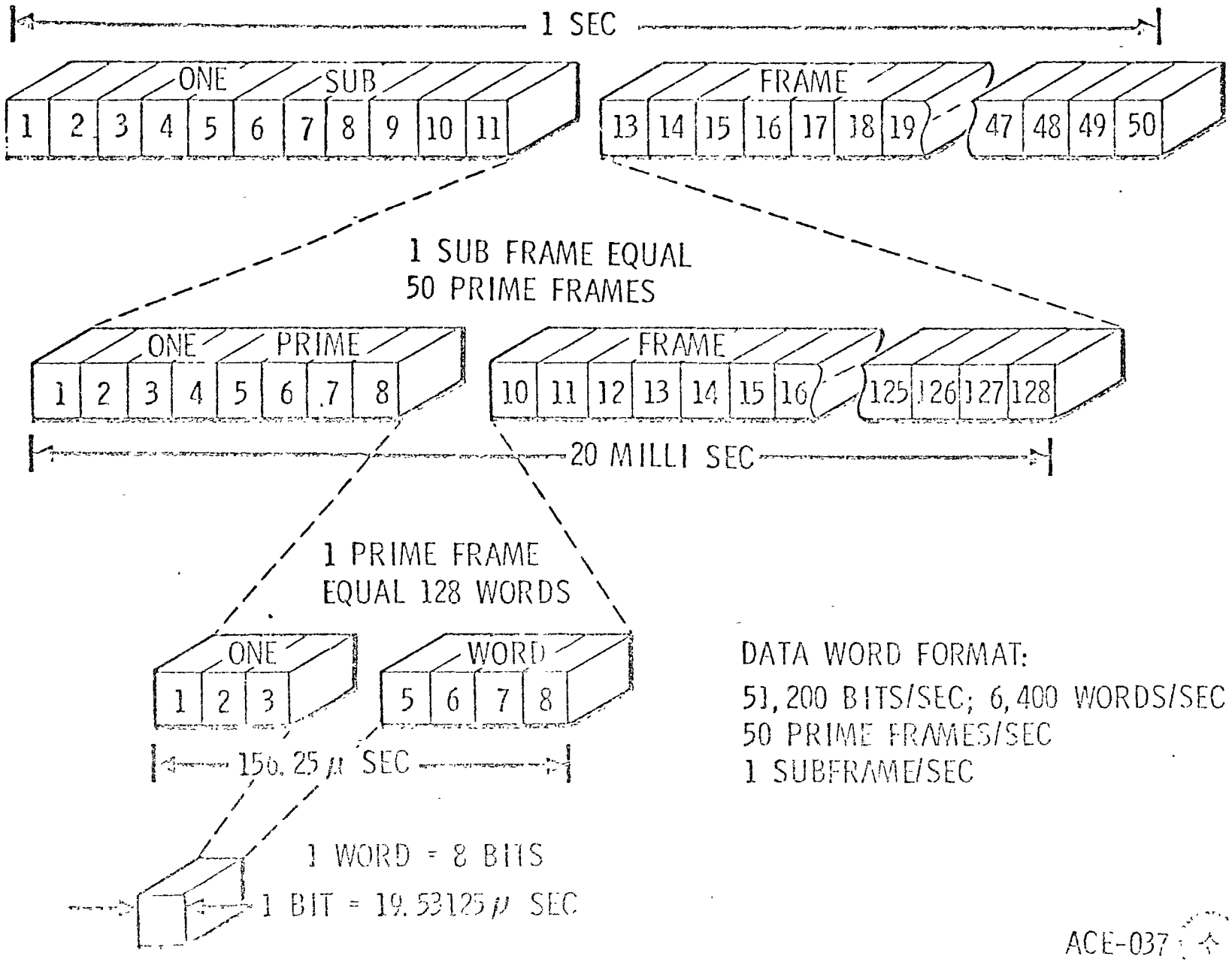
	V H F	U H F
Potencia del Transmisor	+43 dbm	+43 dbm
Modul., Polar. & Cable	- 5.1 db	- 8.1 db
Ganancia Ant. Transm.	- 3.0 db	+12.0 db
Atenuacion del Espacio	-167 db	-185 db (20 000 Km)
Ganancia Ant. Recept.	+18.0 db	+44.0 db
Potencia Entr. al Recep.	-114 db	-94.8 db
Densidad del Ruido	-173.4db/ciclo	-173.4db/ciclo
Potencia del Ruido	-117.3db	-119.2db
S/R Real	+3.2 db	+24.4 db
S/R Requerida	+13.0 db	+13.0 db

PCM BLOCK DIAGRAM



CD-20160

PCM FORMAT

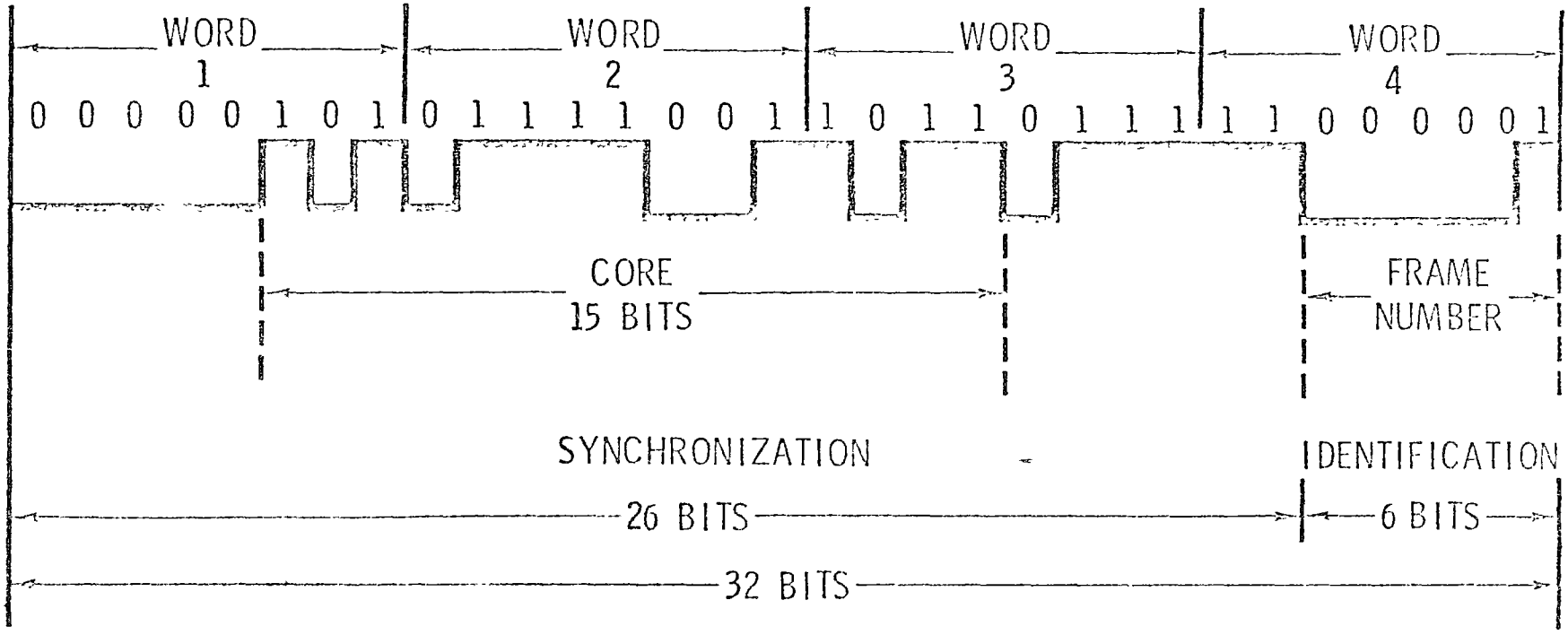


DATA WORD FORMAT:

51,200 BITS/SEC; 6,400 WORDS/SEC
50 PRIME FRAMES/SEC
1 SUBFRAME/SEC

ACE-037

PCM PRIME FRAME SYNCHRONIZATION



PRIME FRAME NUMBER IN BINARY FORM

EXAMPLE: 1 0 0 0 0 0 1 = PRIME FRAME 1

$2^0 = 1$

EXAMPLE: 2 1 1 0 0 1 0 = PRIME FRAME 50

$2^1 = 2$

$2^4 = 16$

$2^5 = 32$

$\frac{}{50}$

CD-218C

PCM NORMAL FORMAT PRIME FRAME NO. 1

BLOCK II

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
				22A 1	22A 2	22A 3	22A 4	11A 1	11A 2	11A 3	11A 4	12A 1	12A 2	12A 3	12A 4
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
11A 5	22D 1	22D 2	10D 1	12A 5	12A 6	12A 7	12A 8	11A 6	11A 7	11A 8	11A 9	51A 1	51A 2	51A 3	51DS 1
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
51DS 2	51DS 3	51DS 4	51DS 5	22A 1	22A 2	22A 3	22A 4	11A 10	11A 11	11A 12	11A 13	12A 9	12A 10	12A 11	12A 12
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
11A 14	22D 1	22D 2	10A 1	12A 13	12A 14	12A 15	12A 16	11A 15	11A 16	11A 17	11A 18	51A 4	51A 5	51A 6	51A 7
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
11D 2	11D 2	11D 2	11D 2	22A 1	22A 2	22A 3	22A 4	11A 19	11A 20	11A 21	11A 22	12A 1	12A 2	12A 3	12A 4
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
11A 23	22D 1	22D 2	10A 2	12A 5	12A 6	12A 7	12A 8	11A 24	11A 25	11A 26	11A 27	51A 8	51A 9	51A 10	51A 11
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
11D 3	11D 4	11D 5	51D 2	22A 1	22A 2	22A 3	22A 4	11A 28	11A 29	11A 30	11A 31	12A 9	12A 10	12A 11	12A 12
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
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SIGNIFICANT DIGIT — NO. OF ZEROS

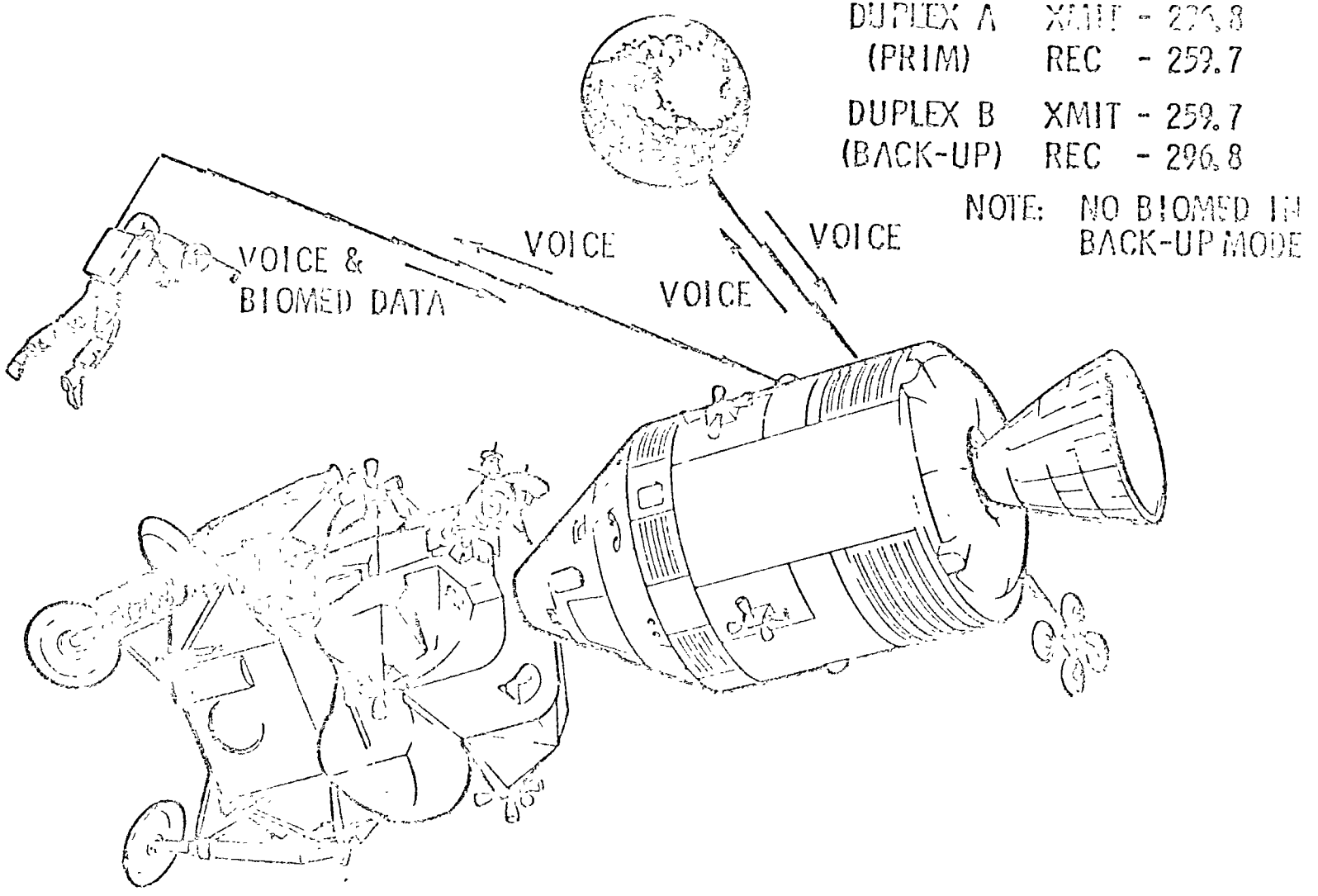
22A
1

CHANNEL

A - ANALOG
DS-DIGITAL SERIAL
DP-DIGITAL PARALLEL

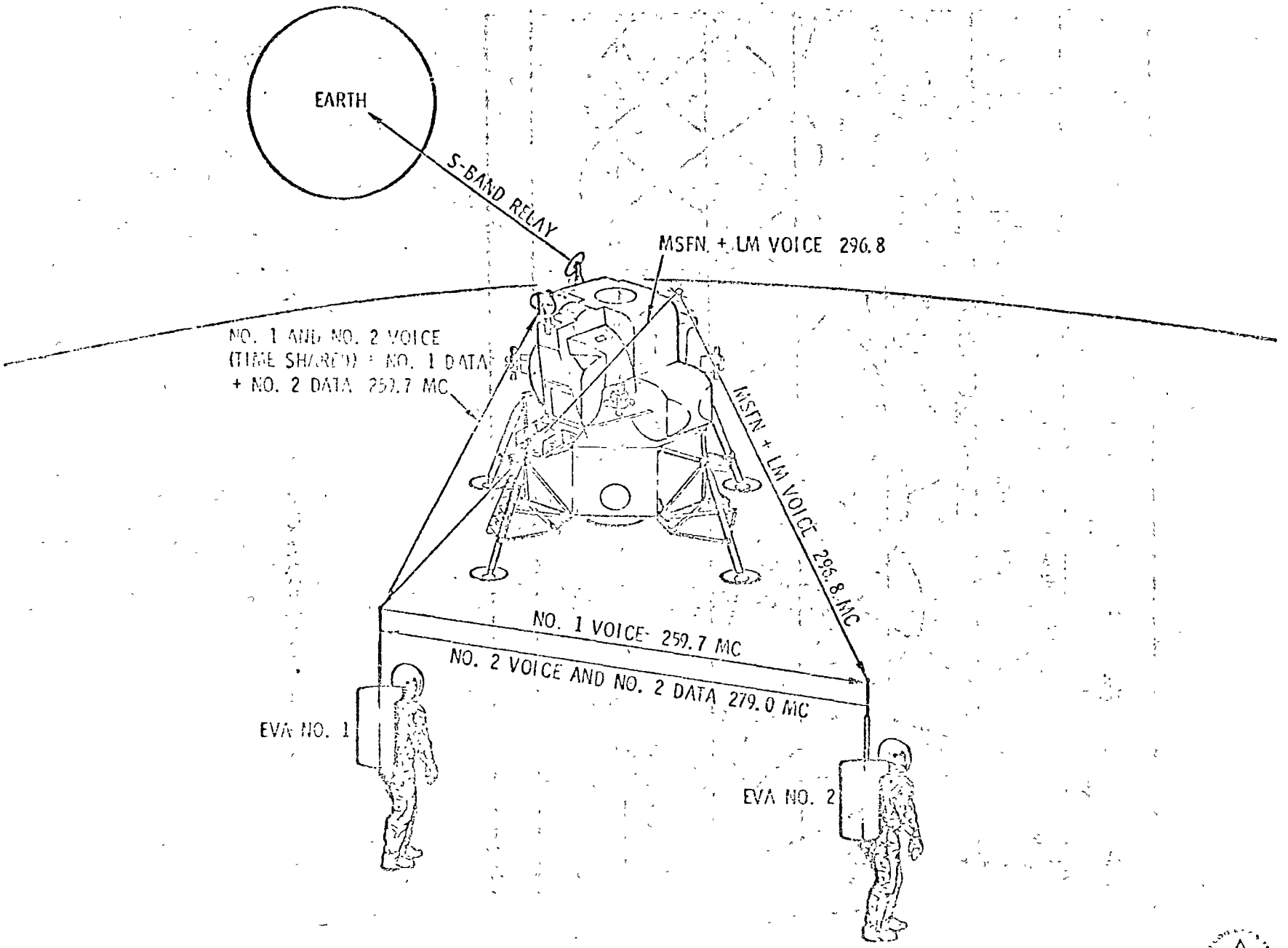
CD-20248

MSFN-CSM-EVA VHF/AM COMM MODE
S-BAND RELAY MODE

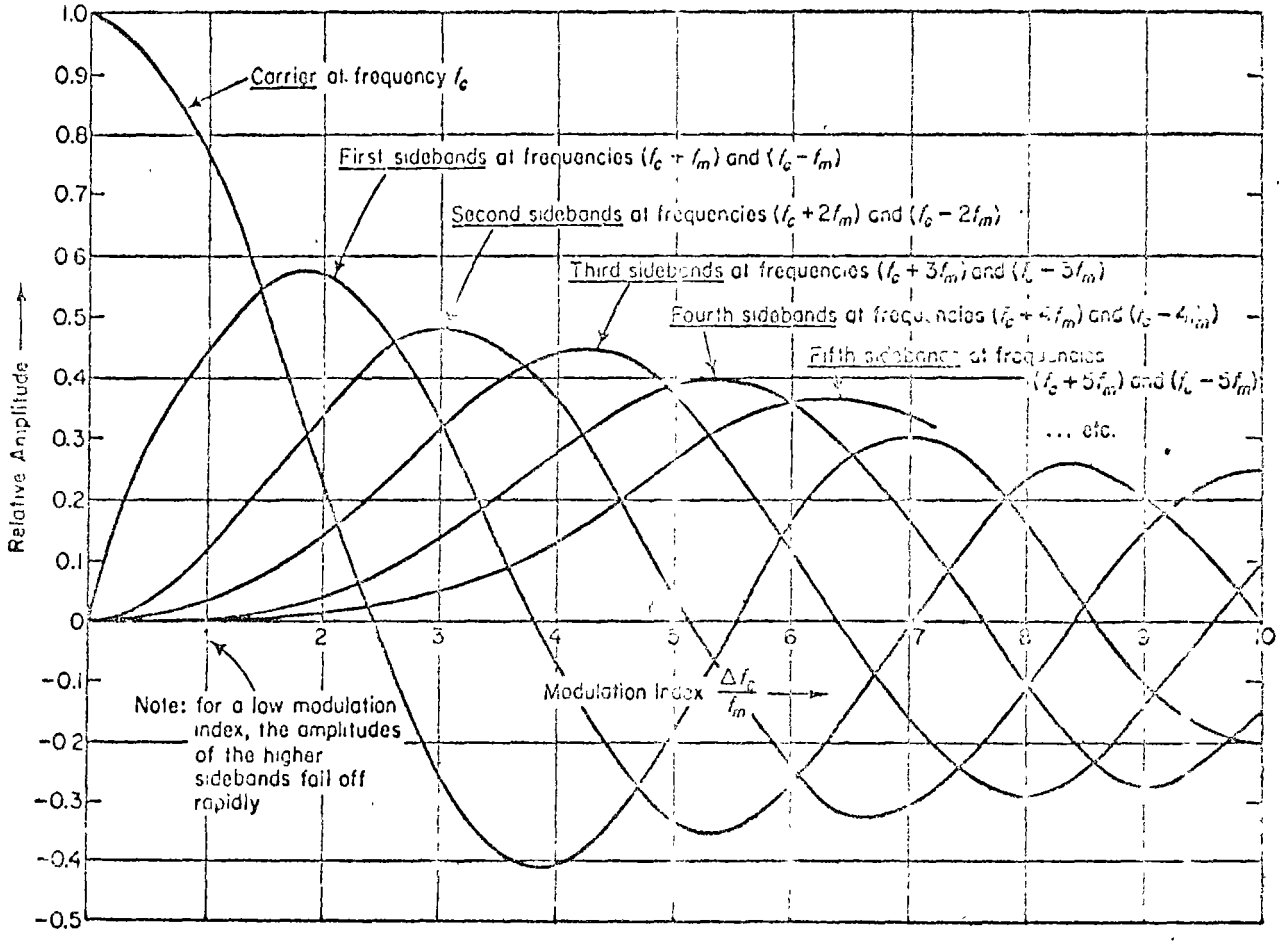


CD-20[illegible]

EVA/LM DUAL RELAY MODE



CD-2124



Componentes Espectrales de una Señal FM

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LA ELECTRONICA EN LAS COMUNICACIONES

Ruido en las Comunicaciones

M. en C. Luis A. Castillo Lanz

IV. RUIDO EN LAS COMUNICACIONES

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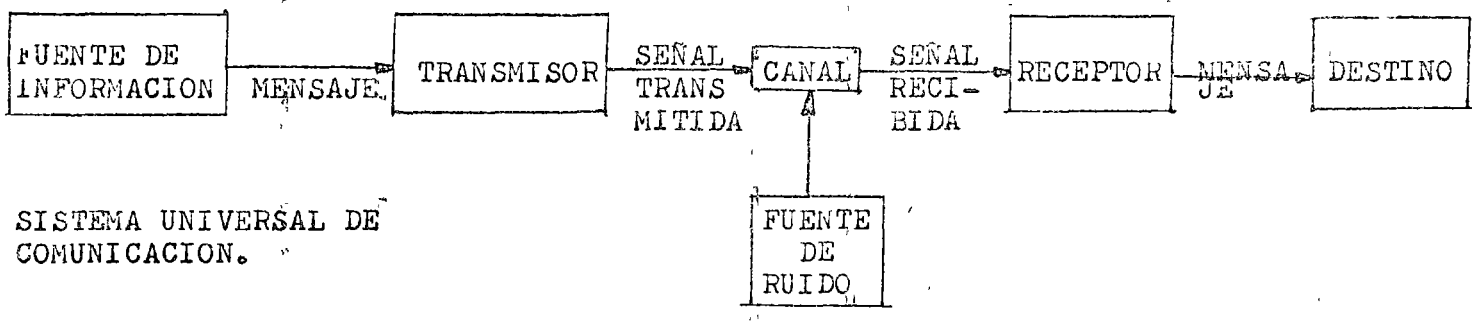
IV. 1 FUENTES DE RUIDO. Todo mensaje recibido puede diferir del mensaje transmitido, es por esto que en el Sistema Universal de Comunicación originalmente propuesto por Claude E. Shannon en 1948 se incluye una fuente de ruido que produce tales alteraciones o mutilaciones sobre la señal.



SISTEMA UNIVERSAL DE COMUNICACION.

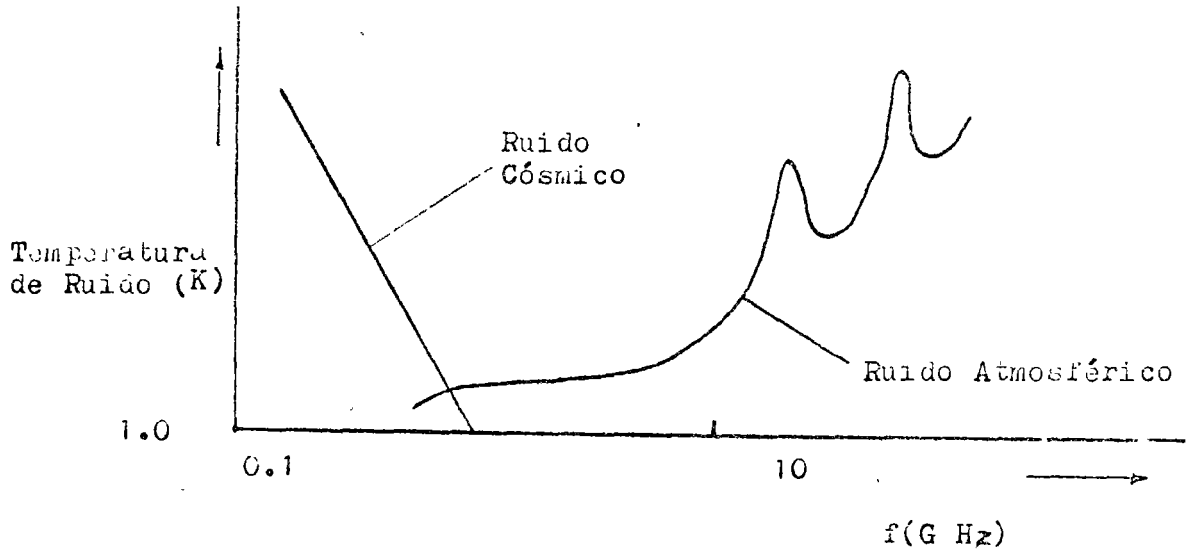
El ruido es un disturbio aleatorio siempre presente en todo Sistema de Comunicación, que se añade a la señal deseada. Su presencia tiende a impedir la recepción de la señal deseada y es un factor limitante en su detección, por lo que es determinante en el funcionamiento del Sistema. Otro factor importante es la interferencia producida por otras señales transmitidas.

El ruido y la interferencia aunque similares son diferentes en cuanto a su naturaleza en un punto importante. El ruido esta compuesto por voltajes de ocurrencia aleatoria no relacionados en fase ó frecuencia. Mientras que la interferencia es periódica y de forma regular.

Las propiedades aleatorias del ruido requieren del estudio de su comportamiento estadístico, mientras que algun conocimiento de sus caracteristicas de fase y frecuencia pueden obtenerse empleando técnicas de Transformada de Fourier.

Podemos distinguir varios tipos de ruido:
El artificial que es principalmente producido por equipos eléctricos de diverso tipo y puede ser eliminado o minimizado por reolocalización del equipo, filtrado, rediseño de componentes, etc.

El ruido natural es debido a radiación cósmica, perturbación atmosférica y ruido de circuito asociado a las componentes electrónicas del equipo.



La radiación cósmica y la perturbación atmosférica generalmente se introducen al Sistema por la antena receptora. El primero comprende principalmente radiaciones electromagnéticas del sol y fuentes galácticas. Su efecto directo puede reducirse apuntando adecuadamente la antena.

Las perturbaciones atmosféricas tales como tormentas eléctricas - son de efectos no continuos, por lo que son muy dificiles de eva - luar y por consiguiente de analizar.

Nos concentraremos en el ruido de circuito que es debido a fluc - tuaciones espontaneas de voltaje (ó corriente), siempre esta pre - sente y representa una limitación básica en la transmisión de - información.

IV. 1.1. RUIDO TERMICO

Los conductores contienen un gran número de electrones "libres" y iones fuertemente ligados por fuerzas moleculares. Los iones - vibran aleatoriamente alrededor de su posición normal (promedio).- La intensidad de esta vibración es función de la temperatura. Suceden entonces continuos choques entre los electrones "libres" y los iones transfiriendose mutuamente energía. Esta constituye la- resistencia del conductor, mientras que los electrones libres constituyen la corriente, la cual sobre un largo período de tiempo da- como promedio cero ya que los electrones se muevon en todas direcciones. Existen fluctuaciones aleatorias sobre este promedio - cuyo valor medio cuadrático es proporcional a KT, donde K es la - constante de Boltzmann $K=1.38\times10^{-23}$ Joule/^{o}K y T la temperatura -

absoluta en grados Kelvin. No existen fuerzas "organizado" este - movimiento en determinadas direcciones por lo que podemos tratarlo como un equilibrio termodinámico.

El efecto del ruido térmico fué primeramente investigado experi - mentalmente por Johnson (1) y teoricamente por Nyquist (2).

Nyquist en su investigación basada en razonamientos termodinámicos (Ver Apéndice), mostró que la Potencia de ruido Pn asociada con - cualquier resistor esta dada por:

$$P_n = kTB \text{ watts}$$

donde $K=1.38 \times 10^{-23}$ Joule/^oK.

T=Temperatura absoluta en ^oK.

B=Ancho de banda del Sistema en Hz.

Resultado que implica condiciones de acoplamiento, caso general en los canales de comunicación, ya que es necesaria la transferencia- de la máxima potencia de la señal atravez del Sistema.

IV. 1.1.1. CIRCUITO EQUIVALENTE

La representación práctica del ruido térmico en una resistencia - es por medio de una fuente $\overline{v_t^2}$ en serie con un resistor sin ruido - (ideal) R según el teorema de Thevenin, o bien una fuente de co - rriente $T_t 2$ en paralelo con una conductancia G, según el teorema - de Norton.

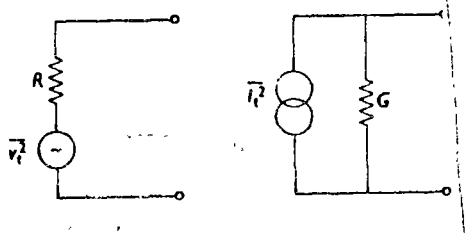


Fig. 3.

Bajo condiciones de acoplamiento, la carga también es R (ideal) y la máxima potencia de ruido disponible es obtenida.

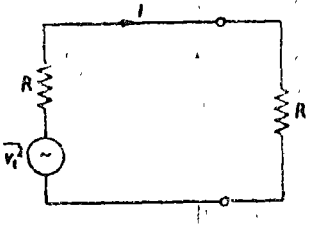


Fig. 4.

$$i = \sqrt{\overline{V_t^2}}\,/2R,$$

$$P_{max} = i^2R = \overline{V_t^2}\,/R^2 \times R = \overline{V_t^2}/4R,$$

De Nyquist $P_{max} = P_n = kTB,$

$$\overline{V_t^2}\,/4R = kTB,$$

$$\overline{V_t^2} = 4kTBR$$

Resultado que fué verificado por los experimentos de Johnson.

Para la fuente de corriente: $\overline{i_t^2} = G^2\overline{V_t^2} = 4kTBG$

IV. 1.1.2. FUENTES MULTIPLES DE RUIDO TERMICO

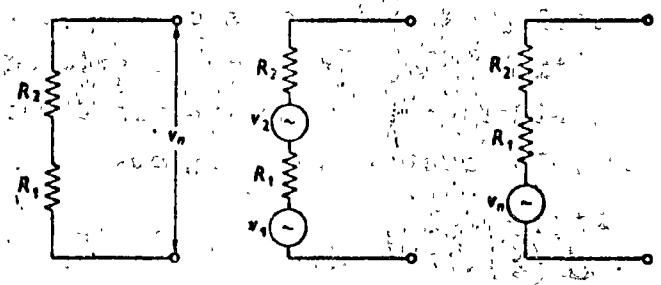


Fig. 5.

Si V_n es el r.m.s. del voltaje de ruido a la salida de las terminales tenemos:

$$V_n^2 = V_1^2 + V_2^2$$

$$V_1^2 = 4kBT_1R_1,$$
$$V_2^2 = 4kBT_2R_2,$$
$$V_n^2 = 4kBT_1R_1 + 4kBT_2R_2,$$

o bien, $V_n = \sqrt{4kB(R_1T_1 + R_2T_2)}$

Generalmente en la práctica ambas resistencias están a la misma temperatura.

$$T_1 = T_2$$

$$V_n = \sqrt{4kTB(R_1+R_2)}$$

de modo que ambas resistensias se comportan como una sola resistencia ruidosa de valor=R_1+R_2 .

IV 1.2. RUIDO IMPULSIVO

El flujo de corriente de un diodo de vacío se debe a la emisión de electrones del cátodo, que entonces viajan hacia el ánodo. Cada electrón lleva una cantidad discreta de carga al ánodo que produce un pequeño pulso de corriente. La suma de todos estos pulsos produce, en promedio, la corriente de ánodo Ia en el diodo.

La emisión de electrones es un proceso aleatorio que depende de las condiciones de la superficie del cátodo, la forma de los electrodos y el potencial entre ellos. Esto da lugar a fluctuaciones aleatorias en el número de electrones emitidos, de modo que la corriente del diodo contiene una componente variable con el tiempo. Cada electrón a su llegada al ánodo es como un impulso de corriente i(t) durante un tiempo τ , como se muestra en la fig6a. Cada pulso puede ser considerado como una función Dirac delta $\delta(t)$ y aproximado por un pulso rectangular, fig.6b.

Por lo que: $$\int_{-\infty}^{\infty} \delta(t)\,dt = e$$

El área del pulso rectangular es tal que:

$$e/\tau \times \tau = e$$

Si $g(\omega)$ es la transformada de Fourier de $\delta(t)$

$$g(\omega) = \int_{-\infty}^{\infty} \delta(t)\, e^{-j\omega t}\, dt = e\ \frac{\operatorname{Sen}\omega\tau/2}{\omega\tau/2}$$

$$y\ |g(\omega)|^2 = e^2 \cdot \left[\frac{\operatorname{Sen}\omega\tau/2}{\omega\tau/2}\right]^2$$

donde $|g(\omega)|^2$ es la densidad espectral de energía.

De la fig. 6 c observamos que si el tiempo τ es muy pequeño, digamos 10^{-9}s, entonces $1/\tau \simeq 10^9$ Hz, y la densidad espectral -

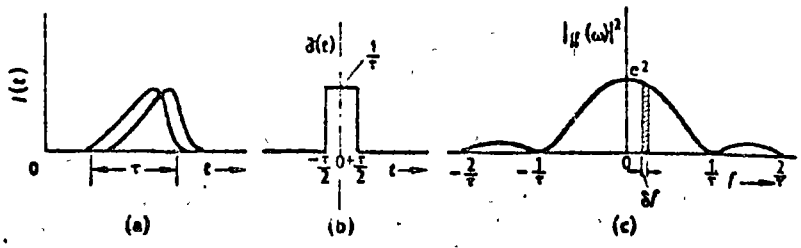


Fig. 6

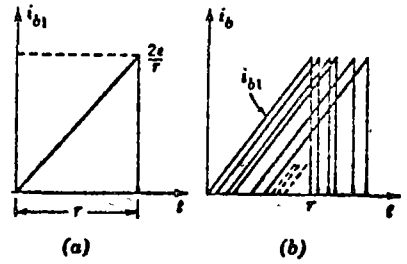


FIG. 7

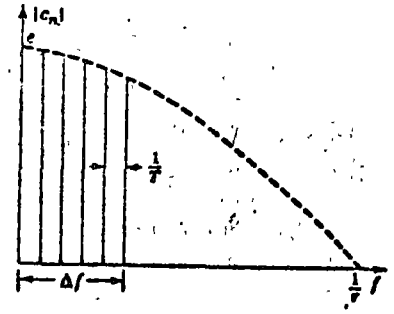


FIG. 8

sobre la banda $\Delta f = B$ es suficientemente uniforme, especialmente a bajas frecuencias. De modo que la energía total W en la banda B esta dada por:

$$W = \int_{-\infty}^{\infty} |g(\omega)|^2 df = 2\int_{0}^{\infty} |g(\omega)|^2 df,$$

$$W = 2e^2 B.$$

Si n electrones llegan al ánodo en un tiempo T, suficientemente largo, la potencia de ruido impulsivo promedio en una carga de $1\,\Omega$ es:

$$I_s^2 = \frac{nW}{T} = n\,2e^2 B/T$$

substituyendo por la corriente de ánodo promedio:

$$I_a = \frac{ne}{T}$$

$$I_s = 2e I_a B$$

$$I_s = \sqrt{2e I_a B}$$

Como un ejemplo, tomemos Ia como $1ma$ y B como 5K Hz entonces:

$$I_s^2 = 2(1.6 \times 10^{-19}) \times 10^{-3} \times (5 \times 10^3) = 1.6 \times 10^{-18}$$

$$I_s = 1.26 \times 10^{-9} \text{ amp. r.m.s.}$$

Del mismo modo usando consideraciones estadísticas se puede demostrar que la emisión de electrones corresponde a la distribución de Poisson de la cual es posible obtener una expresión para el valor medio cuadrático de la corriente de ruido impulsivo $\overline{i_s^2}$.

IV. 1.2.1. CIRCUITO EQUIVALENTE

El circuito equivalente se muestra en la fig. 9 dónde $\overline{i_s^2}$ es el equivalente a un generador de corriente y la resistencia de ánodo del diodo r_d se considera infinita.

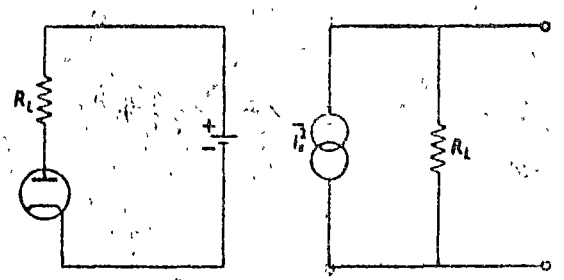


Fig. 9

IV. 1.2.2. RUIDOS TERMICO E IMPULSIVO COMBINADOS.

De hecho el efecto del ruido impulsivo es producir mayor ruido -

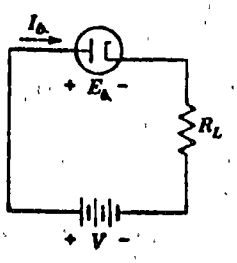


FIG. 10

Circuito de diodo.

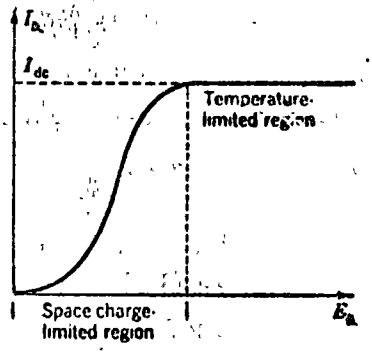


FIG. 11

Característica corriente-voltaje de diodo.

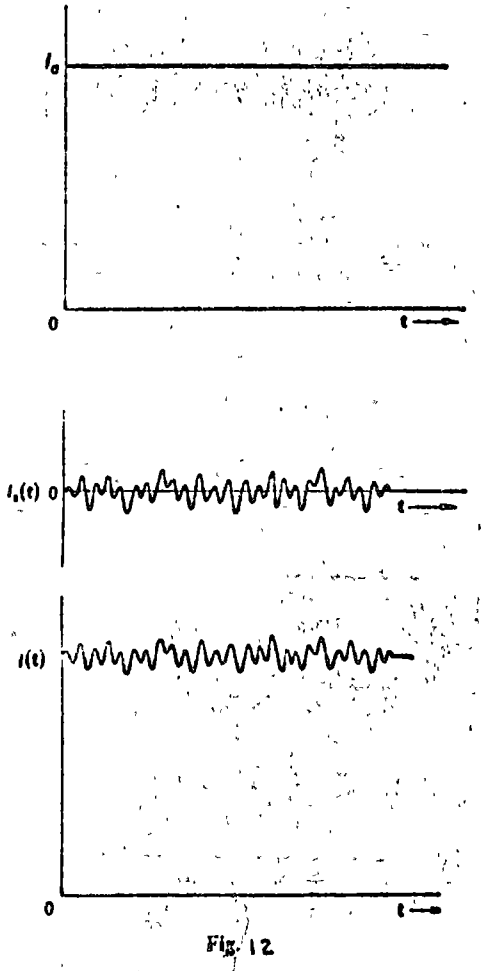


Fig. 12

I_a Corriente de ánodo promedio.

$i_s(t)$ Componente de corriente de ruido impulsivo.

en el circuito como ruido térmico, de modo que puede reducirse a - un equivalente en ruido térmico y asociarse a una resistencia equivalente Req.

Para un triodo, dicha resistencia puede insertarse en serie con - la reja y esta dada por:

$$R_{eq} \simeq 2.5\, g_m$$

dónde g_m es la conductancia mutua del triodo.

El circuito equivalente del ruido térmico e impulsivo combinados se muestra en la fig. 13

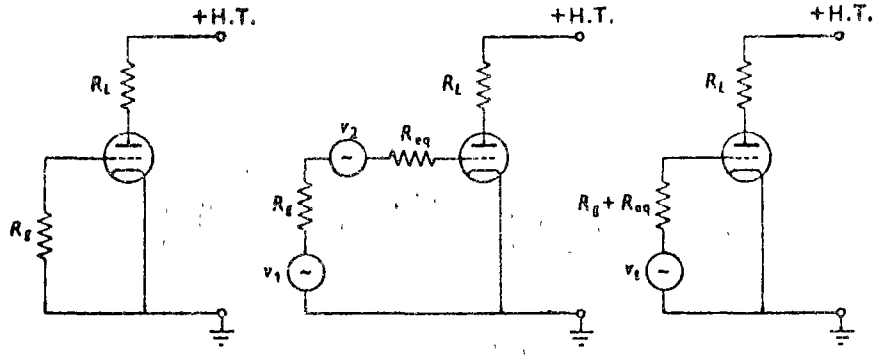


Fig. 13

El voltaje rms del ruido "térmico equivalente" esta dado por:

$$V_t = \sqrt{V_1^2 + V_2^2},$$

$$V_1^2 = 4kTBR_g,$$

$$V_2^2 = 4kTBR_{eq},$$

$$V_t = \sqrt{4kTB(R_g + R_{eq})}.$$

IV. 2. MEDICIONES DE LAS CARACTERISTICAS DEL RUIDO

La forma de onda del ruido es causada por la superposición de un gran número de eventos que ocurren aleatoriamente. Es imposible hacer consideraciones precisas acerca de la magnitud del efecto en algún instante de tiempo en particular, pero ya que se trata de un gran número de eventos su comportamiento en promedio esta bien definido y una descripción satisfactoria de la forma de onda del ruido puede hacerse en términos estadísticos.

La fig. 14 muestra una forma de onda típica del ruido, en la que se observan fluctuaciones alrededor de un valor promedio $\bar{x}(t)$. Para este proceso el promedio en el tiempo es igual al promedio estadístico por lo que se trata de un proceso ergódico. Este valor medio $\bar{x}$ representa entonces la constante o (cero) componente de d.c., que multiplicada por la resistencia da la potencia media.

IV. 2.1. MEDIA Y VARIANZA

En ocasiones es necesario estudiar un proceso con el valor medio $\bar{x}$ sustraído de todos los valores. Esto quiere decir físicamente que estamos interesados en la componente a.c. del fenómeno en estudio.

Esta definido por:

$$\overline{(x - \bar{x})^n}$$

y es conocido como momentos centrales. Para n=1 tenemos cero y para n=2 obtenemos una cantidad conocida como variancia de la distribución.

$$\sigma^2 = \overline{(x - \bar{x})^2} = \overline{x^2} - \bar{x}^2$$

La raíz cuadrada de la variancia es la desviación estandar σ, la cual en nuestro lenguaje corresponde al valor r.m.s. de la componente a.c. . La variancia σ^2 es en ocasiones llamada potencia a.c. en $1\ \Omega$. Para el caso del estudio del ruido $\bar{x}=0$ de modo que:

$$\sigma^2 = \overline{x^2}$$

IV. 2.2. DENSIDAD Y DISTRIBUCION DE PROBABILIDAD.

La distribución de probabilidad que resulta de la adición de los efectos de un gran número de diferentes eventos, según el teorema-

del Límite Central, es la distribución Gaussiana.

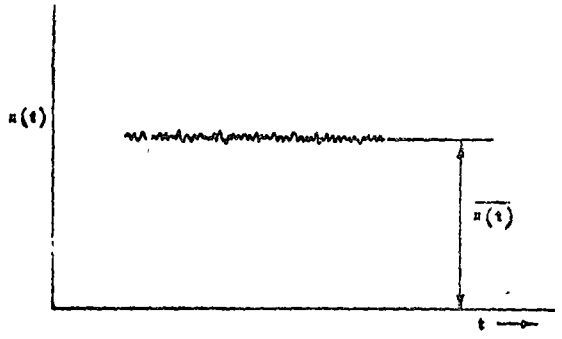


Fig. 14 (a) Típica forma de onda de ruido.

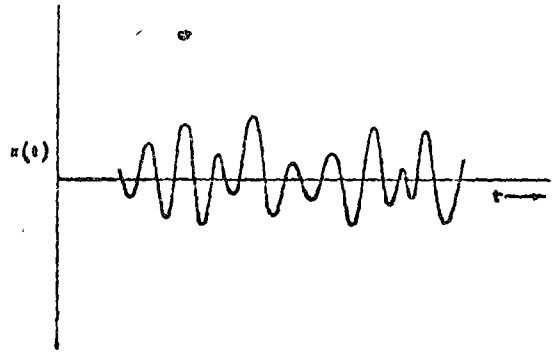


Fig. 14 (b) Diagrama amplificado para mostrar fluctuaciones alrededor del valor medio.

$$F(x) = \frac{1}{\sigma (2\pi)^{1/2}} \exp\left(-x^2/2\sigma^2\right).$$

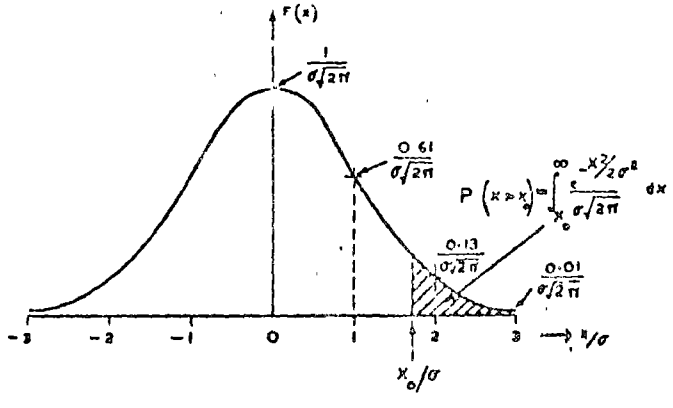


Fig. 15 Distribución de probabilidad de Gauss.

IV. 2.3. ESPECTRO

A continuación enunciaremos las definiciones matemáticas de algu - nos parámetros importantes.

La energía E de una señal f(t) es la energía disipada por un vol - taje f(t) aplicado a una resistencia de 1 ohm.

$$E = \int_{-\infty}^{\infty} f^2(t)\, dt .$$

Si F(w) es la transformada de Fourier de f(t)

$$E = \int_{-\infty}^{\infty} f^2(t)\, dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |F(\omega)|^2 d\omega .$$

De modo que $|F(w)|^2$ es el espectro de la densidad de energía.

Para aquellas señales que se extienden en el intervalo $(-\infty, \infty)$, - tal como el ruido, tienen energía infinita. Por lo que en estos - casos es necesario definir la potencia promedio disipada por un - voltaje f(t) aplicado a una resistencia de 1 ohm.

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f^2(t)\, dt .$$

$$P_{av} = \int_{-\infty}^{\infty} \lim_{T \to \infty} \frac{|F_T(\omega)|^2}{T}\, df = \int_{-\infty}^{\infty} G(f)\, df .$$

Donde G(f) es la densidad de potencia espectral, definida como - la potencia promedio a la frecuencia f en una resistencia de $1\,\Omega$. Una medida de la cantidad de ruido producido por un circuito tal - como un amplificador ó un receptor, puede tenerse al comparar las- relaciones de señal a ruido a la entrada y a la salida, como se - muestra en la fig. 16.

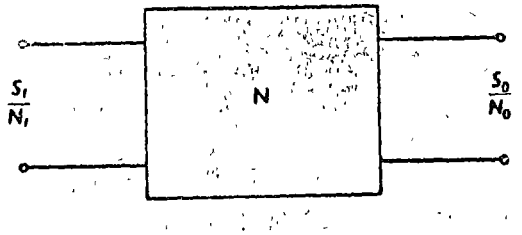


Fig. 16

Por lo que entonces el Factor de ruido será:

$$F = \frac{(S_i/N_i)}{(S_o/N_o)} ,$$

o bien $$F = \frac{N_o}{S_o/S_i \times N_i} ,$$

Si G es la ganancia del circuito y Ni=KTB

$$F = \frac{N_o}{GkTB}$$

IV. 2.3.1. CIRCUITOS EN CASCADA

Consideremos dos circuitos en cascada con factores de ruido F_1, F_2 y ganancias G_1, G_2 respectivamente. Si F es el factor de ruido de la combinación de ambos circuitos en la banda B y, alimentamos una señal de ruido con potencia KTB, tendremos:

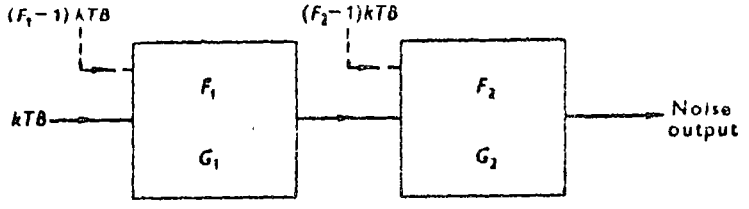


Fig. 17.

$$F = \frac{F_1 kTB G_1 G_2 + (F_2-1) kTB G_2}{kTB G_1 G_2} ,$$

$$F = F_1 + (F_2-1) / G_1 .$$

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LA ELECTRONICA EN LAS COMUNICACIONES

APLICACION A LAS COMUNICACIONES DIGITALES

3.3 MULTIPLEXAJE EN TIEMPO

DR. JORGE VALERDI CARAM

AGOSTO DE 1976.

3.3 MULTICANALIZACION

La multicanalización en tiempo (MT) divide la señal transmitida en intervalos discretos de tiempo, cada uno capaz de portar información de una entrada diferente. Un sistema conceptual MT se muestra en la figura 3.3.1. Las diferentes señales que se van a transmitir son periódicamente muestreadas y usadas para modular una portadora de pulsos MAP, la cual produce la señal de banda base que se ilustra en la figura 3.3.2.

Puesto que una señal particular tiene acceso al canal sólo durante períodos de tiempo recurrentes, MT es un proceso en serie contrastado con MF el cual es un proceso paralelo.

Generalmente, el conmutador es implementado haciendo uso de circuitos electrónicos; aunque algunos sistemas absoletos utilizaron conmutadores rotatorios mecánicos. En el lado del receptor, otro conmutador en sincronía con el conmutador del transmisor, separa los pulsos recibidos y los aplica a los demoduladores de pulsos, los cuales en la mayoría de los casos son filtros paso-bajo.

Un ejemplo de un conmutador construido de interruptores MOSFET se muestra en la figura 3.3.3. La salida de cada interruptor está conectada a un nodo común el cual es la salida del conmutador. Cada circuito alimentador aplica voltaje a la compuerta (G) de un interruptor MOSFET. Este voltaje controla el estado del transistor MOSFET: un nivel de -15v. lo apaga y un nivel de +15v lo prende. Las entradas de la lógica de control que originan estos estados son 0v. y + Vv., respectivamente.

Con fuentes de alimentación de $\pm$15v. y un rango dinámico de $\pm$ 10v. para la señal analógica de entrada, el transistor MOSFET debe tener un voltaje de corte de compuerta-fuente de -5v. máximo, y voltajes de rompimiento de compuerta-fuente y compuerta-colector de $\pm$ 25 v. mínimo.

El nodo de salida del conmutador debe de conectarse a una carga de alta impedancia para prevenir que parte de la entrada analógica sea absorvida a través de la resistencia de colector-fuente del canal que esté prendido. De

no ser ésto posible, entonces el conmutador debe estar seguido de un amplificador acoplador para así aislar la carga del nodo común.

El amplificador debe de dar una ganancia unitaria muy exacta, la cual requiere que el rechazo en nodo común y la ganancia a circuito abierto del amplificador operacional sean altas. Una exactitud de 0.01% en la ganancia requiere que ambos parámetros sean mayores que 80 dB.

Conmutación utilizando un contador binario

En la figura 3.3.4 se muestra un conmutador que utiliza un contador binario a base de flip-flops, para seleccionar en forma secuencial, las 10 entradas analógicas.

En este contador, si un 1 aparece en el primer flip-flop y todos los demás están puestos a 0, el 1 circulará en forma continua alrededor del contador siempre y cuando los pulsos del reloj existan.

Puesto que solamente un flip-flop tiene un 1 a la vez, y el 1 permanece constante durante la duración del pulso del reloj, el interruptor analógico (IA) conectado a este flip-flop será el único seleccionado y el voltaje analógico de ese canal es el único que estará presente a la salida del conmutador.

Conmutación con transistores bipolares

En la figura 3.3.5 se muestra un conmutador construído para aplicaciones de PCM en telemetría (fabricado por GE) y diseñado para conmutar señales analógicas de 0 a 5 v. de una fuente cuya resistencia máxima fuera de 5000 Ω , y con una exactitud de $\pm$ 0.2% de la escala máxima.

En este circuito en particular se tienen 64 entradas de señal analógicas. Estas entradas están divididas en 8 grupos de 8 canales cada uno, y cada grupo de 8 interruptores analógicos conectados a 1 de las 8 ramas.

Las ventajas de esta configuración son que las corrientes de fuga provenientes de los canales apagados que fluye en los canales prendidos son altamente reducidos, y la serie de configuraciones de interruptores con pares de transistores que hay para cada interuptor analógico se obtiene sin pagar el exceso de dos transistores

de conmutación por canal.

Para seleccionar un canal en particular, su línea de selección debe estar a un potencial cercano a 0v, para que el transistor de comando del interruptor analógico esté polarizado de tal manera que no conduzca. Bajo estas condiciones, la corriente de comando en la base del transistor-interruptor, fluirá para ese canal, haciendo uso de la fuente V_a de +15v

Por ejemplo, si el canal 1 es seleccionado, los transistores-interruptores Q_{1-1} y Q_{2-1} conducirán (estarían prendidos), es decir, los transistores Q_{3-1}, Q_{4-1}, Q_{5-1} y Q_{6-1} no conducirían (estarían apagados). Para habilitar el sumidero de corriente a la corriente de base aplicada al interruptor analógico, los transistores Q_{7-1} y Q_{8-1} conectados a los colectores de estos interruptores están también apagados durante el tiempo de selección. Bajo estas condiciones, una corriente igual a la que ha sido suministrada a las bases de Q_{1-1} y Q_{2-1} es conducida hacia la fuente de -24v a través de la resistencia de 825 000 Ω .

La función del amplificador operacional que controla los colectores de todos los transistores de conmutación analógica de las ramas, es la de proporcionar mejor exactitud. Este amplificador disminuye el error de conmutación analógica.

Selección y diseño de conmutadores Analógicos

Como ya se ha mencionado, interruptores analógicos no son perfectos, y que conforme conmutan señales analógicas también añaden errores a dichas señales. Estos errores están en función de la "transmisión" de la señal de alimentación del interruptor a la línea de la señal analógica, es decir, el voltaje V_{OF}, así como la resistencia de saturación durante conducción r_s, y la impedancia de apagado y corrientes de fuga del interruptor.

A continuación se da un listado de éstos y otros parámetros de importancia que deben ser considerados en la selección o diseño de un conmutador analógico.

1. La exactitud total de conmutación, requerida. Este factor es de importancia cuando se están determinando las características eléctricas del conmutador.

2. Número de canales.
El número de canales conmutados tiene un efecto directo en la exactitud. Algún tipo de ramificación puede ser necesaria si dicho número es muy grande. Las corrientes de fuga y la capacitancia aumenta conforme el número de canales aumenta, Si la capacitancia aumenta, la velocidad de conmutación disminuye, y más tiempo es necesario para que los transientes se atenúen a niveles de error aceptables.

3. Polaridad y rango de valores de voltaje analógico de entrada.
Además de la polaridad y voltajes de operación supuestamente normales, es importante conocer el máximo voltaje posible en ambas polaridades. Si el voltaje de algun canal analógico resulta ser más alto que lo normal, la operación de conmutación en los otros canales debe ser insensible a esta anomalía.

4. Impedancia de la fuente de voltaje analógico.
La resistencia de la fuente es normalmente la mas importante. En algunos casos donde el valor de resistencia es alto, la capacitación de la fuente puede ser importante. Este es el factor que determina la corriente permisible de salida del conmutador y la cantidad de señal de control (comando) de interrupción que alimenta la fuente

5. Diferencia de voltaje entre la fuente analógica y la referencia de tierra.
En sistemas complejos puede haber diferencias considerables en los voltajes de tierra a los que algunos canales de entrada analógicas se refieren, debido a las caídas en voltaje de la línea de tierra entre los diferentes equipos. Este hecho determina la necesidad por un rechazo en modo común y una conmutación diferencial en las entradas analógicas.

6. Cruce entre canales.
Este es la fuga de una señal (resistiva, capacitiva, radiada) de los canales que no están prendidos, hacia los canales que sí están prendidos.

7. Razón de muestreo.
Esta razón es determinada por el ancho de banda de la señal analógica que debe de recuperarse.

8. Tiempo de encendido.
Este es el tiempo requerido, después de que la señal de control es recibida, para que la salida analógica del conmutador iguale la entrada, con una cierta tolerancia.

9. Tiempo de apagado.
Este es el tiempo requerido, después de que la señal de control ha dejado de ser aplicada, para que tanto la impedancia de conmutación (de apagado) y por los transientes, alcancen valores especificados.

10. Tiempo de muestra durante el encendido.
En el caso de comandos por medio de transformadores o capacitadores en transistores bipolares, este es un factor importante. El tamaño del transformador o del capacitor, está determinado por esta duración.

11. Impedancia de carga, originada por la salida del interruptor analógico.
La corriente, resistencia y la capacitancia del circuito comandado por la salida del interruptor analógico, deben ser consideradas. Por ejemplo, si un amplificador diferencial de transistores es comandado, no sólo la impedancia de entrada del amplificador es importante; también la corriente de polarización de entrada a los transistores del amplificador diferencial, que fluye a través del interruptor analógico y consecuentemente también en la fuente de voltaje analógico, causando errores.

12. Requisitos físicos.
Estos factores incluyen tamaño, peso, vida, rango de temperatura, vibración, impacto, humedad y gases corrosivos.

13. Potencia de entrada.
Los voltajes y los watts constituyen la potencia de entrada. Las variaciones en la potencia de voltaje de entrada, incluyendo exactitud a corriente directa, rizo, y los transitorios, deben de ser considerados en el diseño del conmutador.

TABLA 1

PARAMETROS EN LA CONMUTACION DE SEÑALES ANALOGICAS PARA VARIOS TIPOS DE TRANSISTORES

Analog Switch Type	V_{nf}				r_s* at I_{BC} = 1 mA, Ω	I_c at 25°C, nA	C_o, pF	h_{FEI} at 25°C	$\frac{\Delta V_{OF}}{\Delta I_B}$
	Inverted Connection at I = 1 mA		Normal Connections at I = 1 mA						
	Single Transistor V_{OFI}, mV	Matched Transistors ΔV_{OFI}, mV	Single Transistor V_{OFN}, mV	Matched Transistors ΔV_{OFN}, mV					
Silicon diode	...	...	600	10	50	1-50	1-10	...	...
Silicon transistors									
Alloy	0 5-3	0 1	10-25	1-2	5-30	1-20	5-30	1-10	Low
Grown	30-100	...	10-80	...	100-300	1-500	5-20	1-3	High
Mesa	1-50	0 1-5	20-100	2-10	50-100 200-2 K	1-500	5-75	0 01-0.6	High
Planar	1-...	0.1-...	30-...	3-...	50-100	0 01-10	2-75	0 1-1	High
Planar epitaxial	0.2-2	0.05-0.5	10-20	1-2	5-20	0 01-10	2-75	1-10	Low
Integrated transistor (2 devices on a single silicon substrate)	...	0.025	...	...	20-200	0 01-10	2-[illegible]	...	Low
Germanium transistors									
Alloy	0.2-2	0.05-0.5	5-10	0.5-1	2-10	1,000-10,000	2-50	1-5	Low
Field effect transistors									
Junction	0.0	0 0	0.0	0.0	2-4000	Alloy. 10-1000 Planar: 0 01-100	2-70	...	Voltage-controlled device
MOS	0.0	0 0	0.0	0.0	2-...	0.001-...	2-...	...	Voltage-controlled device

* Los rangos de los parámetros en r_s son valores aproximados para transistores de baja potencia y pueden cambiar como resultado de las mejoras en los procesos de manufactura.

V_{of} = voltaje a través de un diodo como resultante de la corriente de polarización directa

h_{FEI} = ganancia en corriente

V_{OF} = voltaje de desviación que aparece a través de las terminales C-E de un transistor cuando está encendido por una corriente de base, y la corriente a través C-E es cero

V_{OFN} = voltaje de desviación a través de las terminales C-E cuando la corriente de base en exceso que satura al transistor, fluye de B-E, es decir, en la conexión normal

V_{OFI} = voltaje de desviación existente a través de las terminales C-E cuando la corriente de base en exceso que satura al transistor, fluye de B-C, es decir, en la conexión invertida

r_s = resistencia dinámica de conducción

I_{BC} = corriente directa que fluye de las terminales B-C

ANEXO: Comparación de varios tipos de transistores de conmutación

En la Tabla 1 se dá una comparación de los parámetros analógicos de conmutación para varios tipos de transistores. Varias observaciones se pueden hacer a partir de dicha tabla.

- para transistores bipolares, el voltaje V_{OF} invertido es generalmente mucho menor que el voltaje V_{OF} obtenido cuando el transistor se conecta en la forma acostumbrada.

- algunos transistores, tales como los de unión por crecimiento de silicio, pueden dar un voltaje en la conexión normal V_{OF} menor que su voltaje invertido V_{OF}. Esto es debido a que para este tipo de transistor, la región del colector tiene más resistencia que la región del emisor. Por lo tanto para valores más altos de corriente base, la corriente de base de encendido en conexión invertida que fluye de la base al colector origina una caída de voltaje relativamente grande en la región del colector. Algunos de los transistores fabricados por crecimiento de silicio, tal como el 2N336, pueden usarse como interruptores a corriente alterna de voltajes analógicos, es decir, cortadores de señal (o chopers), debido a su baja capacitancia de salida Co; sin embargo, estos transistores deben ser excitados con corrientes de base muy pequeñas para que la caída a través de la resistencia de colector o emisor no sea un problema.

- los transistores de fabricación por crecimiento, mesa, y planares, tienen generalmente resistencia de colector mayores que los transistores por aleación y los epitaxiales planares, lo cual resulta en un voltaje V_{OF} y resistencias de saturación, mayores. Además, la geometría física del transistor mesa resulta en un valor de beta inversa extremadamente pequeña, lo cual hace muy difícil el utilizar este tipo de transistor como conmutador analógico para señales bipolares.

- en general, para transistores bipolares, los tipos epitaxiales

planares de silicio y los de aleación tienen las mejores características para conmutación analógica. Tienen el voltaje V_{OF} mas bajo y por lo tanto el menor incremento ΔV_{OF} cuando están bien acoplados; la resistencia r_s mas baja; una corriente de fuga mínima h_{FEI} es grande, y una variación de V_{OF} respecto a variaciones en corriente de base ΔI_B menor que los demás

- en muchas aplicaciones el transistor FET es el mejor interruptor analógico.

- el transistor MOSFET es bastante popular en sistemas de conmutación y multiplexaje analógico de baja corriente debido a las ventajas que tiene con el transistor bipolar por lo que respecta a exactitud y simplicidad en circuito.

- por las mismas razones los transistores de unión FET de resistencia r_{ds} baja son muy usados en la implementación de decodificadores D/A muy exactos.

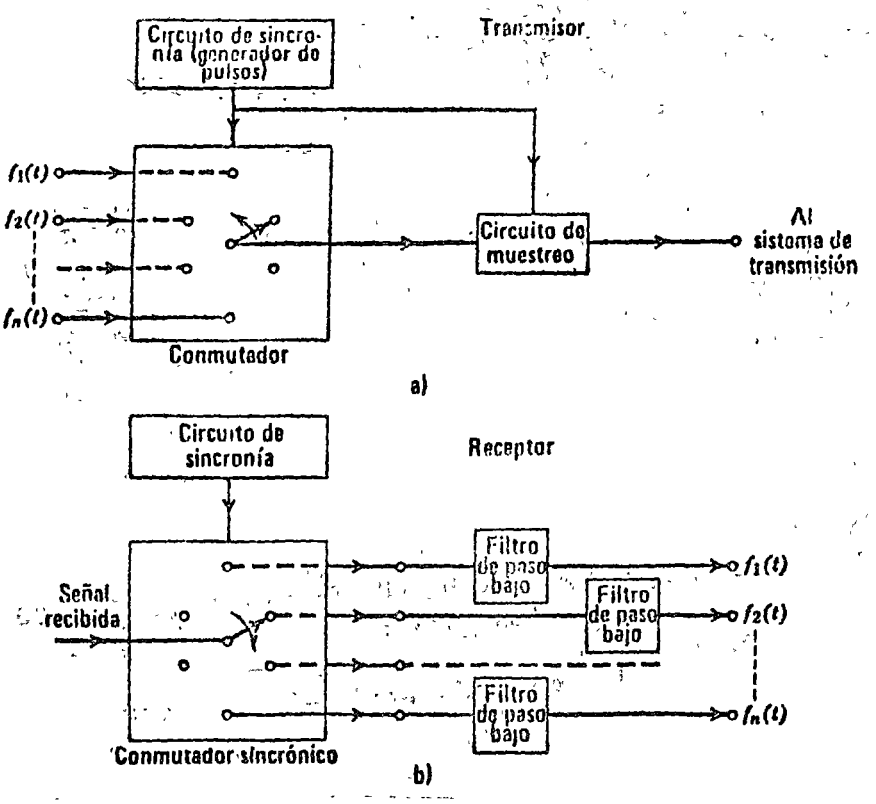
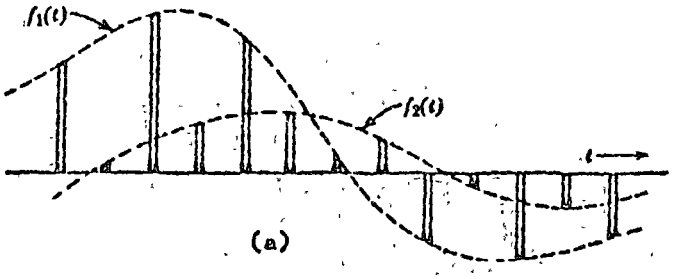


FIG. 3.3.1 SISTEMA CONCEPTUAL DE MULTICANALIZACION EN TIEMPO (MT)

(a) Transmisor

(b) Receptor



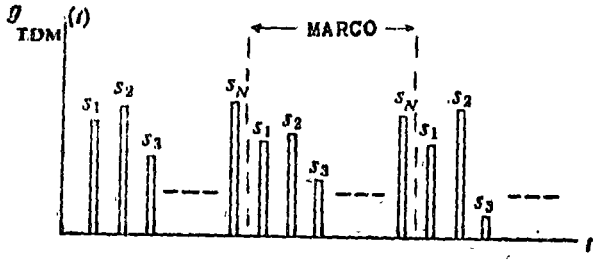


FIG. 3.3.2 SEÑAL DE BANDA BASE EN MT

(a) Muestreo de 2 señales

(b) Señal compuesta de N muestras

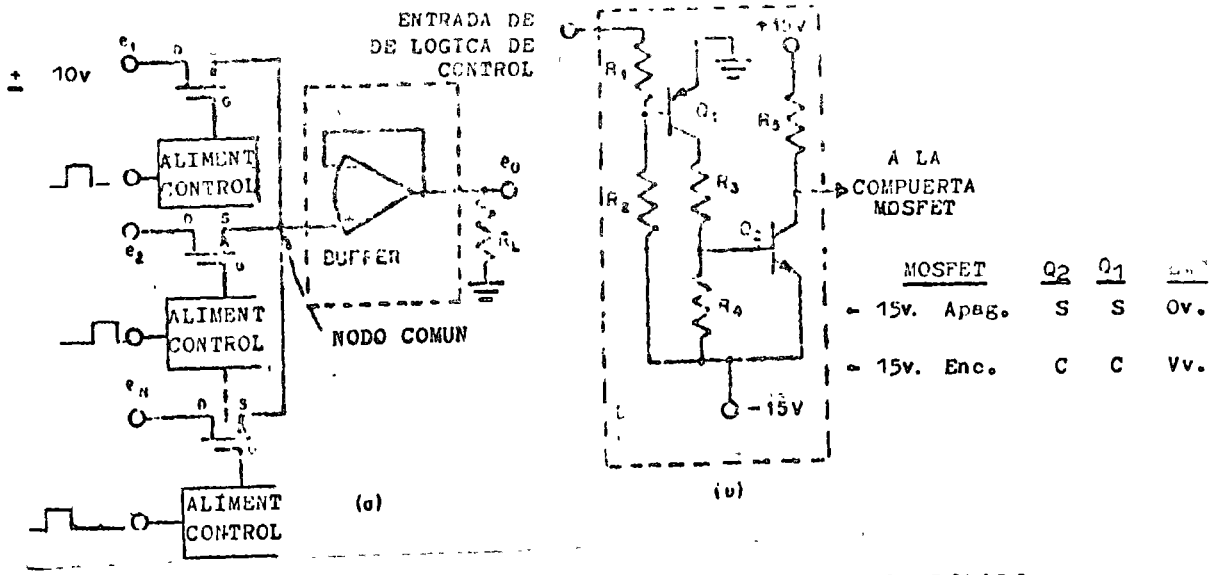
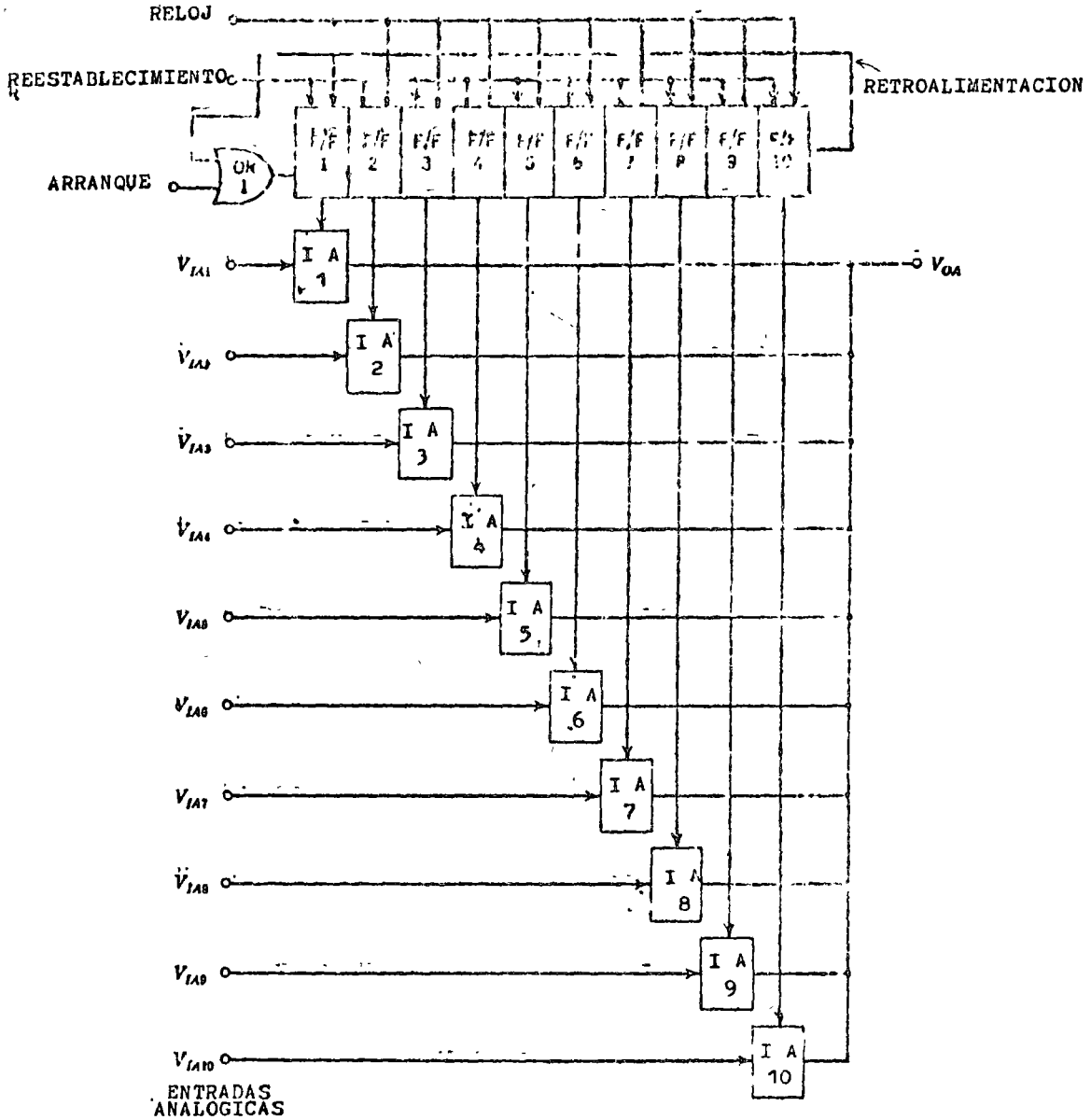


FIG. 3.3.3 MULTICANALIZACION A BASE DE UN CONMUTADOR CONTROLADO POR MOFSET

(a) Diagrama
(b) Circuito del Alimentador-Controlador



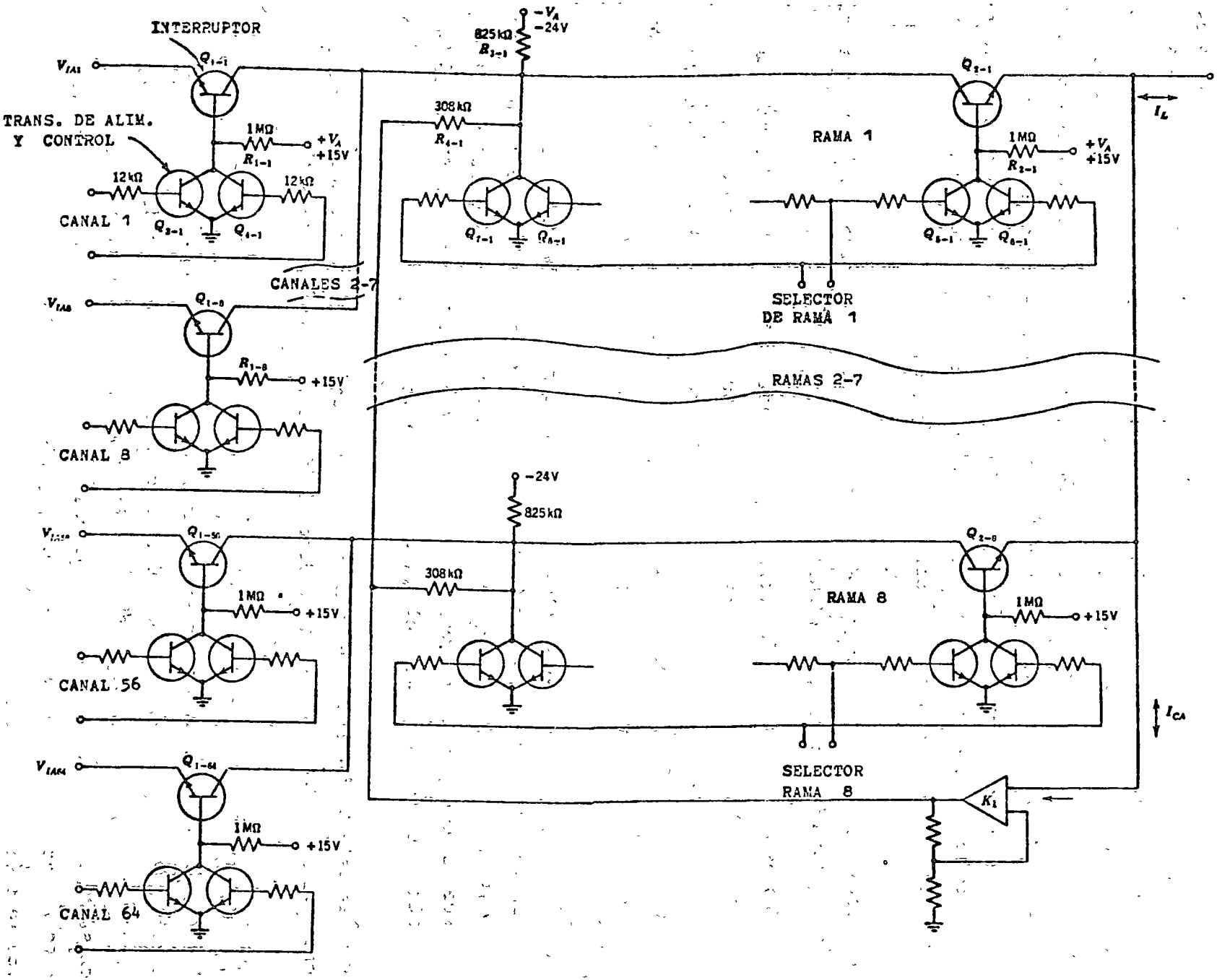


FIG. 3.3.5 CONMUTADOR A BASE DE TRANSISTORES BIPOLARES

3.4 MODULADORES DIGITALES

En esta sección se analizarán las técnicas de traslación de las señales digitales que se presentan como desviaciones en amplitud de corriente directa, a una señal de radio-frecuencia, es decir modificar a una portadora para transportar una envolvente de menor frecuencia. Para esto, hay que recordar la función básica de la modulación: convertir la información que se va a envíar, a la forma de onda mas adecuada a las caracterísitcas del canal. Esta modulación puede ser en amplitud, frecuencia o fase, como se ilustra en la figura 3.4.1, donde estos tres tipos de modulación son ejemplificados para una secuencia binaria 1001. Mas adelante se precisará mas sobre estas formas de onda.

Por otro lado, en la transmisión de pulsos de corriente directa, se identifican dos usos de los métodos de modulación:

- Uno es el utilizado en las redes de larga distancia, y es donde la banda de voz es trasladada a otra frecuencia central para agruparla con otros canales (MF); por ejemplo, la formación de grupos (12 canales), supergrupos (5 grupos), grupos maestros (5 supergrupos 300 canales), supergrupos maestros (3 grupos maestros = 900 canales), etc.

- Dado un canal con ciertas propiedades, diseñado originalmente para transmitir voz y no dígitos binarios, la modulación se utiliza para facilitar y mejorar el envío de bits por el canal. En este caso, la modulación permite que se obtengan las máximas velocidades de transmisión y que su diseño dé la máxima protección contra el ruido y la distorsión del canal.

Por ser este último punto de gran interésa los propósitos de estas notas, se presenta a continuación una breve descripción de los canales telefónicos.

SEÑALES DIGITALES EN REDES TELEFONICAS

Existen dos maneras fundamentales para transmitir señales digitales. Una forma es diseñar y construir, una red especializada para el propósito de transmitir dígitos binarios. Otra manera es adaptar las facilidades existentes de la red telefónica, para poder transmitir estas señales digitales. A continuación se estudian modos para el envío de información a través de la red telefónica.

Las redes telefónicas, diseñadas para manejar señales de voz, tienen características que hacen difícil la transmisión de dígitos binarios de corriente directa, ya que su banda pasante se estima ser de 300 a 3 400 Hz.

El origen de que el ancho de banda sea de 3 100 Hz se puede apreciar en la figura 3.4.2 (a), en donde se ve que para que la voz sea reconocible y entendible, solamente se requiere transmitir el rango indicado, aunque el oído cubra un mayor ancho de banda.

Entonces, el sistema telefónico atenuará, en forma mas o menos igual, todas las frecuencias existentes entre 300 y 3 400 Hz; las señales superiores a 4 000 Hz son atenuadas casi en su totalidad, como se puede ver en la figura 3.4.3.(a). En la figura 3.4.3(b) se muestra también la forma de la atenuación de la banda pasante, que es de particular interés para la evaluación de las propiedades de los circuitos para transmisión de datos. Asimismo, en la figura 3.4.3(c) se tiene la comparación de una línea telefónica común comparada con otra línea acondicionada de mayor calidad.

En fin, para permitir la transmisión de datos en redes de voz, es necesario convertir la información de C-D, en una señal que ocupe la banda disponible en la red telefónica.

3.4.1 MODULACION EN AMPLITUD (ASK)

Una de las maneras de convertir un mensaje binario de "1"s y "0"s a radio frecuencia es modulando en amplitud a una portadora senoidal. Este tipo de modulación se conoce como ASK (Amplitude Shift Keying) y se le ha traducido como Modulación por Desviación en Amplitud (MDA) y también como Modulación Binaria en Amplitud (MBA).

La convención para esta modulación digital es enviar un pulso senoidal S(t) cuando un 1 está presente, y enviar un espacio cuando un 0 está presente, es decir:

$$S(t) = \begin{cases} A \operatorname{sen}(2\pi f_c t) & o < t < T \\ 0 & \text{cualquier otro intervalo} \end{cases}$$

Con esta técnica, los estados binarios están representados por la presencia o ausencia de un tono de audio o portadora. Esta modalidad es también conocida como telegrafía ON-OFF. Los elementos básicos de un sistema ASK se pueden apreciar en la figura 3.4.4.

Para transmisión de datos menor o igual a 1 200 bits/seg., un sistema ASK utiliza una frecuencia en la portadora de 1 600 Hz.

Las características principales de un sistema ASK se pueden resumir como sigue:

(1) Bastante simple en un proceso de modulación-demodulación
(2) Costo relativamente bajo
(3) Susceptible a cambios repentinos en la amplitud
(4) Ineficiente en el proceso de modulación (33% max.)
(5) Desperdicio del espectro al exigir doble banda lateral.

Cuando las velocidades de transmisión son altas (mayores a 4 800 b/seg.), el punto (5) anteriormente mencionado se convierte en un factor importante. Recurriendo a las técnicas analógicas de eliminación de una banda lateral para transmitir una señal portadora modulada en amplitud por banda lateral única (AM-BLU), se puede recurrir al mismo concepto para la transmisión digital. De esta manera se mejora la eficiencia en el uso del espectro.

Puesto que la información esencial está presente en cada una de las bandas laterales, no se pierde contenido durante este proceso. La portadora debe conservarse para poder recuperar la componente C-D de la información en la envolvente. Sistemas digitales de este tipo utilizan modulación por banda lateral residual, de la cual únicamente una de las bandas laterales es retenida, pero debido a la curva de corte de los filtros, una porción de la portadora y un residuo de la otra banda lateral son también incluídas.

Lo anterior se logra tomando una señal de doble banda lateral y filtrando la banda lateral deseada. Como resultado de esto, la señal utiliza alrededor de 3/4 del ancho de banda requerido en doble banda lateral.

Las velocidades de operación en moduladores de banda lateral residual que

operan a 2 400 b/seg., son usados en canales telefónicos; para velocidades de 4 800 b/seg., se han utilizado técnicas de nivel múltiple o M-ASK. La frecuencia de la portadora está normalmente localizada entre 2 200 y 2 700 Hz.

ESPECTRO EN ASK

Para ilustrar un caso típico del espectro originado por una secuencia de bits, considérese la secuencia 101010... que es transmitida a una razón de 2 fm bits/seg. Si se ignora el efecto de la fase en el espectro resultante se tiene que si el índice de modulación es 1 (máximo índice antes sobremodular) este espectro es un tren de compomentes discretas espaciadas por un valor de fm y con bandas laterales centradas en fc. Estas compomentes tendrán su amplitud igual a la de una función sinc(x), como se puede ver en la figura 3.4.5(a).

Si se considera un tren de pulsos diferentes con duración τ seg. y envíados a una velocidad de S pulsos/segundos, aparecen mas componentes discretos si τS es menor que 1, como se puede ver en la figura 3.4.5(b). En este caso también, las componentes discretas siguen la forma de la función sinc(x), y se encuentran centradas en S,2S,3S, ...

Como este tren de pulsos modula a una portadora de frecuencia fc, su espectro se encuentra centrado precisamente en fc, donde aparece una componente relativamente grande que no lleva información. En este caso $\tau S = 1/6$, es decir, existen seis intervalos entre pulsos.

Como ya se mencionó anteriormente, la información qué realmente es necesaria transmitir sin perder el contenido, es una banda lateral sin la portadora. Además, no todas las compomentes discretas tienen que envíarse; se podrían envíar las componentes contenidas en los dos o tres primeros lóbulos que contienen las componentes mas significativas.

Lo anterior se presenta ya que para transmitir todo el espectro mostrado, se tendría que utilizar un ancho de banda innecesario, o si el ancho de banda del canal está fijo, se restringiría la velocidad de transmisión. También se requeriría una potencia apreciable para transmitir todas las componentes. Además, la energía disponible se debe de limitar a valores que no perjudiquen a otros

usuarios que comparten las mismas facilidades, por lo tanto, es altamente deseable utilizar toda la potencia disponible para transmitir esa parte del espectro que con el mayor contenido de información. Este criterio aumenta las posibilidades de poder separar, de manera eficiente, a la señal del ruido.

Volviendo a los concepto de potencia, ésta es proporcional al cuadrado de la amplitud, por lo que la potencia transmitida en la portadora es proporcional a A_c^2, y a la potencia de cada banda lateral es proporcional a $(A_m/2)^2$. Para un factor de modulación de 1 (Ac = Am), se requiere 4 veces mas potencia para transmitir la portadora, que no contiene información, que para transmitir cualquiera de las bandas laterales. Factores de modulación menores a 1 implican que la portadora puede requerir 6 ó 8 veces la potencia de las bandas laterales.

TRANSMISION DE NIVEL MULTIPLE

La presentación anterior se refirió a modulación en amplitud de dos niveles. Si ahora se amplían los conceptos anteriores a más niveles, con el propósito de aumentar la cantidad de información contenida en un intervalo, se presentan otras desventajas.

Considérese un sistema ASK de 4 niveles (representando 4 - ASK), como los de la figura 3.4.4(b), en donde cada nivel puede representar un par de bits ("dibits") 00, 01, 10 ó 11. Este proceso da un menor margen para errores en el umbral de decisiones del regenerador. Teóricamente el número de bits sencillos que lleva la señal puede ser doblado; sin embargo la susceptibilidad al ruido es mayor. La razón de la diferencia en niveles que deben detectarse respecto al ruido, es apreciablemente menor.

En forma similar, 8 niveles permitirían que se transportaran tres bits por nivel, y proporcionar de esta manera tres veces la velocidad del sistema de 2 niveles, pero las diferencias de nivel que deben detectarse son menores.

Desafortunadamente, AM en sí, ya es vulnerable al ruido; la modulación de multi-niveles es todavía mas vulnerable. Sin embargo existen varios sistemas construídos bajo este principio: los modems Al Data System desarrollados por Bell System. en relación con SAGE, la red norteamericana de defensa aérea, utilizó modulación en amplitud de tres niveles, de los cuales sólo dos portaban

información, el tercero servía para mantener la sincronía de marco.

3.4.2 MODULACION EN FRECUENCIA (FSK)

Otra manera de convertir bits a pulsos de radiofrecuencia es asignando una frecuencia diferente a cada símbolo binario, obteniéndose de esta manera la modulación FSK (Frequency Shift Keying), que se le ha traducido como Modulación por desviación de Frecuencia, y también como Modulación binaria en Frecuencia.

Si las dos portadoras equivalentes al 1 y al 0 son senoides de frecuencia f_1 y f_2 respectivamente, estas se pueden representar como:

$$S(t) = \begin{cases} A \text{ sen } 2\pi f_1 t & 0 < t < T \\ A \text{ sen } 2\pi f_2 t \end{cases}$$

es decir, que la amplitud de la señal modulada y el ángulo de la senoide contendrá la información a transmitir.

Este tipo de modulación puede realizarse siguiendo métodos convencionales de FM, como se puede apreciar en la figura 3.4.6(a), para modular y recuperar el tren de pulsos original. Cabe hacer notar que también existe otro procedimiento de detección utilizando dos filtros pasa-banda a la entrada del receptor; la salida de estos filtros se compararía y en base a la señal que resulta mayor se decidirá por un 1 ó un 0 (ver figura 3.4.6(c)).

Los sistemas FSK tienen las siguientes características:

(1) Implementación no mas compleja que ASK
(2) Costo medio
(3) Prácticamente inmune al ruido en la amplitud
(4) Insensible a cambios de ganancia
(5) Requiere un gran ancho de banda (mayor que ASK)

El punto (4) anterior se presenta ya que la señal recibida puede ser amplificada y limitada, requiriéndose entonces una etapa simple amplificadora-limitadora, mientras que los sistemas AM exigen un control automático de ganancia para poder operar en un rango dinámico grande.

El concepto del punto (3) se refiere a que FSK tiene una mejoría de 3 a 4 dB sobre ASK en la mayoría de los medios ruidosos, particularmente en los umbrales de distorsión (es decir, en el punto donde la distorsión es tal que la impresión de símbolos está a punto de suspenderse). Conforme la desviación en frecuencia es mayor, la ventaja sobre AM mejora más todavía en un medio ruidoso, Además, este es el modo mas atractivo de enviar pulsos, en un medio con desvanecimientos. El uso de moduladores-demoduladores FSK ha sido bién recibido en casi todo el mundo para transmitir datos a 1 200 b/seg. o menos. El sistema Bell lo ha adoptado en los Dataphone-200, y por el gobierno Inglés en su Datel-200 y 600.

Existen recomendaciones del CCITT (# V.21, 22 y 23 Libro Blanco, vol. VIII) que recomiendan que para la transmisión de datos a 200 bauds en redes telefónicas conmutadas debe ser:

- Desviación de frecuencia: $\pm$ 100 Hz
- Frecuencia central, canal 1: 1 080 Hz
- Frecuencia central, canal 2: 1 750 Hz

También se recomiendan ahí, las razones de modulación para la transmisión sincrona a 600 y 1 200 bauds. Para el canal envío de información, se sugieren las siguientes frecuencias

	F_o	F_1	F_o
Modo 1 (hasta 600 bauds):	1 500 Hz	1 300 Hz	1 700 Hz
Modo 2 (hasta 1 200 bauds):	1 700 Hz	1 300 Hz	2 100 Hz

Para transmisiones de mas alta velocidad (2 400, 4 800 bauds, etc.), se ha recomendado hacer uso de moduladores de fase (ver sección 3.4.3) que han mostrado ser mas complejas en su construcción pero mas confiables en su transmisión.

ESPECTRO EN FSK.

Para calcular el especto que genera un tren de pulsos 101010..., se observa que éste se obtiene a partir de la gráfica de amplitudes de funciones Bessel, originando un espectro que tiene una cantidad infinita de componentes discretos en sus dos bandas laterales, también simétricas en fc.

Para apreciar el efecto de variar el índice de modulación Afc/fm de 0.5 a 10, se muestran en la figura 3.4.7 cuatro espectros resultantes al modular en frecuencia una portadora con un tren de pulsos 101010... Se puede ver, también, que la amplitud de la portadora no es tan grande, relativamente hablando, respecto a las bandas laterales, como sucede en la modulación por amplitud. En algunos casos, la portadora desaparece completamente sobre todo cuando el índice de modulación aumenta. La información, sin embargo, se extiende ampliamente a los lados de la portadora. Igualmente que en AM, se puede suprimir una de las bandas laterales, ya que tanto la banda superior como la inferior son imágenes espejo una de la otra.

Por otro lado, se puede utilizar la transmisión de niveles múltiples en una manera similar al tratado en la sección anterior, comprimiendo mas información en el ancho de banda dado, pero incrementando la susceptibilidad a los errores. Los "dibits" mencionados en AM, pueden modular a una portadora para que esta presente cuatro frecuencias diferentes. Esto doblaría la velocidad de transmisión, pero la relación señal/ruido requerida para alcanzar la misma probabilidad de error, P_e, será mucho mayor; para la misma potencia en la señal, ocurrirían mas errores.

3.4.3 MODULACION EN FASE

Se ha observado que para tener un sistema de modulación por pulsos codificados, se deben emplear pulsos bipolares (-V y V), en lugar de los unipolares (0,V). De esta manera, en MPC bipolar, los símbolos binarios se representan por S(t) y -S(t). A este tipo de modulación se le conoce como modulación binaria en fase (MBF), que es la traducción del inglés de Phone Shift Keying (PSK).

Para transmitir información binaria, se asigna a cada símbolo una de las dos fases disponibles; estas fases puden ser 0° y 180° ó 90° y 270°, es decir:

$$S(t) = \begin{cases} A \operatorname{sen}(2\pi f_c t) & o < t \leq T \quad \text{para un 0 binario} \\ -A \operatorname{sen}(2\pi f_c t) & o < t \leq T \quad \text{para un 1 binario} \end{cases}$$

De esta manera, se hace uso de una portadora sin cambiar su amplitud o frecuencia para enviar información binaria, sino cambiando su fase, como se ilustra en la figura 3.4.1(c).

Algunas características de este tipo de modulación digital son:

(1) Implementación mas compleja que FSK y ASK
(2) Costo medio (debido a los circuitos integrados)
(3) Prácticamente inmune a los ruidos en la amplitud
(4) Insensible a cambios ligeros en ganancia
(5) Requiere menor ancho de banda que FSK y ASK
(6) Toda la potencia disponible es utilizada en la información
(7) Sincronización de la portadora es requerida

Una de las aplicaciones mas importantes de FSK es la transmisión binaria a altas velocidades (9 600, 56 000. 1 M b/seg.), ya que ofrece la mejor eficiencia en ancho de banda e inmunidad contra el ruido comparado con ASK, y FSK. Por su forma de transportar la información, es sumamente crítico que la estabilidad en fase de los circuitos sea bastante alta.

En algunos casos es conveniente enviar la información en la fase relativa al pulso anterior. Por ejemplo, el bit 1 se representa enviando un pulso de R.F de la misma fase que el pulso anterior. El bit 0 está representado por un pulso de R.F de fase opuesta al anterior. Las señales se demodulan en el receptor integrando y almacenando la información contenida en un pulso durante el intervalo de un bit, para poderlo comparar con el pulso siguiente.

ESPECTRO DE PSK

En general se puede decir que la modulación por fase es equivalente a FM (con un cambio de variable en el índice de modulación), sobre todo si la moduladora es senoidal.

Por otro lado si la modulación es un tren de pulsos cuadrados, el efecto sería equivalente a dos señales moduladas en amplitud que se superponen en sus espacios; las dos señales tendrán componentes en las mismas frecuencias.

Entonces, los sistemas que transmiten patrones de bits en esta forma, generalmente tienen un espectro mas parecido a AM que a FM.

DETECCION

Existen básicamente dos métodos para la detección de datos modulados en fase: Referencia fija y la Diferencial. Ya que el receptor no tiene idéa de la fase (salvo cuando se le envía una secuencia de entrenamiento), es necesario generar información sobre las fases, ya sea de la misma señal o examinando los cambios que ocurren en la fase.

El primer método requiere de una referencia fija suministrada por el transmisor. Para mantener una alta eficiencia se transmite esta información con un mínimo de potencia en un tono piloto con un ancho de banda muy angosto y múltiplo armónico de la portadora.

M - PSK

Como ejemplo de la complejidad que contiene un sistema de fase múltiple, la figura 3.4.8 muestra un diagrama de 4-PSK, es decir, un sistema de modulación digital de 4 fases. La información está dividida en pares de bits (los antes mencionados dibits), y el primer bit de cada par modula una senoidal, el segundo bit modula la misma senoide retardada 90°. En forma similar, se utilizan dos ondas senoidales se usan para la detección, una 90° defasada de la otra.

La detección diferencial no genera una referencia fija de la fase en el receptor, sino que la información es codificada por medio de cambios en la fase. Si en un sistema 2-PSK el bit 1 es codificado como un cambio de +90° en la fase de la señal, y el bit 0 como un cambio de -90°, en el sistema 4-PSK los cambios pueden ser:

Bits	Cambio de Fase
00	-135°
01	- 45°
11	+ 45°
10	+135°

El detector entonces no necesita una referencia e identifica los cambios de fase. Se requiere, sin embargo, de un retardo de 1 símbolo de la señal recibida para poder compararla con la otra entrante.

Tal como la modulación en frecuencia reemplazó a ASK debido a su mayor inmunidad al ruido, igualmente PSK está siendo mas utilizado que los otros dos tipos de modulación anteriormente presentados; sin embargo, a la fecha existen mas unidades FSK instaladas que de cualquier otra.

Como las pequeñas variaciones en fase no pueden transmitirse y detectarse con precisión, PSK no se usa normalmente para enviar música o voz, en donde ASK y FSK son muy eficientes.

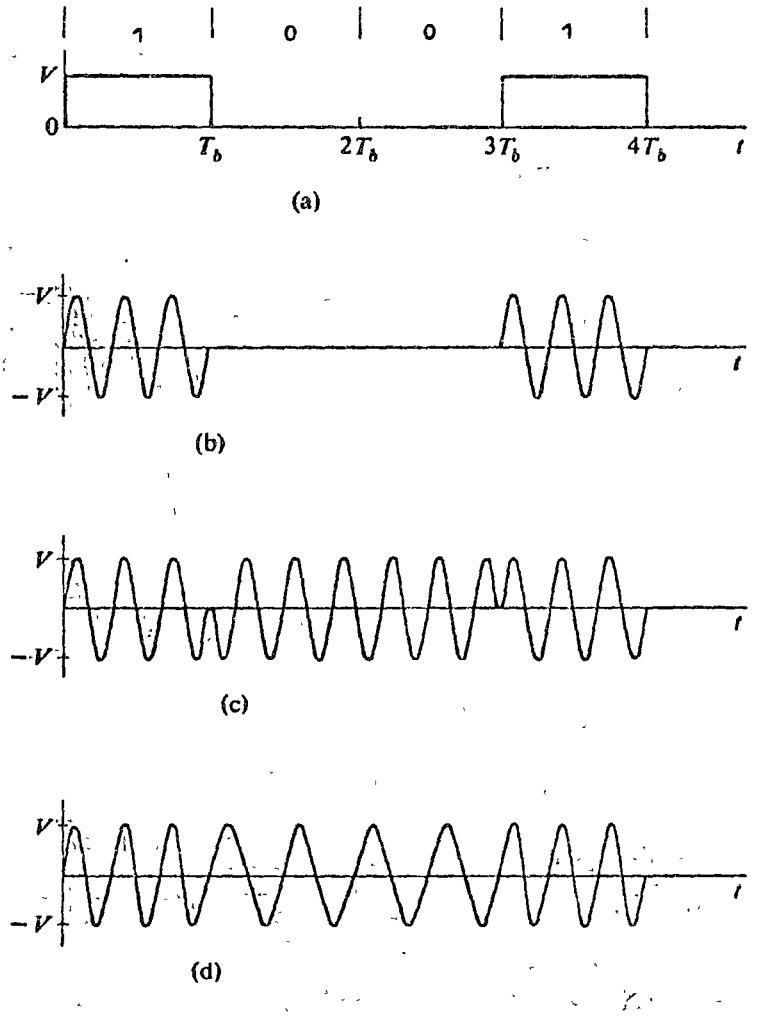
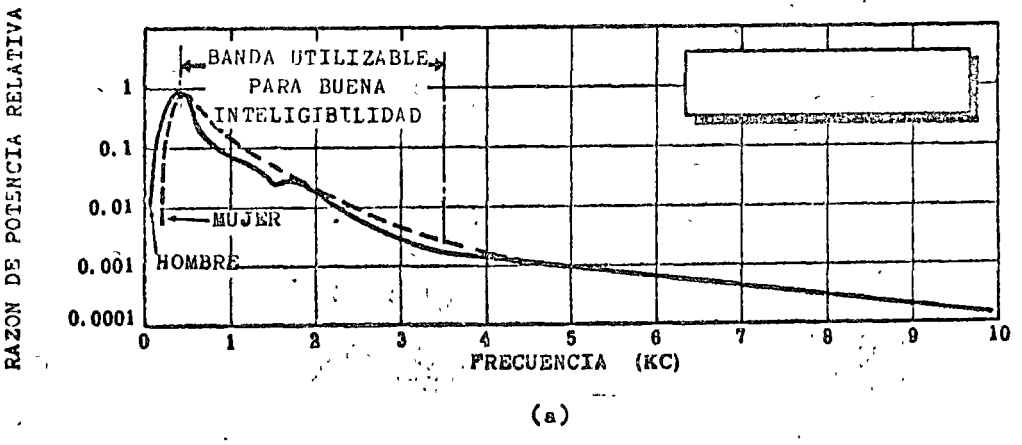
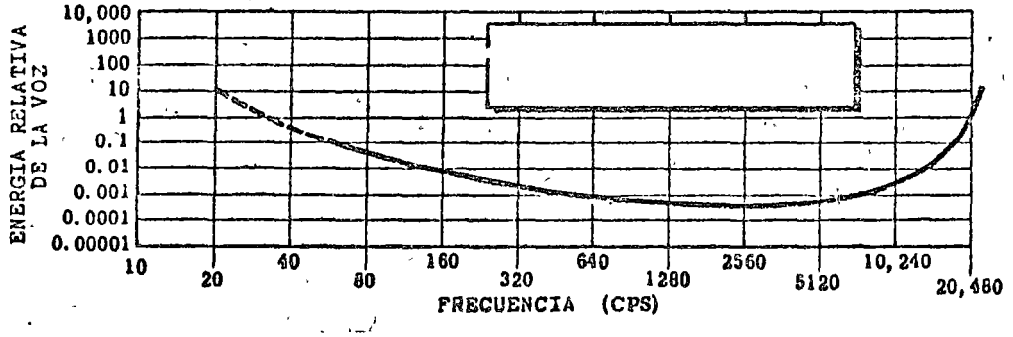


FIG. 3.4.1 FORMAS DE ONDA EN LA MODULACION BINARIA DE UNA PORTADORA

(a) Tren de pulsos
(b) Modulación en Amplitud
(c) Modulación en Fase
(d) Modulación en Frecuencia



(a)

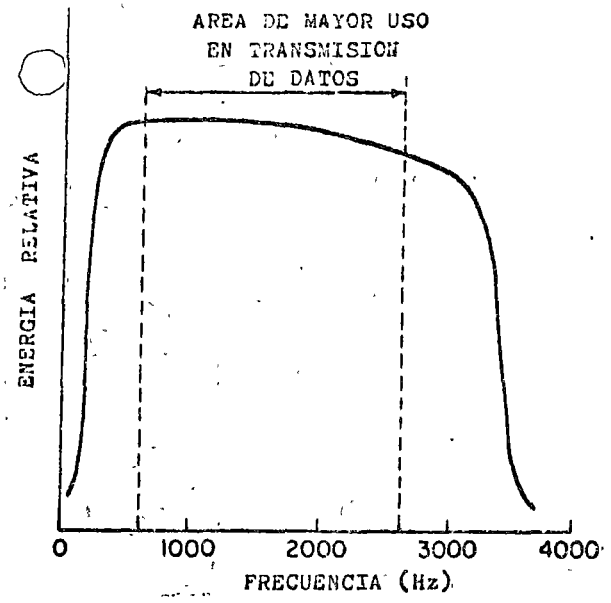


(b)

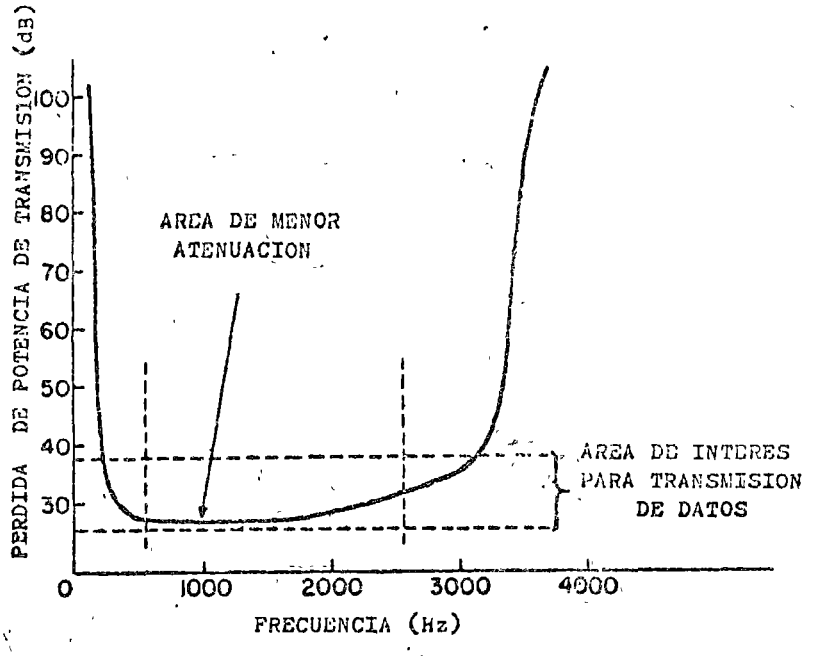
FIG. 3.4.2 CARACTERISTICAS DE LA RESPUESTA HUMANA

(a) Espectro de la voz

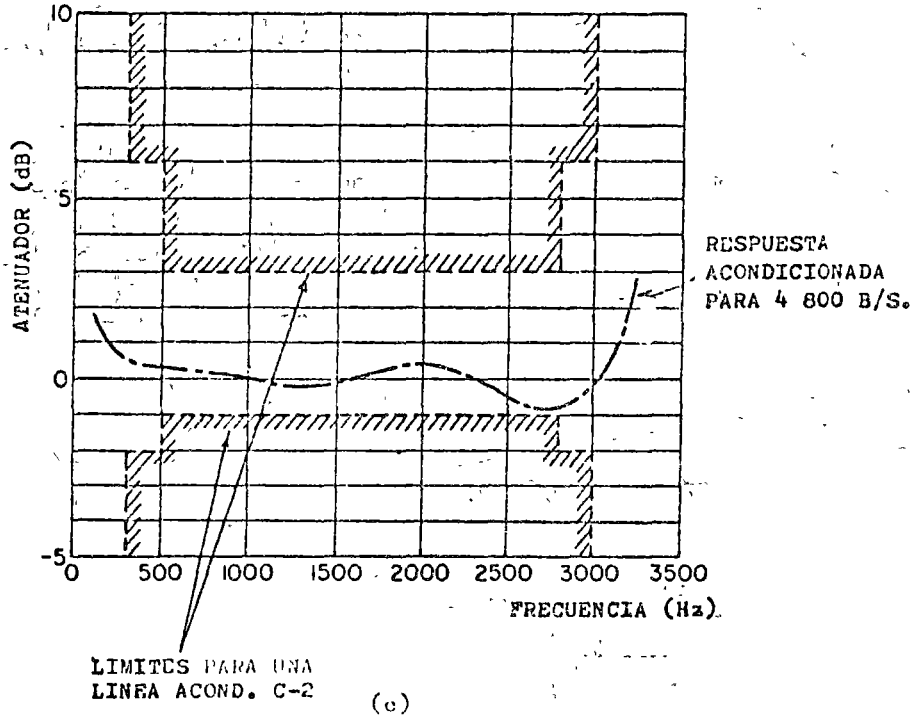
(b) Rango audible



(a)



(b)



(c)

FIG. 3.4.3 CARACTERISICAS DE UN CANAL TELEFONICO

(a) Respuesta típica
(b) Atenuación
(c) Límites normales para una línea de alta calidad

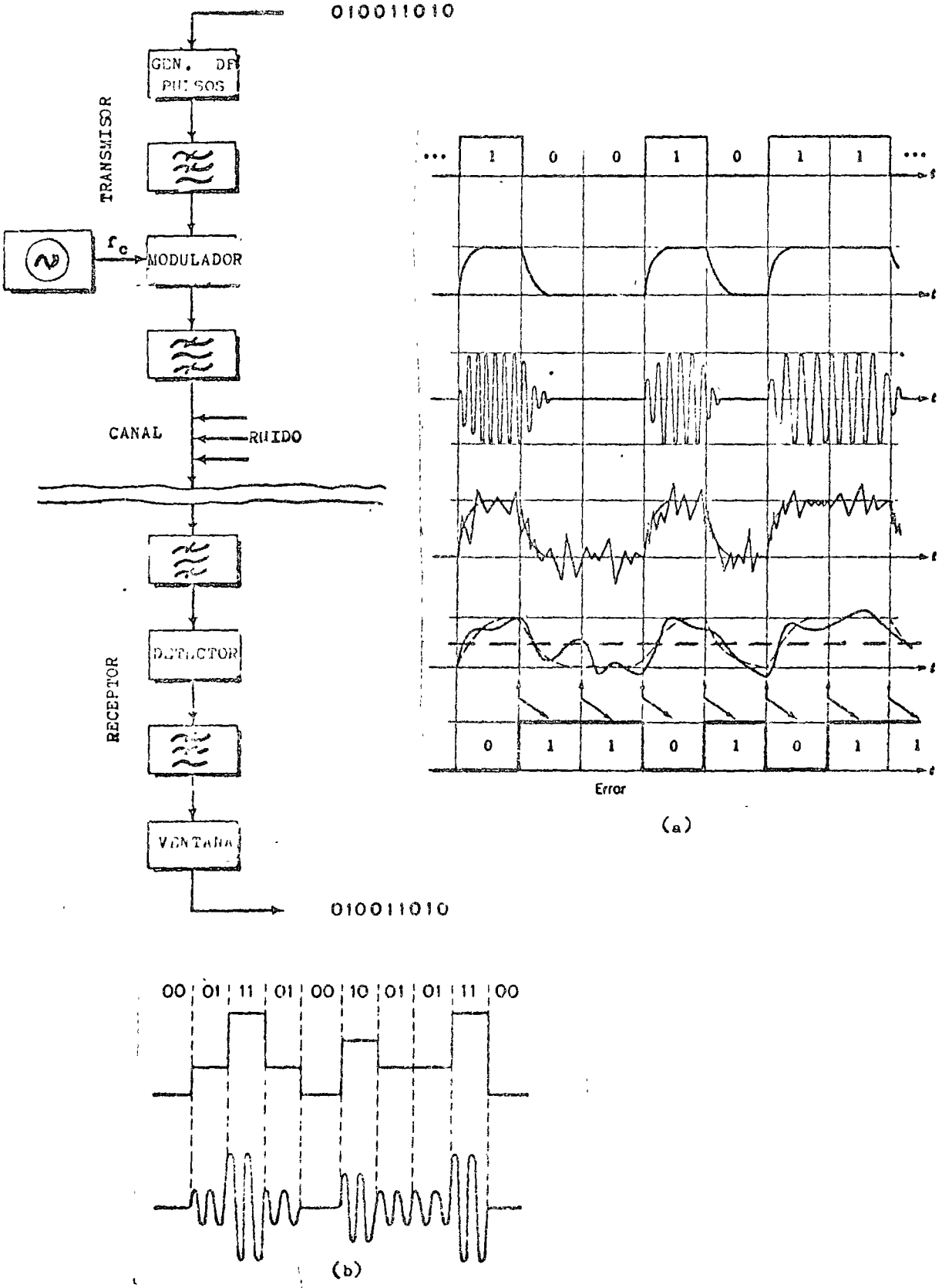
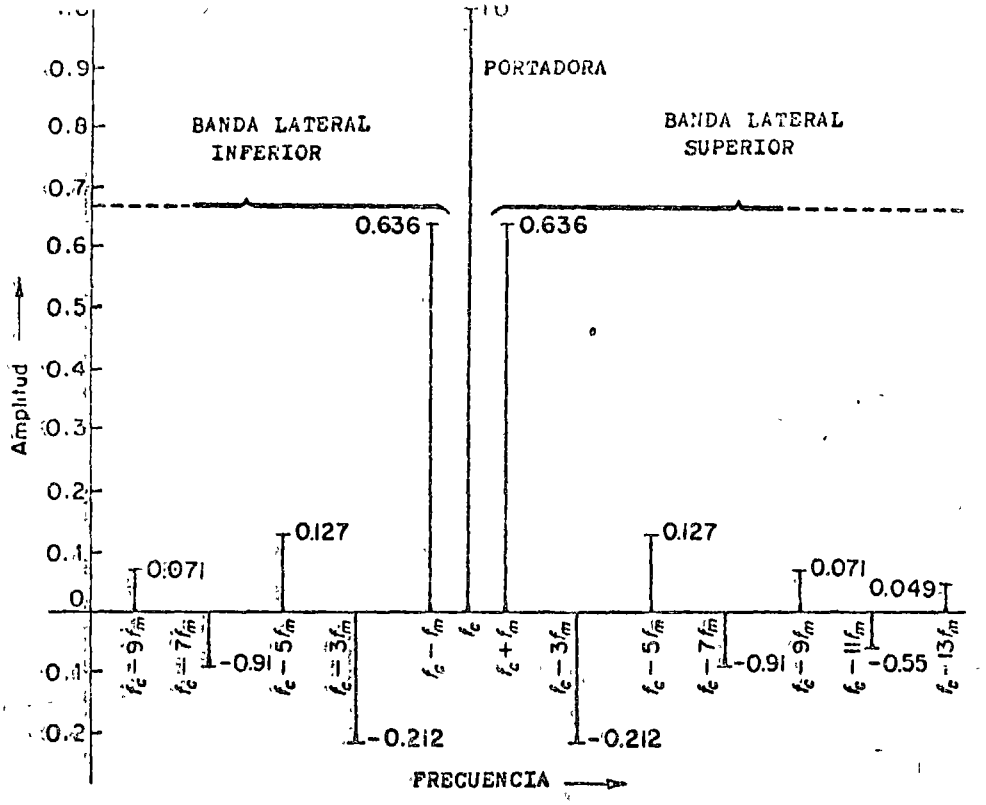
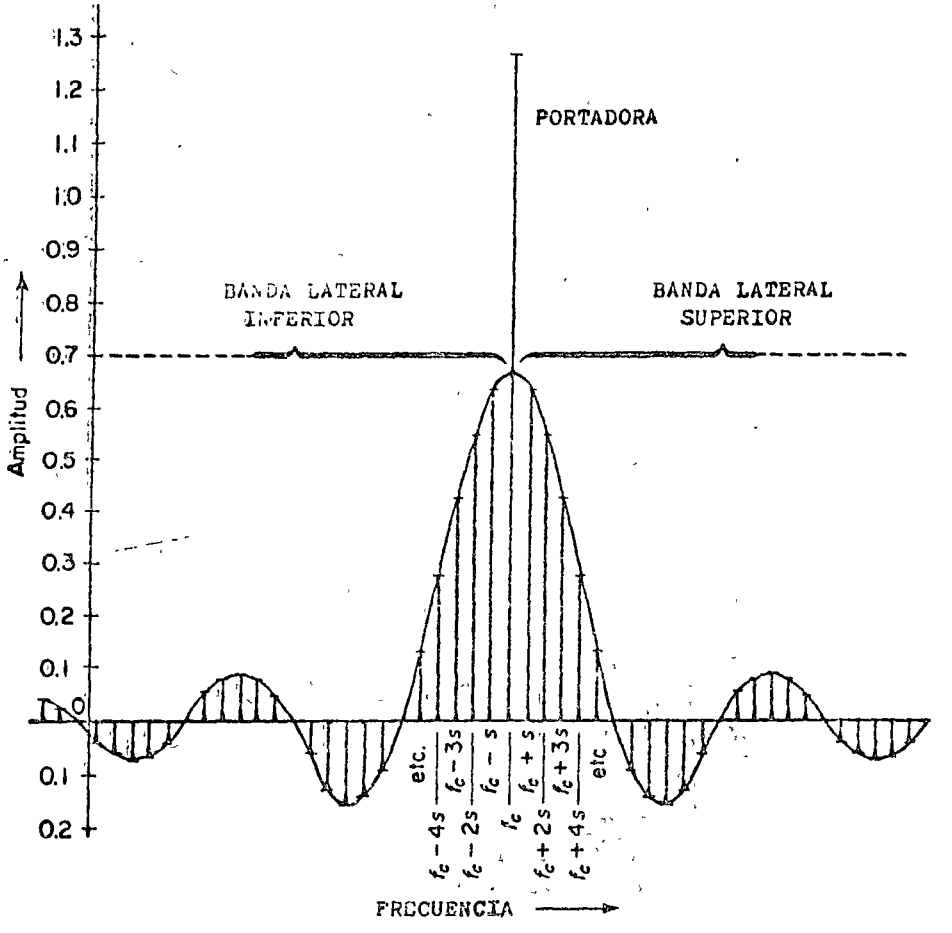


FIG. 3.4.4 ETAPAS UTILIZADAS EN UN PROCESO ASK

(a) Sistema binario
(b) Sistema cuaternario



(a)



(b)

FIG. 3.4.5 ESPECTRO RESULTANTE AL MODULAR EN AMPLITUD A UNA PORTADORA CON UNA SERIE DE DIGITOS BINARIOS

(a) Serie 01010101 ...

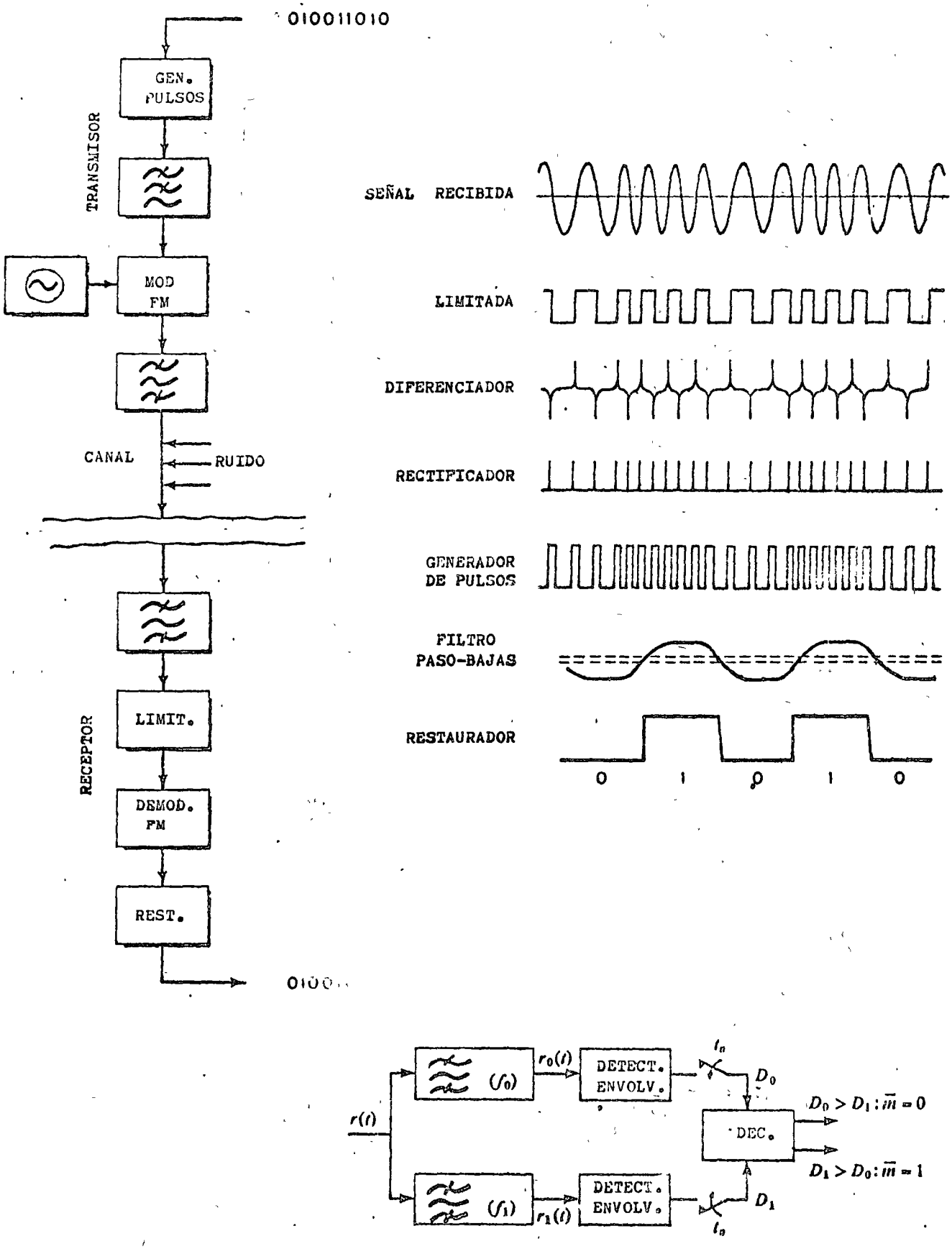


FIG. 3.4.6 MODULACION DIGITAL EN FRECUENCIA

(a) Diagrama a bloques
(b) Formas de onda
(c) Diagrama conceptual usando dos filtros

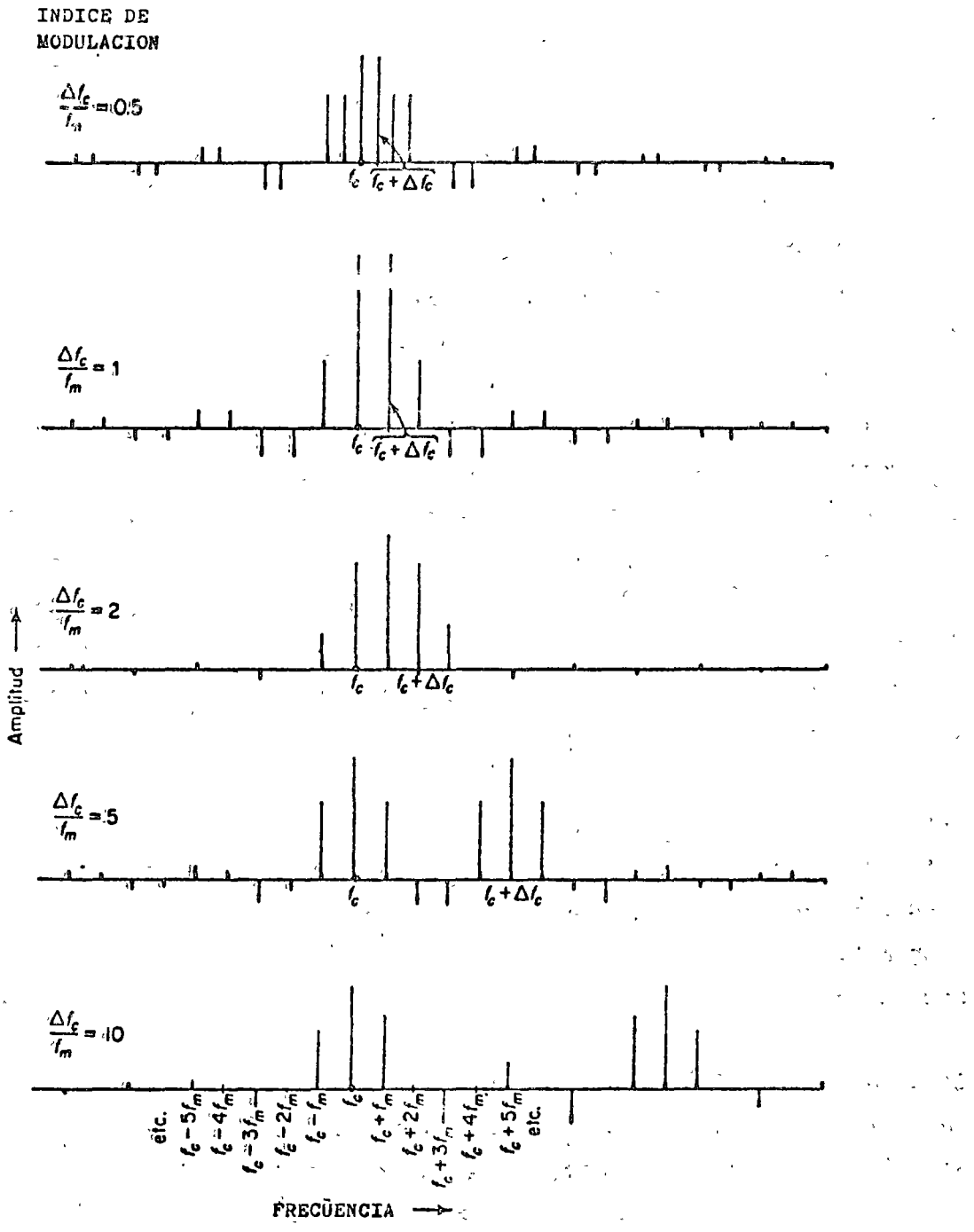


FIG. 3.4.7 ESPECTRO DE FSK PARA LA SECUENCIA 01010101 ...

3.5 SISTEMAS DE COMUNICACION DIGITAL

Como ya se mostró en la Sección 3.2, existen varias etapas para la conversión de información analógica, a su forma digital equivalente. Estas etapas son: Muestreo, Cuantización y Codificación. Para formar un sistema general de comunicaciones digitales, se deben incluir las etapas de modulación (Ver Fig. 3.3.1), que como se vió en la sección 3.4, estas pueden ser en frecuencia, amplitud o fase.

Tanto la cuantización como la codificación de niveles a símbolos binarios se pueden identificar integrados al conversor analógico-digital (A/D), cubierto en el capítulo I. La multicanalización que en la Fig. 3.5.1 se muestra como MUX, se analizó en la sección 3.3. Su presencia se debe a que muchas veces la fuente de información analógica de entrada al conversor A/D es un tren de pulsos MAP compuesto, es decir, la señal MAP será la salida de un conmutador analógico que muestrea a varias fuentes de información en forma periódica.

Las etapas de modulación, equivalen a la posibilidad de que existan varios sistemas como el mostrado (u otros analógicos), que se deseen transmitir usando la misma portadora. De esta manera se comparte el espectro de transmisión de RF entre varias subportadoras que pueden contener tipos de modulación diferentes, es decir, se tiene multicanalización en frecuencia.

Esta información modulada pasa por el canal, que bien puede ser la atmósfera, un cable, etc. y es distorsionada por el ruido que se supone que es aditivo*. Se omiten efectos tales como: retardos de propagación, desvanecimientos, multitrayectorias, interferencias entre símbolos, y efectos similares debidos al medio y a los circuitos de transmisión y recepción.

Después de demodular la señal digital, haciendo la operación inversa del modulador, se procede a la detección. Esta etapa examina a la señal en

---

* Esto se argumenta con el teorema del Límite Central, que está fuera del objetivo de estas notas.

banda base que contiene ruido y hace una decisión sobre cuál de las posibles señales enviadas (0 ó 1) está presente en el intervalo de análisis.

Es en esta etapa donde se evalúa al receptor (o más bien a la etapa de decisión), para lo cual existen parámetros que cuantifican esta evaluación. Si el sistema es digital, se hace uso de la probabilidad de error, Pe, que es la razón del número de decisiones incorrectas respecto al número total de decisiones intentadas. Si el sistema es analógico, se calcula el error cuadrático medio, o su raíz cuadrada (r.m.s.), entre la señal original y la recibida, esto es:

TIPO DE SEÑAL	ERRORES	DEFINICION
Digital	P_e	# errores/# de muestras
Analógica	R.M.S.	$\sqrt{\langle \epsilon^2 \rangle}$; $\epsilon = m(t) - \tilde{m}(t)$

Para decidir si P_e es aceptable para una aplicación dada, se tienen que definir los rangos permisibles de error que se está dispuesto a tolerar. Como ejemplo, y con el fin de dar órdenes de magnitud, se presentan los siguientes valores para aplicaciones específicas*:

P_e	Aplicación
10^{-2} - 10^{-1}	Telegrafía
10^{-3} - 10^{-2}	Télex
10^{-4} - 10^{-3}	Voz
10^{-5} - 10^{-3}	Facsímile
10^{-8} - 10^{-6}	Datos de Computadora

El problema de analizar el rendimiento de un sistema de comunicaciones digitales es complejo, debido a la multiplicidad de parámetros que se deben de considerar. Definitivamente, la evaluación de un sistema está condicionado a las subjetividades del usuario y del valor que tengan los errores en su información.

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* Cabe aclarar que son estimaciones subjetivas.

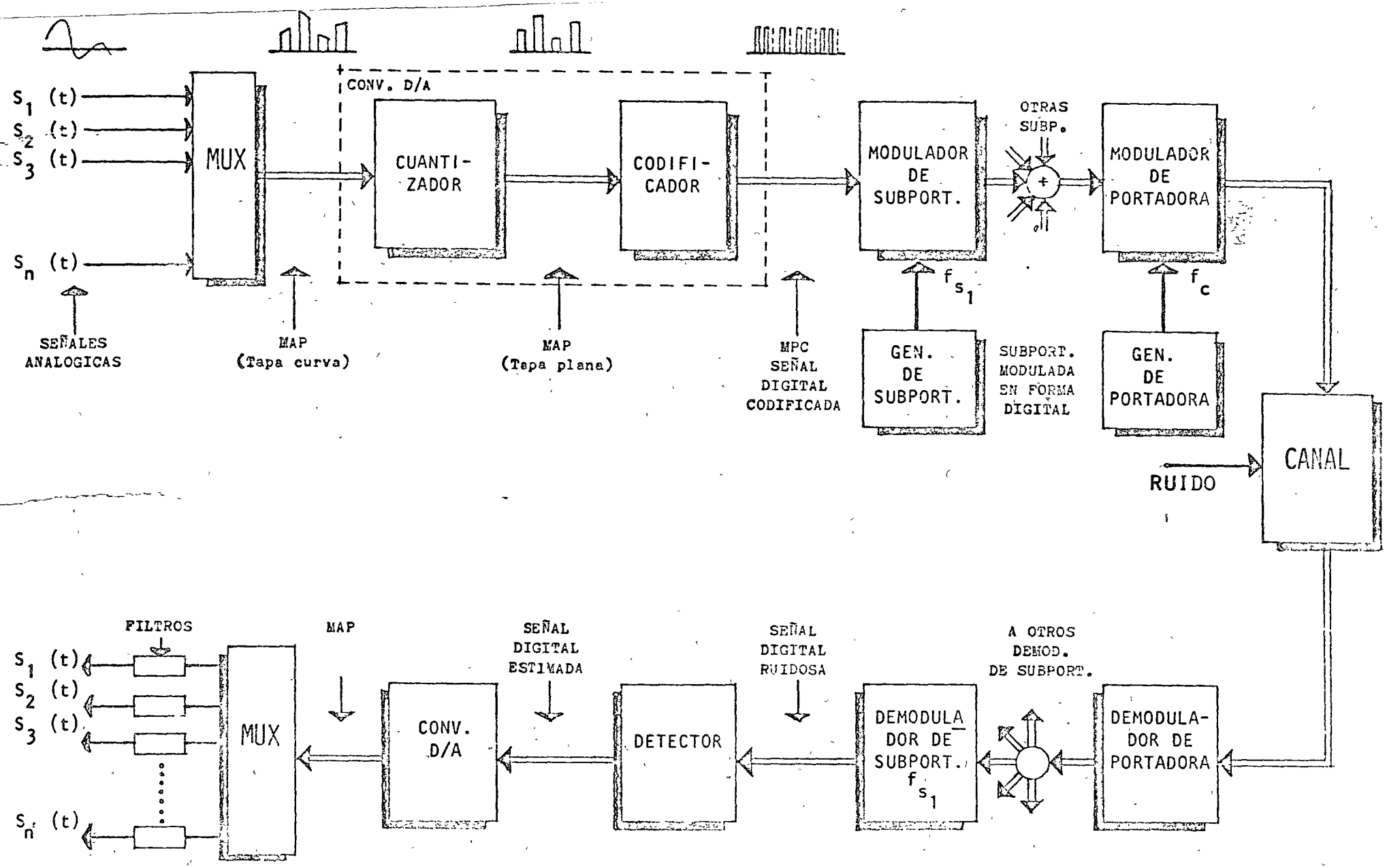


FIG. 3.5.1 Sistema de Comunicaciones Digitales **

* No incluye Codificación para protección contra el ruido

** Se omiten etapas de:
a) Compresión-Expansión
b) Repetidores
c) Inf. de Sincronía

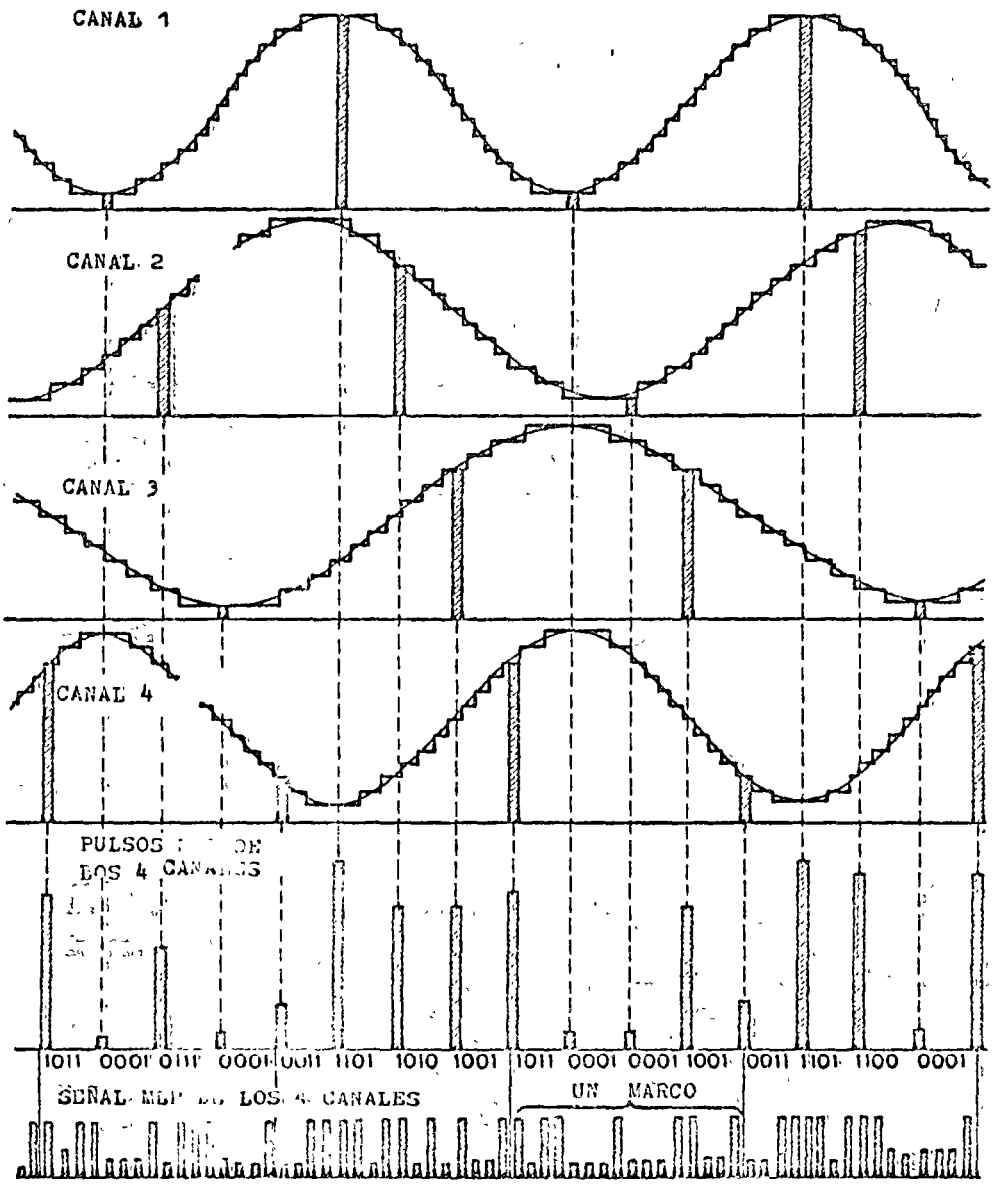


FIG. 3.5.2 MULTICANALIZACION EN TIEMPO CON MPC

PRACTICA IV

SISTEMA DE MODULACION DELTA

1.0 Objetivo: Familiarizar físicamente al alumno con el proceso de Modulación y Demodulación Delta.

2.0 Teoría Básica:

Modulación Delta es uno de los métodos de conversión de señales analógicas en señales digitales. Se diferencia de PCM en que en lugar de transmitir los valores absolutos de cada muestra de la señal se transmite la diferencia de éstas.

El modulador Delta Simple consiste básicamente en un sistema realimentado de la siguiente forma:

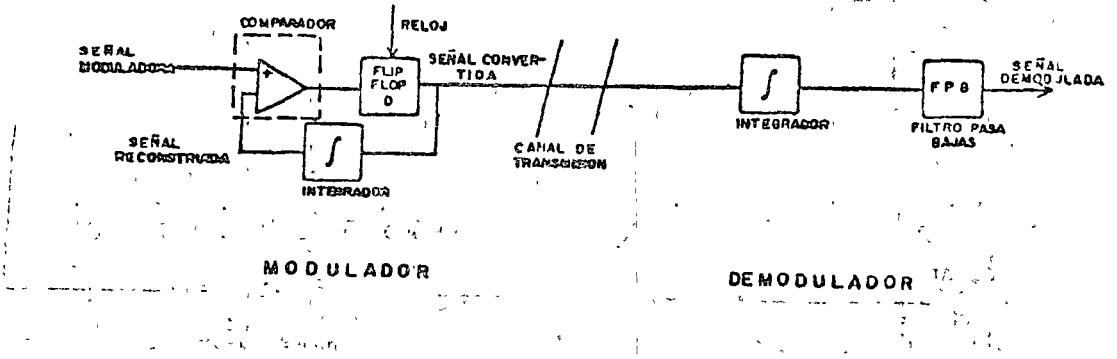


FIG. 1 SISTEMA DE MODULACION DELTA CON INTEGRACION SIMPLE

El comparador sirve para indicar cuando la señal reconstruída por el integrador ha alcanzado a la señal moduladora, el flip flop D sirve para modular un tren de pulsos con la salida del comparador.

El modulador transmite las diferencias detectadas por el comparador.

Las señales formadas son:

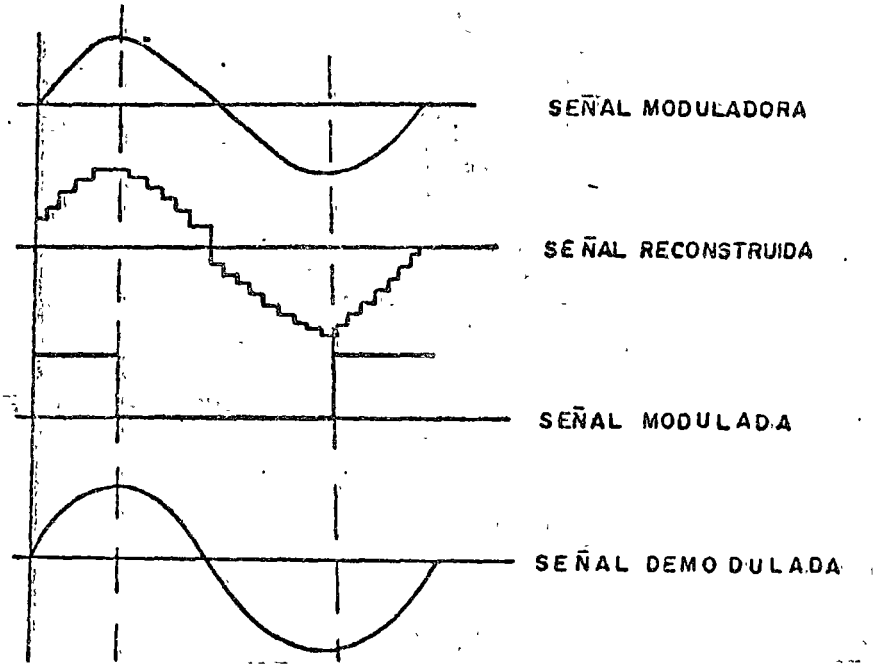


FIG. 2

El sistema descrito anteriormente tiene limitaciones. Si la pendiente de la señal moduladora aumenta al crecer la frecuencia, el modulador ya no se puede encadenar a ésta, porque los escalones tienen tamaño fijo. Para solucionar esto, se debe aumentar la frecuencia de los pulsos de reloj, o utilizar el método COMPANDED compresión-expansión, en el que se varía el tamaño de los escalones o su frecuencia, siguiendo alguna medida de la pendiente de la señal moduladora.

En las figuras tres y cuatro, se ilustran un modulador y demodulador que utilizan el método de compresión expansión, mencionado en el párrafo anterior.

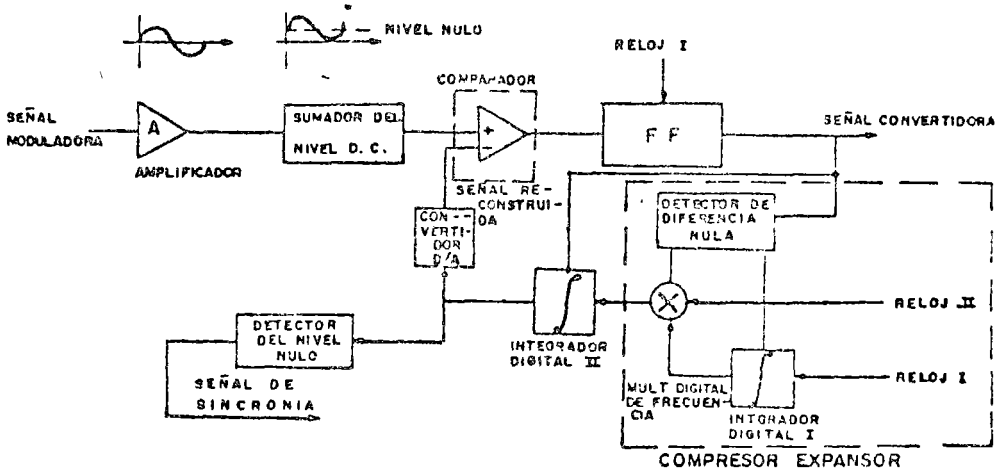


Fig. 3

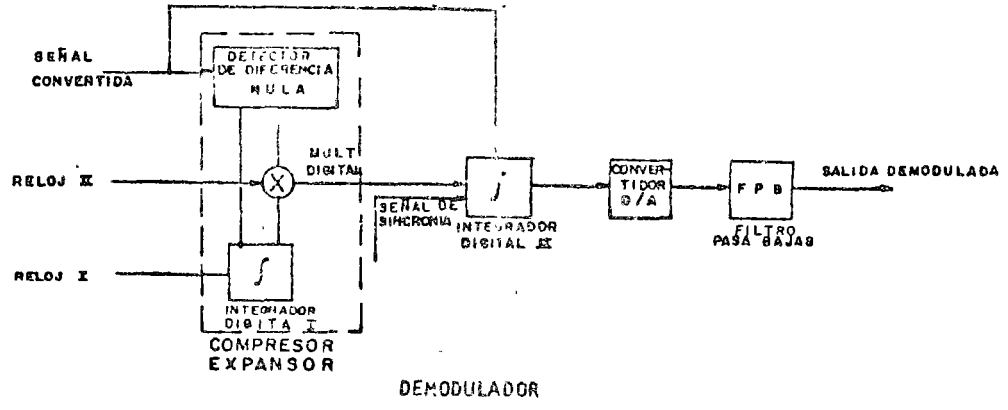
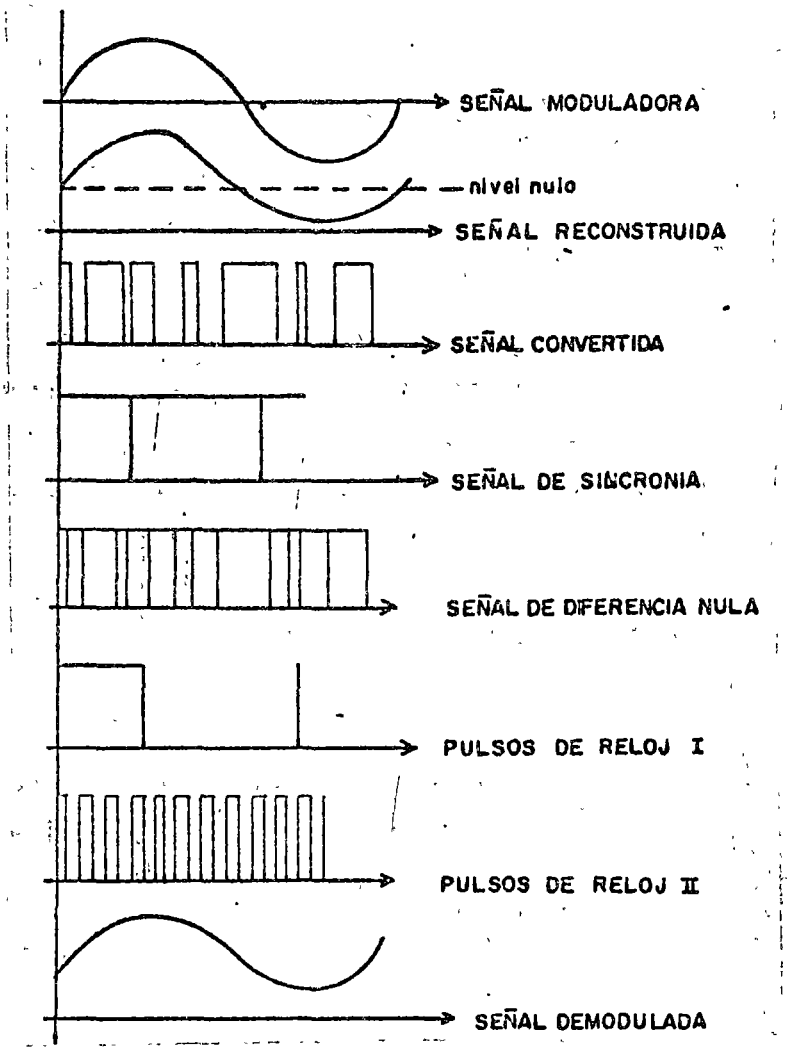


FIG. 4

Todas las funciones del sistema están realizadas con circuitos integrados digitales. El integrador es un contador, el multiplicador es un módulo variador de frecuencia. El detector de diferencia nula reinicializa al multiplicador e integrador. Las señales en los diferentes puntos son:



SEÑALES DETECTADAS EN PUNTOS DE PRUEBA

FIG. 5

La frecuencia de transmisión es 640 KHz porque B = 4 KHz, se toman 16 muestras por lo tanto la frecuencia de muestreo fm=4 x 16 = 64 KHz, y el sistema necesita diez ciclos en el bloque compresor-expansor para cuantizar una muestra, por lo que la frecuencia de transmisión ft = 10 x fm = 640 KHz. El reloj II es diez veces ft para funcionamiento del multiplicador.

3.0 EQUIPO EMPLEADO

Generador de funciones

Osciloscopio (ancho de banda superior a 10 MHz)
Analizador de espectros
Graficador x-y
Fuentes 5V, 12V, y -12V

4.0 EXPERIMENTOS A REALIZAR

4.1 Generar una senoide de 4 KHz y alimentarla al sistema. Comparar las salidas en los puntos de prueba con las señales mostradas en la presente.

4.2 Obtenga la figura de Lissajous entre la entrada y la salida. Escribir sus conclusiones.

4.3 Conectar la entrada a tierra y observar la salida del modulador. Escriba sus conclusiones.

4.4 Obtenga el espectro de frecuencia de la señal moduladora, de la señal modulada y de la señal demodulada. Utilice el graficador y acote los resultados.

PRACTICA V

MODULACION CON PULSOS DE UNA PORTADORA EN AMPLITUD (ASK), FASE (PSK) Y FRECUENCIA (FSK)

Objetivo: Adentrar físicamente al alumno en los procesos de modulación mediante pulsos, trabajando en el dominio del tiempo y en el de la frecuencia.

1- Teoría Básica

La modulación de amplitud mediante pulsos consiste en representar el estado uno por una señal portadora, mientras que el estado cero es representado por la ausencia de señal (0 volts) (ver Fig. 1a.).

Los estados en la modulación de frecuencia mediante pulsos se representan por 2 señales senoidales de diferente frecuencia, la frecuencia f(1) para el estado uno y f(0) para el estado cero (ver Fig. 1b).

En la modulación de fase mediante pulsos se emplea una sola señal senoidal portadora y la diferencia entre las señales que representan los estados uno y cero, es un desfasamiento (ver Fig. 1c).

2- Análisis de las Señales Moduladas

De la figura 2 se pueden obtener las siguientes expresiones analíticas para las señales moduladas:

$$g_{ASK}(t) = m(t)\, c_1(t)$$

$$g_{PSK}(t) = m'(t)\, c_1(t)$$

$$g_{FSK}(t) = m(t)\, c_1(t) + \overline{m(t)}\, c_2(t)$$

El espectro de amplitud de las funciones anteriores puede obtenerse tomando en cuenta que el producto en el domidio del tiempo se transforma en la operación convolución en el dominio de la frecuencia y además que:

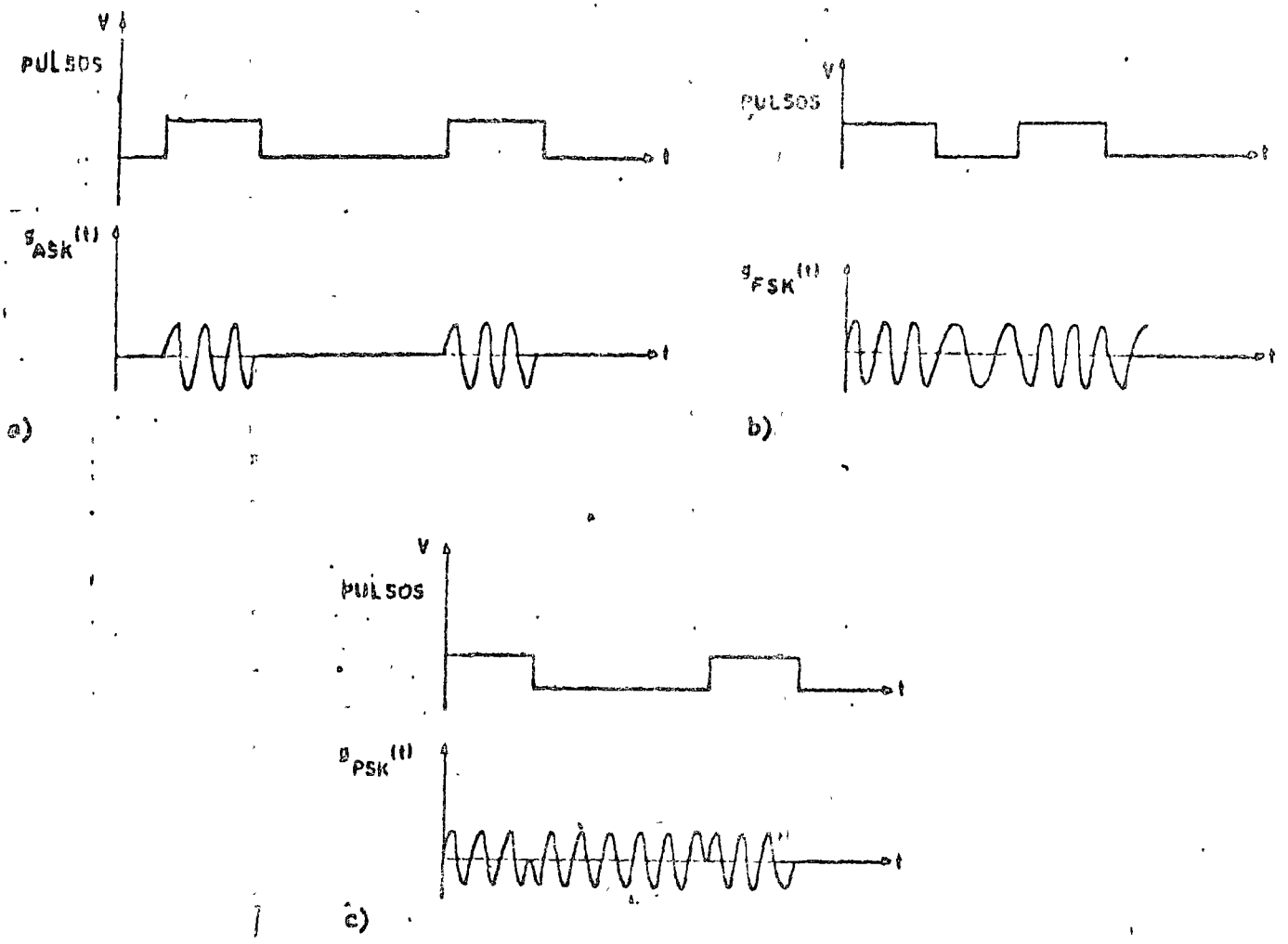


Figura 1. Modulación de: a)Amplitud, b)Frecuencia, c)Fase mediante pulsos.

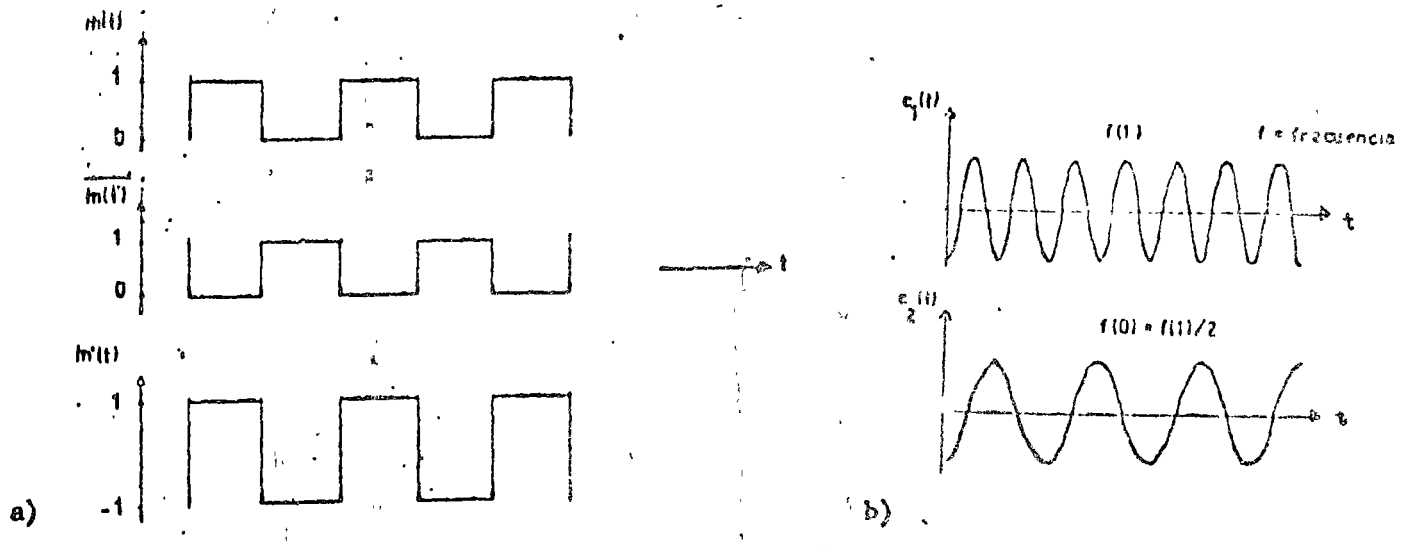


Figura 2. Señales: a) Modulantes, b) Portadoras

$$M(f) \ * \ \delta(f-f_0) = M(f-f_0)$$

3- Experimentos a realizar

Conecte el modulador digital al osciloscopio y al analizador de espectro para hacer las observaciones tanto en el dominio del tiempo como en el de la frecuencia.

a) Para una frecuencia de la señal portadora de 5 KHz. y seleccionado como señal modulante una secuencia 1010... de 1000 bits/seg. (del mod. digital). Observe para cuando se selecciona: ASK, PSK, FSK y PULSOS.

   Es importante para una mejor apreciación, que las ondas en el osciloscopio se encuentren fijas. Para lograrlo, tome la salida de sincronización del modulador digital y conéctela a la sincronización del osciloscopio, mueva lentamente el selector de frecuencia alrededor de la frecuencia deseada hasta lograr que la onda se fije.

b) Realice los mismos experimentos, para cuando en vez de usar los pulsos de la secuencia, se usan los pulsos de la codificación de una señal senoidal de amplitud 0.6 volts y frecuencia 0.1 Hz. introducida a la entrada del modulador digital. Ponga el selector de pulsos ADC.

c) Ahora introduzca pulsos de amplitud 2 volts y 10% de ciclo de trabajo con una frecuencia de 1 KHz, a la entrada del modulador digital. Ponga el selector de pulsos en la posición Pulsos Ext. y para la señal portadora use $f(\frac{n}{d})$=10 KHz. Observe y grafique para cuando se selecciona ASK, PSK, FSK y Pulsos.

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LA ELECTRONICA EN LAS COMUNICACIONES

PRACTICA VI

MEDICIONES DE LAS CARACTERISTICAS DEL RUIDO

AGOSTO DE 1976.

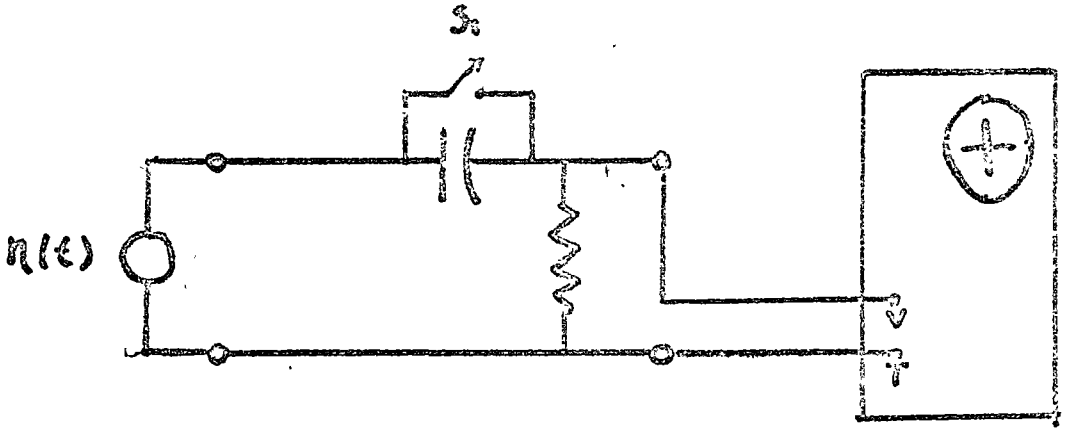
Palacio de Minería Calle de Tacuba 5, primer piso. México 1, D. F. Tels: 521-40-23 521-73-35 5123-123

PRACTICA VI

MEDICIONES DE LAS CARACTERISTICAS DEL RUIDO

Objetivo: Explicar en forma práctica algunos métodos usados en la determinación de características estadísticas del ruido.

1- Determinación de la media: La media de una señal $x(t)$ se puede determinar usando el arreglo mostrado en la figura 1.

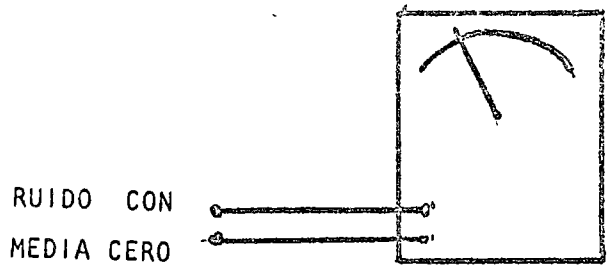


ARREGLO USADO EN LA DETERMINACION DE LA MEDIA DE UNA SEÑAL $x(t)$

FIG. 1

La media de $x(t)$ será igual a la diferencia de nivel que se registre en el osciloscopio al abrir y cerrar el interruptor S_1.

2- Determinación de la varianza: Para medir la varianza del ruido que esté analizando se puede emplear el siguiente arreglo:



VOLTMETRO RMS

FIG. 2

La varianza será igual a la lectura del volmetro RMS ya que:

$$\sigma^2 = \int_{-\infty}^{\infty} x^2 p(x)\,dx \quad . \quad . \quad . \qquad (1)$$

si el proceso que genera a el ruido es ergódico:

$$\int_{-\infty}^{\infty} x^2 p(x)\,dx = \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{T/2} x^2(t)\,dt \quad . \quad . \quad . \quad . \qquad (2)$$

$$\sigma^2 = \lim_{T\to\infty} \int_{-T/2}^{T/2} x^2(t)\,dt \quad . \quad . \quad . \quad . \quad . \qquad (3)$$

además

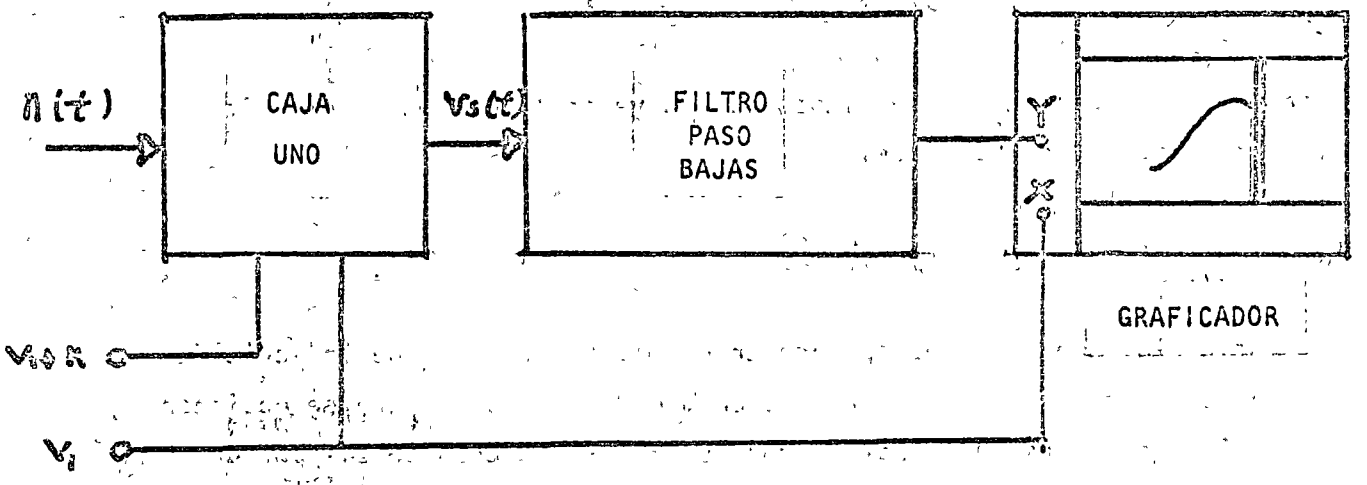
$$v_{rms} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} x^2(t)\,dt}$$

por lo que se concluye que:

$$\sigma = v_{rms} \quad - \quad - \quad - \quad - \quad - \quad - \qquad (4)$$

3- Determinación de la función de densidad de probabilidad

Para determinar la función de densidad de probabilidad se puede emplear el siguiente arreglo:

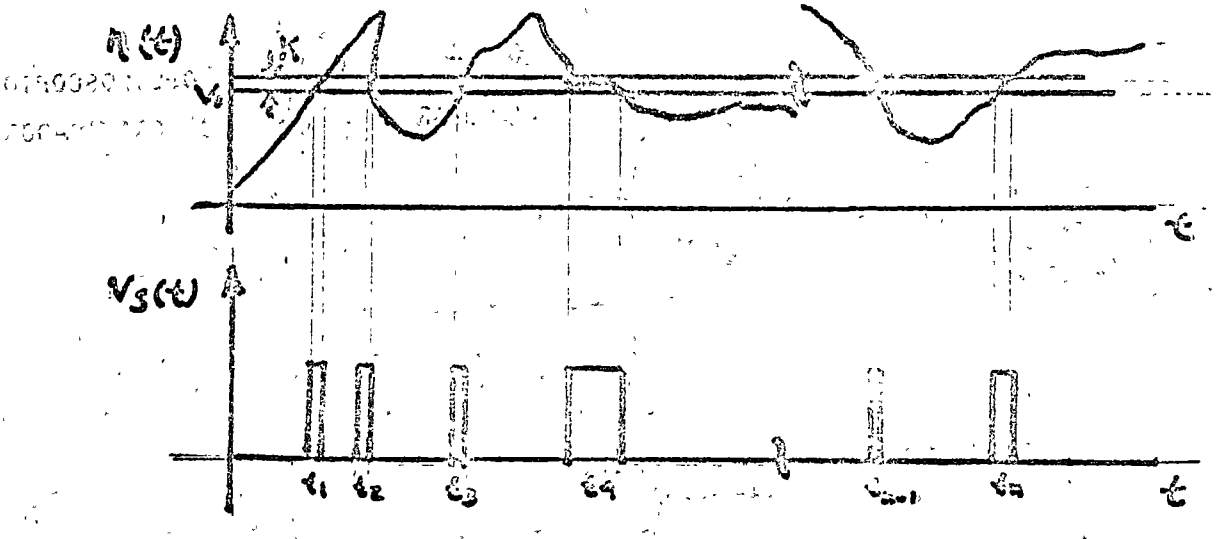


ARREGLO EMPLEADO EN LA DETERMINACION DE p(x)

FIG. 3

La caja uno es básicamente un comparador de ventana cuyos umbrales varían linealmente.

En la figura (3) se muestran la salida y la entrada de la caja uno para un valor fijo de v_1.



ENTRADA Y SALIDA DE LA CAJA UNO

FIG. 4

Si el proceso es ergódico y k es pequeño

$$p(v_1 < n < v_1+k) = \frac{1}{T}\sum_{i=1}^{n} t_i$$

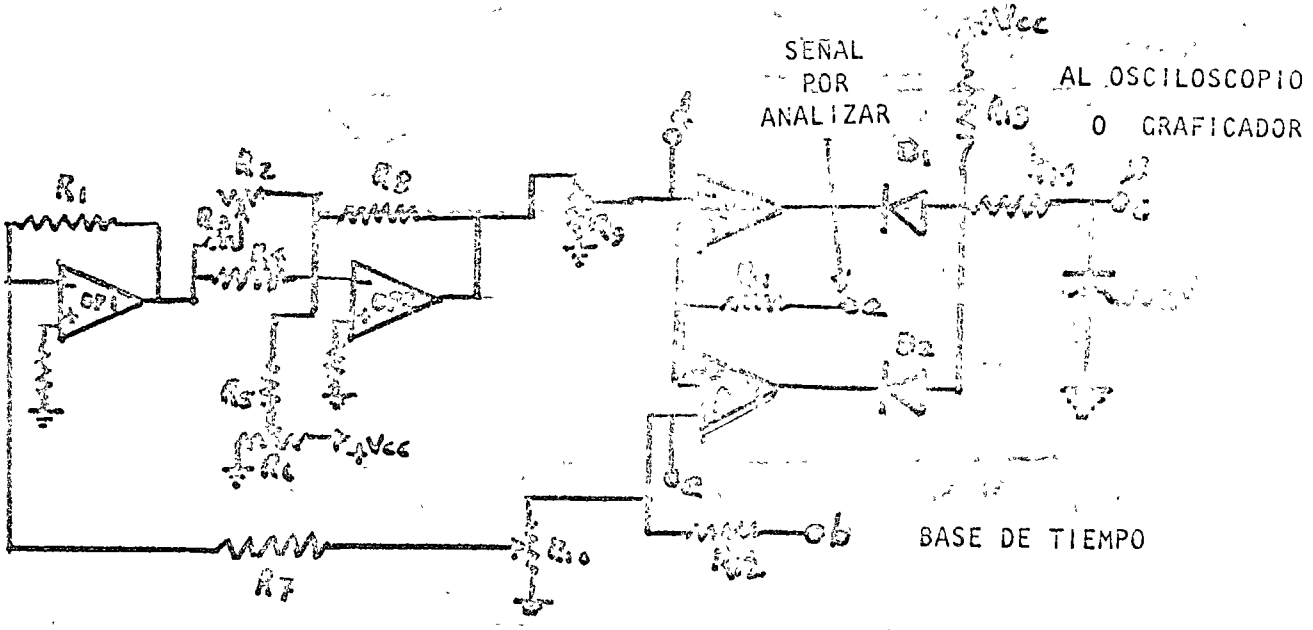
donde T es el tiempo que v_1 permanece en un valor fijo. De la ecuación anterior se puede concluir que:

$$p(v_1) \sim \sum t_i$$

El valor de la sumatoria que aparece en el miembro derecho de la ecuación anterior está en relación del valor promedio de los pulsos que se obtienen a la salida de la caja uno, por lo cual si se pasan dichos pulsos por un filtro pasa bajas, lo que se obtiene a la salida del filtro es un voltaje que es proporcional al valor de la función de densidad de probabilidad para $n = v_1$.

Si ahora en lugar de tener fija la ventana en un valor, se le barre desde un cierto valor negativo a otro positivo de tal manera que la amplitud de la señal por analizar quede contenida dentro de los límites del intervalo anterior, lo que se obtiene en el graficador es el dibujo de la función de densidad de probabilidad.

En la figura cinco se ilustra un circuito empleado para implementar lo que se ha dicho anteriormente.



CIRCUITO EMPLEADO PARA DETERMINAR p(x)
FIG. 5

Los pasos a seguir para calibrar el circuito son los siguientea;

a) Polarización: ± 12 v

b) Base de tiempo - la base de tiempo a usarse, debe ser una onda diente de sierra, con una frecuencia de aproximadamente 0.1 Hz y una amplitud máxima de ± 12 v. El punto donde se aplica está indicado en la figura 5 .

c) Calibración de la ventana.- Conecte una onda triangular de 100 Hz y ± 8 v. de amplitud al punto b. Observe en un osciloscopio de doble trazo las señales en los puntos d y e. Ajuste R_2, R_9 y R_{10} hasta obtener las mismas pendientes.

d) Ajuste de la anchura de la ventana.- En el arreglo utilizado en la calibración anterior, apague el generador de onda triangular, desconecte del osciloscopio los puntos d y e; haga coincidir los dos trazos del osciloscopio en uno solo; conecte al osciloscopio los puntos d y e; la separación que muestren los dos trazos será la anchura de la ventana. Dicha anchura se puede variar ajustado R_6. El intervalo de valores típicos es $0.5 \leq v_t \leq 2.5$ dependiendo de la amplitud de la señal que se esté analizando.

e) Ajuste con ruido.- Conecte el arreglo mostrado en la figura 6, varíe R_6 hasta que el valor de la varianza coincida con el valor que indica el voltmetro rms.

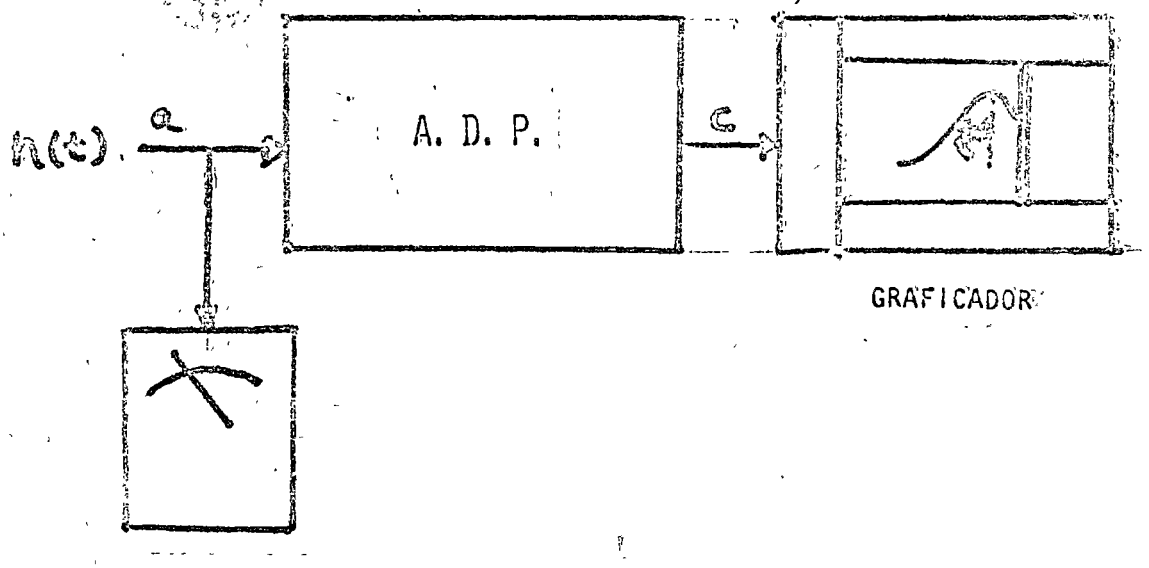
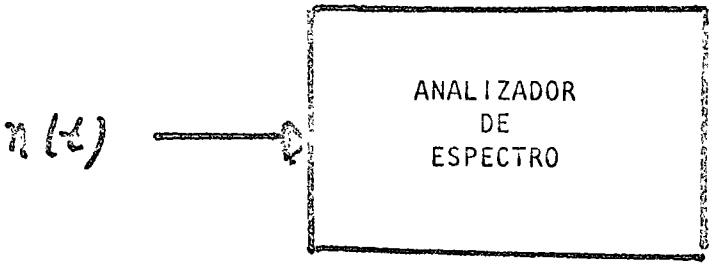


FIG. 6

4- Determinación del Espectro

El arreglo siguiente es empleado en la determinación del espectro del ruido.



ARREGLO EMPLEADO EN LA DETERMINACION DEL ESPECTRO DEL RUIDO

FIG. 7

PRACTICA VII

CODIFICADOR-DECODIFICADOR EMPLEANDO UN CODIGO DE BLOQUES (7,3), SISTEMATICO

1- Objetivo: familiarización con el uso de los códigos de bloques y, en particular, con el código (7,3) sistemático.

2- Aparatos: Generador de pulsos, fuente de corriente directa, osciloscopio, Codificador-Decodificador.

3- Características General del CODEC:

Trabaja en base a un código de bloques (7,3) sistemático. Utiliza un generador de pulsos externo como reloj del sistema. Lleva incorporado un introductor de errores sencillos para simular los que provocaría el ruido del canal de transmisión.
Muestra mediante LEDS los vectores U, X, Y, y S.
Está realizado en su totalidad con circuitos integrados TTL con polarización de 5 volts y tierra.

4- Desarrollo Matemático:

a) Introduciendo varias combinaciones en el vector U y observando su correspondiente vector X a la salida del codificador, halle cada una de las componentes de X. ¿Es sistemático el código empleado?

b) Conocido X, encuentre la matriz generadora G y la de verificación de paridad H .

c) Encuentre los síndromes correspondientes a cada vector Z de error. Hágalo solamente para errores sencillos. ¿Cuantos errores dobles, aparte de los sencillos, sería posible corregir?

5- Pasos a seguir:

a) Alimente las entradas de 5 v., tierra y clock del CODEC

b) Elija cualquier vector U de entrada al codificador y observe en el osciloscopio la salida X. Compruebe que ésta coincida con la mostrada por los LEDS.

c) Conecte la salida X del codificador a la entrada del introductor de errores y verifique que éste funcione introduciendo errores sencillos en cada bit del vector X.
Vea en el otro canal del osciloscopio la salida Y del introductor de errores y compárela con X.

d) Ahora conecte la salida Y del introductor de errores a la entrada del decodificador. Ponga el selector de errores en la posición "0" (sin error). Observe que el vector U de salida coincide con el de entrada al codificador. Introduzca errores en cada posición. El vector U permanece invariante, lo cual demuestra que el decodificador está corrigiendo cualquier error sencillo.

e) Verifique la correspondencia entre el vector Z de error y el Síndrome, para errores en cada uno de los dígitos de X. Compare la Tabla de Decodificación encontrada en la práctica con la calculada en el inciso 4.c.

f) Repita (c), (d) y (e) para otras combinaciones de U. Experimente en otras frecuencias.

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