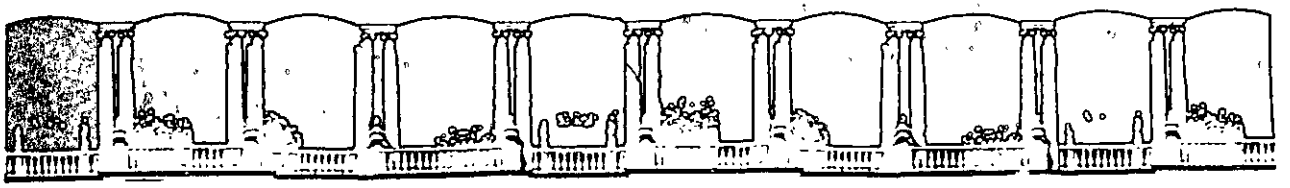

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

FACULTAD DE INGENIERIA U.N.A.M.
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CENTRO DE INFORMACION Y DOCUMENTACION
"ING. BRUNO MASCANZONI"

El Centro de Información y Documentación Ing. Bruno Mascanzoni tiene por objetivo satisfacer las necesidades de actualización y proporcionar una adecuada información que permita a los ingenieros, profesores y alumnos estar al tanto del estado actual del conocimiento sobre temas específicos, enfatizando las investigaciones de vanguardia de los campos de la ingeniería, tanto nacionales como extranjeras.

Es por ello que se pone a disposición de los asistentes a los cursos de la DECFI, así como del público en general los siguientes servicios:

- **Préstamo interno.**
- **Préstamo externo.**
- **Préstamo interbibliotecario.**
- **Servicio de fotocopiado.**
- **Consulta a los bancos de datos: librunam, seriunam en cd-rom.**

Los materiales a disposición son:

- **Libros.**
- **Tesis de posgrado.**
- **Noticias técnicas.**
- **Publicaciones periódicas.**
- **Publicaciones de la Academia Mexicana de Ingeniería.**
- **Notas de los cursos que se han impartido de 1980 a la fecha.**

En las áreas de ingeniería industrial, civil, electrónica, ciencias de la tierra, computación y, mecánica y eléctrica.

El CID se encuentra ubicado en el mezzanine del Palacio de Minería, lado oriente.

El horario de servicio es de 10:00 a 19:30 horas de lunes a viernes.

Palacio de Minería Calle de Tacuba 5 Primer piso Deleg. Cuauhtémoc 06000 México, D.F. APDO. Postal M-2285
Teléfonos: 512-8955 512-5121 521-7335 521-1987 Fax 510-0573 521-4020 AL 26

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

A LOS ASISTENTES A LOS CURSOS

Las autoridades de la Facultad de Ingeniería, por conducto del jefe de la División de Educación Continua, otorgan una constancia de asistencia a quienes cumplan con los requisitos establecidos para cada curso.

El control de asistencia se llevará a cabo a través de la persona que le entregó las notas. Las inasistencias serán computadas por las autoridades de la División, con el fin de entregarle constancia solamente a los alumnos que tengan un mínimo de 80% de asistencias.

Pedimos a los asistentes recoger su constancia el día de la clausura. Estas se retendrán por el periodo de un año, pasado este tiempo la DECFI no se hará responsable de este documento.

Se recomienda a los asistentes participar activamente con sus ideas y experiencias, pues los cursos que ofrece la División están planeados para que los profesores expongan una tesis, pero sobre todo, para que coordinen las opiniones de todos los interesados, constituyendo verdaderos seminarios.

Es muy importante que todos los asistentes llenen y entreguen su hoja de inscripción al inicio del curso, información que servirá para integrar un directorio de asistentes, que se entregará oportunamente.

Con el objeto de mejorar los servicios que la División de Educación Continua ofrece, al final del curso deberán entregar la evaluación a través de un cuestionario diseñado para emitir juicios anónimos.

Se recomienda llenar dicha evaluación conforme los profesores impartan sus clases, a efecto de no llenar en la última sesión las evaluaciones y con esto sean más fehacientes sus apreciaciones.

Atentamente

División de Educación Continua.

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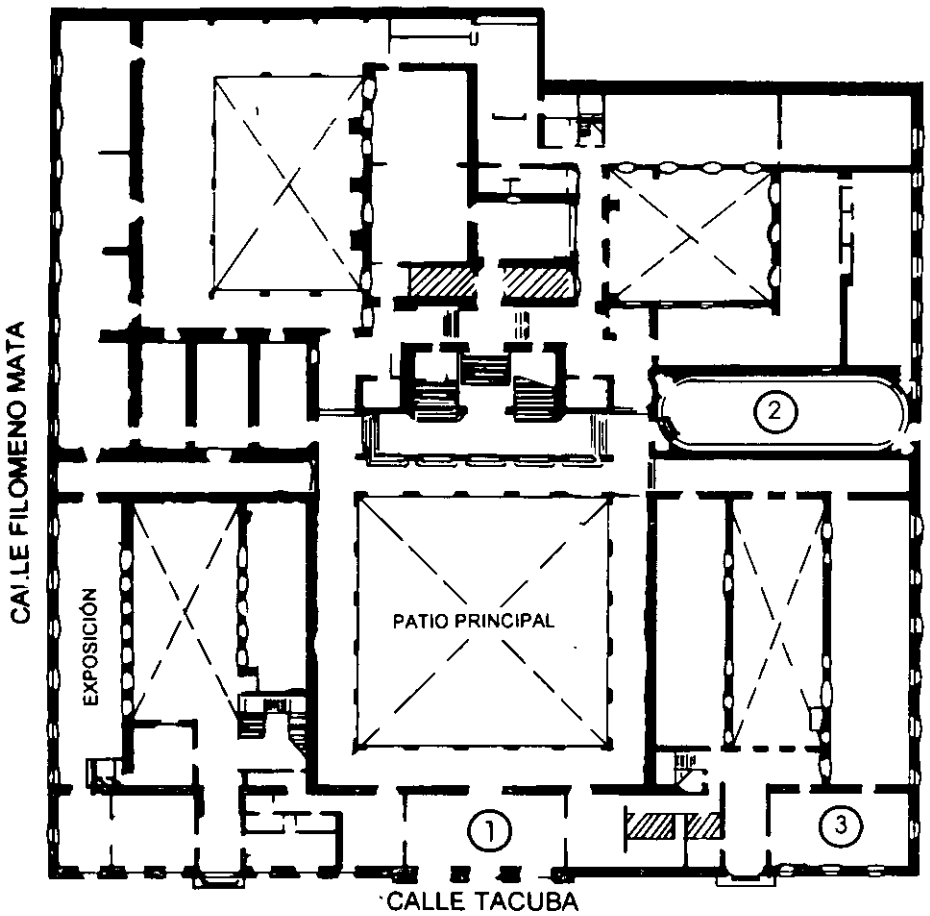
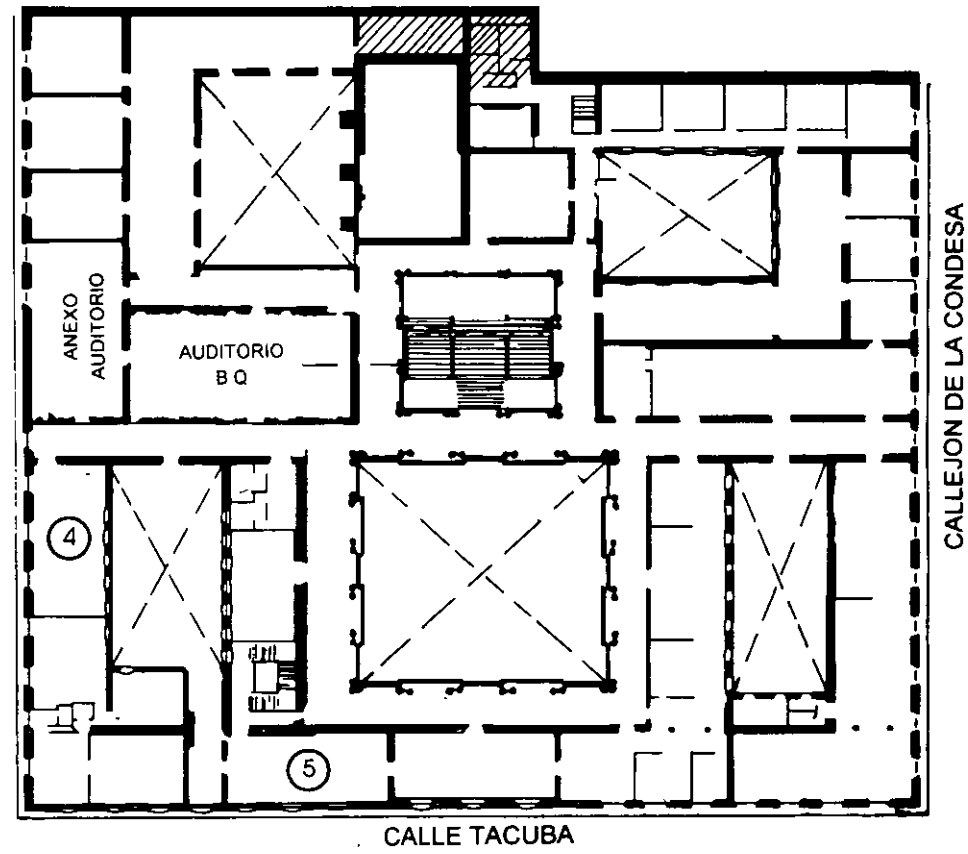
PALACIO DE MINERIA

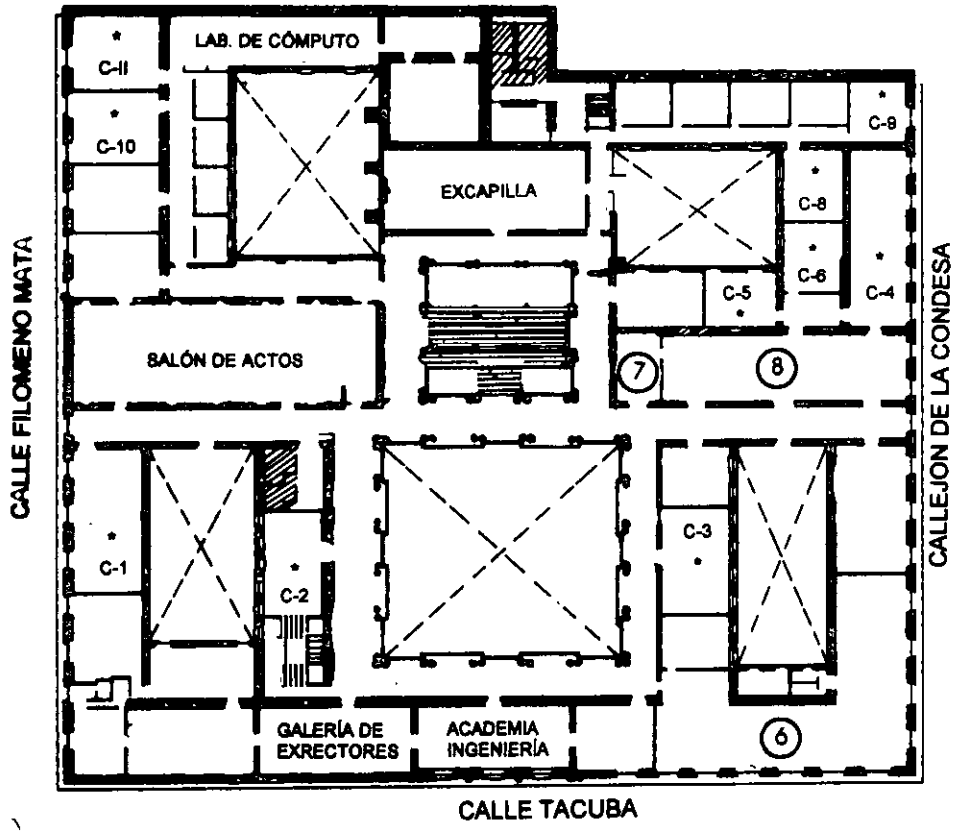


PLANTA BAJA



MEZZANINNE

PALACIO DE MINERIA



Ier. PISO

GUÍA DE LOCALIZACIÓN

1. ACCESO
2. BIBLIOTECA HISTÓRICA
3. LIBRERÍA UNAM
4. CENTRO DE INFORMACIÓN Y DOCUMENTACIÓN "ING. BRUNO MASCANZONI"
5. PROGRAMA DE APOYO A LA TITULACIÓN
6. OFICINAS GENERALES
7. ENTREGA DE MATERIAL Y CONTROL DE ASISTENCIA
8. SALA DE DESCANSO

SANITARIOS

* AULAS

DIVISIÓN DE EDUCACIÓN CONTINUA
FACULTAD DE INGENIERÍA U.N.A.M.
CURSOS ABIERTOS

DIVISIÓN DE EDUCACIÓN CONTINUA
DEC

DIVISION DE EDUCACION CONTINUA
FACULTAD DE INGENIERIA, UNAM
CURSOS ABIERTOS

DIVISIÓN DE EDUCACIÓN CONTINUA

CURSO: **CC105 MANTENIMIENTO DE PC'S Y PERIFERICOS (PARTE II)**
FECHA: **23 de noviembre al 4 de diciembre de 1998**

EVALUACIÓN DEL PERSONAL DOCENTE

(ESCALA DE EVALUACIÓN 1 A 10)

CONFERENCISTA	DOMINIO DEL TEMA	USO DE AYUDAS AUDIOVISUALES	COMUNICACIÓN CON EL ASISTENTE	PUNTUALIDAD
ING. JUAN CARLOS MAGAÑA C.				

Promedio _____

EVALUACIÓN DE LA ENSEÑANZA

CONCEPTO	CALIF.
ORGANIZACIÓN Y DESARROLLO DEL CURSO	
GRADO DE PROFUNDIDAD DEL CURSO	
ACTUALIZACIÓN DEL CURSO	
APLICACIÓN PRACTICA DEL CURSO	

Promedio _____

EVALUACIÓN DEL CURSO

CONCEPTO	CALIF.
CUMPLIMIENTO DE LOS OBJETIVOS DEL CURSO	
CONTINUIDAD EN LOS TEMAS	
CALIDAD DEL MATERIAL DIDÁCTICO UTILIZADO	

Promedio _____

Evaluación total del curso_____

Continúa...2

1. ¿Le agradó su estancia en la División de Educación Continua?

SI ☐ NO ☐

Si indica que "NO" diga porqué: _____

2. Medio a través del cual se enteró del curso:

Periódico *La Jornada*	
Folleto anual	
Folleto del curso	
Gaceta UNAM	
Revistas técnicas	
Otro medio (Indique cuál)	

3. ¿Qué cambios sugeriría al curso para mejorarlo?

4. ¿Recomendaría el curso a otra(s) persona(s) ?

SI ☐ NO ☐

5.¿Qué cursos sugiere que imparta la División de Educación Continua?

6. Otras sugerencias

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

DIRECTORIO DE PROFESORES

ING. JUAN CARLOS MAGAÑA CISNEROS

CONSULTORES ICIMEX, S.A. DE C.V.
AV. UNIVERSIDAD No. 1810 - A - 1
COL. ROMERO DE TERREROS
DELEGACION COYOACAN
C.P. 04310 MEXICO, D.F.
TEL: 658 37 26

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

1.- INTRODUCCION

NOVIEMBRE - DICIEMBRE DE 1998

Palacio de Mineria Calle de Tacuba 5 Primer piso . Deleg Cuauhtémoc 06000 Mexico, D.F. APDC Postal M-2285
Telefonos 512-8955 512-5121 521-7335 521-1987 Fax 510-0573 521-4020 AL 26

MANTENIMIENTO DE PC'S Y PERIFERICOS PARTE II

T E M A R I O

- EVALUACION PREVIA DEL GRUPO

- 1.-INTRODUCCION

- 2.- REPASO Y CONSOLIDACION DE CONCEPTOS
- 2.1 Arquitectura de una Microcomputadora.
- 2.2 Características de los procesadores Pentium, Celeron y Pentium II.
- 2.3 Tecnologías ISA, EISA, PCI, Flash Bios.
- 2.4 Inventario de diagnóstico de control
- 2.5 Sección de práctica

- 3.- HERRAMIENTAS DE DIAGNOSTICO
- 3.1 Programas de Diagnóstico.
- 3.2 "EPROM's" de Diagnóstico.
- 3.3 Rutinas al "BIOS"; poderosa herramienta.
- 3.4 Setup de Configuración
- -Ambientes win95.
- -Ambientes win98.
- 3.5 Equipos de Diagnóstico.
- 3.6 Tarjetas de Diagnóstico
- 3.7 Sección de Práctica.

- 4.- MICROCONTROLADORES PRINCIPALES Y SISTEMAS MINIMOS
- 4.1 Controlador de Bus.
- 4.2 Controlador de DMA.
- 4.3 Generador de Reloj
- 4.4 Controlador de Periféricos Programable.
- 4.5 Controlador de Unidades de Disco.
- 4.6 Controlador de Teclado.
- 4.7 Sección de Práctica. con manejo de Osciloscopio y puntas Lógicas

- 5.- PERIFERICOS Y AJUSTES PRINCIPALES
- 5.1 Monitores.
- 5.2 Unidades de Disco.
- 5.3 Impresores.
- 5.4 No Breaks y UPS's
- 5.5 Sección de Práctica. Con manejo de Dispositivos de Diagnósticos y Alineación

- 6.- MANTENIMIENTO CORRECTIVO BASICO-MEDIO
- 6.1 Diagramas.
- 6.2 Señales de Prueba y Diagnóstico.
- 6.3 Microcontroladores, relojes y bases de tiempo.
- 6.4 Tendencia del servicio y Metodología Práctica
- 6.5 Sección de Práctica.

- 7.- DISCOS DUROS
- 7.1 Principales tecnologías y sus características.
- 7.2 Fallas de origen y mantenimiento físico.
- 7.3 Mantenimiento lógico.
- 7.4 Utilerías y Software de apoyo.

"MANTENIMIENTO DE PC's Y PERIFERICOS AVANZADO"

O B J E T I V O S

Obtener de los participantes el perfil medio de conocimientos con base a un evento de retroalimentación (TEST), a efecto de lograr la plataforma de partida, firme y bien orientada que permita un buen aprovechamineto.

Reafirmar en el grupo los conocimientos previos del tema y elevar su gradiente con tópicos y tendencias de actualidad, reforzándolo con teoría y principalmente prácticas, en cada apartado del temario, a efecto de que consolide los hábitos adecuados en el mantenimiento preventivo y correctivo básico-medio de sus equipos, sin pretender llegar a detalles de alto nivel en el campo de la Ingeniería del Hardware para Microcomputadoras.

Lograr que los participantes estén ciertos de que no se debe abusar de la confianza adquirida, ni perderle el respeto a los equipos, ya que durante el desarrollo del curso deberán ir aplicando con seguridad, los conocimientos logrados, sin el mínimo riesgo para el hardware.

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

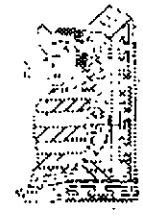
(PARTE II)

2.- REPASO Y CONSOLIDACION DE CONCEPTOS

NOVIEMBRE - DICIEMBRE DE 1998

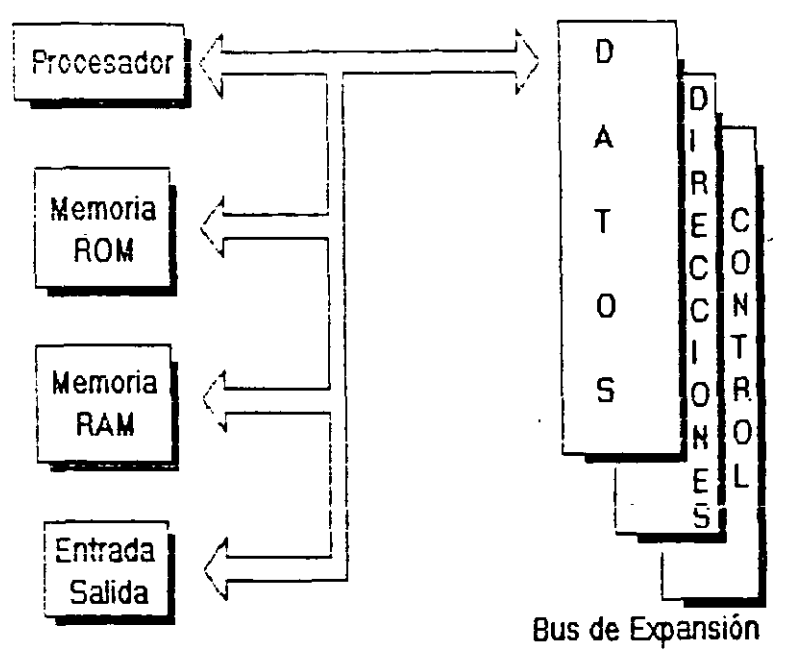
MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

2.- REPASO Y CONSOLIDACION DE CONCEPTOS



NOVIEMBRE DE 1998

Arquitectura de una computadora



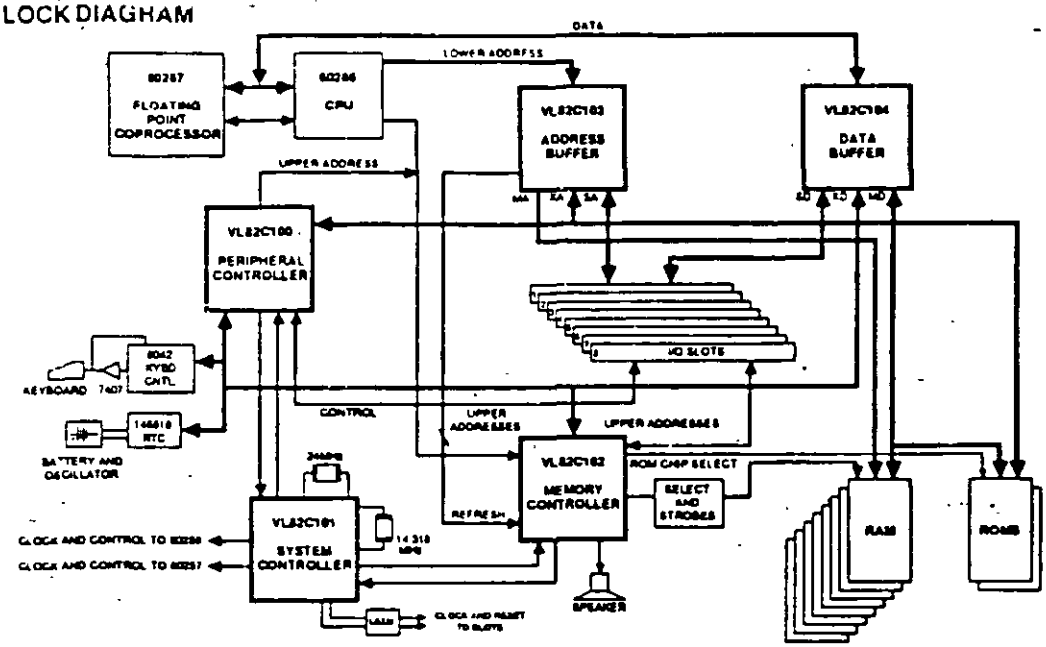
apuntes

Arquitectura de una computadora

B.1 System Block Diagram

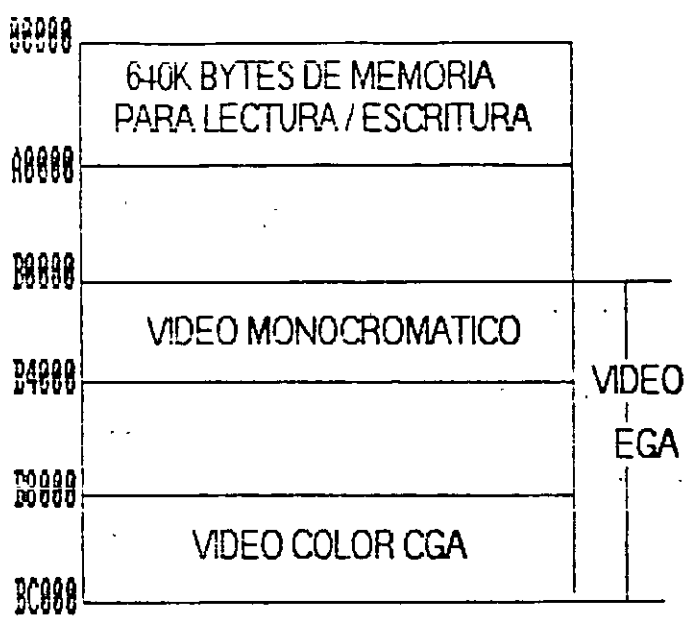
ATTACHMENT II

BLOCK DIAGRAM



apuntes

Mapa de memoria XT (RAM)



apuntes

Mapa de memoria XT (ROM)

apuntes

C.1 System Memory Map

Address Range	Start-End	Name	Function
000000-03FFFF	000K-256K	Bank 0	System memory (256K)
040000-07FFFF	256K-512K	Bank 1	System memory (256K)
080000-09FFFF	512K-640K	Bank 2	System memory (128K)
0AFFFF-0BFFFF	640K-768K	Video	Display card buffer (128K)
0C0000-0DFFFF	768K-896K	I/O ROM	Expansion ROM (128K)
0E0000-0EFFFF	896K-960K	ROM	System usage (64K)
0F0000-0FFFFF	960K-1024K	ROM	BIOS (64K)
100000-11FFFF	1024K-1152K	Bank 2	System memory (128K)
120000-15FFFF	1152K-1408K	Bank 3	System memory (128K)
160000-FDFFFF	1408K-16146K	RAM	Expansion RAM (14870K)
FE0000-FEFFFF	16146K-16210K	ROM	System usage (64K)
FF0000-FFFFFF	16210K-16274K	ROM	BIOS (64K)

apuntes

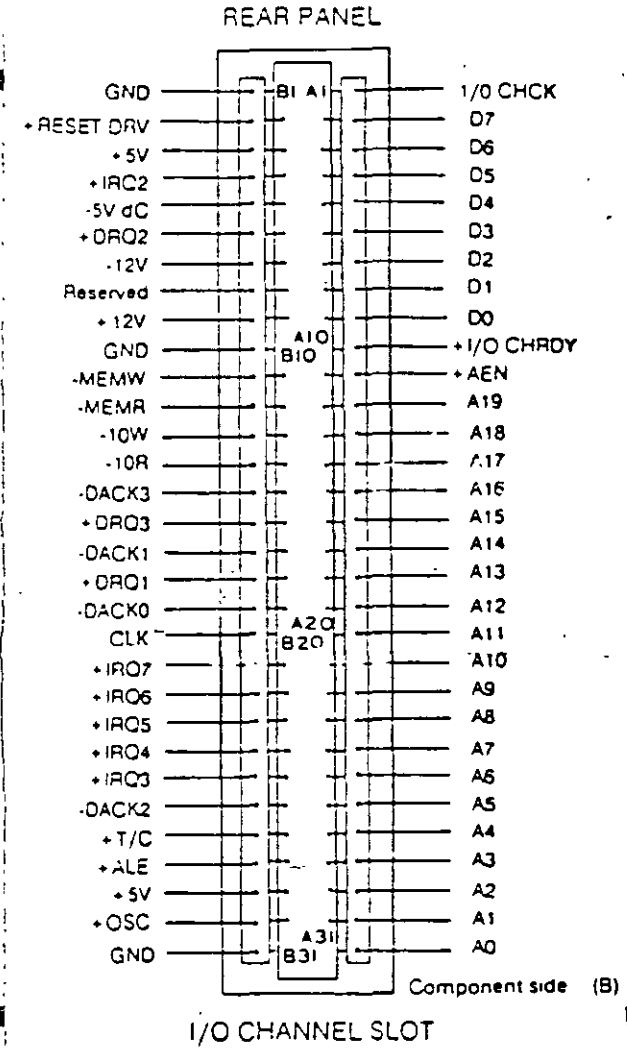
Arquitectura de una computadora

D.1 I/O Address Map

Hex Range	Devices	Usage
000-01F	DMA Controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	8042 (keyboard)	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear math Coprocessor busy	System
0F1	Reset math coprocessor	System
0F8-0FF	Math coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, bisynchronous 2	I/O
3A0-3AF	Bisynchronous 1	I/O
3B0-3BF	Monochrome display and printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphics monitor adapter	I/O
3F0-3F7	Diskette controller	I/O
3F8-3FF	Serial port 1	I/O

apuntes

Arquitectura de una computadora bus XT



apuntes

D.2 I/O Channel

Rear Panel

GND	B1	A1	-I/O CH CK
RESET DRV	B2	A2	SD7
+5Vdc	B3	A3	SD6
IRQ2	B4	A4	SD5
-5Vdc	B5	A5	SD4
DRQ2	B6	A6	SD3
-12Vdc	B7	A7	SD2
0WS	B8	A8	SD1
+12Vdc	B9	A9	SD0
GND	B10	A10	-I/O CH RDY
-SMEMW	B11	A11	AEN
-SMEMR	B12	A12	SA19
-IOW	B13	A13	SA18
-IOR	B14	A14	SA17
-DCK3	B15	A15	SA16
DRQ3	B16	A16	SA15
-DACK1	B17	A17	SA14
DRQ1	B18	A18	SA13
-REFRESH	B19	A19	SA12
CLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
-DACK2	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5Vdc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0

slot 1 - slot 8

apuntes

-MEMCS16	D1	C1	SBHE
I/O CS16	D2	C2	LA23
IRQ16	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
-DACK0	D8	C8	LA17
DRQ0	D9	C9	-MEMR
-DACK5	D10	C10	-MEMW
DRQ5	D11	C11	SD08
-DACK6	D12	C12	SD09
DRQ6	D13	C13	SD10
-DACK7	D14	C14	SD11
DRQ7	D15	C15	SD12
+5Vdc	D16	C16	SD13
-MASTER	D17	C17	SD14
GND	D18	C18	SD15

slot 10 - slot 15

apuntes

E.1 DMA Channels

Channel	Function
0	Spare (8-bit transfer)
1	SDLC (8-bit transfer)
2	Floppy disk (8-bit transfer)
3	Spare (8-bit transfer)
4	Cascade for DMA controller 1
5	Spare (16-bit transfer)
6	Spare (16-bit transfer)
7	Spare (16-bit transfer)

E.2 DMA Controller Registers

Hex Address	Command Codes
0C0	CH0 base and current address
0C2	CH0 base and current word count
0C4	CH1 base and current address
0C6	CH1 base and current word count
0C8	CH2 base and current address
0CA	CH2 base and current word count
0CC	CH3 base and current address
0CE	CH3 base and current word count
0D0	Read status register/Write command register
0D2	Write mode register
0D4	Read temporary registers/write command register
0D6	Write mode register
0D8	Clear byte pointer flip-flop
0DA	Read temporary register/Write mask clear
0DC	Clear mask register
0DE	Write all mask register bits

apuntes

E.3 Page Register Addresses

Page Register	I/O Hex Address
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

E.4 Interrupts

Level	Function
0	System timer output 0
1	Keyboard output buffer full
2	Interrupt from controller 2 (level 8-15)
3	Serial port 2
4	Serial port 1
5	Parallel port 2
6	Diskette controller
7	Parallel port
8	Real-time clock
9	Software redirected to INT 0AH
10	Reserved
11	Reserved
12	Reserved
13	80287
14	Hard disk drive
15	Reserved

apuntes

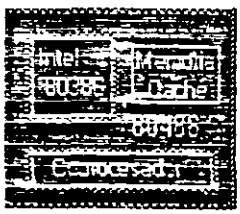
E.5 Timers

Channel	Function
0	System timer
1	Refresh request generator
2	Tone generation for speaker

apuntes

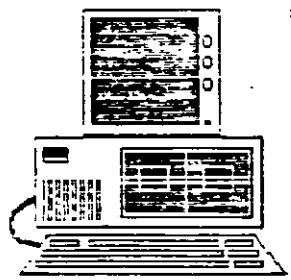
Características de los Procesadores

* Modo REAL *Modo PROTEGIDO



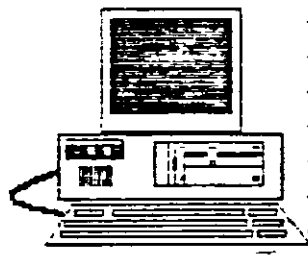
apuntes

Características de las distintas arquitecturas



XT 8088

* Liberación:1982
* Direccionamiento:1MB
* Memoria Usuario:640KB
* Almacenamiento:
  32MB (MS-DOS 2.xx)
  70MB (MS-DOS 3.xx)
* Velocidad:de 4.77 a 10 Mhz.
* $:

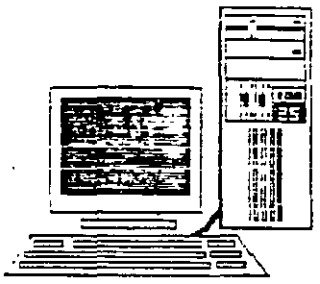


AT 80286

* Liberación:1986
* Direccionamiento:16MB
* Memoria Usuario:15MB
* Almacenamiento:2GB
* Velocidad:de 8 a 16 Mhz.
* $:

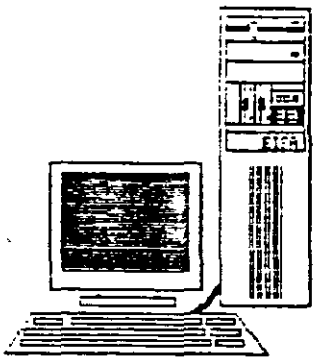
apuntes

Características de las distintas arquitecturas



AT 80386-80386/SX

* Liberación:1982
* Direccionamiento:4GB
* Memoria Usuario:
  Limitante Tecnológica
* Almacenamiento: en TB
* Velocidad:de 16 a 30 Mhz.
* $:



AT 80486

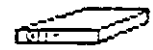
* Liberación:1990
* Características
  Similares al 386
* Incluye Memoria Caché
  y Coprocesador
* Tecnología:RISC
* Velocidad:de 25 a 55 Mhz.
* $:

apuntes

Principales Periféricos
Características

IMPRESORES

- *Paralelo / Serial*
- *Impacto / No Impacto*
- *Vel. de impresión (c.p.s.)*
- *Tipo de Alimentación*
- *Buffer*



MODEMS

- *Homologados*
- *Internos / Externos*
- *Vel. de Transmisión (B.p.s.)*
- *Protocolo*
- *Inteligentes*
- *Niveles de M.P.N.*

CONTROLADORES

- *Dependiendo del tipo; se ponderan varios puntos.*

UNIDADES DE ALMACENAMIENTO Y/O RESPALDO

- *Capacidad*
- *Tecnología*
- *Velocidad*
- *Costo*

Configuración switches XT

The locations of the two switches are shown in the following illustration of the system board.

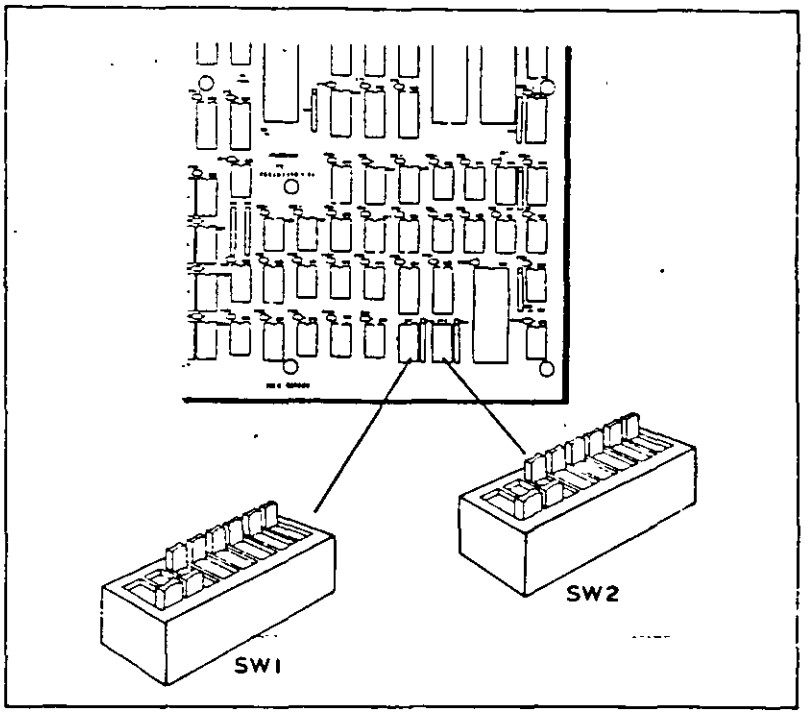


Fig. Locations of the DIP switches

ap.unbes

Configuración switches XT

A.3 Descriptions of the corresponding DIP Switches

1) SW1 -- DIP Switch One

Switch No.	Default Setting	Function
SW1-1	OFF	Enables disk drive.
SW1-2	ON	Disables 8087 interrupt.
SW1-3	*	(SW1-3 and SW1-4 determine the
SW1-4	*	amount of RAM installed on the system board.)
SW1-5	*	Determines display type.
SW1-6	*	Determines display type.
SW1-7	*	(SW1-7 and SW1-8 determine the
SW1-8	*	number of disk drive(s) installed to the system unit.)

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Configuración switches XT

2) SW2 -- DIP Switch Two

Switch No.	Default Setting	Function
SW2-1		Reserved.
SW2-2		Reserved.
SW2-3		Reserved.
SW2-4		Reserved.
SW2-5		Reserved.
SW2-6	*	Determines the maximum amount of RAM which can be installed to the system board without using a memory expansion adapter.
SW2-7	ON	Enables the built-in RS-232C port.
SW2-8	ON	Enables the built-in parallel port.

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Configuración switches XT

A.5 Quick reference for Switch Settings involved with the memory size

SW2-6 ON - indicates the 640KB version.
OFF - indicates the 256KB version.

SW1-3	SW1-4	Enabled Bank	256K Version	640K Version
ON	ON	1	64K	256K
OFF	ON	1,2	128K	512K
ON	OFF	1,2,3	192K	576K
OFF	OFF	1,2,3,4	256K	640K

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Configuración switches AT

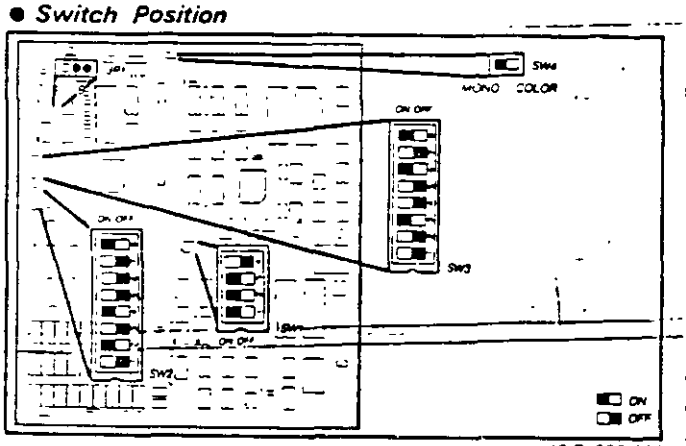
Quick Guide

■ On or closed □ OFF or open

FUNCTION SELECTION		SW1								SW2								SW4	
		1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	COLOR / MONO	
RAM SIZE	256KB				□	□													
	512KB				■	□													
	640KB				□	■													
	RAM				■	■										■			
DISPLAY TYPE	ENABLE						■											COLOR	A
	COLOR						□											*COLOR*	B
	MONO / DRIVE						□											MONO	B
SYSTEM SPEED	HIGH SPEED (*7.16MHz*)															■			
	LOW SPEED (*4.77MHz*)															□			
DRIVE NUMBER	1 DISK DRIVE			■										■	■				
	2 DISK DRIVE			□										□	■				
	4 DISK DRIVE			□										■	■				
BOOT	ENABLE			□															
	DISABLE			■															
COM1	ENABLE	■																	
	DISABLE	□																	
COM2	ENABLE	■																	
	DISABLE	□																	
CURRENT SETTING																			

FD: RAM WINDOW ADDRESS ON BOARD DISPLAY DISABLE | please refer to manual for

Switch Position



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Configuración switches AT

SW1 - SWITCH ONE

Switch No.	Setting	Function
SW1-1	OFF	Disable COM1
	ON (DEFAULT)	Enable COM1
SW1-2	OFF	Disable COM2
	ON (DEFAULT)	Enable COM2
SW1-3	OFF	Enable real time clock (RTC1)
	ON (DEFAULT)	Enable real time clock (RTC0)
SW1-4	OFF (DEFAULT)	Disable IRQ2
	ON	Enable IRQ2

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Que es un jumper ?

apuntes

Jumpers AT

JUMPER SETTING FOR DISPLAY AT JP1

The built-in display interface supports flicker free scrolling for the following display types:

- IBM monochrome compatibility
- IBM color graphics compatibilitv
- Hercules monochrome graphics compatibility
- Plantronics color plus compatibility

You may enable or disable the built-in display adapter by setting the JP1 jumper.

When using EGA card, the build-in display interface should be disabled by closing jumper JP1 at position A and setting SW2-6 to ON. The slide switch SW4 must be set to COLOR or MONOCHROME respectively when using color or monochrome monitor. Set SW4 to color if EGA mode is used.

apuntes

Configuración switches AT

Refer to the table on the floppy disk driver bracket. Adjacent to 768 KB and under SW2 you will see two small rectangles. The rectangles indicate how the switches are set. The third switch on switch block SW2 (SW2-3), and the fifth switch on switch block SW3 (SW3-5) are both set to OFF; and the fourth switch on the switch block SW2 (SW2-4), and the sixth switch on switch block SW3 (SW3-6) are both set to ON.

Again referring to the table, the two diskette drive configuration requires you to set the switches SW2-1, SW2-7 and SW2-8 to OFF, OFF and ON respectively.

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FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

3.- HERRAMIENTAS DE DIAGNOSTICO

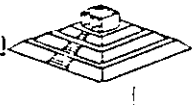
NOVIEMBRE - DICIEMBRE DE 1998

MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

3.- HERRAMIENTAS DE DIAGNOSTICO

NOVIEMBRE DE 1998

PROGRAMAS DE DIAGNOSTICO



Serial Number: 00-000000

COPYRIGHT (c) 1990, 1991 TouchStone Software Corporation
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Press Any Key to Continue

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PROGRAMAS DE DIAGNOSTICO

CheckIt 2.1

L O A D I N G

INVESTIGATING SYSTEM CONFIGURATION.

Local	√	Check for Remote Operation
AMI	√	Identify BIOS Manufacturer
Complete	√	Determine System Components
Complete	√	Look for RAM (Base, Extended, Expanded)
Not Present	√	Look for Math Co-processor
Not Present	√	Look for Mouse

System Configuration Checks Complete.

Press Any Key to Continue

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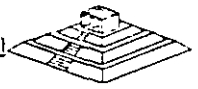
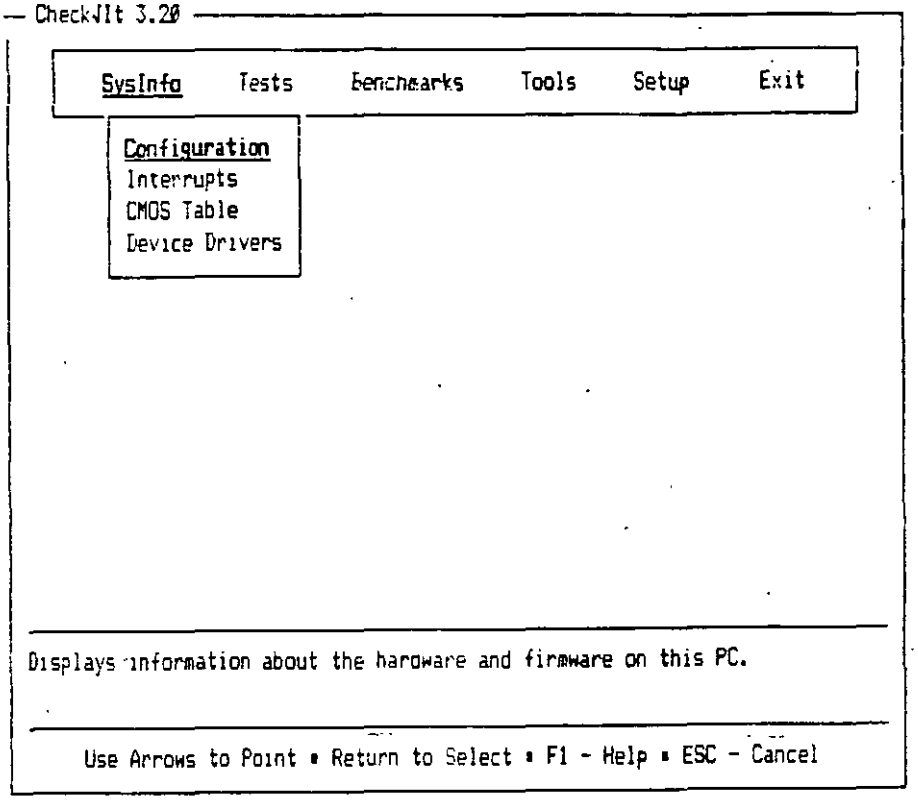
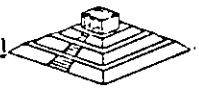
PROGRAMAS DE DIAGNOSTICO





PROGRAMAS DE DIAGNOSTICO



CheckIt 3.20

SysInfo Tests Benchmarks Tools Setup Exit

Configuration Information

```
     DOS Version: 3.31
        ROM BIOS: Unknown                    BIOS Date: Unknown

   Processor Type: 80286 XT Machine
 Math Coprocessor: Not Present
      Base Memory: 640K                Largest Free Block: 200K
  Extended Memory: None
  EXPANDed Memory: None
     Video Adapter: CGA
     Video Address: B800h                  Video RAM Size: 16K
     Hard Drive(s): Drive 0 (C:) = 33M
  Floppy Drive(s): A:Present
    Clock/Calendar: None
 Parallel Port(s): LPT1=3BCh, LPT2=378h
    Serial Port(s): COM1=3F8h
       Joystick(s): None
             Mouse: None
```

F2 - Copy to Activity Log Press Any Other Key to Continue

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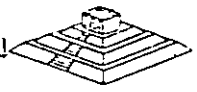
PROGRAMAS DE DIAGNOSTICO



CheckIt 2.1

SysInfo Tests Benchmarks Tools Setup Exit

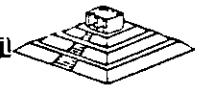
Configuration Information

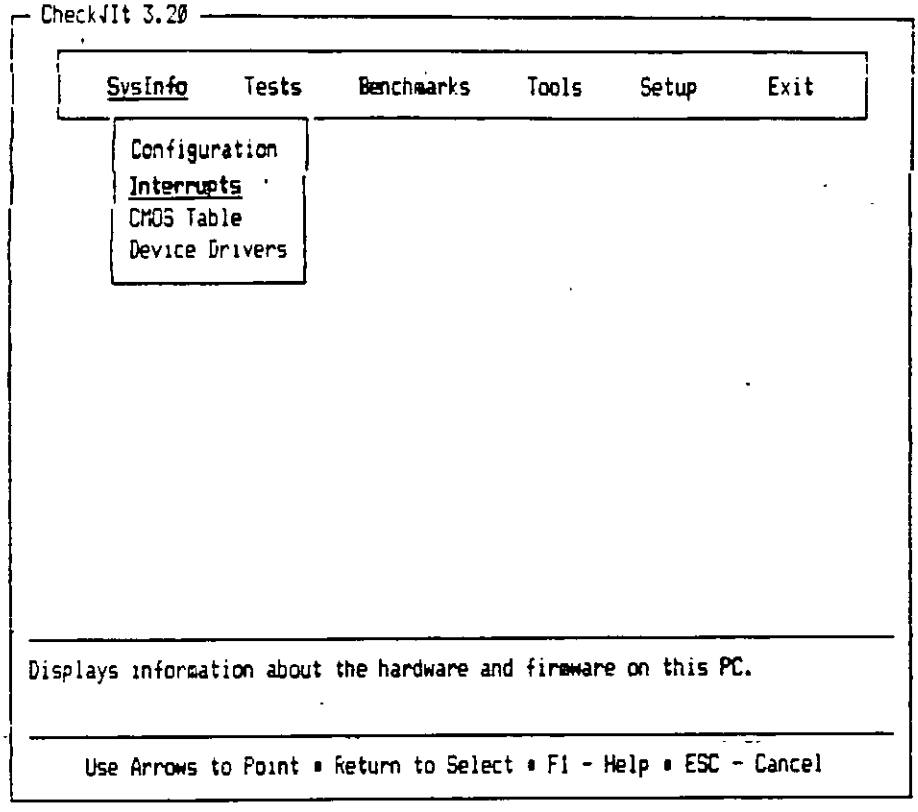
```
    DOS Version: 3.31
       ROM BIOS: AMI                          BIOS Date: 04/09/90

  Processor Type: 8086 AT Machine
Math Coprocessor: Not Present
     Base Memory: 640K                        Available: 436K
 Extended Memory: 1024K                       Available: 0K
 EXPANDed Memory: No EMS driver installed
   Video Adapter: EGA                      EGA Switches: 0110
   Video Address: A000h                 Video RAM Size: 256K
    Hard Drive(s): Drive 0 (Non-DOS) = 43M
 Floppy Drive(s): A:1.2M(5¼"), B:1.44M(3½")
  Clock/Calendar: CMOS Clock
Parallel Port(s): LPT1=378h, LPT2=278h
  Serial Port(s): COM1=3F8h, COM2=2F8h
           Mouse: None                      Joystick(s): None
```

F2 - Copy to Activity Log • Press Any Other Key to Continue

PROGRAMAS DE DIAGNOSTICO





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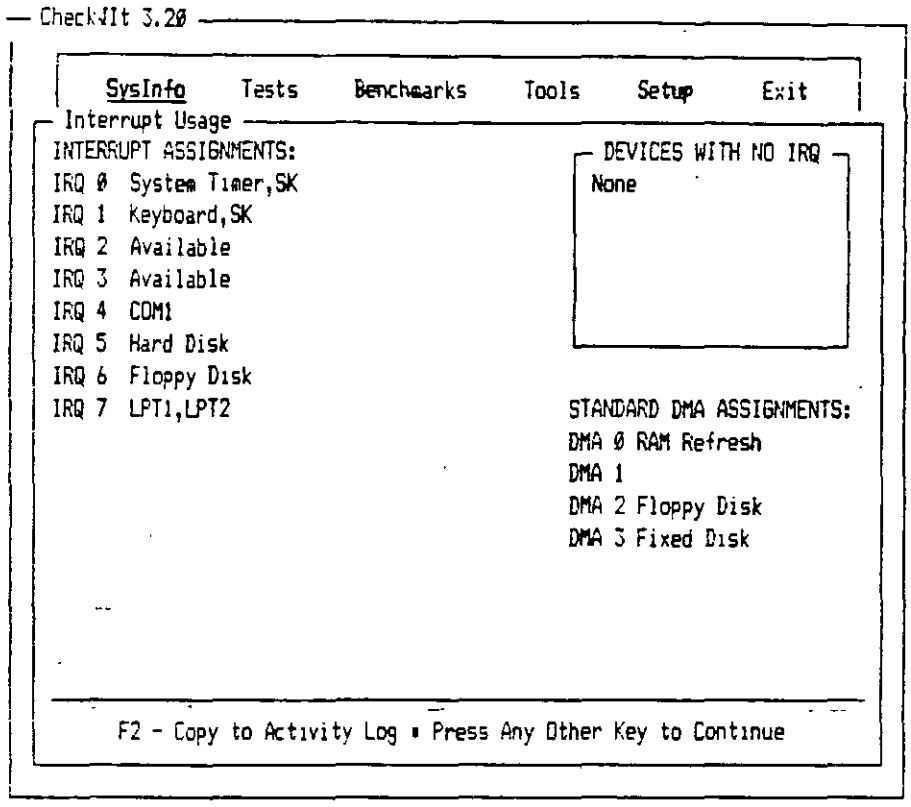
PROGRAMAS DE DIAGNOSTICO



PROGRAMAS DE DIAGNOSTICO

CheckIt 2.1

SysInfo Tests Benchmarks Tools Setup Exit

Interrupt Usage

INTERRUPT ASSIGNMENTS:

IRQ 0 System Timer,SK
IRQ 1 Keyboard,SK
IRQ 2 [Cascade]
IRQ 3 COM2,NET$OS
IRQ 4 COM1
IRQ 5 Available
IRQ 6 Floppy Disk
IRQ 7 LPT1
IRQ 8 Clock/Calendar
IRQ 9 Available
IRQ 10 Available
IRQ 11 Available
IRQ 12 Available
IRQ 13 Reserved for NPU
IRQ 14 Hard Disk
IRQ 15 NET$OS

DEVICES WITH NO IRQ
LPT2

STANDARD DMA ASSIGNMENTS:

DMA 0
DMA 1
DMA 2 Floppy Disk
DMA 3
DMA 4 [Cascade]
DMA 5
DMA 6
DMA 7

F2 - Copy to Activity Log Press Any Other Key to Continue

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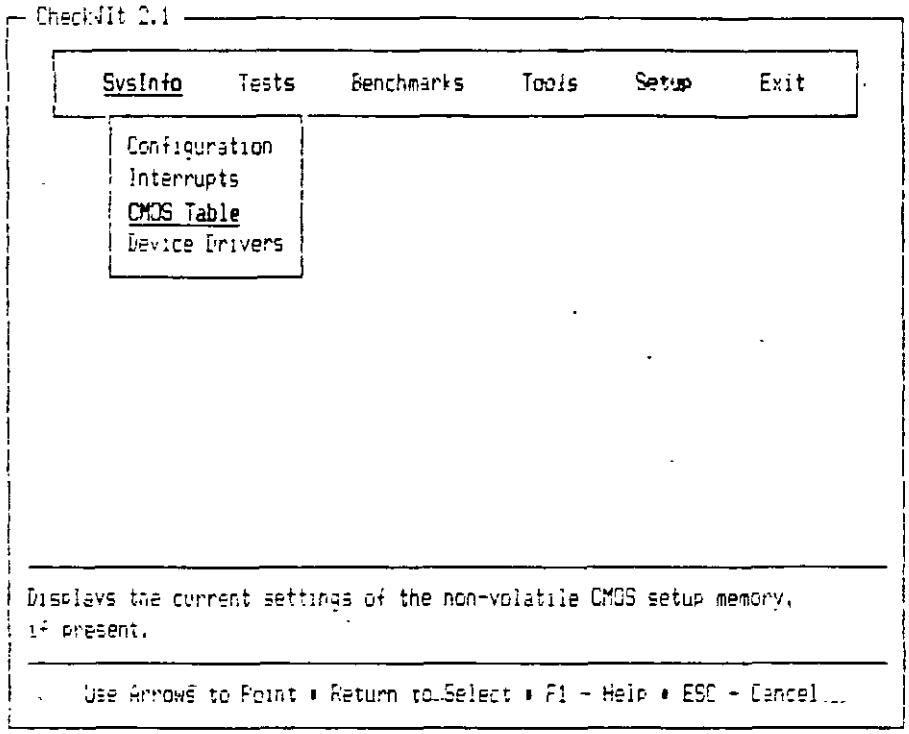
PROGRAMAS DE DIAGNOSTICO



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PROGRAMAS DE DIAGNOSTICO

CheckIt 2.1

SysInfo Tests Benchmarks Tools Setup Exit

Display CMOS Table

Current Date & Time: 11/01/1990 18:34:49

Floppy Drive A: 1.2M(5¼")
Floppy Drive B: 1.44M(3½")

Base Memory Size: 640K
Extended Memory Size: 1024K

Primary Display: EGA, PGA, VGA, etc.

DRIVE	TYPE	CYLS	HEADS	SECTS	WRITE PRECOMP	PARK PLACE	STEP RATE	CTRL BYTE	TOTAL BYTES
0:	46	820	6	17	820	820	0	0	42,823,680
1:	0	No Drive, ESDI Drive, or SCSI Drive.							

F2 - Copy to Activity Log ▪ Press Any Other Key to Continue

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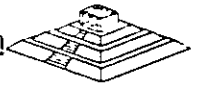
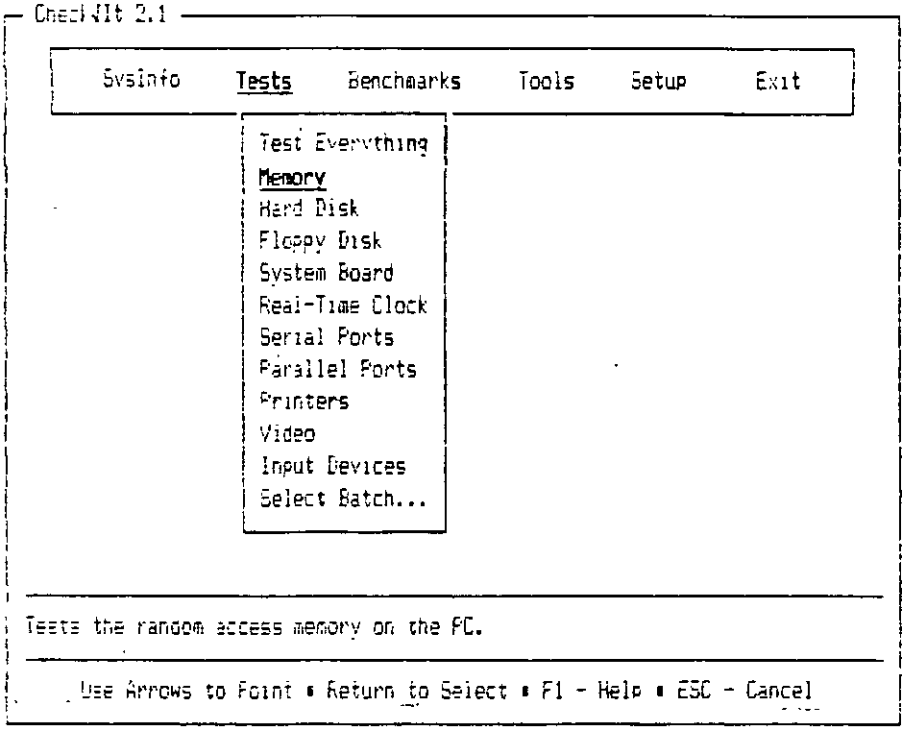
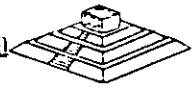
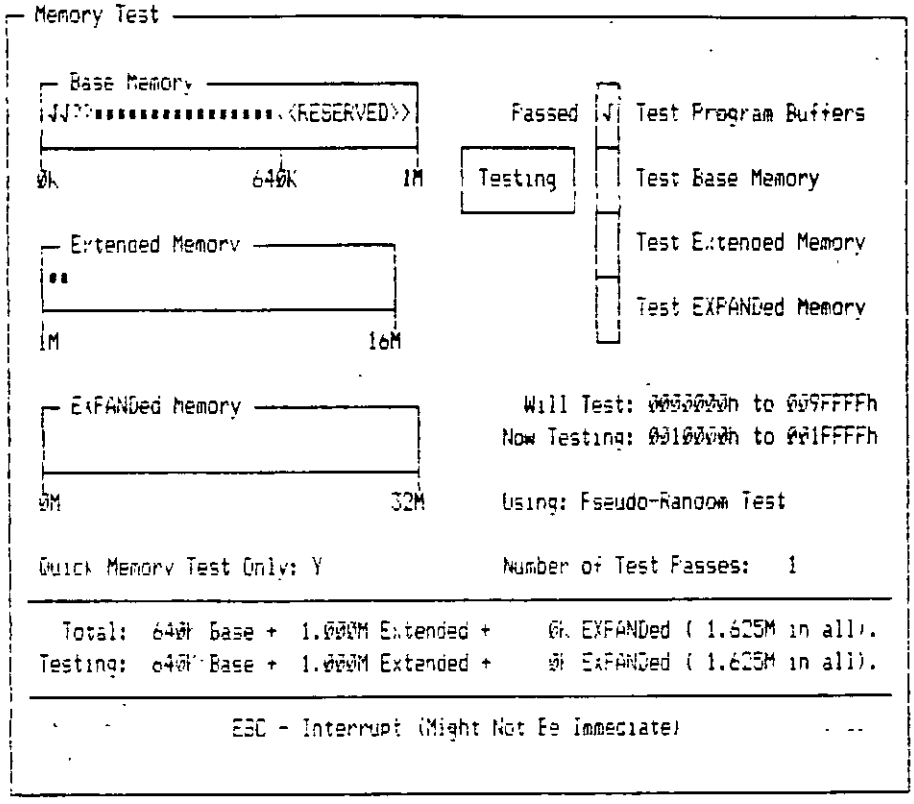
PROGRAMAS DE DIAGNOSTICO



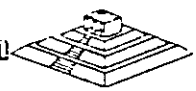


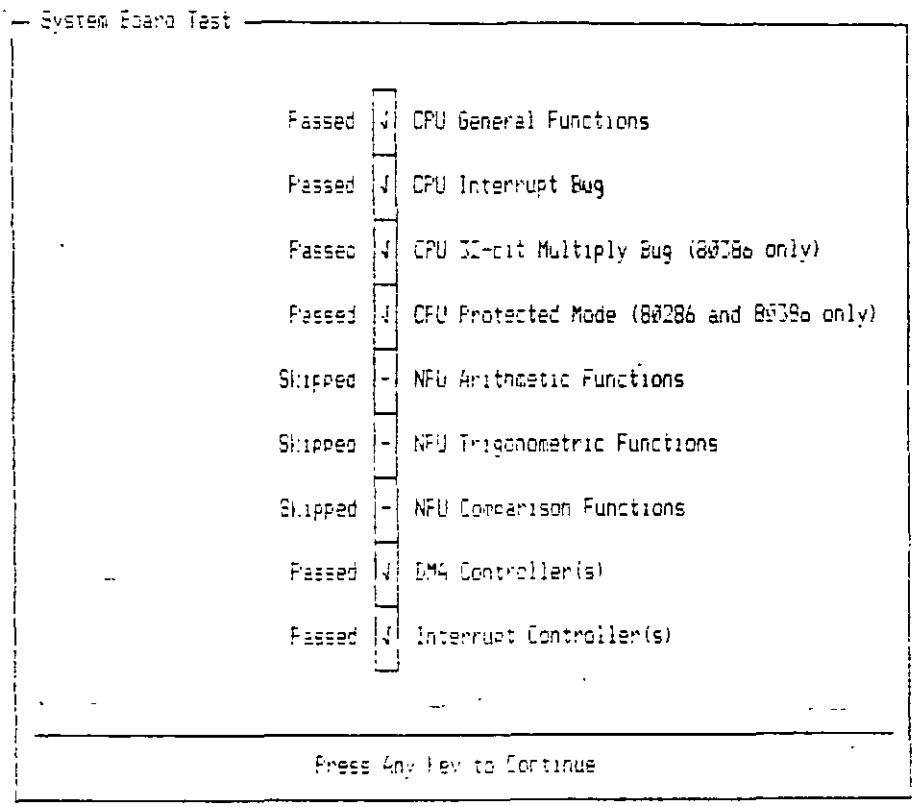
PROGRAMAS DE DIAGNOSTICO



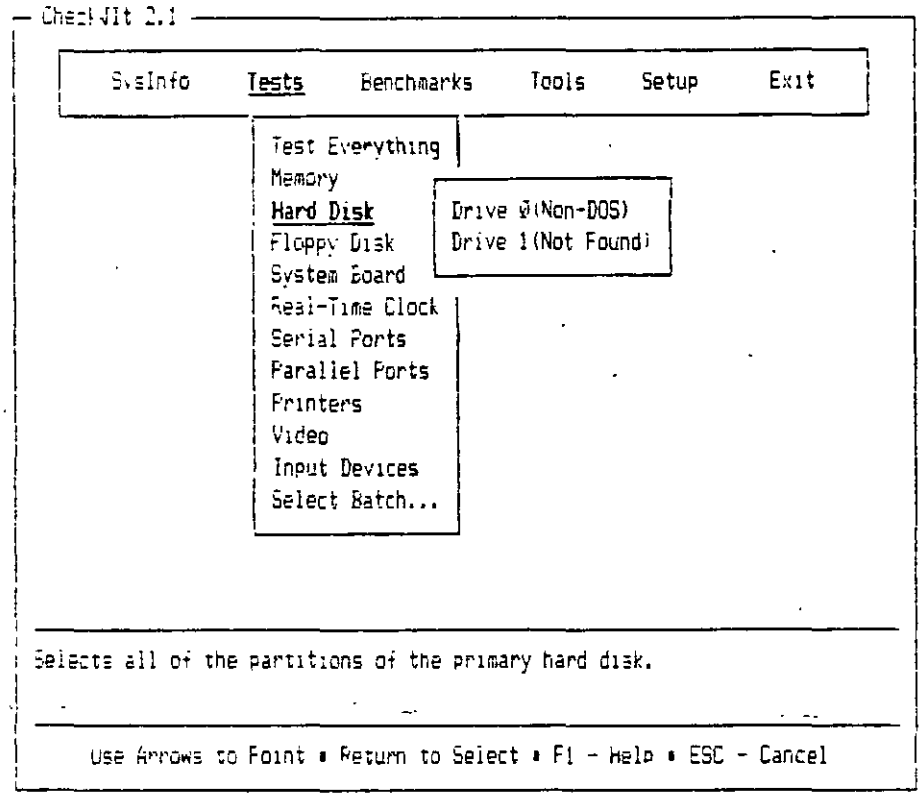


PROGRAMAS DE DIAGNOSTICO

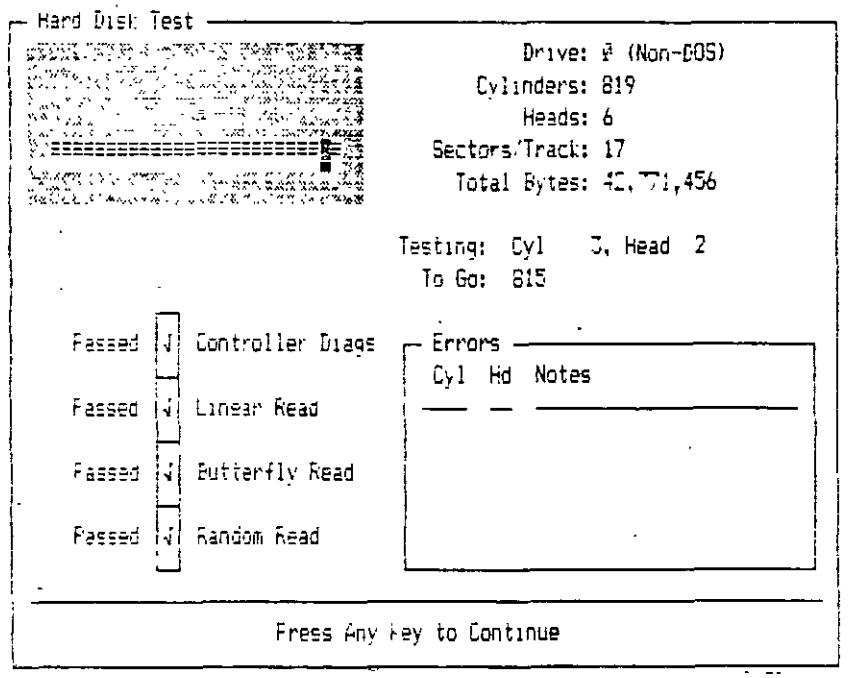




PROGRAMAS DE DIAGNOSTICO



PROGRAMAS DE DIAGNOSTICO



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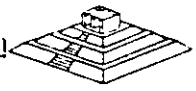
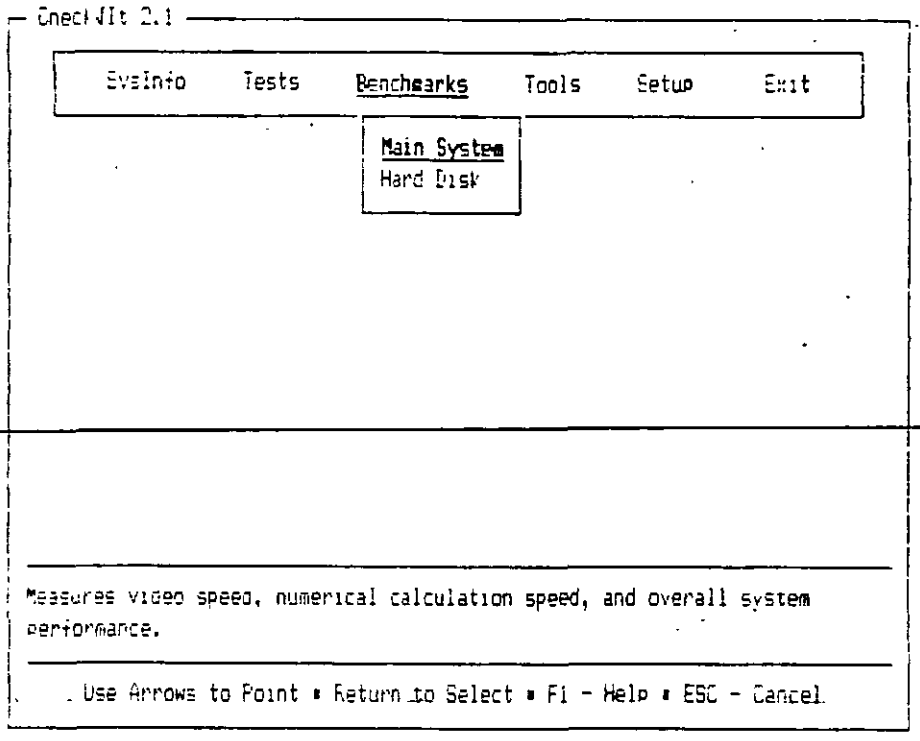
PROGRAMAS DE DIAGNOSTICO





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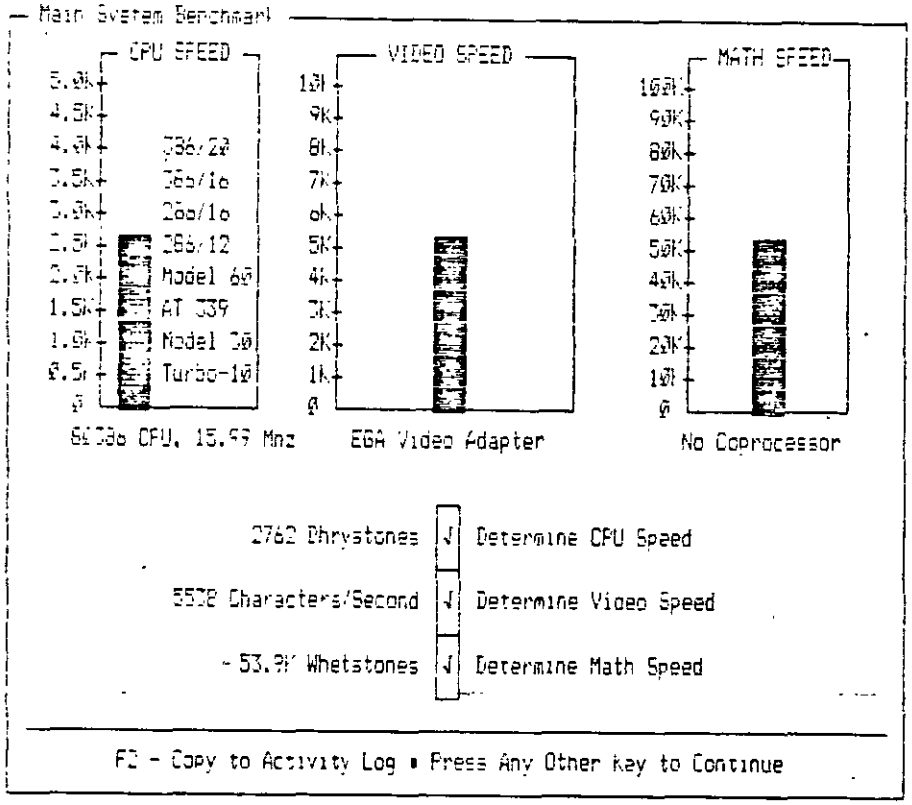
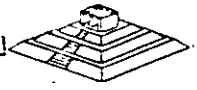
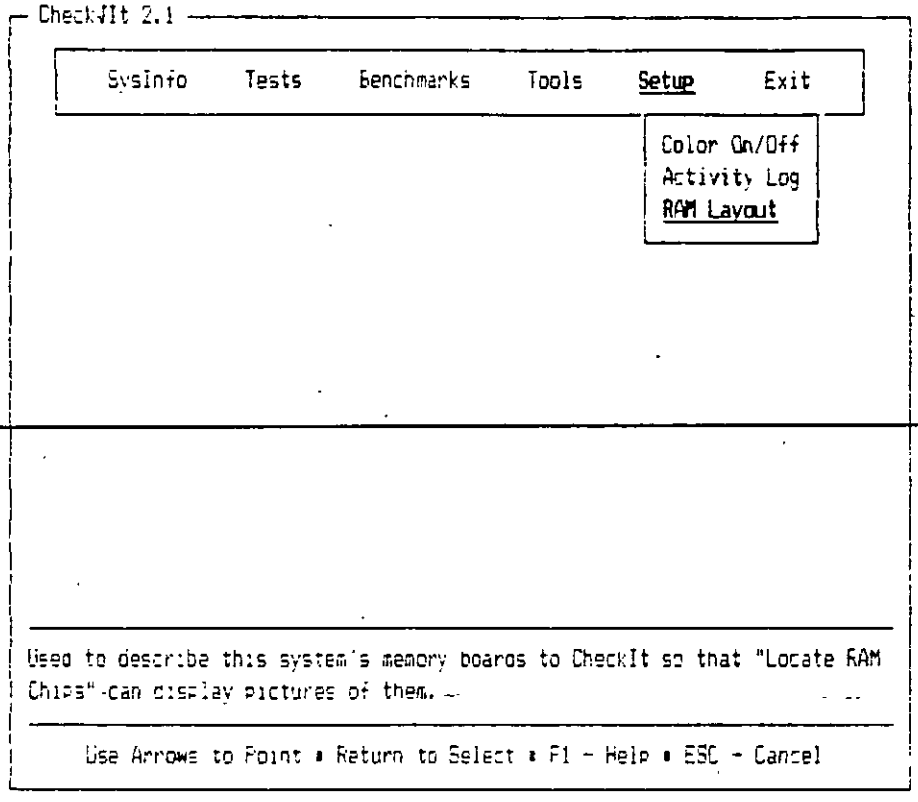
PROGRAMAS DE DIAGNOSTICO



PROGRAMAS DE DIAGNOSTICO





PROGRAMAS DE DIAGNOSTICO

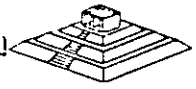
RAM Layout

Sample Board	32 Bits:	640K Base	(Address 000000h to 09FFFFh)
		384K Extended	(Address 100000h to 15FFFFh)
Slot 1	16 Bits:	2.000M Expanded	(Address 000000h to 1FFFFFh)
Slot 2	Undefined.		
Slot 3	Undefined.		
Slot 4	Undefined.		

Select Activity: C

V-View C-Change D-Delete -Select Board ESC-Cancel

PROGRAMAS DE DIAGNOSTICO



RAM Layout

Sample Board

Slot 1

Slot 2

Slot 3

Slot 4

Name: Sample Board Word Size: 32 Bits
Bank 0 on Top? Y Parity on Right? Y

RAM Chips:	Bank	Size	Bank	Size	Bank	Size	Bank	Size
	0	256K	4	None	8	None	12	None
	1	256K	5	None	9	None	13	None
	2	None	6	None	10	None	14	None
	3	None	7	None	11	None	15	None

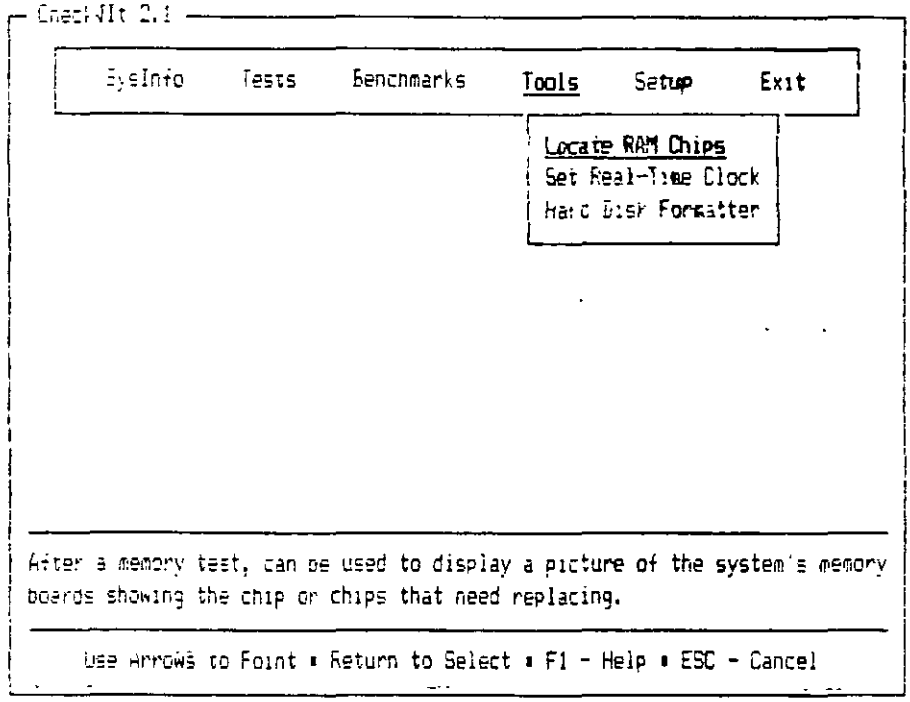
Base? Y	Amount:	640K	Start:	0K (00000h)
Extended? Y	Amount:	384K	Start:	1.000M (00100000h)
EXPANDed? N	Amount:		Start:	(h)

Total RAM on Board: 2.000M

Enter a name to identify the board you are modifying.

- Select Field • ESC - Cancel

PROGRAMAS DE DIAGNOSTICO



PROGRAMAS DE DIAGNOSTICO

Locate RAM Chips

Sample Board

Bank 0	0	1	2	3	4	5	6	7 => P	256K
	8	9	10	11	12	13	14	15 => P	256K
	16	=>17	18	19	20	=>21	22	23 => P	256K
	24	25	26	27	28	29	30	31 => P	256K

MORE

32 Bit Words

640K Base (Address 00000000h to 009FFFFFh)
384K Extended (Address 01000000h to 015FFFFFh)

This is the memory layout for the motherboard.

- View Board • F2 - Copy to Activity Log • ESC - Cancel

BIOS AMERICAN MEGATRENDS

CMOS SETUP (C) Copyright 1985-1989, American Megatrends Inc,.

Date (mn/date/year)	:	Wed, Mar 15 1989	Base memory size	:	640 KB		
Time (hour/min/sec)	:	13 : 29 : 34	Ext. memory size	:	384 KB		
Floppy drive A:	:	1.44 MB, 3 1/2"	Numeric processor	:	Not installed		
Floppy drive B:	:	1.2 MB, 5 1/4"					

	Cyln	Head	WPcom	LZone	Sec	Size
Hard disk C: type : 47 = USER TYPE	1224	16	1224	1224	36	330 MB
Hard disk D: type : 40	820	6	820	820	17	42MB

Primary display : VGA or EGA
Keyboard : Installed

Scratch RAM option : 1

Sun	Mon	Tue	Wed	Thu	Fri	Sat
26	27	28	1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	1
2	3	4	5	6	7	8

FIXED type = 01....46, USER defined type = 47
For type 47 Enter: Cyln,Head,WPcom,LZone,Sec,
(WPcom is 0 for ALL, 65535 for NONE)

ESC = Exit, ↓ ← ↑ → = Select, PgUp/PgDn = Modify

Use the ↓ ← ↑ → keys to highlight the parameters you want to change. Use the <PgUp> and <PgDn> keys to modify the values.

Date and Time

Use the ↓ ← ↑ → keys to select the parameters you want to change. Use the <PgUp> and <PgDn> keys to cycle through the available settings.

Floppy Disk Drives

Select the Floppy drive field. Press the <PgUp> and <PgDn> keys to cycle through the available settings. Available floppy disk drives are 5 1/4" (360KB, 1.2MB) and 3 1/2" (720KB, 1.44MB). If your system does not have a floppy drive B, be certain to specify "Not installed".

Primary Display

Select the Primary display field to establish the primary video display adapter type. Press the <PgUp> and <PgDn> keys to cycle through the available settings:

- Monochrome (Monochrome adapter, including MDA and Hercules)
- Color 40x25 (Color Graphics Adapter initialized in 40-column mode).
- EGA (Enhanced Graphics Adapter) or VGA (Video Graphic Array).
- Color 80x25 (Color Graphics Adapter initialized in 80-column mode).

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Hard Disk Drives

For hard disk drives, use the <PgUp> and <PgDn> keys to cycle through the 46 types of disk drives supported. Type 47 is given to help the user defined its own drive type which will be stored in the CMOS. See Table 3.2 for a printed list of these drive types.

Bypassing Keyboard Error

To configure the system for non dedicated file servers, you can set the keyboard "Not installed" in the SETUP menu so that BIOS will not report any "Keyboard error" and will not wait for "F1" key to be pressed during system boot.

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Bypassing Video Error

To configure the system for non dedicated file servers, you can set the video "Not installed" in the SETUP menu if you do not have a display connected. The BIOS will not report any "Video error" and will not wait for any "F1" key to be pressed during system boot.

Bypassing Floppy Error

To configure the system without floppy controller, you can set both the BIOS supported floppy drives (A and B) as "Not installed". In that case BIOS will not check for the floppy controller and will not report any error.

After you have finished with the SETUP program, press the <Esc> key. A prompt will then appear:

Write data into CMOS and exit (Y/N)

Type "Y" and press the <Enter> key. The computer performs a cold boot (equivalent to turning the power off and back again), followed by memory test, and then tries to boot from the disk drive. If your hard disk has not yet been initialized, be sure that you have a bootable DOS diskette.

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Table 3.2 Supported Hard Disk Drives

Type	Cylinders	Heads	Write Precomp	Landing Zone	Capacity
1	306	4	128	305	10MB
2	615	4	300	615	20MB
3	615	6	300	615	31MB
4	940	8	512	940	62MB
5	940	6	512	940	47MB
6	615	4	None	615	20MB
7	462	8	256	511	31MB
8	733	5	None	733	30MB
9	900	15	None	901	112MB
10	820	3	None	820	20MB
11	855	5	None	855	35MB
12	855	7	None	855	50MB
13	306	8	128	319	20MB
14	733	7	None	733	43MB
15	Reserved				
16	612	4	All	663	20MB
17	997	5	300	977	41MB
18	977	7	None	997	57MB
19	1024	7	512	1023	60MB
20	733	5	300	732	30MB
21	733	7	300	732	43MB
22	733	5	300	733	30MB
23	306	4	All	336	10MB
24	925	7	All	925	54MB
25	925	9	None	925	69MB
26	754	7	754	754	44MB
27	754	11	None	754	69MB
28	699	7	256	699	41MB
29	823	10	None	823	68MB
30	918	7	918	918	53MB
31	1024	11	None	1024	94MB
32	1024	15	None	1024	128MB

Continue on next page ...

Table 3.2 Supported Hard Disk Drives

Type	Cylinders	Heads	Write Precomp	Landing Zone	Capacity
33	1024	5	1024	1024	43MB
34	612	2	128	612	10MB
35	1024	9	None	1024	77MB
36	1024	8	512	1024	68MB
37	615	8	128	615	41MB
38	987	3	987	987	25MB
39	987	7	987	987	57MB
40	820	6	820	820	41MB
41	977	5	977	977	41MB
42	981	5	981	981	41MB
43	830	7	512	830	48MB
44	830	10	None	830	69MB
45	917	15	None	918	114MB
46	1224	15	None	1223	152MB

apuntes

BIOS AWARD

The SETUP program lets you specify your system's configuration of diskette drives, hard disk drives, video display, memory, date and time. The SETUP program is built-in, you do not need a diskette to use it.

Note

The following procedures assume your system has the Award 286 Modular BIOS installed. If your system has a different BIOS installed, these procedures will not work.

To run SETUP program, simultaneouly press the < Ctrl > < Alt > < Esc > keys. The SETUP screen appears on your display:

```
                    AWARD SOFTWARE CMOS SETUP

DATE (MM/DD/YY)      6/15/89
TIME (HH:MM:SS)      11:08:14

DISKETTE 1           1.2M
DISKETTE 2           360K
                          CYLS   HEADS   SECTORS   PRECOME
DISK 1               22   733    5       17        300
DISK 2NONE

VIDEO                EGA

BASE MEMORY          512
EXTENDED MEMORY      0

ERROR HALT           NO DISK ERROR HALT
SPEED SELECT         NO CHANGE

↓ ↑ moves between items, ← → selects values
F10 records changes, F1 exits, F2 for color toggle
```

apuntes

Table 3.3 Supported Hard Disk Drives

Type	Cylinders	Heads	Write Precomp	Landing Zone	Specific Disk
0	306	4	128	305	
1	615	4	300	615	Seagate 225
2	615	6	300	615	
3	940	8	512	940	
4	940	6	512	940	
5	615	4	0	615	
6	462	8	256	511	
7	733	5	0	733	Seagate 4038
8	900	15	0	901	
9	820	3	0	820	
10	855	5	0	855	
11	855	7	0	855	
12	855	7	0	855	
13	306	8	128	319	Seagate 225
14	733	7	0	733	
15	Reserved				
16	612	4	0	663	
17	997	5	300	997	
18	997	7	0	997	
19	1024	7	512	1023	
20	733	5	300	732	
21	733	7	300	732	
22	733	5	300	733	Seagate 4038
23	306	4	0	336	
24	Reserved				
25	1024	9	0	1023	Seagate 4096
26	1224	7	0	1223	Maxtor 2085
27	1224	11	0	1223	Maxtor 2140
28	1224	15	0	1223	Maxtor 2190
29	1024	8	0	1023	Maxtor 1085
30	1024	11	0	1023	Maxtor 1105
31	918	11	0	1023	Maxtor 1170

Continue on next page ...

Table 3.3 Supported Hard Disk Drives

Type	Cylinders	Heads	Write Precomp	Landing Zone	Specific Disk
32	925	9	0	926	CDC 9415
33	1024	10	0	1023	Generic 10hd
34	1024	12	0	1023	Generic 12hd
35	1024	13	0	1023	Generic 13hd
36	1024	14	0	1023	Generic 14hd
37	1024	2	0	1023	Generic 2hd
38	1024	16	0	1023	Generic 16hd
39	918	15	0	1023	Maxtor 1140
40	820	6	0	820	Seagate 251
41	1024	5	512	1024	Miniscribe 6053
42	988	5	128	988	Core Int'l AT 43
43	1024	5	124	1023	CMS-K40
44	1024	8	512	1024	Miniscribe 6085

Setting the Video Display Configuration

Select the VIDEO field to establish the primary video display adapter type. Press the ← → keys to cycle through the available settings:

- EGA (Enhanced Graphics Adapter).
- 40 Color (Color Graphics Adapter initialized in 40-column mode).
- 80 Color (Color Graphics Adapter initialized in 80-column mode).
- MONO (Monochrome adapter, including MDA and Hercules)

Select the settings that suits your display adapter.

Registros de Reloj

D.4 Real-Time CLock Information

(Addresses 00-0D)

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status register A	0A
11	Status register B	0B
12	Status register C	0C
13	Status register D	0D

apuntes

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

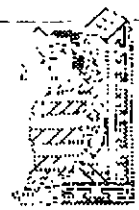
4.- MICROCONTROLADORES PRINCIPALES Y SISTEMAS MINIMOS

NOVIEMBRE - DICIEMBRE DE 1998

Palacio de Mineria Calle de Tacuba 5 Primer piso Deleg Cuauhtemoc 06000 México, D F APDO Postal M-2285
Telefonos 512-8955 512-5121 521-7335 521-1987 Fax 510-0573 521-4020 AL 26

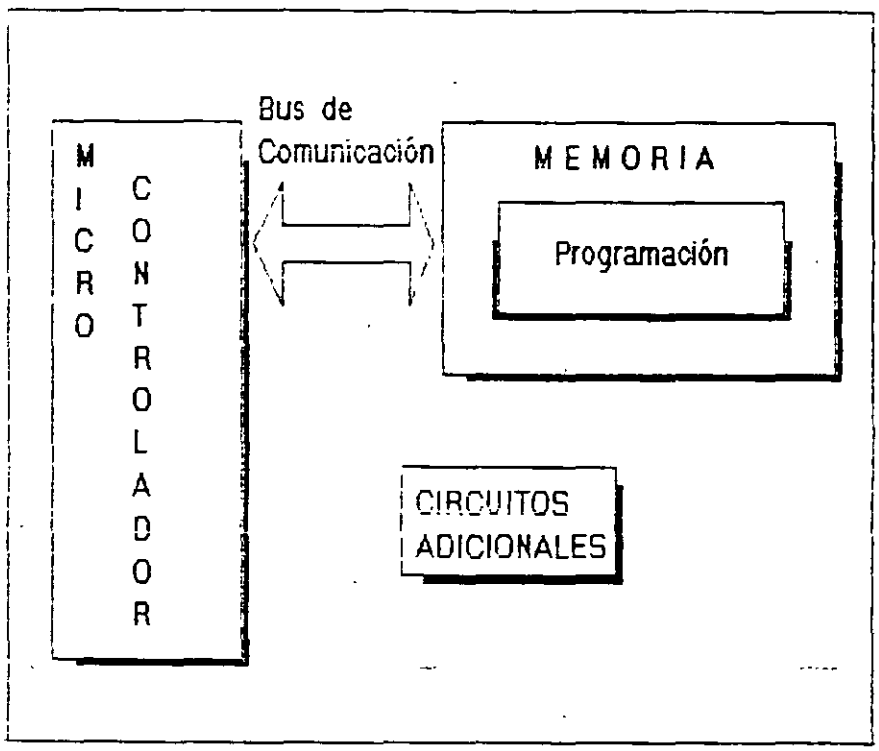
MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

4.- MICROCONTROLADORES PRINCIPALES Y SISTEMAS MINIMOS



NOVIEMBRE DE 1998

Sistemas Mínimos



apuntes

Microcontroladores Principales y Sistemas Mínimos

Generador de Reloj: *82284 - 82384 - 8284*
Controlador de DMA: *8257 - 8237*
Controlador de
Periféricos Programable: *8255*
Controlador de
Unidades de Disco: *82064 - 82062*
Controlador de Teclado: *8040 - 8248*
Controlador de
Interrupciones Programable: *8259*
Controlador de Puerto Serie: *8250*
Controlador Programable
de Interval Timer: *8253*

Pin Name	Description	Type
AD0-AD7	Address Data Bus	Bidirectional, tristate
A8-A15	Address Bus	Output, tristate
A16/S3, A17/S4	Address Segment identifier	Output, tristate
A18/S5	Address Interrupt enable status	Output, tristate
A19/S6	Address status	Output, tristate
$\overline{SSO}$	Status output	Output, tristate
$\overline{RD}$	Read control	Output, tristate
READY	Wait state request	Input
TEST	Wait for test control	Input
INTR	Interrupt request	Input
NMI	Non maskable interrupt request	Input
RESET	System Reset	Input
CLK	System Clock	Input
MN/$\overline{MX}$	= GND for a maximum system	
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	Machine cycle status	Output, tristate
$\overline{RQ}$/GT0, $\overline{RQ}$/GT1	Local bus priority control	Bidirectional
QS0, QS1	Instruction queue status	Output
$\overline{LOCK}$	Bus hold control	Output, tristate
MN/$\overline{MX}$	= V_{CC} for a minimum system	
IO/$\overline{M}$	Memory or I/O access	Output, tristate
$\overline{WR}$	Write control	Output, tristate
ALE	Address Latch enable	Output
DT/$\overline{R}$	Data transmit receive	Output, tristate
$\overline{DEN}$	Data enable	Output, tristate
$\overline{INTA}$	Interrupt acknowledge	Output, tristate
HOLD	Hold request	Input
HLDA	Hold acknowledge	Output
V_{CC}	+5V power supply	

Maximum System Signals

8088 Pin Out and Signal Assignments

Instruction		Object Code	Bytes	Clock Periods
CBW		98	1	2
CLC		F8	1	2
CLD		FC	1	2
CLI		FA	1	2
CMC		F5	1	2
CMP	ac data	0011110w kk [kl]	2 or 3	4
CMP	mem/reg data	100000sw mod 111 r/m [DISP] [DISP] kk [kl]	3, 4, 5 or 6	reg 4 mem 10 + EA
CMP	mem/reg$_1$,mem/reg$_2$	001110dw mod rr r/m [DISP] [DISP]	2, 3 or 4	reg to reg 3 mem to reg 9 + EA reg to mem 9 + EA
CMPS		1010011w	1	22 9 + 22/repetition*
CWD		99	1	5
DAA		27	1	4
DAS		2f	1	4
DEC	mem/reg	1111111w mod 001 r/m [DISP] [DISP]	2, 3 or 4	reg 3, mem 15 + EA
DEC	16 bit reg	01001rrr	1	2
DIV	mem/reg	1111011w mod 110 r/m [DISP] [DISP]	2, 3 or 4	8 bit reg 80 — 90 16 bit reg 144 — 162 8 bit mem (86 — 96) + EA 16 bit mem (150 — 168) + EA
ESC	mem/reg	11011xxx mod xxx r/m [DISP] [DISP]	2, 3 or 4	mem 8 + EA reg 2
HLT		F4	1	2
IDIV	mem/reg	1111011w mod 111 r/m [DISP] [DISP]	2, 3 or 4	8 bit reg 101 — 112 16 bit reg 165 — 184 8 bit mem (107 — 118) + EA 16 bit mem (171 — 190) + EA
IMUL	mem reg	1111011w mod 101 r/m [DISP] [DISP]	2, 3, or 4	8 bit reg 80 — 98 16 bit reg 128 — 154 8 bit mem (86 — 104) + EA 16 bit mem (134 — 160) + EA
IN	ac DX	1110110w	1	8
IN	ac port	1110010w	2	10

Instruction		Object Code	Bytes	Clock Periods
INC	mem/reg	1111111w mod 000 r/m [DISP] [DISP]	2, 3 or 4	reg 3 mem 15 + EA
INC	16 bit reg	01000rrr	1	2
INT		11001100* 11001101 type	1 2	52 51
INTO		CE	1	interrupt 53 no interrupt 4
IRET		CF	1	24
JA JNBE	disp disp	77 disp	2	4/No Branch 16/Branch
JAE JNB	disp disp	73 disp	2	4/No Branch 16/Branch
JB JNAE	disp disp	72 disp	2	4 No Branch 8 Branch
JBE JNA	disp disp	76 disp	2	4 No Branch 16 Branch
JCXZ	disp	E3 disp	2	6 No Branch 18 Branch
JE JZ	disp disp	74 disp	2	4 No Branch 16/Branch
JG JNLE	disp disp	7F disp	2	4 No Branch 16/Branch
JGE JNL	disp disp	7D disp	2	4/No Branch 16 Branch
JL JNGE	disp disp	7C disp	2	4 No Branch 16/Branch
JLE JNG	disp disp	7E disp	2	4 No Branch 16/Branch
JMP	addr	EA kk ii hh 00	5	15
JMP	disp	EB disp	2	15
JMP	disp16	E9 kk ii	3	15
JMP	mem	FF mod 101 r/m [DISP] [DISP]	2, 3 or 4	mem ptr 32 24 + EA
JMP	mem/reg	FF mod 100 r/m [DISP] [DISP]	2, 3 or 4	reg ptr 16 11 mem ptr 16 18 + EA
JNE JNZ	disp disp	75 disp	2	4/No Branch 16/Branch
JNO	disp	71 disp	2	4 No Branch 16/Branch
JNP JPO	disp disp	7B disp	2	4/No Branch 16/Branch
JNS	disp	79 disp	2	4 No Branch 16 Branch
JO	disp	70 disp	2	4 No Branch 16 Branch

* Implied type = 3

Instruction		Object Code	Bytes	Clock Periods
AAA		37	1	4
AAD		D5 0A	2	60
AAM		D4 0A	2	83
AAS		3F	1	4
ADC	ac data	0001010w kk [ll]	2 or 3	4
ADC	mem/reg$_1$,data	100000sw mod 010 r/m [DISP] [DISP] kk [ll]	3, 4, 5 or 6	reg 4 mem 17 + EA
ADC	mem/reg$_1$ mem/reg$_2$	000100dw mod rrr r/m [DISP] [DISP]	2, 3 or 4	reg to reg 3 mem to reg 9 + EA reg to mem 16 + EA
ADD	ac data	0000010w kk [ll]	2 or 3	4
ADD	mem/reg data	100000sw mod 000 r/m [DISP] [DISP] kk [ll]	3, 4, 5 or 6	reg 4 mem 17 + EA
ADD	mem/reg$_1$ mem/reg$_2$	000000dw mod rrr r/m [DISP] [DISP]	2, 3 or 4	reg to reg 3 mem to reg 9 + EA reg to mem 16 + EA
AND	ac data	0010010w kk [ll]	2 or 3	4
AND	mem/reg data	1000000w mod 100 r/m [DISP] [DISP] kk [ll]	3, 4, 5 or 6	reg 4 mem 17 + EA
AND	mem/reg$_1$,mem/reg$_2$	001000dw mod rrr r/m [DISP] [DISP]	2, 3 or 4	reg to reg 3 mem to reg 9 + EA reg to mem 16 + EA
CALL	addr	9A kk ll hh gg	5	28
CALL	disp16	E8 kk ll	3	19
CALL	mem	FF mod 011 r/m [DISP] [DISP]	2, 3 or 4	32 bit mem pointer 37 + EA
CALL	mem/reg	FF mod 010 r/m [DISP] [DISP]	2, 3 or 4	16 bit reg pointer 16 16 bit mem pointer 21 + EA

intel

82284
CLOCK GENERATOR AND READY INTERFACE FOR iAPX 286 PROCESSORS

(82284-10, 82284-8, 82284-6)

- Generates System Clock for iAPX 286 Processors
- Uses Crystal or TTL Signal for Frequency Source
- Provides Local READY and MULTIBUS®* READY Synchronization
- Available in 18-Lead Cerdip Package (See Packaging Spec, Order #231369)
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The 82284 is a clock generator/driver which provides clock signals for iAPX 286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

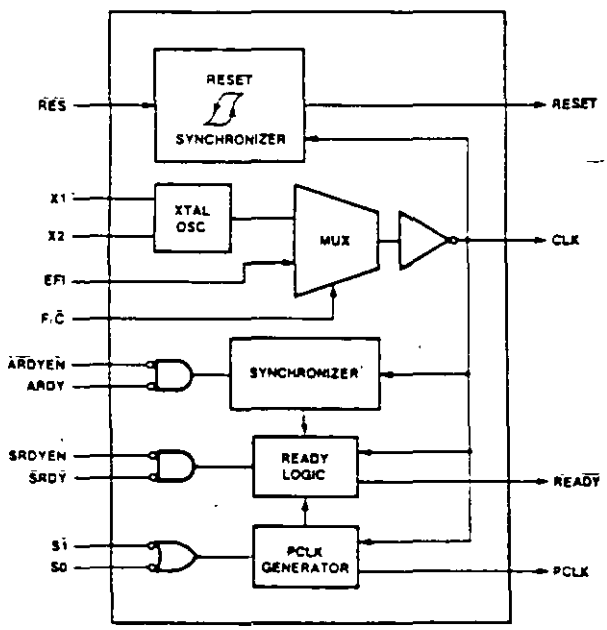


Figure 1. 82284 Block Diagram

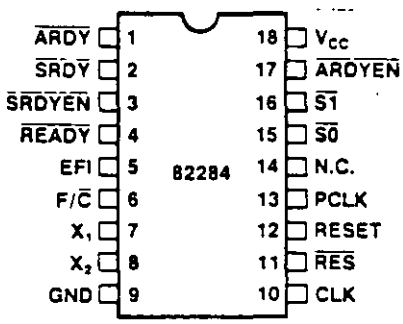


Figure 2.
82284 Pin Configuration

*MULTIBUS is a patented bus of Intel.

Intel Corporation Assumes no Responsibility for the Use of Any Circuitry Other Than Circuitry Embodied in an Intel Product. No Other Circuit Patent Licenses are Implied.

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GENERADOR DE RELOJ

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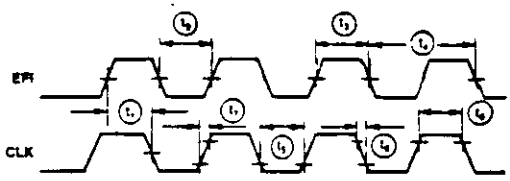
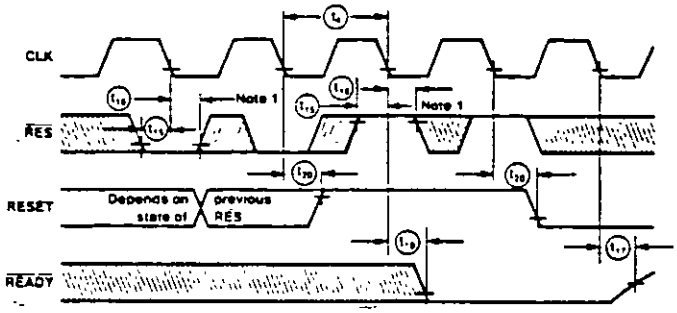
Waveforms

CLK as a Function of EFI (82284-6 only)



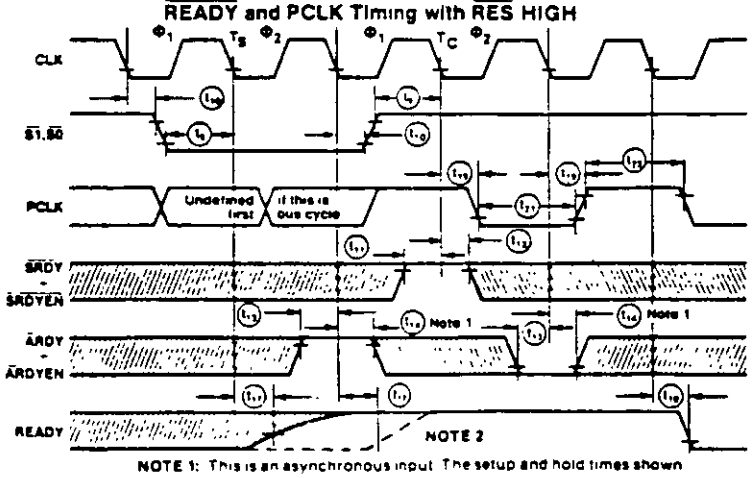
NOTE: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

RESET and READY Timing as a Function of RES with S1, S0, ARDY to ARDYEN, and SRDY + SRDYEN HIGH



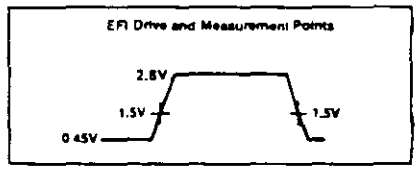
NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

READY and PCLK Timing with RES HIGH

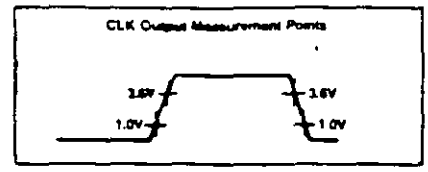


NOTE 1: This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
NOTE 2: If SRDY + SRDYEN or ARDY + ARDYEN are active before and/or during the first bus cycle after RESET READY may not be deasserted until after the falling edge of Φ2 of T_S

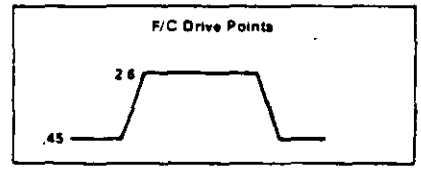
GENERADOR DE RELOJ



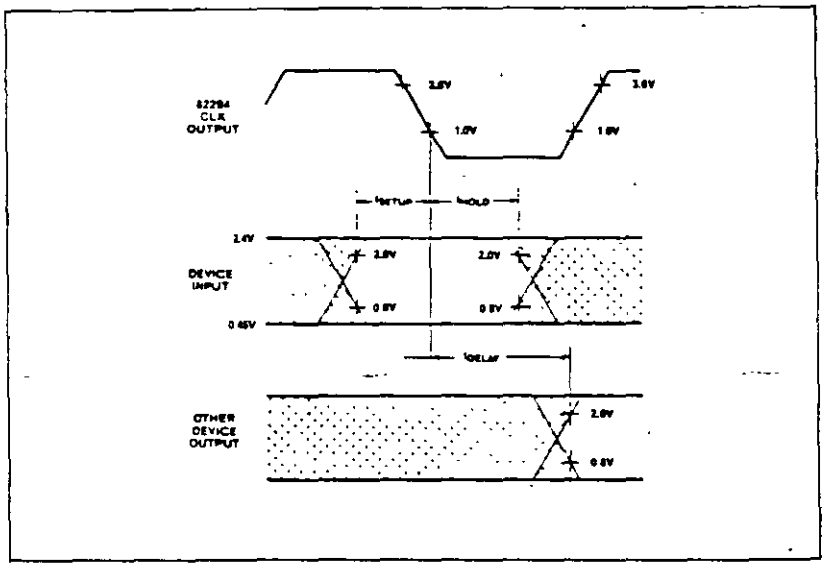
NOTE 9



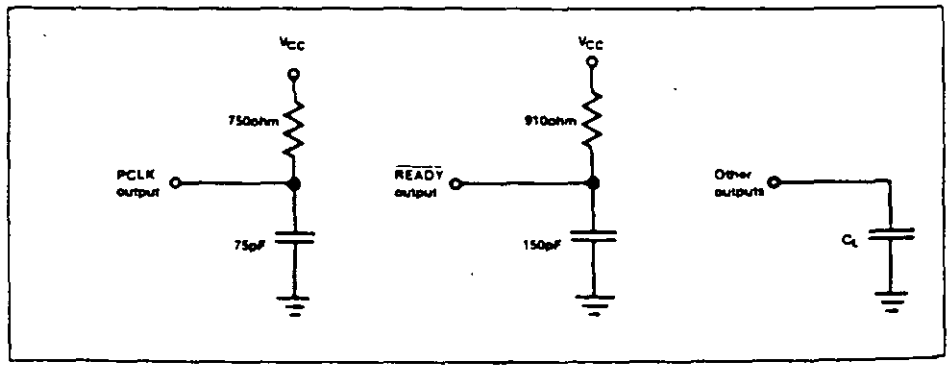
NOTE 10



NOTE 11



NOTE 12 AC Setup Hold and Delay Time Measurement—General



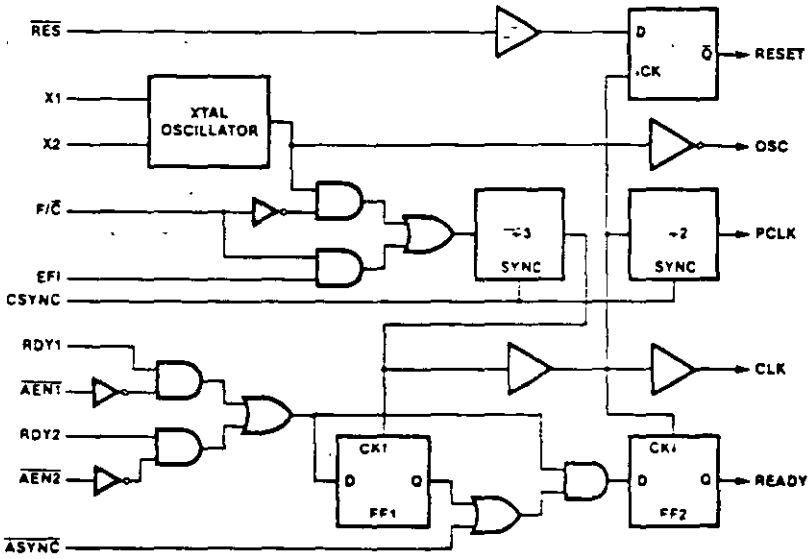
NOTE 13 AC Test Loading on Outputs

GENERADOR DE RELOJ

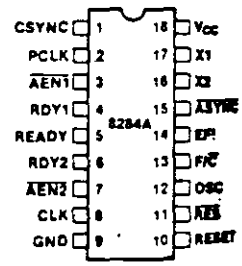
intel

8284A/8284A-1
CLOCK GENERATOR AND DRIVER FOR iAPX 86, 88 PROCESSORS

- Generates the System Clock for the iAPX 86, 88 Processors:
  5 MHz, 8 MHz with 8284A
  10 MHz with 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and MULTIBUS® READY Synchronization
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other 8284As
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range



8284A/8284A-1 Block Diagram



8284A/8284A-1 Pin Configuration

GENERADOR DE RELOJ

intel

8237A/8237A-4/8237A-5
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

- Enable/Disable Control of Individual DMA Requests
- Four Independent DMA Channels
- Independent Autoinitialization of all Channels
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- High performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Available in EXPRESS - Standard Temperature Range
- Available in 40-Lead Cerdip and Plastic Packages

(See Packaging Spec, Order #231369)

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 8237A is designed to be used in conjunction with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K address and word count capability.

The 8237A-4 and 8237A-5 are 4 MHz and 5 MHz selected versions of the standard 3 MHz 8237A respectively.

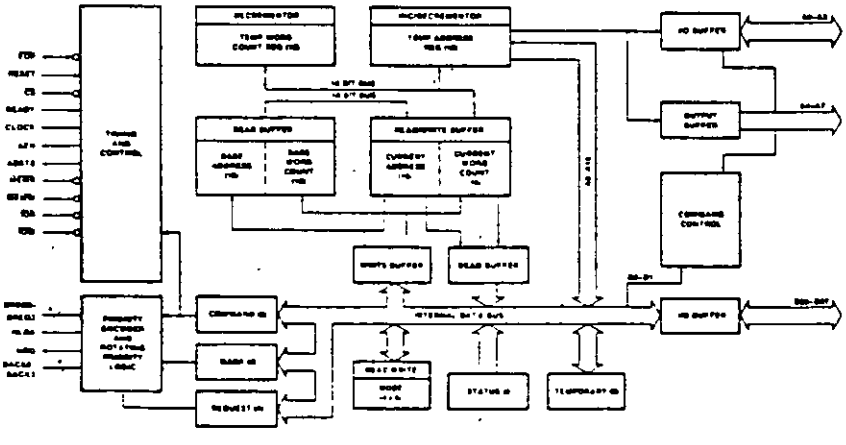


Figure 1. Block Diagram

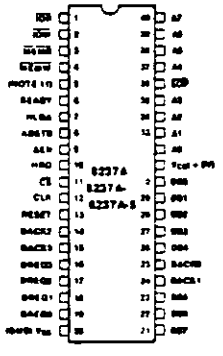


Figure 2. Pin Configuration

CONTROLADOR DE DMA

Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Ground.
CLK	I	**Clock Input:** Clock input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 3 MHz for the standard 8237A and up to 5 MHz for the 8237A-5
$\overline{CS}$	I	**Chip Select:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus
RESET	I	**Reset:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**Ready.** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time
HLDA	I	**Hold Acknowledge:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses
DREQ0-DREQ3	I	**DMA Request:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0-DB7	I/O	**Data Bus:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location
$\overline{IOR}$	I/O	**I/O Read:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer
$\overline{IOW}$	I/O	**I/O Write:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer
$\overline{EOP}$	I/O	**End of Process:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ Line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs
A0-A3	I/O	**Address:** ... four least significant address ... are bidirectional three-state ... s. In the Idle cycle they ... s and are used by the CP... dress the register ... read. In the Active cyc... outputs and provide ... 4 bits of the output ...

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
A4-A7	O	**Address:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**Hold Request:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.
DACK0-DACK3	O	**DMA Acknowledge:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**Address Enable:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**Address Strobe:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{MEMR}$	O	**Memory Read:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	O	**Memory Write:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The 8237A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 8237A contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 8237A Internal Registers

The 8237A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A. The Program Command Control block decodes the various commands given to the 8237A by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 8237A systems this input will usually be the ø2 TTL clock from an 8224 or CLK from an 8085AH or 8284A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 8237A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 8237A-5.

DMA Operation

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 and S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 8237A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half

and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 8237A will enter the Idle cycle and perform "SI" states. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the 8237A. When $\overline{CS}$ is low and HLDA is low, the 8237A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237A in the Program Condition. These commands are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-FLop and Master Clear.

ACTIVE CYCLE

When the 8237A is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed. In 8080A, 8085AH, 8088, or 8086 system this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 8237A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 8237A Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode—This mode is used to cascade more than one 8237A together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 8237A is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 8237A will respond to DREQ and DACK but all other outputs except HRQ will be disabled. The ready input is ignored.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 8237As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

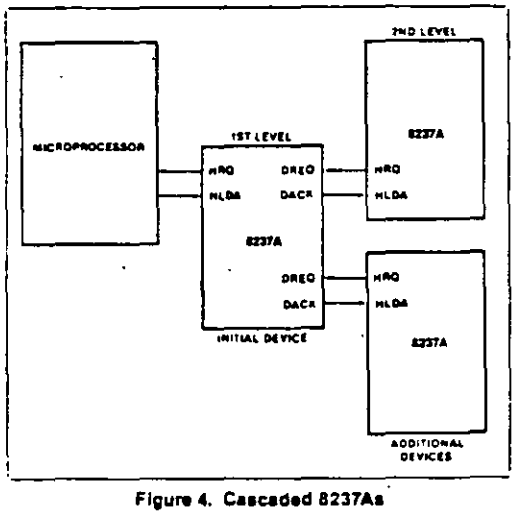


Figure 4. Cascaded 8237As

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from and I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers. The 8237A operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. The ready input is ignored in verify mode.

Memory-to-Memory—To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 8237A includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 to 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The 8237A requests a DMA service in the normal manner. After HLDA is true, the device, using four state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 8237A internal Temporary register. Channel 1 then performs a four-state transfer of the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service.

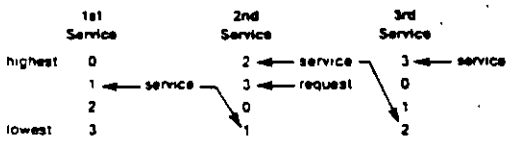
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 8237A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize—By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not altered when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected. In order to Autoninitialize both channels in a memory-to-memory transfer, both word counts should be programmed identically. If interrupted externally, $\overline{EOP}$ pulses should be applied in both bus cycles.

Priority—The 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the 8237A can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

Address Generation — In order to reduce pin count, the 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237A directly. Lines A0-A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register — Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Register — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

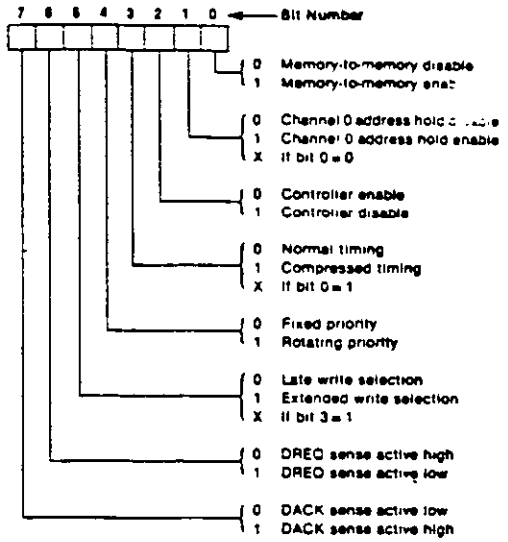
Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

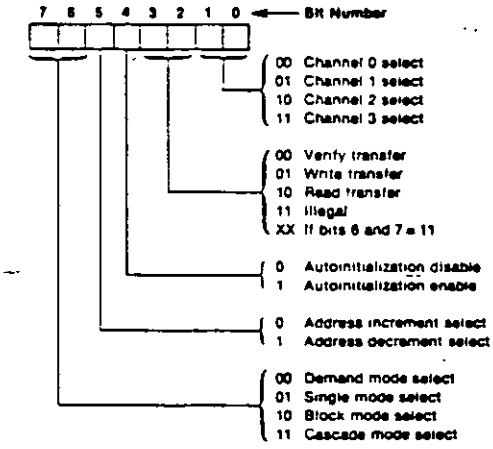
Mode Register — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register — The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.

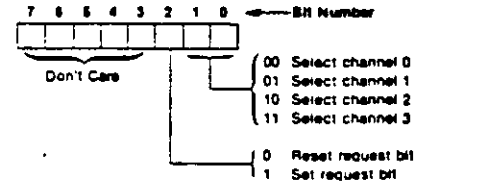
Command Register



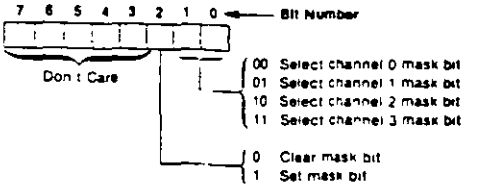
Mode Register



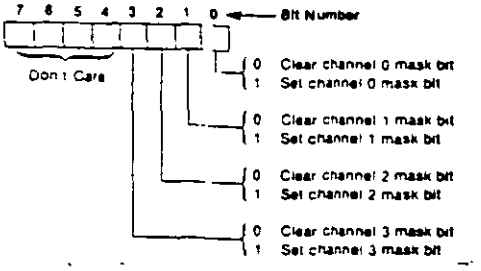
Request Register



Mask Register — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



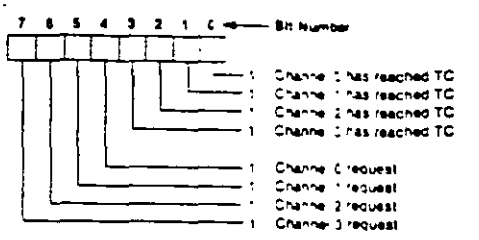
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

Status Register — The Status register is available to be read out of the 8237A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands — These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The three software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 8237A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip-Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

Figure 7. Word Count and Address Register Command Codes

PROGRAMMING

The 8237A will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 8237A is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 8237A is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

APPLICATION INFORMATION

Figure 8 shows a convenient method for configuring a DMA system with the 8237A controller and an 8080A/8085AH microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 8237A takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes — the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high speed, 8-bit, three-state latch in a 20-pin package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 8237A is used.

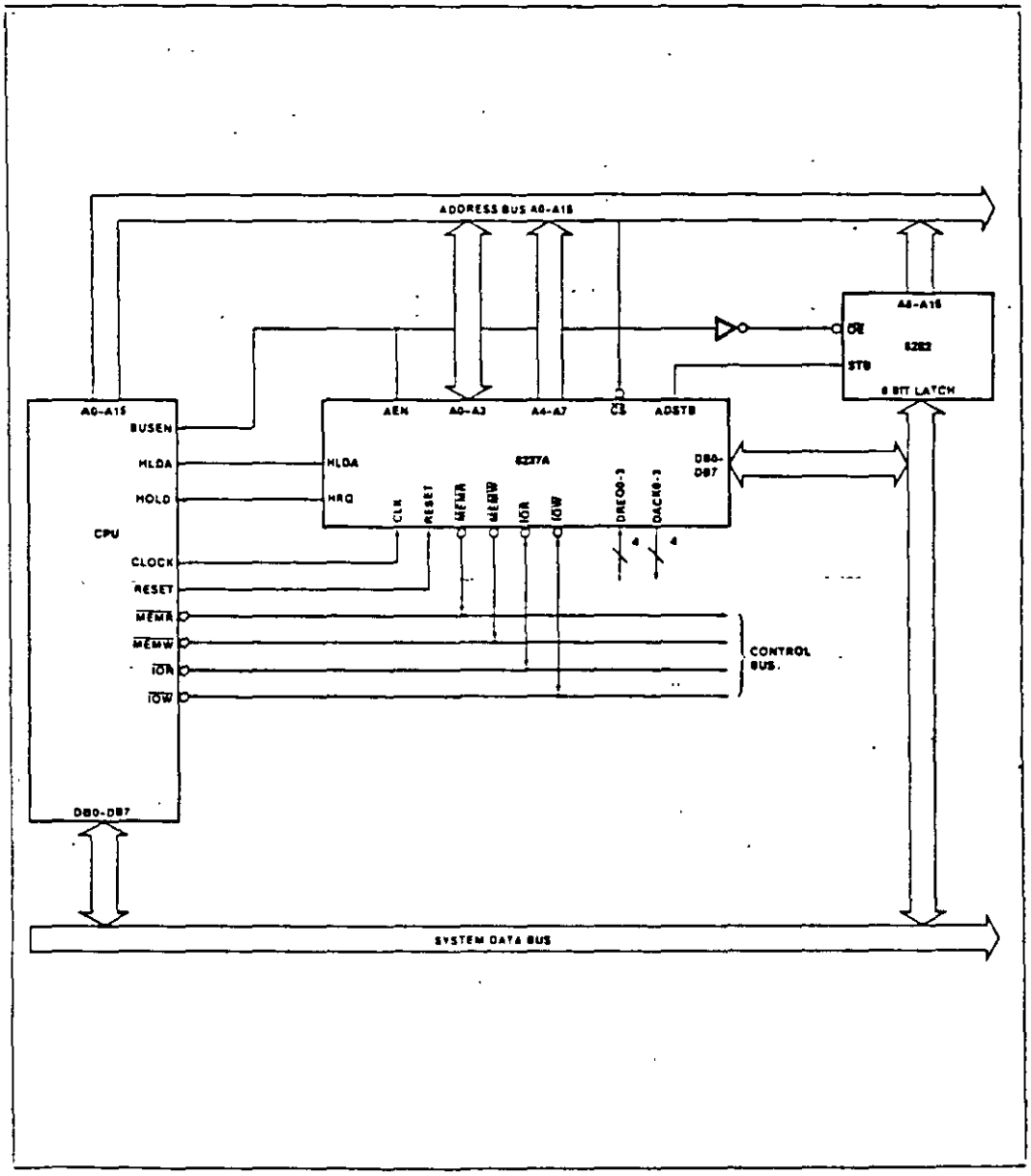


Figure 8. 8237A System Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −0.5 to 7V
Power Dissipation ..... 1.5 Watt

NOTICE. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

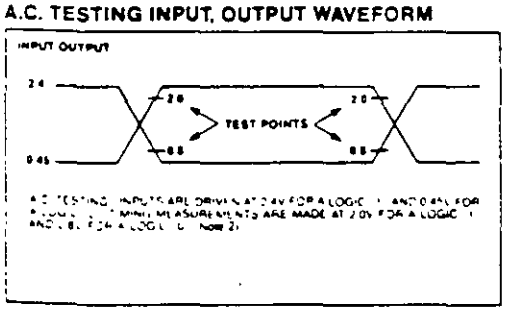
D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Symbol	Parameter	Min.	Typ (1)	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200 µA
		3.3			V	I_{OH} = -100 µA (HRQ Only)
V_{OL}	Output LOW Voltage			.40	V	I_{OL} = 2.0mA (data Bus, $\overline{EOP}$) I_{OL} = 3.2mA (other outputs) I_{OL} = 2.5mA (ADSTB) (Note 8)
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 0.5	V	(Note 8)
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
I_{LI}	Input Load Current			±10	µA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current			±10	µA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		110	130	mA	T_A = +25°C
			130	150	mA	T_A = 0°C
C_O	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0V
C_I	Input Capacitance		8	15	pF	
C_{IO}	I/O Capacitance		10	18	pF	

NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal process parameters.
2. Input timing parameters assume transition times to 20 ns or less. Waveform measurement points for both input and output signals are 2.0V for HIGH and 0.8V for LOW, unless otherwise noted.
3. Output loading is 1 TTL gate plus 150pF capacitance, unless otherwise noted.
4. The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3KΩ pull-up resistor connected from HRQ to V_{CC}.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. The values of V_{OL} and V_{IH} have been changed from the 1985 specification to allow more design margin.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the 8237A, at least 500 ns for the 8237A-4 and at least 400 ns for the 8237A-5 as recovery time between active read or write pulses. The same recovery time is needed between an active read or write pulse followed by a DMA transfer.
10. $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2K pullup to V_{CC}.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however that pin 5 be tied to V_{CC}.
12. Output Loading on the Data Bus is I_{OL}, Gate plus 100pF capacitance.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" (Note 2).

A.C. CHARACTERISTICS—DMA (MASTER) MODE (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, GND = 0V)

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAEL	AEN HIGH from CLK LOW (S1 Delay Time		300		225		200	ns
TAET	AEN LOW from CLK HIGH (S4 Delay Time		200		150		130	ns
TAFAB	AEN Active to Float Delay from CLK HIGH		150		120		90	ns
TAFC	AEN from READ or WRITE Float from CLK HIGH		150		120		120	ns
TAFDB	AEN Active to Float Delay from CLK HIGH		250		190		170	ns
TAHR	AEN from READ HIGH Hold Time	TCY–100		TCY–100		TCY–100		ns
TAHS	AEN from ADSTB LOW Hold Time	40		40		30		ns
TAHW	AEN from WRITE HIGH Hold Time	TCY–50		TCY–50		TCY–50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 7)		250		220		170	ns
	DRQ HIGH from CLK HIGH Delay Time (Note 10)		250		190		170	ns
	DRQ LOW from CLK HIGH Delay Time		250		190		170	ns
TASM	ADR Stable from CLK HIGH		250		190		170	ns
TASS	CS to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock High Time (Transitions < 10 ns)	120		100		80		ns
TCL	Clock LOW Time (Transitions < 10 ns)	150		110		68		ns
TCY	CLK Cycle Time	320		250		200		ns
TDCL	CLK HIGH to READ or WRITE LOW Delay (Note 4)		270		200		190	ns
TDCTR	READ HIGH from CLK HIGH (S4 Delay Time (Note 4)		270		210		190	ns
TDCTW	WRITE HIGH from CLK HIGH (S4 Delay Time (Note 4)		200		150		130	ns
TDQ1	DRQ Valid from CLK HIGH Delay Time (Note 5)		160		120		120	ns
TDQ2			250		190		120	ns
TEPS	EOP LOW from CLK LOW Setup Time	60		45		40		ns
TEPW	EOP Pulse Width	300		225		220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		190		170	ns
TFAC	READ or WRITE Active from CLK HIGH		200		150		150	ns
TFADB	ADR Float to Active Delay from CLK HIGH		300		225		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	100		75		75		ns
TIDH	Input Data from MEMR HIGH Hold Time	0		0		0		ns
TIDS	Input Data to MEMR HIGH Setup Time	250		190		170		ns
TODH	Output Data from MEMW HIGH Hold Time	20		20		10		ns
TODV	Output Data Valid to MEMW HIGH	200		125		125		ns
TQS	DREQ to CLK LOW (S1, S4 Setup Time (Note 7)	0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		60		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		150		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		110		90	ns

A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 12)		200		200		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	100	20	100	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{READ}$ Width	300		250		200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		160		ns

WAVEFORMS

SLAVE MODE WRITE TIMING

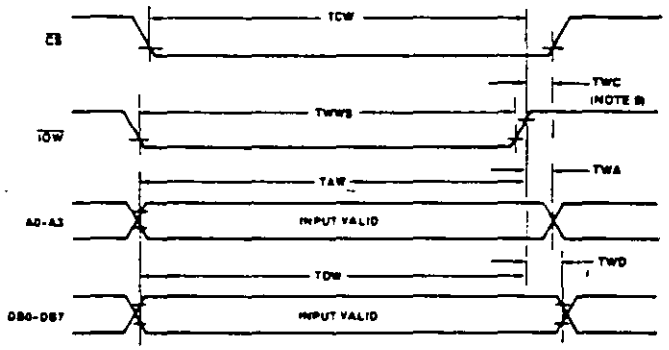


Figure 9. Slave Mode Write

SLAVE MODE READ TIMING

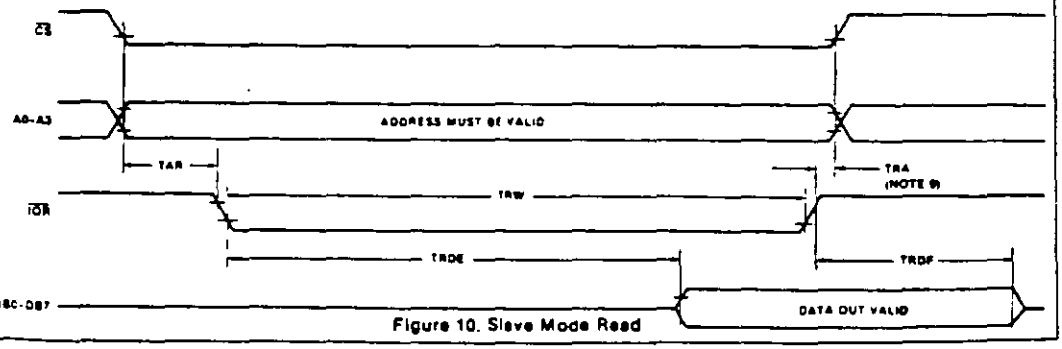


Figure 10. Slave Mode Read

WAVEFORMS (Continued)

DMA TRANSFER TIMING

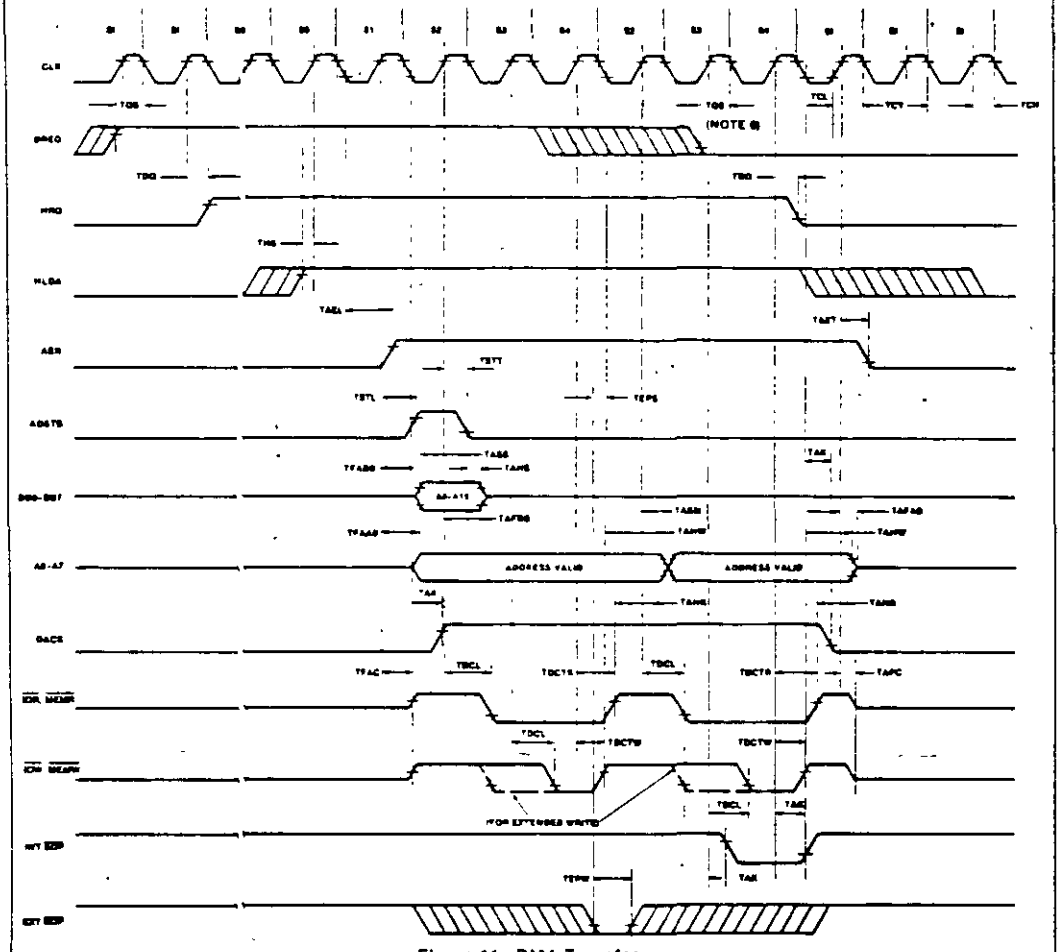


Figure 11. DMA Transfer

WAVEFORMS (Continued)

MEMORY-TO-MEMORY TRANSFER TIMING

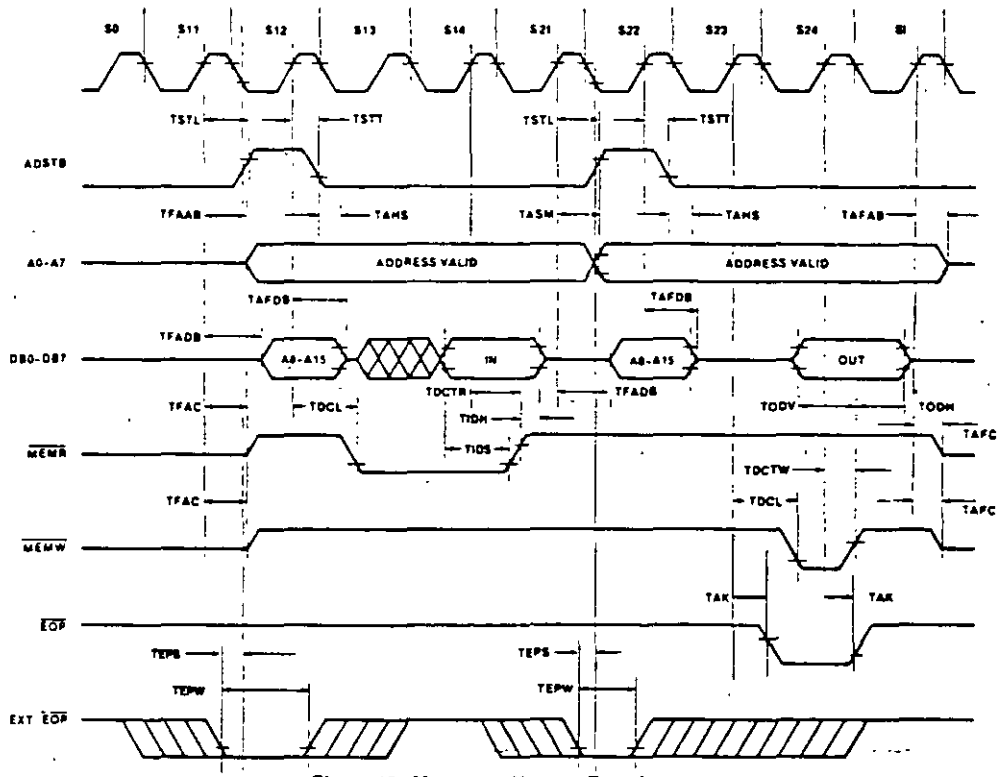


Figure 12. Memory-to-Memory Transfer

READY TIMING

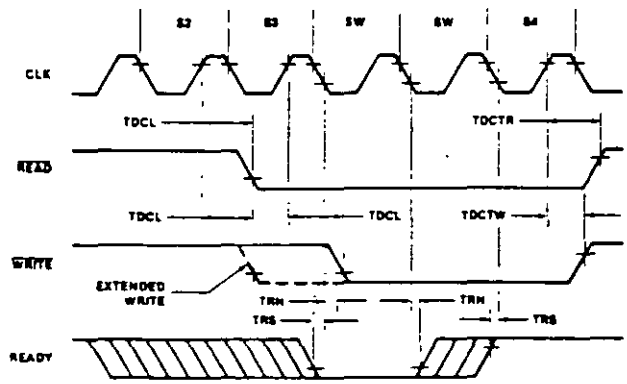


Figure 13. Ready

WAVEFORMS (Continued)

COMPRESSED TRANSFER TIMING

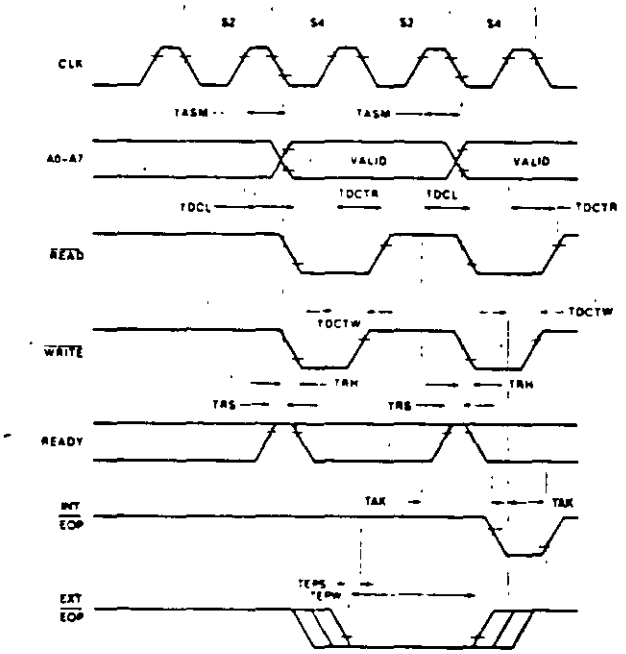


Figure 14. Compressed Transfer

RESET TIMING

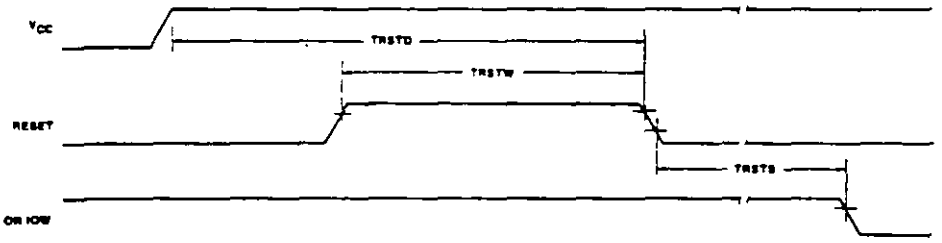


Figure 15. Reset

intel

8257/8257-5
PROGRAMMABLE DMA CONTROLLER

- MCS-85® Compatible 8257-5
- 4-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Single TTL Clock
- Single +5V Supply
- Auto Load Mode
- Available in EXPRESS
  - Standard Temperature Range
- Available in 40-Lead Cerdip and Plastic Package.

(See Packaging Spec, Order #231369)

The Intel® 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

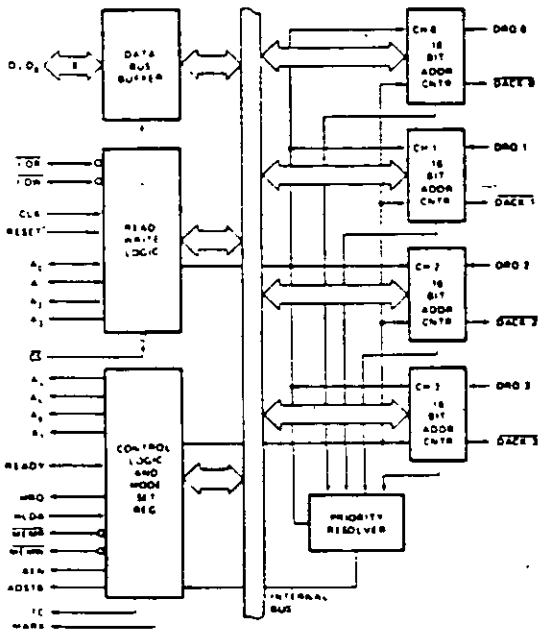


Figure 1. Block Diagram

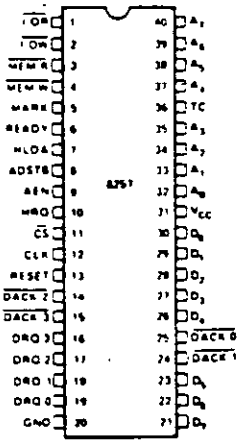


Figure 2. Pin Configuration

CONTROLADOR DE DMA

99

FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable Direct Memory Acess (DMA) device which, when coupled with a single 8-bit latch provides a complete four-channel DMA controller for use in Intel microcomputer systems. After being initialized by software the 8257 can transfer a block of data containing up to 16,384 bytes between memory and a peripheral device directly without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral the 8257:

1. Acquires control of the system bus
2. Acknowledges that requesting peripheral which is connected to the highest priority channel
3. Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8-bit latch via the data bus (the outputs of the latch should drive address lines A_8-A_{15}), and
4. Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence as long as a peripheral maintains its DMA request. Thus the 8257 can transfer a block of data to/from a high speed peripheral (e.g. a sector of data on a floppy disk) in a single burst. When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral. (2) DMA write, which causes data to be transferred from a peripheral to memory, and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and, (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel.

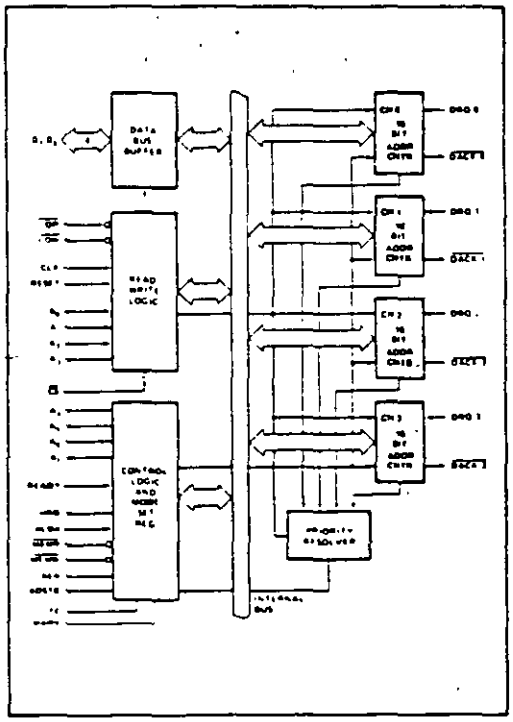


Figure 3. 8257 Block Diagram Showing DMA Channels

intel

8259A/8259A-2/8259A-8
PROGRAMMABLE INTERRUPT CONTROLLER

- iAPX 86, iAPX 88 Compatible
- MCS-80®, MCS-85® Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28-Pin Dual-In-Line Package
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS 80/85, Non-Buffered, Edge Triggered).

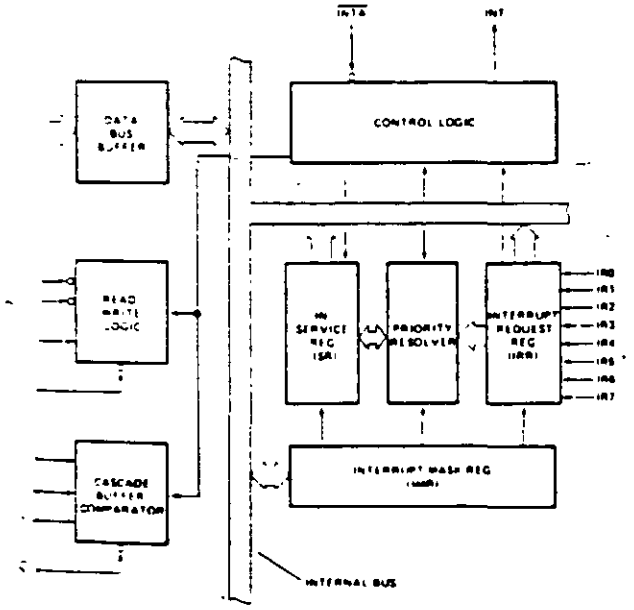


Figure 1. Block Diagram

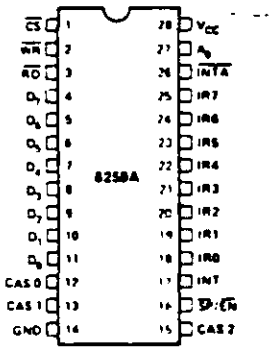


Figure 2. Pin Configuration

Intel Corporation Assumes No Responsibility for the use of Any Circuitry Other Than Circuitry Embodied in an Intel Product. No Other Circuit Patent Licenses are Implied.
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MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

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NOVIEMBRE - DICIEMBRE DE 1998

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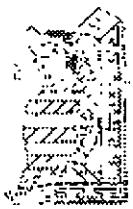
MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

5.- PERIFERICOS Y AJUSTES PRINCIPALES



NOVIEMBRE DE 1998

MONITOR DE VIDEO

La creciente evolución de las microcomputadoras hace que la necesidad de monitores de video de buena calidad haya experimentado también un crecimiento significativo. Teniendo esto en cuenta, presentamos en este artículo un proyecto de Philips específico para este área, con todos los consejos de montaje y ajustes.

Proyecto: ***Philips Components***
Texto: ***Ing. David M. Risnik***

El prototipo del monitor de video de alta resolución, probado por nosotros, funcionó en perfectas condiciones. Alertamos, sin embargo, que este montaje sólo está indicado para los técnicos experimentados en el tema del video.

Los problemas que pueden surgir en montajes de esta naturaleza se presentan bajo las más variadas formas y solamente quienes poseen las naturales vivencias en tal sector disponen de las habilidades necesarias para solucionarlos.

Los circuitos de alta tensión poseen un comportamiento típico de funcionamiento, y exigen conceptos prácticos para la solución de sus problemas.

Si bien por un lado consideramos que es un proyecto muy atractivo y satisfactorio para los que se dedican a este tema, creemos oportuno hacer esta aclaración para evitar trastornos a los lectores que no tengan la necesaria experiencia en el área. Recomendamos a todos, por otra parte, la lectura del artículo, que es muy didáctico.

El monitor de video puede considerarse el periférico de mayor importancia en una microcomputadora, y muchas veces se le confunde como parte integrante de la misma. Vamos entonces, antes de presentar su circuito, a definir rápidamente sus características de funcionamiento.

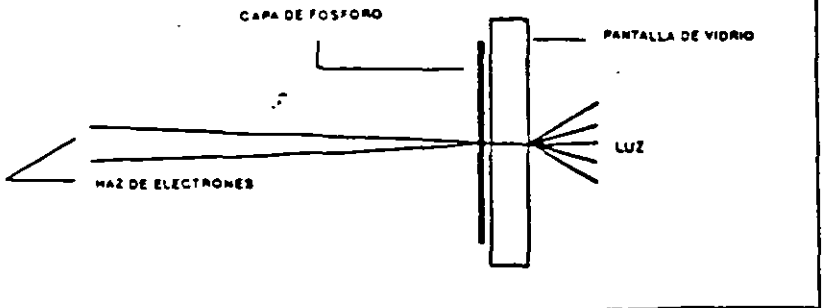
Toda información a ser intercambiada entre el usuario y la micro debe estar dispuesta en la forma "inteligible" por el hombre, ya sea en forma de caracteres, símbolos o figuras (gráficos). Para satisfacer esta condición las señales digitales generadas por la microcomputadora son adaptadas para estimular determinados periféricos que trasladan esta información al hombre, en formas que él reconozca. Las impresoras y las terminales de video constituyen ejemplos típicos. En el caso de las impresoras, la información digital, creada especialmente para esta finalidad, se aplica a una cabeza de agujas que disparan sobre una cinta con tinta imprimiendo en el papel las letras, símbolos y dibujos.

En los terminales de video, se desarrolla un proceso bastante semejante, pero con la ventaja de que no existen piezas mecánicas móviles (sujetas a desgaste) ni cintas con tinta, ni papel. Todo el proceso de impresión es electrónico: el papel es sustituido por la pantalla de un cinescopio, y el elemento "tinta", por la luz emitida resultante de la colisión entre el haz electrónico y la capa de fósforo que reviste internamente la cara plana de la pantalla (figura 1).

Los caracteres o gráficos creados digitalmente por la microcomputadora son transformados en una forma de señal (señal de video), que va a "modular" el haz electrónico en constante barrido por la pantalla del cinescopio, informando cuales son los puntos que deben ser iluminados (encendidos) o no.

¡Pero muchos de ustedes es-

1



tarán preguntando si éste no es exactamente el proceso ejecutado por la televisión! Si, claro que si, con algunas diferencias que tienen como fin una mejor eficiencia. Veamos cuáles son estas pequeñas diferencias.

Las señales de video provistas por la computadora poseen características esencialmente digitales, o sea son solamente dos niveles para determinar el brillo de la pantalla:

- CERO (apagado = ausencia de brillo)
- UNO (encendido = brillo máximo)

En oposición a las señales analógicas que admiten infinitas tonalidades de gris, entre el brillo máximo y el negro (figura 2).

Una segunda diferencia importante reside en lo que definimos como "resolución". Vea que, a pesar de que una imagen de televisión nos parece continua, está en realidad constituida por una secuencia de puntos, unos al lado de otros, en la formación de una línea de video la imagen es formada por la sucesión de líneas de video. Cuanto mayor sea el número de puntos que forman una línea de video, tanto mayor será la "resolución" de esta imagen, o sea, la misma se vuelve más nítida.

En televisión, la resolución, o número de puntos de una línea de video, sufre limitaciones por el propio sistema de transmisión de esas imágenes (transmisión por radio frecuencia o RF), que limita la máxima frecuencia de video que se puede transmitir, dentro del sistema definido para un canal de televisión (figura 3).

¡En las microcomputadoras, esta limitación deja de existir, con lo que se pueden lograr definiciones bastante mayores! Una primera ventaja derivada de este hecho, es que podemos colocar en una línea de video un número mayor de caracteres (típico = 80 caracteres o más).

Una microcomputadora puede incluir una etapa moduladora de RF en su salida de video para permitir que esta señal alimente la entrada de antena de un receptor de TV convencional, y así operar como un terminal de video, naturalmente que con restricciones. En primer lugar, derivado solamente del proceso de esta modulación, agregamos a la señal de video una buena dosis innecesaria de ruido. Otro factor perjudicial en estos casos son los problemas derivados del proceso de sintonía de la señal, que pueden muchas veces perturbar y desestabilizar la imagen (interferencias por choques de señales). Y por último, la limitada resolución del receptor de TV, más el tratamiento analógico (etapa de salida de video) de una señal digital (de la microcomputadora), contribuyen a volver la imagen "nebulosa", con poca definición tanto para el texto como para los gráficos (figura 4).

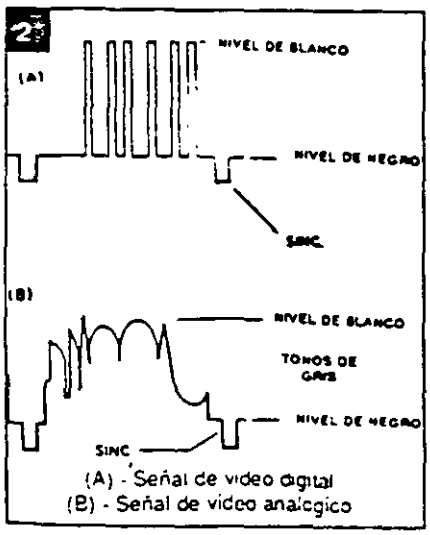
Por todos estos factores, el uso de un monitor de video, diseñado especialmente para el tratamiento de señales digitales, es indiscutiblemente ventajoso para todos los sistemas de microcomputadoras.

Requisitos de un monitor de alta resolución

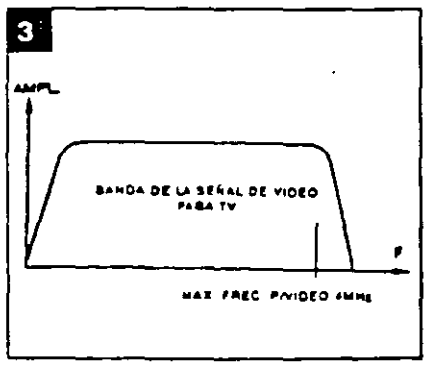
¡Si intentamos reproducir una señal de audio de alta fidelidad (HI-FI) en un equipo de audio de bajos recursos, es evidente que no obtendremos una reproducción de alta fidelidad! Un sistema de audio de alta fidelidad debe ser constituido por amplificadores de buena calidad (respuesta en frecuencia) y "también" por cajas acústicas de buen desempeño.

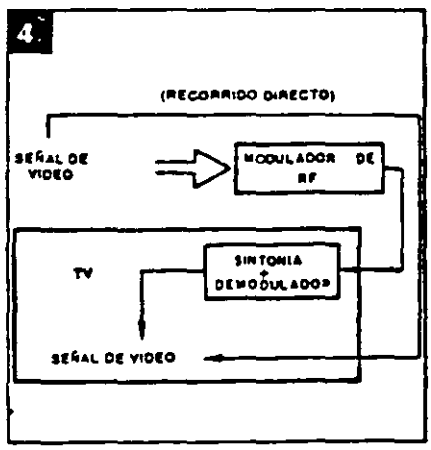
Algo análogo exige el video. La señal de video de alta resolución proporcionada por la microcomputadora, solamente será reproducida a la perfección en un equipo de alta resolución, que incluya circuitos de buena calidad (respuesta en frecuencia y "también" cinescopio con capacidad para reproducciones de alta resolución).

Resaltamos por lo tanto que todos los integrantes de un sistema de alta resolución deben tener calificaciones compatibles de calidad.



(A) - Señal de video digital
(B) - Señal de video analógico





El cinescopio

Un elemento de mucha importancia en el sistema de reproducción de video es sin duda alguna el "cinescopio" o tubo de rayos catódicos, ya que tiene la responsabilidad final de dar una buena imagen. Esta responsabilidad es todavía mayor cuando exigimos una resolución por encima del término medio aceptado en televisión. Vamos a analizar entonces cuáles son los pre-requisitos para obtener una buena resolución en la pantalla del cinescopio.

Como ya mencionamos, una imagen se forma mediante el agrupamiento de puntos en secuencia. A cada uno de estos puntos podemos llamarlo un "elemento de imagen". Por consiguiente, sabemos que cuanto mayor sea el número de elementos de imagen, mayor será la resolución de esta imagen.

En el trazado de una línea de video, los diversos elementos de imagen son yustapuestos uno a continuación del otro. Por deducción lógica, es fácil percibir que para una misma dimensión del cinescoio (ancho de la pantalla), cuanto más elementos de imagen quisiéramos colocar, tanto menores deberán ser los mismos.

El tamaño de un elemento de imagen es definido por el contorno de la emisión de luz que se forma en la posición de la colisión del haz electrónico con la pantalla. Este contorno puede ser considerado aproximadamente como un pequeño círculo. El tamaño de este círculo va a estar en proporción directa con el grosor del haz al chocar con la pantalla. Cuanto mayor fuera el grosor, mayor será el círculo, mayor será el elemento de imagen y por lo tanto se podrá distinguir un menor número de elementos de imagen en una línea de video. En esta condición, si intentamos colocar un número mayor de puntos, los mismos inevitablemente se superpondrán unos con otros, ¡produciendo no más puntos definidos, sino borrones! Ahí está la causa de la baja resolución (figura 5).

El control del grosor del haz electrónico al incidir sobre la pantalla del cinescopio está bajo la supervisión de la llamada "lente electrónica" en el cañón del cinescopio. Esta lente es responsable por el enfoque del haz sobre la superficie de la pantalla, muy semejante al enfoque de un haz de luz sobre una pared.

Cuanto mayor sea este enfoque más concentrado será el haz de electrones al chocar con la pantalla, y por lo tanto menor será el "punto" impreso.

Las lentes electrónicas en el interior del cañón del cinescopio están formadas por campos electrostáticos en una configuración tal que obligan a los electrones a converger al interior del haz. La correcta focalización del haz sobre la pantalla es obtenida por el ajuste de la tensión de alimentación de la rejilla de enfoque del cinescopio.

Los cinescopios de alta resolución poseen la configuración de esta lente electrónica de un modo especialmente diseñado, y exigen tensiones de polarización (de foco) bastante mayores (fig. 6).

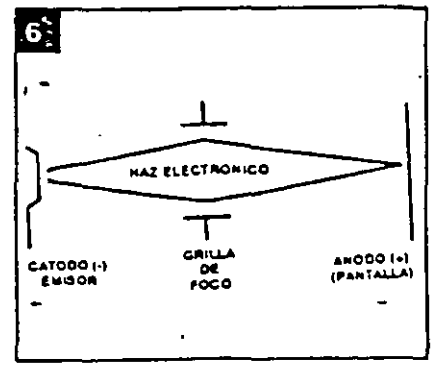
Enfoque uniforme

Muy bien, obtenido un buen enfoque del haz electrónico sobre la pantalla, ¿nuestro monitor de video de alta resolución ya está delineado...? ¡Desgraciadamente todavía no! Falta solucionar un problemita relativo al enfoque: su uniformidad.

En virtud de la escasa curvatura de la pantalla, y de la pequeña distancia entre el centro de deflexión (posición del yugo) y la pantalla, el haz recorre una distancia diferente en función de su posición sobre la pantalla. En otras palabras, para alcanzar los bordes (cantos), el mismo debe recorrer una distancia mayor que la que recorre para alcanzar el centro de la pantalla. Esta distancia es bastante significativa en los cinescopios modernos, de gran ángulo de abertura (110 grados) (figura 7).

Los que trabajan con fotografía saben que el correcto enfoque de un objeto a 2 metros es diferente del correcto enfoque de otro objeto a 5 metros. El mismo problema se puede trasladar al cinescopio:

6



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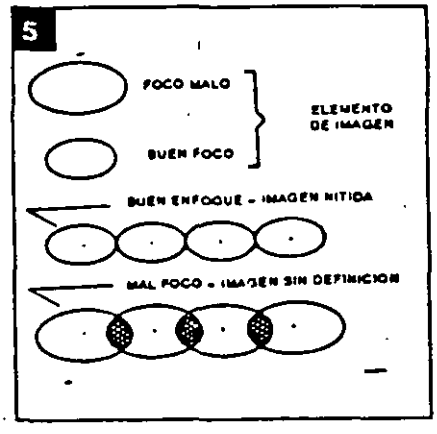

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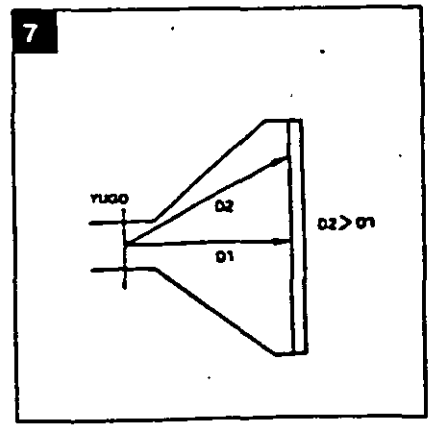

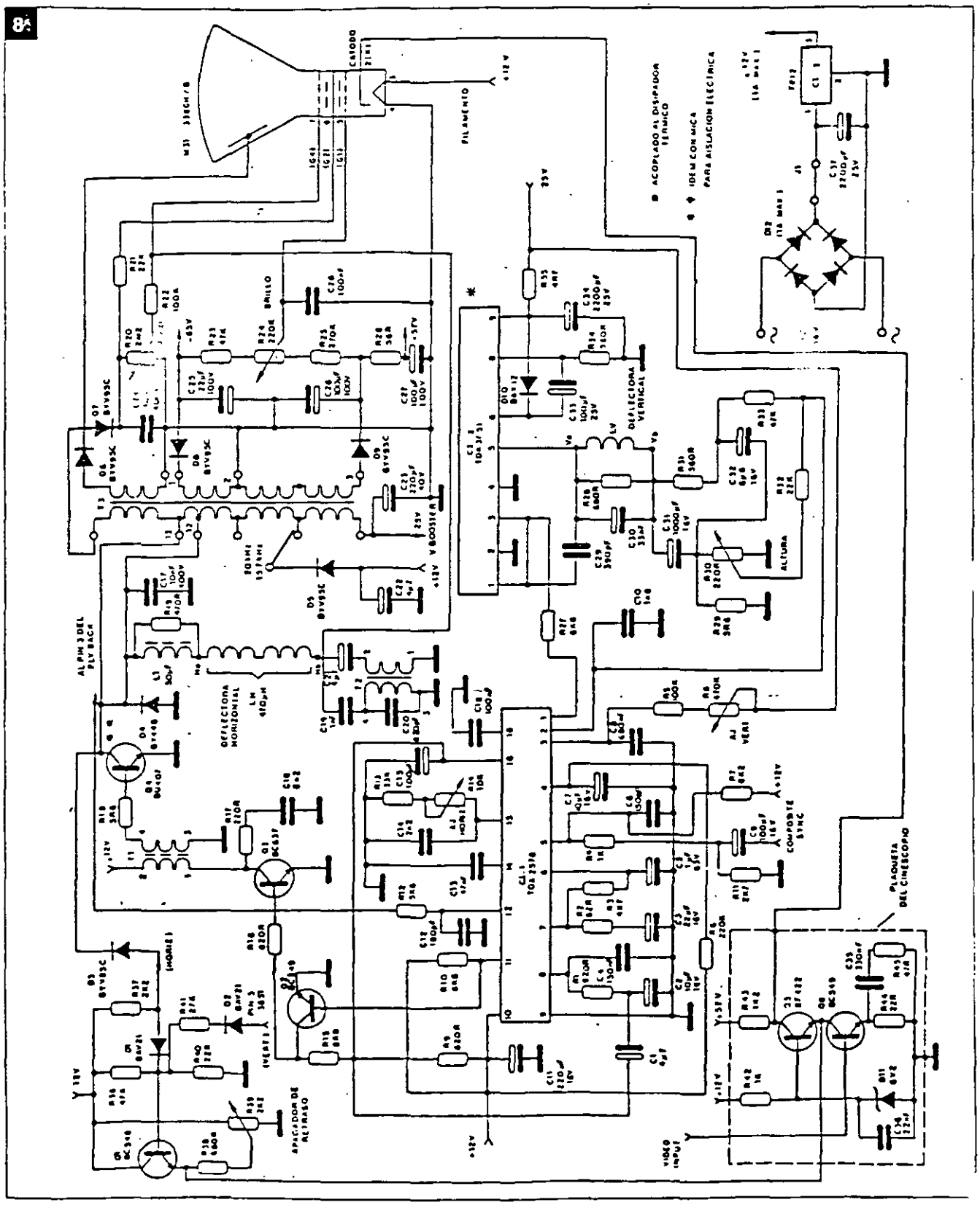

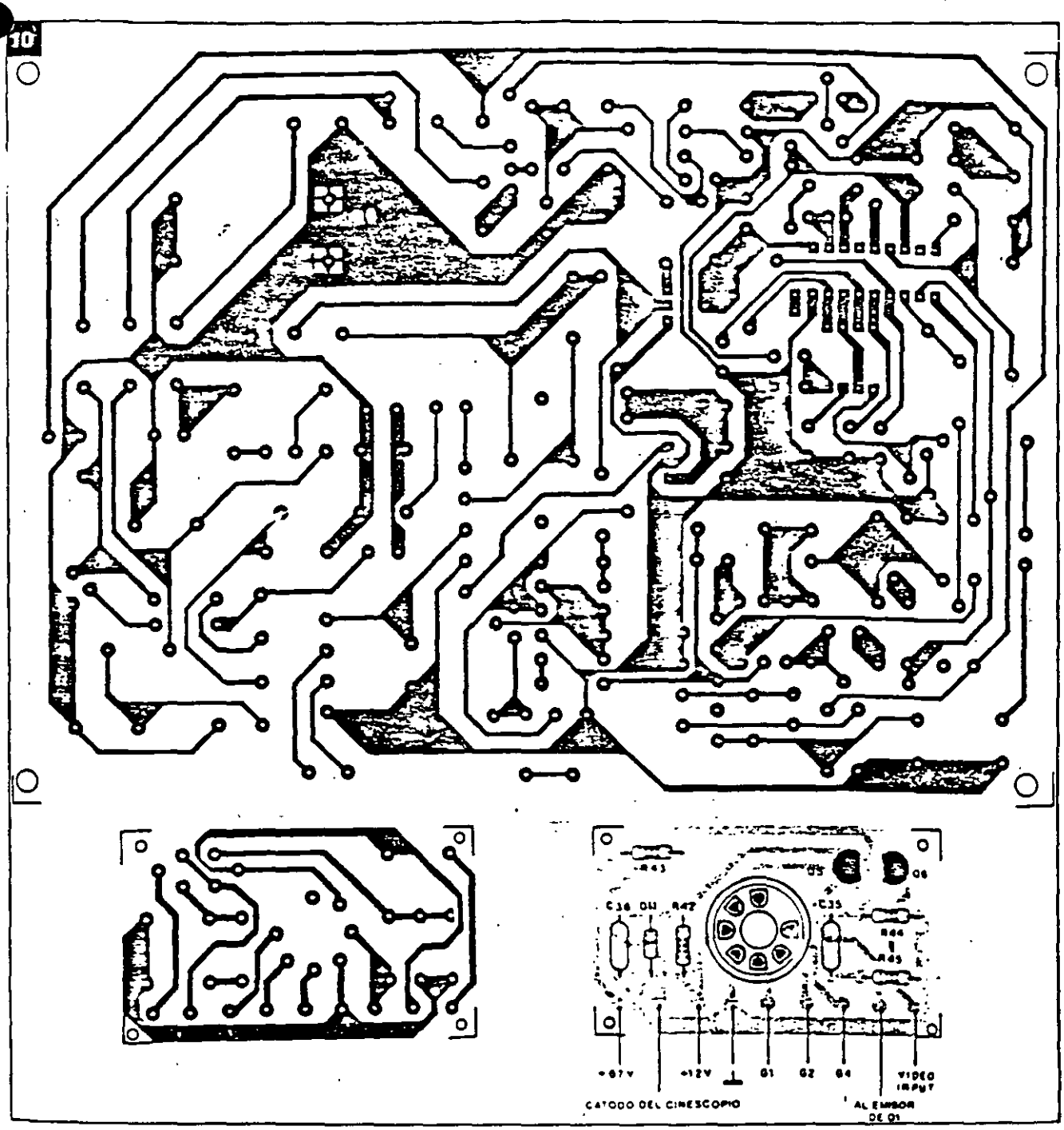

para alimentar los demás elementos del cinescopio y la etapa de salida vertical (=25V).

Montaje

El circuito del monitor de video está compuesto por dos módulos: la placa principal y la plaqueta de cinescopio. La fuente de alimentación, con excepción del transformador de fuerza, se sitúa en la propia placa base. Los diseños de estas dos placas aparecen en la figura 10.

El montaje de la placa principal es sin duda lo que requiere mayores cuidados, y para el mismo elaboramos una secuencia que facilitará esa tarea.

Inicie el montaje por los componentes menores (más livianos), redoblando su atención cuando sean del tipo "polarizado" como por ejemplo capacitores elec-

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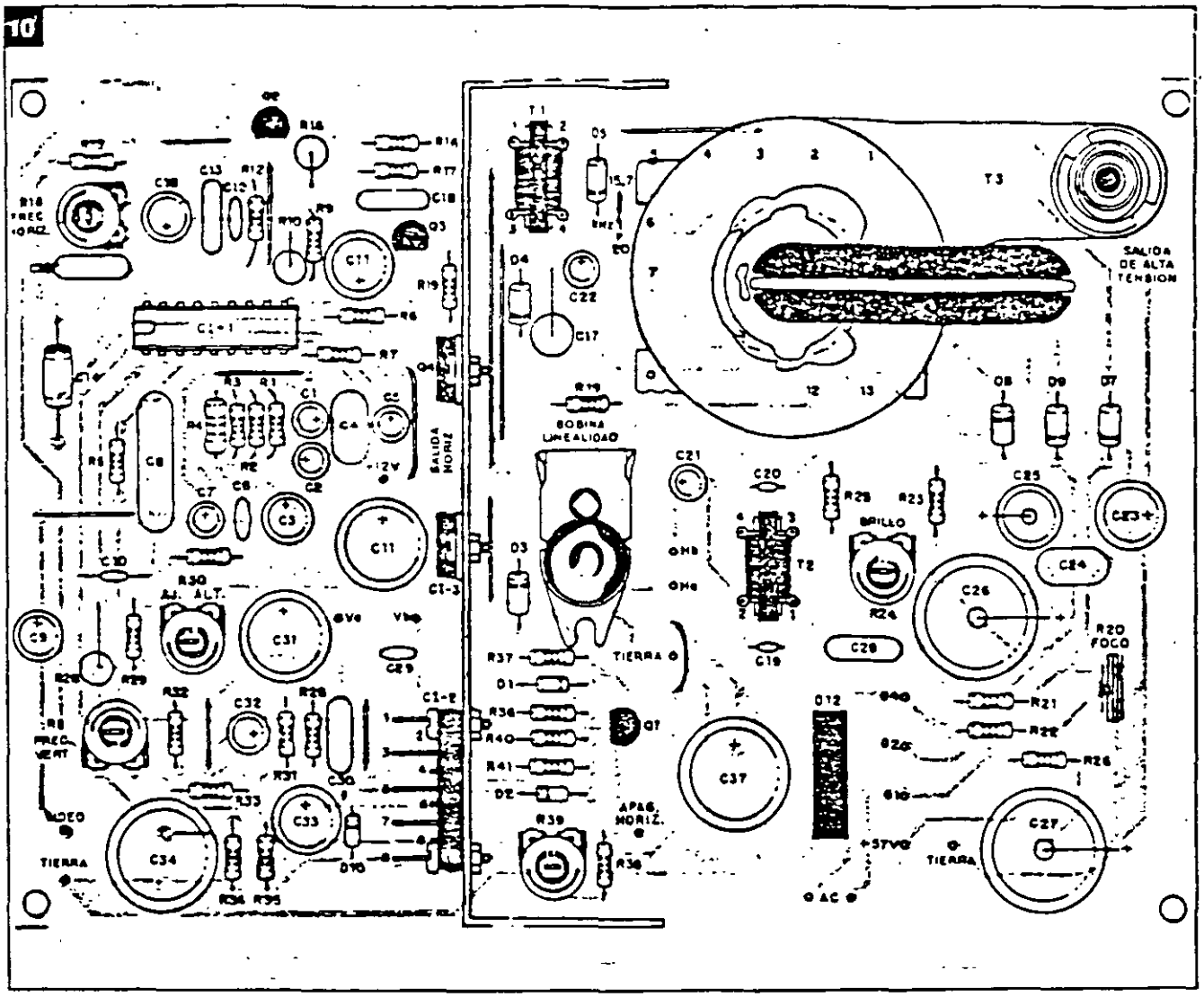
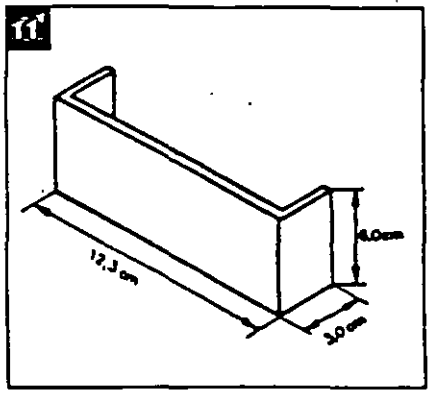


trolíticos, diodos y transistores. Observe la indicación de su polaridad en la placa y asegúrese que está correcta antes de soldarlo.

11



Recuerde también colocar todos los jumpers necesarios.

Estos jumpers deben ser trozos de alambre 22 AWG (diámetro en mm 0,6438) rígido o flexible.

Si usted fuera a operar con equipos de 525/2 líneas la frecuencia horizontal deberá ser de 15,75 kHz.

Seleccione el jumper apropiado (diodo D5 alimentando el pin 4 del Fly-Back). La otra posición (diodo D5 alimentando el pin 5 del Fly-Back) permite la operación con frecuencia horizontal de 20kHz.

Para facilitar la prueba de esta placa principal, es conveniente subdividirla en dos etapas básicas: la de baja tensión y la de alta tensión (etapa de salida horizontal).

Montaje de la primera etapa

En el montaje de esta primera etapa, NO COLOQUE EN EL CIRCUITO LOS SIGUIENTES COMPONENTES:

- el transformador de salida horizontal (T3) (fly-back)
- el transistor de salida horizontal (Q4)
- el CI-2 (salida vertical)
- la bobina de linearidad

- el transitor drive (Q3)

Por ser estos componentes mayores y más pesados, y dado que no contribuyen a la prueba de funcionamiento de esta primera etapa, el manejo de la placa sin ellos se vuelve más fácil, y al mismo tiempo evita culquier tipo de accidente (el núcleo del flyback y de la bobina de linearidad no deben sufrir impactos mecánicos, a riesgo de partirse).

El disipador de aluminio (figura 11), soporte térmico de Q4 (salida horizontal), CI-2 (salida vertical), y CI-3 (regulador de la fuente), también pueden dejarse de lado en esta primera etapa, a menos que usted opte por usar la propia fuente de alimentación del circuito en la prueba. Recomendamos el uso de una fuente regulada externa, con ajuste progresivo de tensión (6 a 12V). Los transformadores T1 (drive) y T2 (foco dinámico) no entrarán en funcionamiento en esta primera etapa, pero pueden montarse en la placa. Atención a la numeración de los pins de estos transformadores; evite colocarlos invertidos (primario y secundario).

Primera prueba de funcionamiento

Con la placa principal montada (a excepción de los componentes descritos más arriba), inspeccione lentamente el conjunto, en busca de irregularidades: controle la posición de los componentes, la polaridad de los diodos y capacitores electrolíticos, y verifique si no existen cortos accidentales provocados por corrimientos de soldadura o terminales doblados. Recuerde si no falta ninguno de los jumpers. En caso de duda, siga las conexiones con el esquema eléctrico.

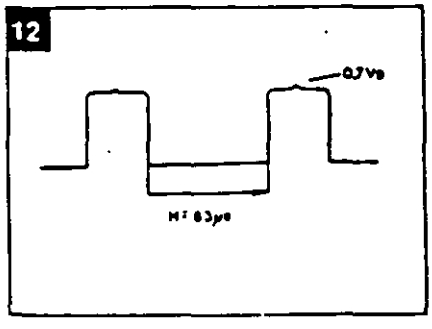
En esta primera prueba verificaremos la correcta operación del oscilador horizontal (CI-1), y para ello, no hay necesidad de colocar ni la plaqueta del cinescopio ni el yugo de deflexión, ni el TRC.

Coloque la placa montada y revisada en el banco de trabajo y alimentela con una fuente auxiliar de 12V. Es conveniente aplicar la tensión de alimentación en modo creciente, monitorizando con un osciloscopio la salida de señal por el pin 11. La figura 12 muestra la forma de onda que deberá estar presente allí. Cualquier irregularidad, vuelva a inspeccionar la placa, desconectando la fuente de alimentación. Debe ser considerado normal un pequeño calentamiento de este circuito integrado (CI-1).

La resistencia R9, de 820 Ω, alimenta el pin 16 proporcionando la corriente mínima para la partida del oscilador (start). La resistencia R12 alimenta el pin 12 con pulsos horizontales (retroalimentación) para efecto de control de la frecuencia (sincronismo). Es conveniente levantarlo en esta primera etapa de prueba, para evitar que bloquee el arranque, una vez que la etapa de salida está inoperante. No es común que aparezcan problemas en esta prueba inicial. No es necesario inyectar ninguna señal de entrada.

Estando todo en orden, verifique también el ajuste de la frecuencia horizontal R14, girándolo para un lado y el otro, observando en el osciloscopio la variación de la frecuencia de la señal de salida, manténgalo en la posición en que obtenga la frecuencia horizontal correcta de 15,75kHz (periodo de 63µs). Más tarde se deberá retocar este ajuste.

Acuérdese de solucionar los problemas por etapas, que resulta mucho más simple y racional que intentar solucionarlos como un todo.

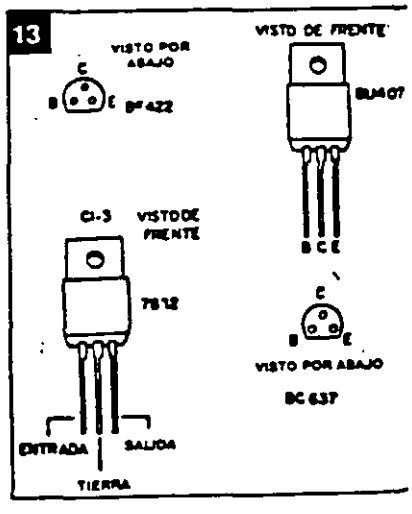


Montaje de la segunda etapa

Coloque ahora el resto del material para completar el montaje de la placa principal.

Al disipador de aluminio en forma de "U" se acoplarán el transistor de salida horizontal (con mica de aislamiento), el regulador de la fuente de 12V y el CI de salida vertical. Solamente el transistor de salida horizontal exige aislar de su colector con la tierra del disipador.

Realice ahora el montaje de la placa del cinescopio. La disposición de las terminales de los transistores está esbozada en la figura 13. Atención al soldar el soquet del cinescopio en la plaqueta. En él existe un pin vacío (sin agujero) que sirve de guía al enchufarlo en los pins del cinescopio. Verifique su posición para que coincida con las conexiones a los elementos del tubo. Una buena referencia son los pins de filamento (3/4). Para localizarlos en el tubo, puede usar un ohmímetro y verificar la baja resistencia entre ellos.



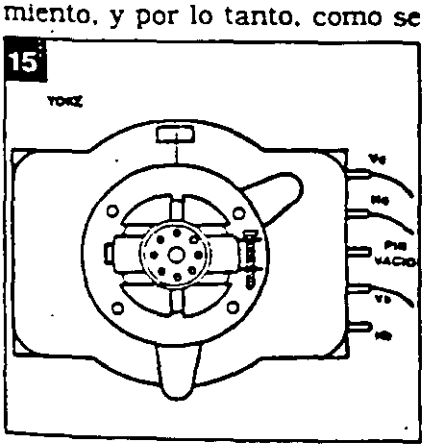
Las conexiones entre la placa del cinescopio y la placa base deberán ser de una extensión suficiente para que concuerden con la disposición mecánica final. Estas conexiones son: la rejilla de foco (pin 7), la rejilla auxiliar G2 (pin 6), la rejilla de control G1 o de brillo (pin 5), el cátodo (pin 2), la tierra (pin 4), filamento y +12V (pin 3) y finalmente la alimentación para el transistor de salida de video +57V en la placa. La tierra de la placa del cinescopio deberá también ser conectada a la tierra del cinescopio (aquadac), como muestra la figura 14.

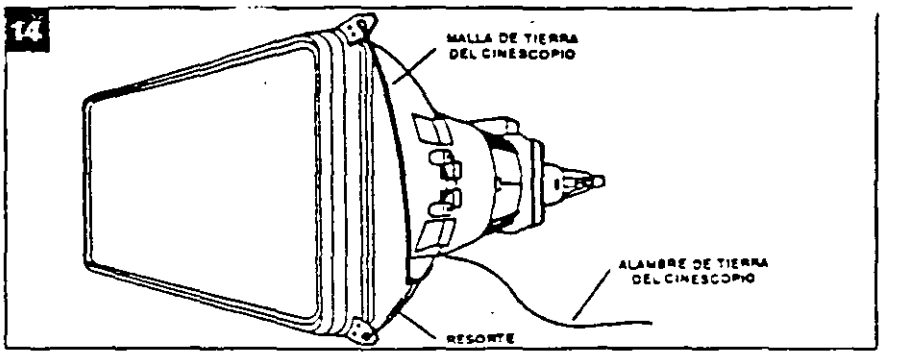
Las conexiones del yugo también deberán hacerse: bobinas deflectoras horizontales (dos alambres) y bobinas deflectoras verticales (dos alambres). Observe por la figura 15 la disposición de los terminales del yugo. En estas conexiones, mantenga también una extensión suficiente conforme se explicó anteriormente.

Por fin, la conexión del transformador de alimentación: la entrada alternada del secundario de 18V del transformador va a alimentar la placa principal, donde será rectificada y filtrada, yendo a alimentar el regulador de 12V.

Prueba final

En esta etapa de prueba final, todos los circuitos del monitor deberán entrar en funcionamiento, y por lo tanto, como se





puede esperar, la probabilidad de que ocurran problemas también son mayores, y debemos estar preparados para resolverlos. En este sentido elaboramos una tabla con las principales formas de onda en el circuito, para que sirvan de referecia en su trabajo (figura 16).

Consiga un osciloscopio y una fuente de alimentación ajustable para dar principio a los trabajos finales.

Siempre recomendamos que preferentemente se use una fuente de alimentación externa (12V x 1A) hasta que coloque el circuito en pleno funcionamiento.

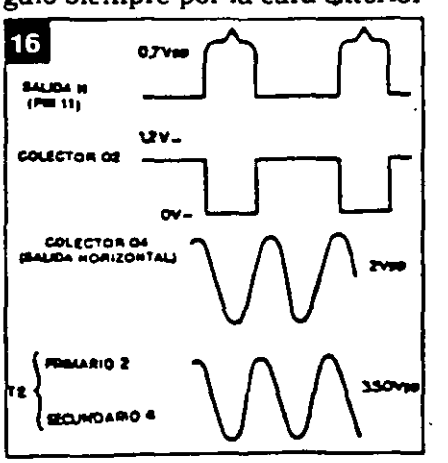
Consideraciones y consejos

a) El yugo es la carga de las etapas horizontal y vertical, por lo tanto cualquier irregularidad en su conexión influirá sobre estas etapas. Revise con cuidado las conexiones de las bobinas horizontales (Ha y Hb) y verticales (Va y Vb) al circuito. En caso de duda, con un ohmetro puede fácilmente localizar las bobinas de deflexión vertical pues las mismas presentarán una resistencia bastante superior (del orden de 12 ohm) comparada a la de las bobinas deflectoras horizontales. El bobinado de la deflexión vertical se hace sobre el núcleo de ferrita del yugo, pues este bobinado exige una inductancia alta, para hacer carga a los 50Hz ó 60Hz de la deflexión vertical. Jamás conecte el circuito sin que la conexión del yugo esté hecha.

b) Use un osciloscopio con entrada para hasta 400V. La lectura de los pulsos horizontales creados en el colector del transistor de salida horizontal puede alcanzar de 250 a 300V de pico. Para efectuar esta lectura el osciloscopio debe permitir la entrada de tensiones de este orden.

c) El chupón del cinescopio conduce la "muy alta tensión" necesaria al ánodo para que el haz de electrones sea atraído hacia la pantalla. Sin esta MAT, aunque el resto del circuito esté funcionando, no habrá brillo en la pantalla. **En ningún caso proceda a la lectura de esta MAT (del orden de 13kV) ya sea con voltímetro o con osciloscopio.**

d) Mucho cuidado al manipular el cinescopio. Su parte más delicada y frágil es el "cuello". Jamás sorgue el cinescopio solamente por este "cuello". Sosténgalo siempre por la cara exterior



de la pantalla.

e) El ánodo del cinescopio (cara interna que reviste el tubo) forma un capacitor con la faz externa de grafito. Asegúrese de que este capacitor esté descargado durante la manipulación del cinescopio. Puede producirse su descarga por un corto resistivo (10k) entre el ánodo y el grafito o tierra del tubo. Evite cortes desagradables y accidentes inesperados.

f) El comportamiento del cinescopio es muy semejante al de una de las "viejas" válvulas.

El brillo de la pantalla es el resultado del pasaje del haz de electrones entre el cátodo (emisor) y el ánodo (receptor). Por lo tanto, son condiciones esenciales para tener el brillo de la pantalla: filamento caliente, tensión de aceleración en el ánodo (MAT), polarización adecuada en los demás elementos como el cátodo, rejilla de control, rejilla auxiliar y rejilla de foco.

g) Como las fuentes auxiliares son generadas por los secundarios del "fly-back" cualquier consumo de estas fuentes que esté por encima de lo normal (por ejemplo, cortocircuitos) se reflejará como dificultad de desempeño del transistor de salida horizontal, pues es él quien provee toda la energía de este sistema. La etapa vertical es alimentada por la tensión de +25V generada en el pin 5 del fly-back. Si por ejemplo el CI-2 estuviera con un consumo exagerado o en corto, el drenaje de corriente de esta fuente auxiliar bloqueará la salida horizontal.

h) Si ocurriera algún tipo de problema en la etapa horizontal, es normal que las tensiones auxiliares no se presenten en sus valores correctos. Por lo tanto, en estos casos, procure solucionar el problema principal, y no tome como referencia estas tensiones auxiliares, que volverán a lo normal en cuanto se resuelva la anomalía.

Ajustes del monitor

Son necesarios los siguientes ajustes, después que el aparato esté funcionando normalmente:

• **Frecuencia horizontal:** determina la frecuencia libre del oscilador horizontal que debe ser igual o muy cercana a la frecuencia de uso.

Sin ninguna señal aplicada a la entrada de video, ajuste por R14 la frecuencia de 15,75kHz en la señal de salida del pin 11 de CI-1. Conecte una señal de video y verifique la correcta sincronía de la imagen en la pantalla. Si fuera necesario, se pueden hacer pequeños retoques con la imagen en la pantalla.

• **Frecuencia vertical:** procedimiento idéntico con relación al osciloscopio vertical. Con una imagen en la pantalla, ajuste mediante R8 hasta conseguir su

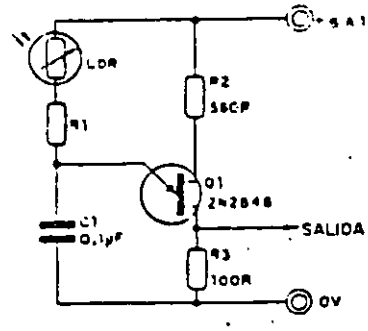
CIRCUITOS & INFORMACIONES

CONVERSOR LUZ/FRECUENCIA

Este circuito proporciona una señal de salida cuya frecuencia depende de la intensidad de la luz que incide en un elemento sensible, en este caso un LDR.

La forma de la onda obtenida puede ser en diente de sierra, como pulsos bien agudos, según el electrodo del transistor de donde parta. En el emisor del transistor unijuntura tenemos una forma de onda diente de sierra y en la base de B1 tenemos pulsos agudos de buena intensidad.

El circuito es un oscilador de relajación donde la constante de tiempo RC es variable, ya que R representa la resistencia del LDR, que es función de la luz incidente.



En la figura se ve el circuito simple que puede alimentarse con tensiones entre 6 y 12V.

La banda de frecuencias para el circuito está entre 100Hz y 5kHz pero puede modificarse cambiando C1. Valores mayores disminuyen las frecuencias de la banda.

El transistor unijuntura aconsejado es el 2N2646 aunque pueden probarse equivalentes.

Una aplicación posible de este circuito está en el desarrollo de un fotómetro digital.

fijación vertical.

• **Altura vertical:** ajusta la ganancia del camino vertical de la señal de deflexión, y por consiguiente, la altura de la imagen en la pantalla. Su ajuste puede realizarse con una imagen que llene todo el contorno de la pantalla (por ejemplo un patrón blanco). Actúe sobre el trimpot hasta conseguir la altura deseada. En monitores de computadora, se recomienda una altura de 3/4 de la pantalla, o la preferencia del usuario.

• **Control de brillo:** el trimpot R24 ajusta la tensión de polarización de la rejilla de control del cinescopio, y por lo tanto determina el punto de corte para el pasaje del haz de electrones. El ajuste del brillo debe permitir que solamente sean visibles las letras o puntos gráficos de la computadora, y no un fondo claro.

• **Ajuste de foco:** como el propio nombre lo dice, obtendrá un punto óptimo de focalización del haz sobre la pantalla. Use una imagen con bastantes detalles gráficos para una mejor apreciación de este ajuste.

• **Ajuste de apagado:** el trimpot R39 ajusta el límite de apagado horizontal y vertical, o sea, para que el retorno del haz no sea visible en la pantalla. Este ajuste se hace observando hasta que la imagen permanezca agradable, sin sombras ni nubes, y sin líneas de retraso vertical. La señal de video debe ser conectada a la entrada.

• **Ganancia de video:** en función del nivel de señal de video a ser aplicado al amplificador de la placa del cinescopio, podrá ser necesario sustituir la resistencia R45 que determina la ganancia de la etapa.

LISTA DE MATERIALES

Resistores
R01 - 820R
R02 - 82R
R03 - 4k7
R04 - 1k
R05 - 100k
R06 - 220k
R07 - 8k2
R08 - 470k (TP)
R09 - 820R
R10 - 6k8
R11 - 2k7
R12 - 5k6
R13 - 33k
R14 - 10k (TP)
R15 - 6k8
R16 - 820R
R17 - 220R
R18 - 5R6
R19 - 470R
R20 - 2M2 (TP)
R21 - 22k
R22 - 100k
R23 - 47k
R24 - 220k (TP)
R25 - 270k
R26 - 56R
R27 - 6k8
R28 - 680R
R29 - 5R6
R30 - 220k(TP)
R31 - 560R
R32 - 22k
R33 - 47k
R34 - 560R
R35 - 4R7
R36 - 47k
R37 - 2k2
R38 - 680R
R39 - 2k2
R40 - 22k
R41 - 27k
R42 - 1k
R43 - 1k2
*R44 - 22R**
R45 - 47R
TP = mini trimpot
** ajusta la ganancia de video*

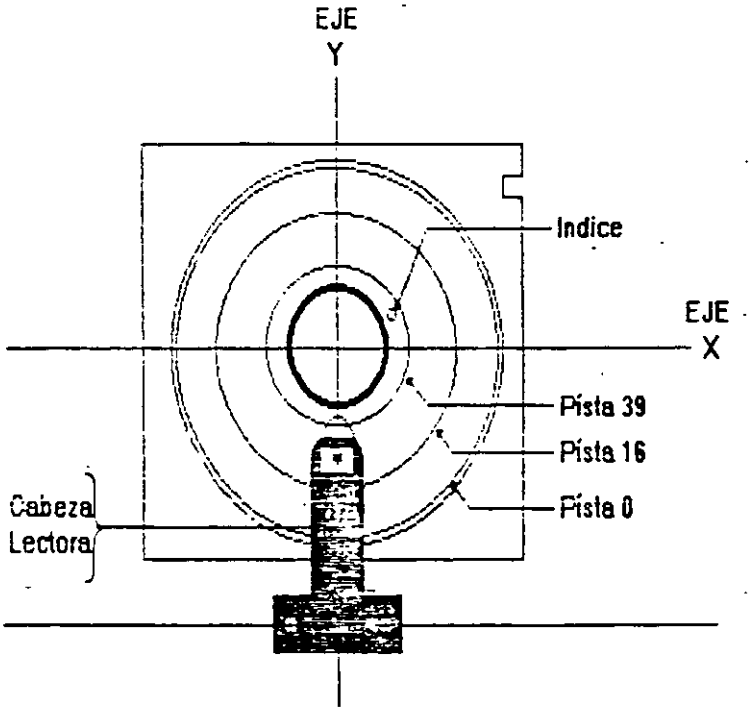
Capacitores:
C01 -4µ 7/16V (EL)
C02 - 10µ /16V (EL)
C03 - 22µ/16V (EL)
C04 - 150n/63V (CR)
C05 - 1µ/63V (EL)
C06 - 150p/50V (CR)
C07 - 10µ/16V (EL)
C08 - 680n/50V (CR)
C09 - 100µ/16V (EL)
C10 - 1n8/50V (CR)
C11 - 220µ/16V (EL)
C12 - 180p/63V (CR)
C13 - 47n/250V (PL)
C14 - 2n2/100V (ST)
C15 - 100µ/16V(EL)
C16 - 100n/250V (PL)
C17 - 10n/400V (PL)
C18 - 8n2/250V (PL)
C19 - 1n/50V (CR)
C20 - 820p/50V (CR)
C21 - 4µ7/16V (EL)
C22 - 4µ7/16V (EL)
C23 - 220µ/40V (EL)
C24 - 10n/600V (PL)
C25 - 22µ/100V (EL)
C26 -100µ/100V (EL)
C27 - 100µ/100V(EL)
C28 - 100n/250V(PL)
C29 - 390p/50V (CR)
C30 - 33n/250VOP (PL)
C31 - 1000µ/16V (EL)
C32 - 6µ8/16V (EL)
C33 - 100µ/25V (EL)
C34 - 2200µ/25V (EL)
C35.- 330n/250V (PL)
C36 - 22n/250V (PL)
C37 - 2200µ/25V (EL)
CR = cerámico
PL = poliéster
EL = electrolítico
ST = styroflex

Diodos:
D1, D2 - BAV21
D3, D5 a D9 - BYV95C
D4 - BY206 ó BY448
D10 - BAX12
D11 - zener 6V2
D12 - puente rectificador

Transistores
Q1 - BC548
Q2, Q6 - BC549
Q3 - BC637
Q4 - BU407
Q5 - BF422
Varios: cinescopio 12" (31 cm) Philips M31 336 GH/B, unidad deflectora (yoke) Philips 3106 108 6777, transformador salida horizontal (fly-back) Philips 3106 108 3167, bobina de linealidad Philips 3106 108 2660, transformador drive (T1) 1171, transformador para foco dinámico (T2) 31681, zócalo para cinescopio 7 pins, zócalo para CI 18 pins, transformador de fuerza con secundario de 18V, cordón de fuerza, placa de circuito impreso base, plaqueta de cinescopio, etc

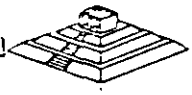
Unidades de Disco Flexible

Ajustes Principales



apuntes

UNIDADES DE DISCO



IBM Personal Computer
Drive Diagnostic Program

Version 1.00
Copyright Dysan Corp. 1983

A. Automatic Drive Tests

B. Manual Drive Tests

C. Diskette Utilities

Enter command (A - C):

Dr: A Trk: 0 Side: 0 Recvs: 0 Seek: o Settle: 15 DS Sound

apuntes

UNIDADES DE DISCO

Drive Set-Up

Enter Drive number (A - D):

Enter Seek Time
(2, 4, 6, 8, ... 32 msecs.):

Enter Head Settle Time (0 to 50 msecs.):

Enter Retries (0 to 20):

Single / Double Sided (S/D):

Sound - Yes/No (Y/N):

Dr: A	Trk: 0	Side: 0	Rtrys: 0	Seek: 6	Settle: 15	DS	Sound

UNIDADES DE DISCO

---------- Automatic Tests ----------

	Side 0	Side 1
RPM:	300	
Centering: Track 21	ok	ok
Radial: Track 0	-13 +13 [+0]	-13 +13 [+0]
16	-13 +13 [+0]	-13 +13 [+0]
39	-13 +13 [+0]	-13 +13 [+0]
Azimuth: Track 34	-42 +42	-42 +42
Number of Passes = 1	*** Drive PASSED All Tests ***	

Press S key - Stop Test at End of Current Pass
Press Esc - Exit to Automatic Test Menu
Press P key - Print Screen
Press Any Other Key to Restart Test

Dr: A Trk: 34 Side: 1 Rtrys: 0 Seek: 6 Settle: 15 DS Sound

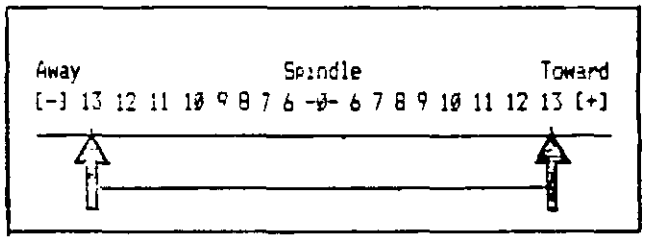
UNIDADES DE DISCO

```
Manual Test Menu

   A.  Setup Drive                    I.  Random Seek, Read & Write
 * B.  RPM                            J.  Track Seek
 * C.  Diskette Centering             K.  Alternate Track Seek
 * D.  Radial Alignment               L.  Last Disk Error Status
 * E.  Azimuth Alignment              M.  Select Side 0
 * F.  Hysteresis                     N.  Select Side 1
   G.  Accordion Seek                 Z.  Main Menu
   H.  Random Seek & Read

Enter command (A - Z):

Dr: A  Trk: 0   Side: 0  Rtrys: 0   Seek: 6   Settle: 15  DS  Sound
```

apuntes

UNIDADES DE DISCO

Radial Alignment



Press Esc - Exit To Menu
Press Any key - Restart Test

Dr: A Trk: 19 Side: 0 Rtrys: 0 Seek: 6 Settle: 15 DS Sound

apuntes

SINTOMA	ACCION CORRECTIVA
Después de encender la impresora la cabeza de impresión se mueve erróneamete	* Apague la impresora y asegúrese que los cables de atracción esteninteractos. Revise queno haya materiales extraños (como lapices, etc.) en la impresora. Manualmente mueva la cabeza de inpresión de izquierda a derecha y revise que el movimiento sea constante. - Efectúe un default reset (ver párrafo 5.3)
Cuando se enciende la impresora la cabeza de impresión se mueve a la derecha y se detiene.	* Restos de papel o suciedad bloquean la luz en el sensor de margen izquierdo. Limpie cualquier suciedad sobre el detector de margen izquierdo.
Al encender la impresora la cabeza de impresión se mueve a la izquierda pero no se detiene al llegar llegar al margen izquierdo (por ejemplo el carro choca contra el extremo izquierdo).	*El sensor de margen izquierdo está defectuoso. Este sensor deberá ser reemplazado por un técnico calificado.
Cuando la impresora se coloca en línea, la cabeza de impresión se mueve pero no imprime.	- Revise el cable de impresión y asegúrese que esté conectado a ésta.
Las agujas de la cabeza de impresión se disparan pero no imprimen o imprimen muy ligero.	- No se ha instalado el cartucho de cinta, o habiéndose instalado está muy usado o la cinta está rota. Instale un nuevo cartucho de cinta. - Retire el cartucho de cinta y revise el mecanismo de avance de cinta moviendo el carro y observando la lengueta para verificar que gire en sentido contrario a las manecillas del reloj.
Inconsistencia en la formación del caracter (impresión de los puntos clara y obscura en forma aleatoria).	* Use la palanca de ajuste de la cabeza de impresión para acercada al papel.

SINTOMA	ACCION CORRECTIVA
El papel no se desliza apropiadamente cuan - do se alimenta desde el frente.	* Si usa formas múltiples, revise el grosor. No deberá exceder de 6 (original+ 5 copias). - El papel tiene un dobles abajo en la orilla que evita que haga contacto co la guía de papel. - Doble el papel hacia arriba para resolver el problema. - La ranura de alimentación de papel está obstruida -limpiela de cualquier suciedad.
La cabeza de impresión rasga el papel en el lado izquierdo	* Mueva la forma ligeramente a la izquierda de tal forma que la orilla de la cabeza de im- presión no abandone el papel. Ver párrafo 1 6.1 paso 4 para colocar el margen izquierdo en el papel.
La cabeza de impresión rasga la orilla derecha	* Programe el margen derecho (FUNC 6, ver párrafo 2.4.4) de tal forma que la cabeza de impresión no abandone el papel.
La primera línea de impresión está en el tope	* Revise la programación de las funciones 2,3 y 39. Mida la longitud de la forma en pulgadas El valor para la función 2 es el número de líneas por pulgadas multiplicándolo por la lon- gitud de la forma. Ejemplo: Con la función 39 programada a 6 líneas/1pulg x 11 pulg. = 66 líneas. 66 es el valor que deberá tener la función 2.
La impresora produce una estrecha columna de impresión	* Revise la programación del margen derecho e izquierdo (FUNC 5 y 6 ver párrafo 2.4.4)
El led de PAPEL permanece iluminado o con- tinua iluminado después de que la impresora ha operado por un corto período.	El papel es demasiado delgado. El papel translucido permite que la luz pase al sensor de luz. Use papel grueso o programe la FUNC 40 en 1.

SINTOMA	ACCION CORRECTIVA
Cuando se coloca en línea, la cabeza de impresión no se mueve o no imprime.	* Asegúrese que el indicador de LINEA está encendido. Presione la tecla LINEA si el indicador no enciende. - Asegúrese que el cable de comunicación esté perfectamente unido a la impresora y al computador. - Revise la programación de FUNC 47 (deberá programarse en cero).
Imprime sobre una misma línea en forma intermitente (omite el avance de línea)	* El camino del papel está obstruido. Limpie el camino del papel. No deberá pasar por las esquinas de un escritorio, orillas de la caja del papel, etc.
El papel no avanza hasta la posición apropiada del tope de la forma.	* Revise la programación de las funciones 2,3 y 39.
El papel avanza continuamente cuando la impresora se enciende.	* Se ha enviado un gran número e comandos de avance de forma desde el computador. Presionando la tecla de RESET deberá detenerse el avance de papel. - La tecla de F.F. o AVAN está pegada. Trate, presionándola, de liberarla.
El papel no avanza cuando se envía un comando de avance de forma.	
El papel se rasga	* Los tractores de formas están demasiado cercanos o demasiado alejados. Ajústelos de acuerdo al tamaño de la forma usada. - Los agujeros de las formas no están alineadas. (Lado izquierdo con respecto al lado derecho).

5.4 CODIGOS DE ERROR

Si una falla es detectada en la memoria no volátil de trabajo el led de ERROR empezará a parpadear y el código de error "6508"aparecerá en el display de panel de control. Una falla en la memoria de trabajo usualmente es el resultado de descargas electrostáticas o fluctuaciones en la línea de alimentación de la impresora. El operador podrá continuar la operación presionando la tecla de CONT. Los valores originales serán cargados en la EN-180 en lugar de los valores programados por el usuario. El operador deberá, por lo tanto programar cualquier función discreta o de valor a los valores usuales y reanudar la operación. Si el error persiste la impresora deberá revisarse tan pronto como sea posible para corregir la falla.

5.5 DIAGNOSTICO

La tabla 5.1 provee los procedimientos para diagnosticar la impresora a nivel del operador. Para diagnosticar la impresora el operador deberá localizar el problema de la impresora en la tabla 5-1 y efectuar la acción correctiva bajo los procedimientos dados. La impresora deberá ser revisada para una operación apropiada entre cada paso de acción correctiva. Si la falla no puede corregirse usando los procedimientos descritos en la tabla 5-1 , un técnico calificado o directamente el departamento de Servicio de Intelecsis deberá proporcionar servicio a la impresora.

PELIGRO: El operador deberá desconectar la impresora de la alimentación de C.A. antes de realizar cualquier acción correctiva que requiere trabajar dentro de la impresora.

TABLA 5-1 DIAGNOSTICOS

SINTOMA	ACCION CORRECTIVA
Después de encender la Impresora, la impresora aparece muerta. (no hay ruido en la maquina, no hay movimiento de la cabeza de impresión no hay luces en el panel frontal.	* Asegúrese que el cable esté incertado en el receptáculo de C.A. - Asegúrese que hay energía en el receptáculo de la pared. - Revise el fusible de línea de la Impresora. Un fusible fundido es una indicación de proble mas más serios.
Después de encender la impresora la impresora produce el sonido normal, pero el LED de ENCEN no se ilumina.	* Presione la tecla de RESET - Revise si el pin 16 del conector está insertado en el conector del panel frontal. Apague la impresora e inserte el pin 16 del conector si éste no está conectado.

MANTENIMIENTO Y DIAGNOSTICO

5.1 INTRODUCCION

Este capítulo provee los procedimientos de mantenimiento periódico y diagnóstico que puede ser realizado por el operador. Estos procedimientos no requieren conocimientos especiales sobre electrónica o impresoras. Cualquier diagnóstico o mantenimiento más allá del nivel presentado en este capítulo deberá ser realizado por un técnico calificado.

5.2 MANTENIMIENTO PERIODICO

PELIGRO: Asegúrese que la impresora esté conectada de la alimentación de 110 VCA antes de entrar en la tarea de limpieza de la impresora.

PRECAUCION: No use limpiadores, solventes o lubricantes sobre cualquiera de las partes funcionales de la impresora.

El único mantenimiento periódico que puede ser realizado es una limpieza periódica (aproximadamente cada tres meses). Use una aspiradora con punta plástica para remover basura del carro, guías del papel y barra de impresión. Una franela seca será usada para limpiar la suciedad acumulada en las flechas del carro y la barra de impresión.

La cubierta superior de la impresora puede limpiarse con alcohol. Para limpiar la cubierta de acrílico hágalo con una franela suave. No use papel para limpiar la cubierta de acrílico.

5.3 DEFAULT RESET

Un método útil para corregir problemas con la EN-180 es el default reset o clear reset. Si la impresora opera ilógicamente o falla al obedecer la programación de cualquier función de valor o discreta el usuario deberá realizar un default reset (ver procedimiento en el párrafo siguiente).

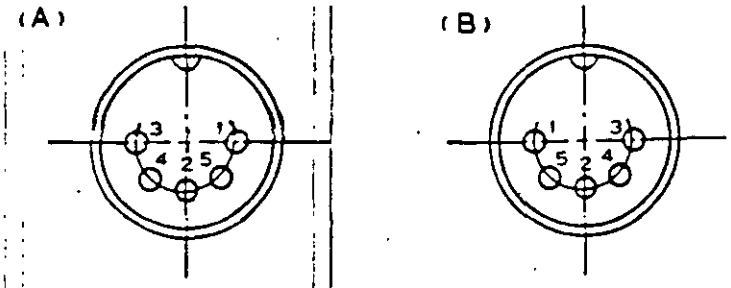
Un grupo de parámetros originales que permanentemente almacenados en la impresora serán cargados en la memoria de trabajo. Para identificar los valores originales de cada función dirigirse al Apéndice A, Apéndice G y H. Cualquier valor programado por el usuario se perderá al aplicar el default reset. Después de ejecutar un default reset, estas funciones deberán programarse con los valores que el usuario requiera.

NOTA: La tarea de reprogramar las funciones de valor y discretas es aún más simple si estos valores han sido anotados previamente.

Para aplicar un default reset o clear reset ejecute los siguientes pasos;

1.- Presione y mantenga la tecla de BORRA
2.- Presione y libere la tecla de RESET
3.- Continúe presionando la tecla de BORRA hasta que la cabeza de impresión regrese y se detenga en su margen izquierdo.

Puerto Teclado



A:Keyboard 5-pin connector

B:Main board 5-pin connector

5 PIN DIN Connector

PIN	SIGNAL
1	+Keyboard Clock
2	+Keyboard Data
3	-Keyboard Reset
4	Ground
5	+5 Volts

apuntes

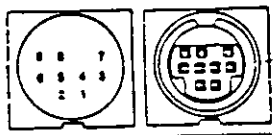
Configuración puertos

PORTS PINS - OUT

SERIAL PORT (J1 , J2)

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground	10	

MOUSE PORT (J5)



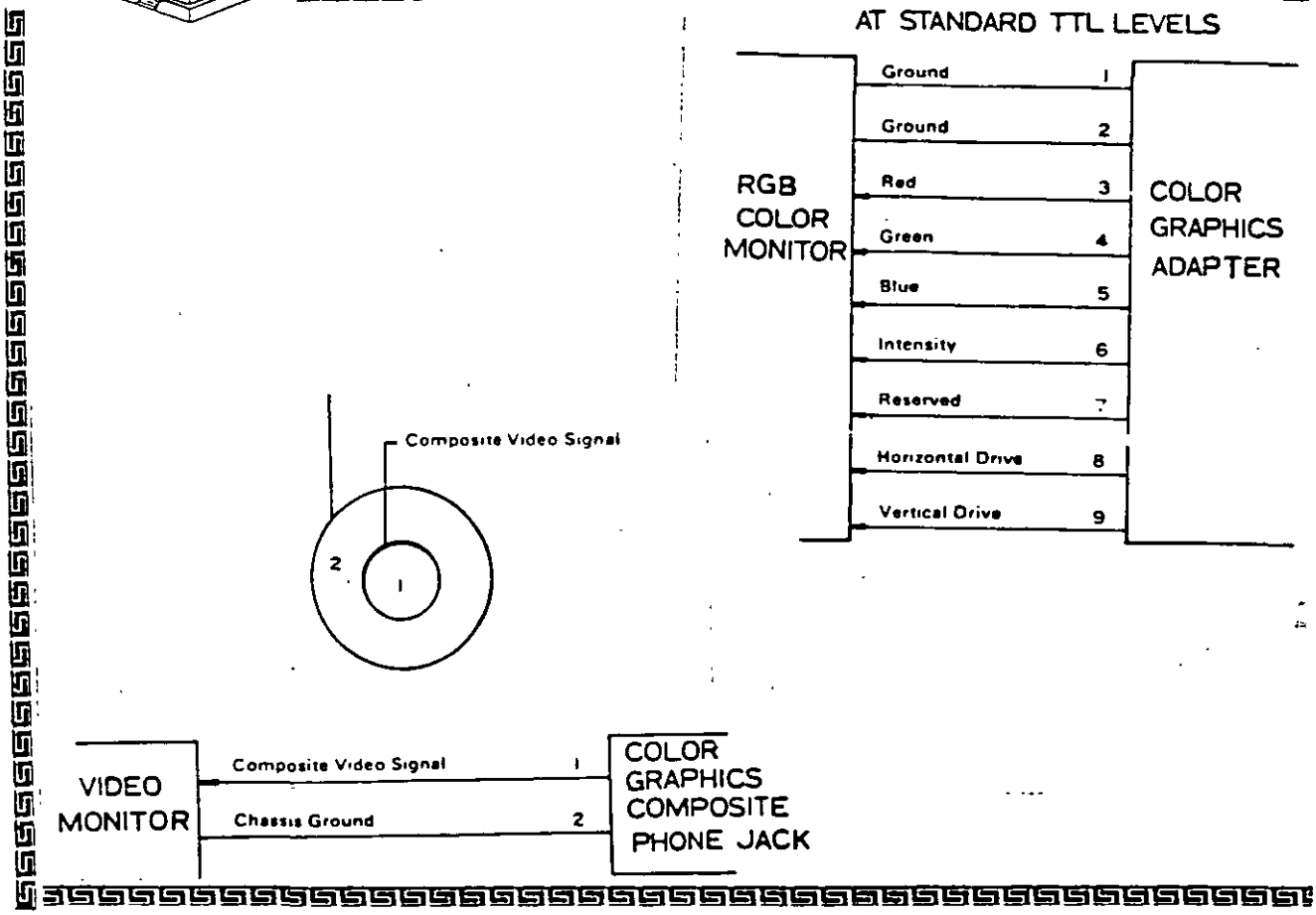
Pin	Signal
1	+5V
2	XA
3	XB
4	YA
5	YB
6	LB
7	MB
8	RB
9	GROUND

GAME PORT (J3)

Pin	Signal	Pin	Signal
1	+ 5V	9	+ 5V
2	D4	10	D6
3	D0	11	D2
4	Ground	12	Ground
5	Ground	13	D3
6	D1	14	D7
7	D5	15	+5V
8	+5V	16	Ground

apuntes

Señales de Video



apuntes

Interface Disco Duro

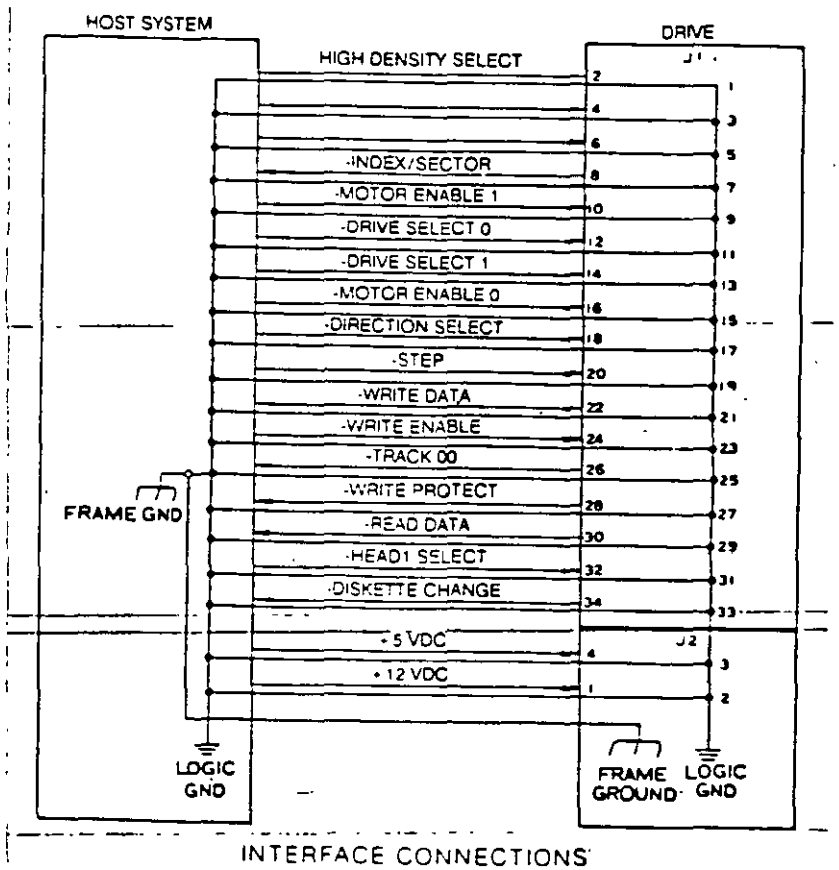
HARDDISK DRIVE INTERFACE (J7)

Pin	Signal	Pin	Signal
1	Reset	2	Ground
3	D 7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Ground	20	Un used
21	Unsued	22	Ground
23	IOW	24	Ground
25	IOR	26	Ground
27	IOCHRDY	28	ALE
29	Unsed	30	Ground
30	IRQBUS	32	JOCS16
33	A1	34	Unsued
35	A0	36	A2
37	CS0	38	CS1
39	SLV ACT	40	Ground

This Card is produced by auto-equipment. If there is any problem. you can send it to us.

apuntes

Interface Unidades de Disco Flexible



INTERFACE CONNECTIONS

apuntes

Puerto RS232 (serial)

PERIPHERAL	Description	Pin No	RS232 PORT
	NC	1	
	Transmitted Data	2	
	Received Data	3	
	Request to Send	4	
	Clear to Send	5	
	Data Set Ready	6	
	Signal Ground	7	
	Carrier Detect	8	
	NC	9	
	NC	10	
	NC	11	
	NC	12	
	NC	13	
	NC	14	
	NC	15	
	NC	16	
	NC	17	
	NC	18	
	NC	19	
	Data Terminal Ready	20	
	NC	21	
	Ring Indicator	22	
	NC	23	
	NC	24	
	NC	25	

Interface "Centronics" (paralelo)

25 PIN Connector		36 PIN Connector	
PIN	SIGNAL	PIN	SIGNAL
1	STROBE	1	STROBE
2	DATA 1	2	DATA 1
3	DATA 2	3	DATA 2
4	DATA 3	4	DATA 3
5	DATA 4	5	DATA 4
6	DATA 5	6	DATA 5
7	DATA 6	7	DATA 6
8	DATA 7	8	DATA 7
9	DATA 8	9	DATA 8
10	ACK -	10	ACK
11	BUSY	11	BUSY
12	PAPER	12	PAPER
13	+ SELECT	13	+ SELECT
14	-AUTO FEED XT	14	-AUTO FEED XT
15	-ERROR	32	-ERROR
16	-INIT	31	-INIT (PRIME)
18-25	GND	15-17, 19-30	GND

IBM

Hardware Maintenance Service

Part N°.6139795

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

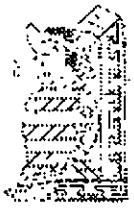
6.- EL BIOS COMO HERRAMIENTA DE DIAGNOSTICO

NOVIEMBRE - DICIEMBRE DE 1998

Palacio de Mineria Calle de Tacuba 5 Primer piso Deleg. Cuauhtemoc 06000 Mexico, D.F. APDO. Postal M-2285
Telefonos 512-8955 512-5121 521-7335 521-1987 Fax 510-0573 521-4020 AL 26

MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

6.- EL BIOS COMO HERRAMIENTA DE DIAGNOSTICO



EL BIOS COMO HERRAMIENTA DE DIAGNOSTICO

Uno de los elementos más importantes de cualquier sistema digital es, desde luego, el programa encargado de coordinar todos los elementos tanto de hardware como de software, que conforman al sistema Genéricamente dicho programa es conocido como Monitor, **IPL o BIOS.**

Las funciones que realiza un programa Monitor son las siguientes:

- Configuración de Interrupciones
- Configuración de DMA
- Configuración de Puertos (Serie y Paralelo)
- Configuración de Teclado y además periféricos
- Transferencia de Control hacia:

a) Un sistema de mayor jerarquía

b) El usuario

Las rutinas de monitor deben ser eficientes y ocupar un espacio mínimo en memoria. Las rutinas básicas de Monitor están orientadas a:

- Cargado de datos en memoria
- Lectura de datos en memoria
- Control de Periférico
- Ejecución de programas

Haciendo un análisis de estas funciones es posible realizar un reconocimiento de hardware instalado en la computadora haciendo una serie de accesos a las rutinas adecuadas de BIOS. Antes de entrar a este punto es importante tratar algunos puntos básicos para una correcta asimilación de los elementos que aquí se expongan.

MAPA DE MEMORIA DEL SISTEMA

Concretamente, en las computadoras personales de **IBM**, el programa de inicialización se conoce como **BIOS (Basic Input Output System)**. En la figura 1 podemos apreciar el Mapa de Memoria de una **IBM PC** original. Este mapa de memoria se ha respetado en su configuración para mantener compatibilidad con modelos posteriores de **PC's y PS/2.**

Analizando el mapa propuesto, el espacio direccionable de 1 Mbytes de 8088 fue dividido en varias áreas funcionales, la que en este momento nos ocupa es la correspondiente al BIOS. Es importante notar que cualquier sistema basado en este microprocesador debe tener memoria ROM en la parte más alta del espacio direccionable de 1 MB debido a que cuando el sistema es encendido, el micro ejecuta el programa que inicia en la dirección FFFFOH.

MAPA DE MEMORIA DE LA IBM PC

Así mismo, tiene reservado los primeros 1024 bytes de RAM para almacenar en él una lista de vectores de interrupción (direcciones de rutinas manejadoras de interrupciones). El resto del mapa de memoria sigue esta división general entre RAM en la parte baja y ROM en la parte alta del espacio direccionable.

EL MICROPROCESADOR 8088

Un microprocesador es un circuito combinacional y secuencial que va a interactuar con otros circuitos para formar en conjunto un sistema digital de cómputo.

En esencia, el microprocesador determina la capacidad del sistema ya que su velocidad establece la velocidad máxima de operación del sistema, siempre que los dispositivos que lo acompañen (memoria, puertos etc.) trabajen a la misma frecuencia de operación, sus pines de datos y direcciones establecen la capacidad de almacenamiento y el tamaño de las palabras, sus pines de control indican el tipo de interface E/S que debe ser usada.

Entre las múltiples funciones que realiza un microprocesador destacan las siguiente:

1. Provee las señales de tiempo y control para todos los elementos del sistema.
2. Búsqueda de instrucciones y datos desde la memoria
3. Transferencia de datos desde y hacia dispositivos de E/S
4. Decodificación de instrucciones.

EL BIOS

El BIOS está echo de código y programas que proporcionan el control a un nivel del dispositivo para la mayor de los dispositivos de entrada salida en el sistema. En la familia IBM PC, el BIOS está contenido en ROM en la tarjeta principal del sistema, junto con un conjunto de rutinas llamadas POST (Power On Self Test), que verifican la máquina cuando ésta es encendida.

El BIOS crea independencia del hardware proporcionando un cierto nivel de separación de éste. Por ejemplo, cuando se hace una llamada al BIOS que envíe un carácter a la impresora, el programador no necesita conocer la dirección de E/S de puerto del impresor o como controlarlo.

El **BIOS** normalmente es invocado vía un conjunto de interrupciones vectorizadas en varios puntos de entrada del **BIOS**. Otros vectores de interrupción son usados para servir la interrupciones de hardware, tales como "operación de disco terminada". En términos prácticos, el software invoca el **BIOS** cargando los registros apropiados en el microprocesador y usando las instrucciones **INT**.

El **BIOS** es extendible. Cuando las rutinas **POST** se ejecutan como parte de su operación busca el espacio de dirección de la **ROM** para rutinas "add-on", las cuales entonces son invocadas así que ellas pueden instalarse por sí mismas. Por ejemplo el **IBM EGA**, extiende la interrupción de vídeo **INT 10**, como se indica en la tabla 2.

La regla para las entradas del **BIOS**, es una interrupción de software por dispositivo. Pueden ser también una o más entradas de hardware, y entradas que apunten a tablas o bloques de datos usados por el manejador del dispositivo.

Los vectores de interrupción, usados como apuntadores a datos en lugar de código, permiten alterar fácilmente el ambiente de trabajo de la computadora.

En lo que se refiere a las localidades de memoria absoluta, nótese lo siguiente: Algunas funciones han sido agregadas a los vectores de interrupción (0:0 a 3FF), pero ninguna función ha sido redefinida. Los mapas de memoria para el despliegue de vídeo (A000:0, B000:0 B800:0) no cambiarán el modo de operación del **BIOS** para un modo de vídeo dado. Si el mapa de bit es alterado, un nuevo modo es definido para soportarlo. Las áreas de datos del **ROM-BIOS** (iniciando en 40:0) retendrán sus definiciones actuales tanto como las funciones correspondientes estén definidas. En otras palabras, las definiciones pueden cambiar a capricho de IBM.

INTERRUPCIONES EN EL 8088

Una interrupción es un microprocesador es la suspensión temporal de la ejecución del proceso que en ese momento realiza el procesador, e inicia la ejecución de otro, que por lo general se conoce como Servidor de la Interrupción. El Controlador de Interrupciones es el encargado de determinar la causa de la interrupción, tomando la acción apropiada y regresando el control al proceso que originalmente fue suspendido. Esto es, se selva es estado actual del sistema en el stack y se salta a una rutina de servicio a la interrupción solicitada, dicha rutina es determinada por el número de la interrupción. Después de que la rutina ha terminado, se realiza un "regreso de interrupción", lo cual causa que el programa que se trabajaba previamente reasuma su ejecución.

Las interrupciones son generalmente causadas por eventos externos al CPU que requieren atención inmediata. El **8088** reserva el primer Kbyte de memoria para almacenar en él la tabla de Vectores de Interrupciones en un formato segmento-desplazamiento (segment-offset). Esto

significa que cada dirección requiere 4 bytes por lo que el 8088 soporta 256 vectores de interrupción. Estos 256 tipos de interrupciones pueden agruparse en tres categorías básicas:

- Internas de Hardware: Generadas por ciertos eventos encontrados durante la ejecución de un programa.
- Externas de Hardware: Realizadas por los controladores de los dispositivos periféricos o por coprocesadores
- Software: Realizadas de manera asíncrona por cualquier programa al ejecutar la simple instrucción INT

Para cada tipo de interrupción hay reservado un vector de interrupción el cual especifica donde se encuentra localizado el programa manejador de interrupciones para ese tipo de interrupción.

El sistema operativo se divide en dos: **ROM-BIOS (Read Only Memory-Basic Input Output System) y DOS (Disk Operating System)**. Las interrupciones 00H a 1FH, son usadas para interrupciones internas de hardware y el . BIOS en tanto que las interrupciones 20H a 3 FH son usadas por el DOS, y el resto, 40H a FFH, está disponible para ser usadas en aplicaciones posteriores.

La forma en que las funciones del sistema operativo son accesadas en el **DOS** a través de interrupciones de software. Cada interrupción accesa a una categoría específica de funciones y éstas son determinadas por el valor del registro AH. Si se necesita información adicional, ésta es pasada en los registros **AL, BX, CX y DX**.

INTERRUPCIONES EN EL ROM-BIOS

Cada una de las interrupciones en le **ROM-BIOS** está asociada con un número de opciones que pueden ser accesadas dependiendo del valor contenido en el registro **AH** al momento de ser solicitada la interrupción. La lista completa de las interrupciones el **BIOS** se da en la tabla 1.

INTERRUPCIONES EN EL DOS

La parte del sistema operativo que es cargada y ejecutada por el cargador del **ROM-BIOS** es llamada **DOS**. Contiene varias funciones que la mayor parte de las veces sonde un nivel mucho más alto que las rutinas de **ROM-BIOS** (hay un cierto traslape sin embargo). Todas las funciones del **DOS** son accesadas a través de la interrupción 21H. La cual usa el registro AH para pasar el número de funciones requerido por el **DOS**. En la tabla 2 se muestran las principales funciones de la interrupción 21H de **DOS**.

RUTINAS DEL BIOS DE DIAGNOSTICO

En este momento ya tenemos los elementos necesarios para poder emplear algunas de las rutinas del **BIOS** más importantes y que nos permitirán realizar algunos diagnósticos sobre el funcionamiento de la computadora. Para ello se diseñará un pequeño programa que maneje algunas de las interrupciones dadas en las tablas 1 y 2, evidentemente no es posible realizar el análisis de todas las que se plantean en dichas tablas, por lo que se ha echo una selección de aquellas que sean más representativas del uso y manejo de las interrupciones.

BIBLIOGRAFÍA

Schildt Herbert C:THE COMPLETE REFERENCE Mc Graw Hill. USA, 1987

BYTE. Inside the IBM Pcs Fourth Annual Apecial Issue Byte- Mc Graw Hill, Volumen 12, Number 12, 1987

Norton, Peter. Programmer's Guide to the IBM PV. Microsoft Press

Los_Virus_Informáticos. UNAM CACAFI, MÉXICO,

THE 8086 REGISTERS

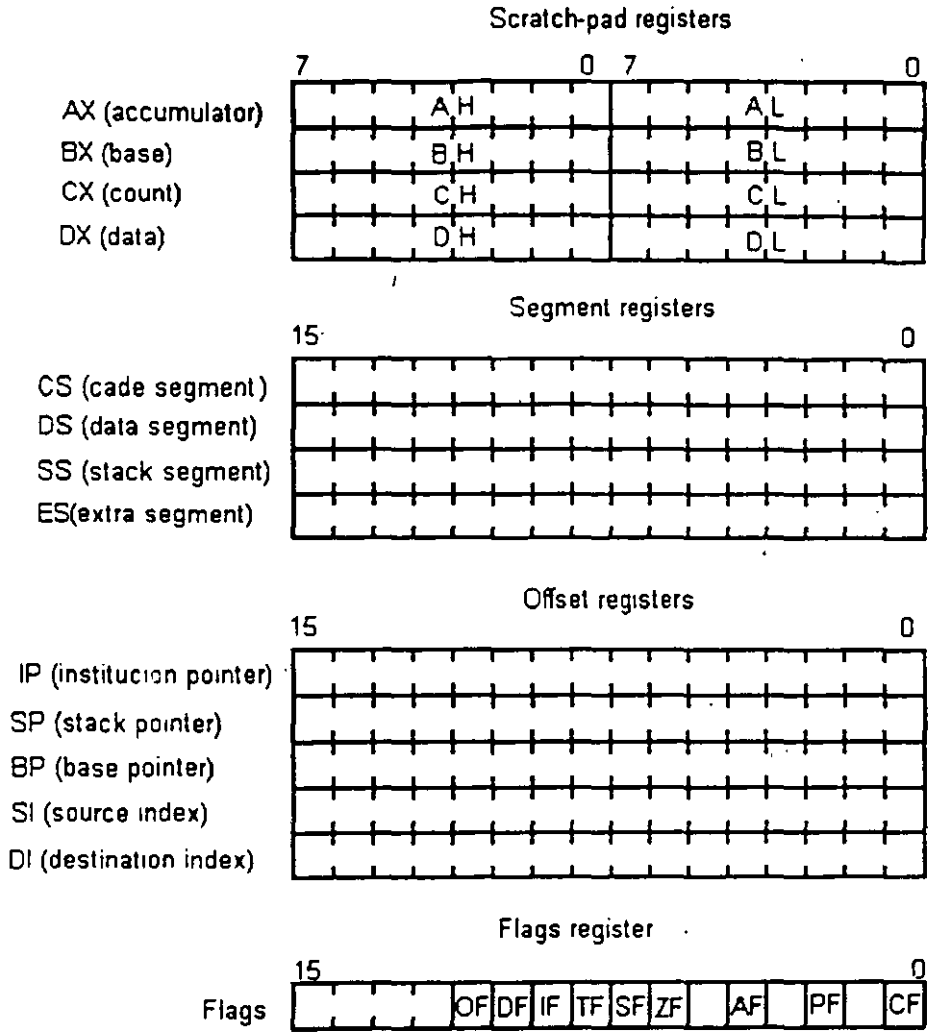


Figure 2.5 the 8086 register and flags

8088
8-BIT HMOS MICROPROCESSOR
8088/8088-2

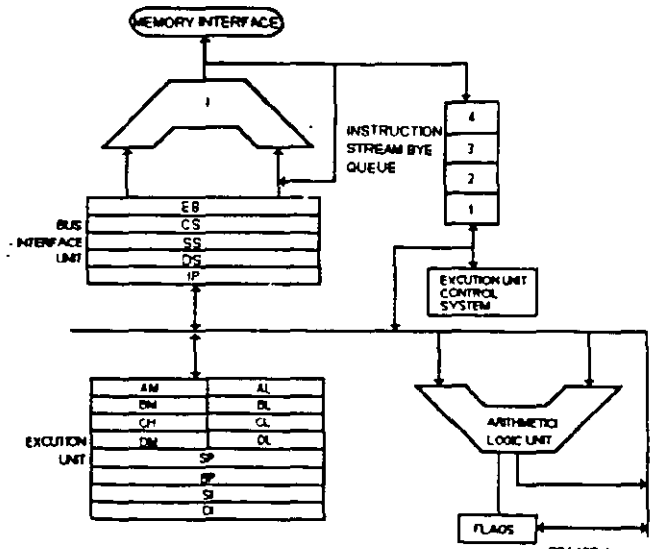


Figure 1 8088 CPU Functional BLock Diagram

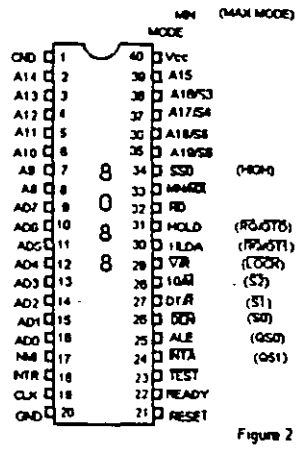


Figure 2 8088 Pin Configura

SECUENCIA POST (POWER ON-SELF TEST) DEL MICROPROCESADOR 8088

- **1.**- Recibe la señal de **POWER GOOD.**
- **2.**- Genera señal de **RESET** al pin 21 del **8088** o del procesador.
- **3.**- Los registros **DS, ES, SS e IP** son puestos a cero, **CS** apunta a **OFFFOh.**
- **4.**- En **OFFFOh** se ejecuta la autoprueba.
- **5.**- Se prohiben las interrupciones.
- **6.**- Se colocan las banderas a 1, y se escribe y lee en los registros.
- **7.**- Se ejecuta el **CHECKSUM** del **BIOS.**
- **8.**- Se inicializan los **8253 y 8237**.
- **9.**- Si el arranque es **WARM** se salta la prueba de memoria.
- **10.**- Se prueban **16KB** de **RAM** con 5 secuencias diferentes.
- **11.**- Se inicializa el **8259** (quién ordena las interrupciones).
- **12.**- Se verifica el **8253**.
- **13.**- Se inicializa el controlador de vídeo (p.e. **6845**) y se prueba la memoria de vídeo.
- **14.**- Aparece el cursor.
- **15.**- Comprueba si existe algo en las ranuras de expansión y comprueba el bus de datos y de direcciones.
- **16.**- Comprueba el resto de la **RAM**.
- **17.**- Comprueba el teclado (que no este pegada alguna tecla, que esté vacio el buffer y coloca el vector de interrupciones).
- **18.**- Busca **ROM** opcional.
- **19.**- Busca las unidades de disco (mediante los **DIPS SW**).
- **20.**- Comprueba los puertos **LPTn y COMn**, almacena las direcciones validas.
- **21.**- Habilita las **NMI**
- **22.**- Sonido por altavoz.
- **23.**- Llama a **INT 19h** (unidad de disco).
- **24.**- Stand by.

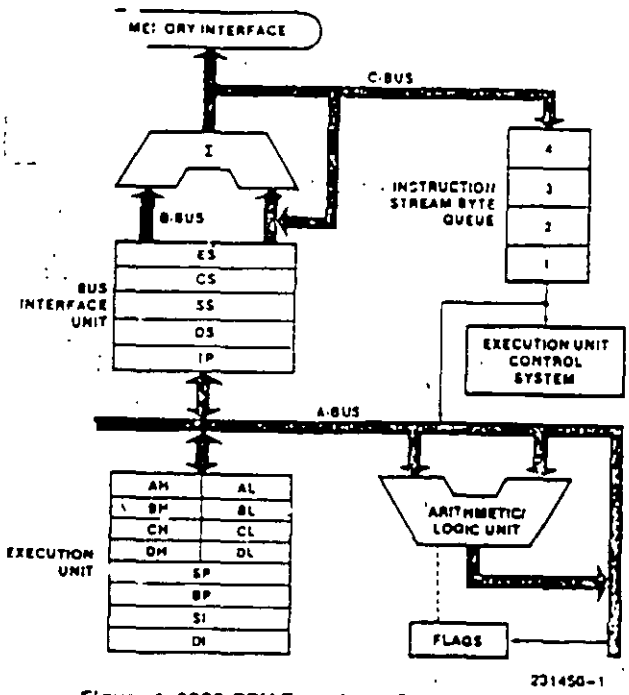


Figure 1. 8088 CPU Functional Clock Diagram

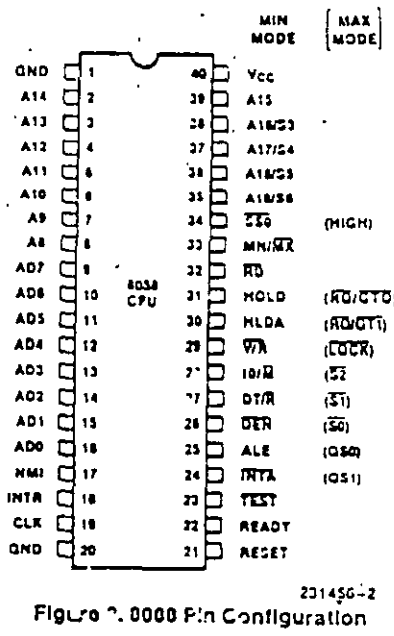
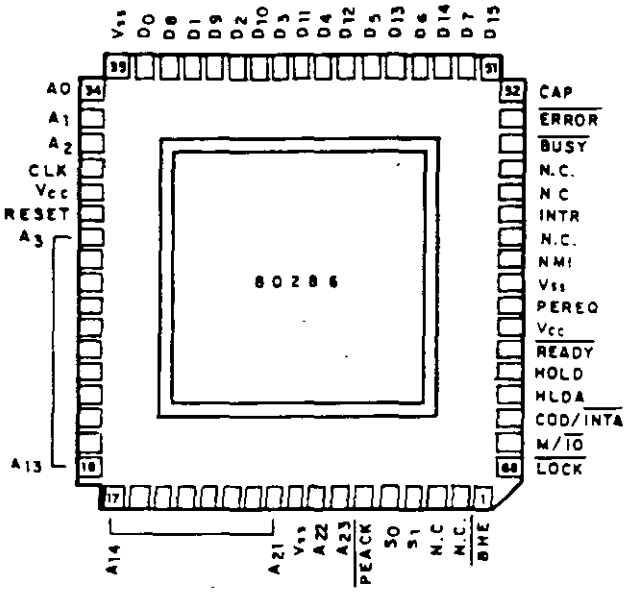
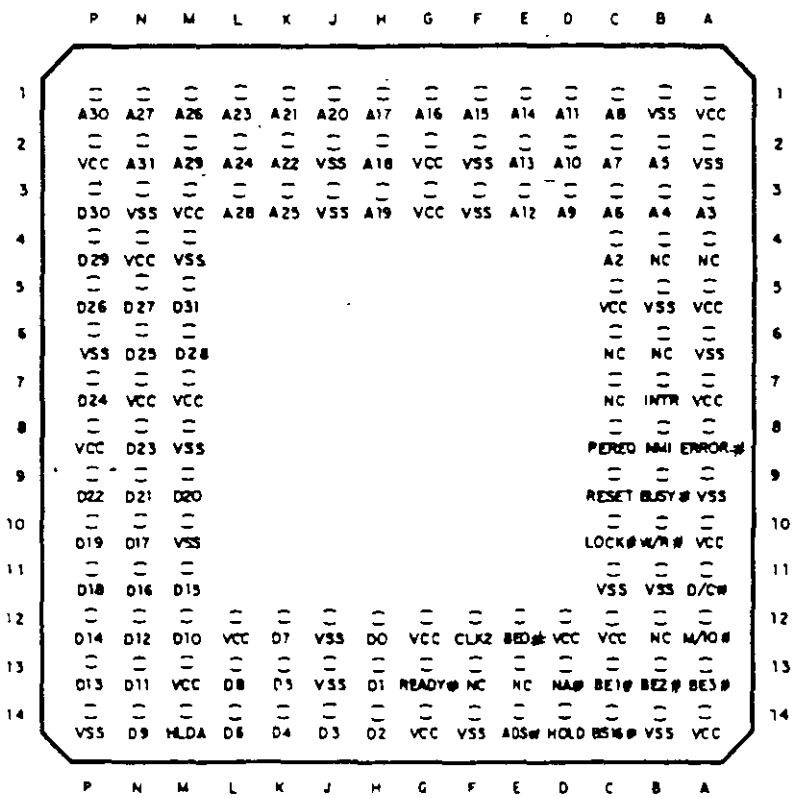


Figure 2. 8088 Pin Configuration



Distribución y denominación de las 68 patitas del 80286, el cual se fabrica en serie con encapsulado de matriz de patitas PGA



Distribución matricial de las 132 patitas del 80386

MOTOROLA

MC14000UB

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

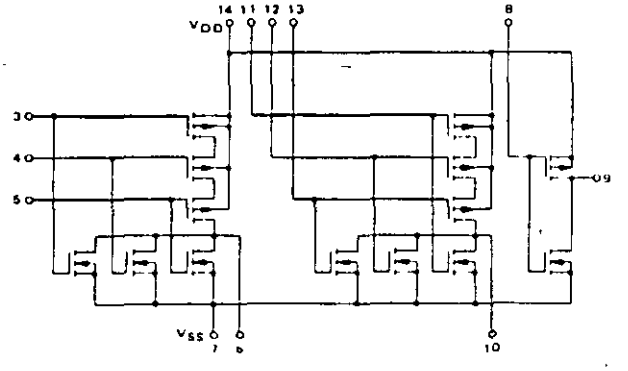
The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin for-Pin Replacement for CD4000UB

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

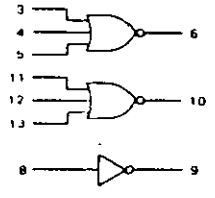
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage — 0 Level	V_{OL}	5.0		0.05		0	0.05		0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05		0	0.05	–	0.05	
		15	–	0.05		0	0.05	–	0.05	
1 Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95		9.95	10		9.95		
		15	14.95	–	14.95	15		14.95		
Input Voltage* — 0 Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0		1.0		2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10		2.0		4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15		2.5		6.75	2.5	–	2.5	
1 Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0		4.0	2.75	–	4.0		Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50		8.0		
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25		12.5		
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2		-1.0	-1.7		-0.7		
(V_{OH} = 4.6 Vdc)		5.0	-0.25		-0.2	-0.36	–	-0.14		
(V_{OH} = 9.5 Vdc)		10	-0.62		-0.5	-0.9		-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8		-1.5	-2.5		-1.1		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88	–	0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25	–	0.9		
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8	–	2.4		
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0		-0.8	-1.7		-0.6		
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36		-0.12		
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9		-0.3		
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-2.5		-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88		0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25		0.9		
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8		2.4		
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5			pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25		0.0005	0.25		7.5	µAdc
		10		0.50		0.0010	0.50	–	15.0	
		15		1.00		0.0015	1.00		30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0		1.0		0.0005	1.0		7.5	µAdc
		10	–	2.0		0.0010	2.0		15.0	
		15		4.0		0.0015	4.0		30.0	
Total Supply Current**,‡ (Dynamic plus Quiescent Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Noise immunity specified for worst case input combination
Noise Margin for both "1" and "0" level =
0.8 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

‡To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

where I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz, is input frequency and N is number of gates per package

**The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	t_{PHL}	5.0	–	115	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

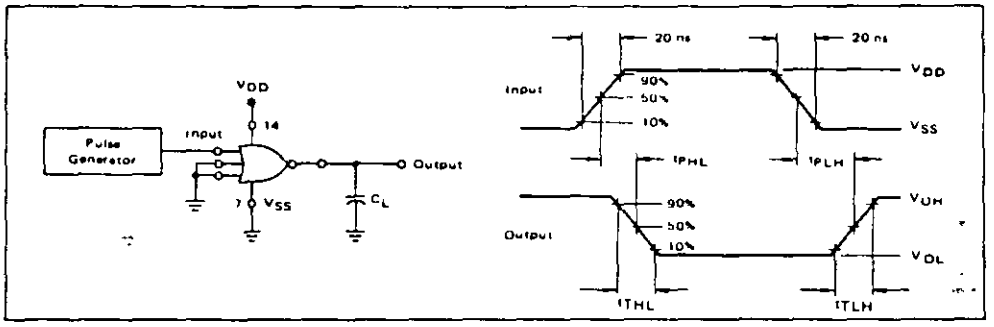


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

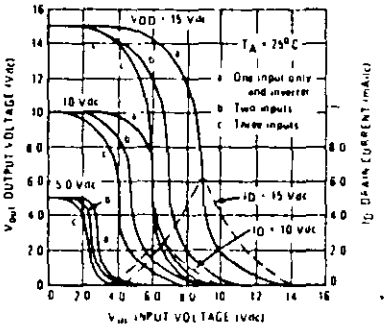
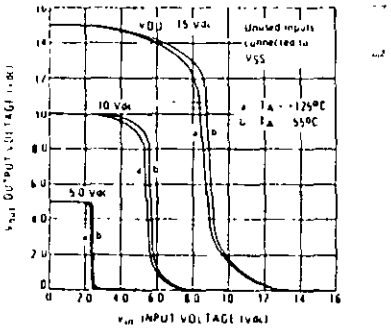
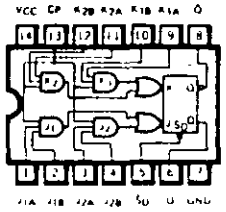


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

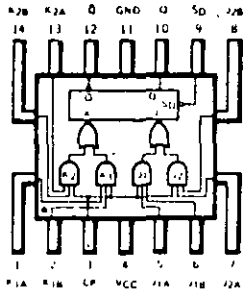


LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



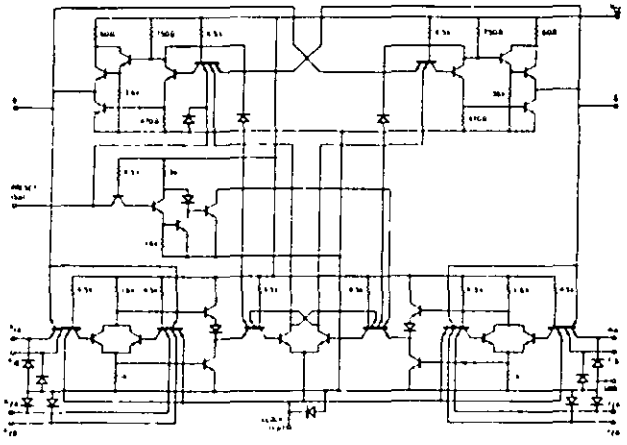
(a)

TRUTH TABLE

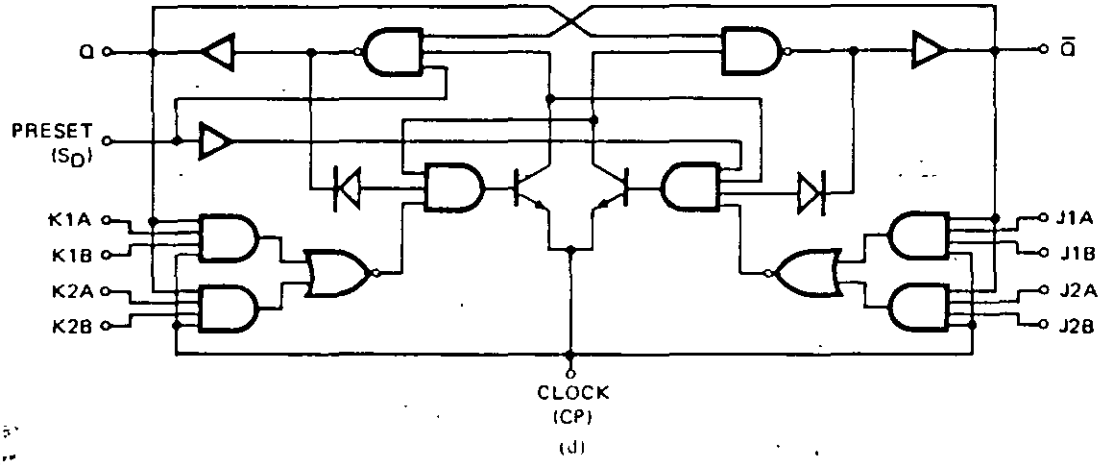
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
J = (J1A·J1B) + (J2A·J2B)
K = (K1A·K1B) + (K2A·K2B)
t_n = Bit time before clock
t_{n+1} = Bit time after clock pulse

(b)



(c)



(d)

Figure 10-76. Characteristics of a 54H101 *JK* edge-triggered flip-flop with AND-OR inputs (a) Connection diagram (b) Truth table (c) Schematic diagram. (d) Logic diagram (Courtesy Fairchild Semiconductor, Inc.)

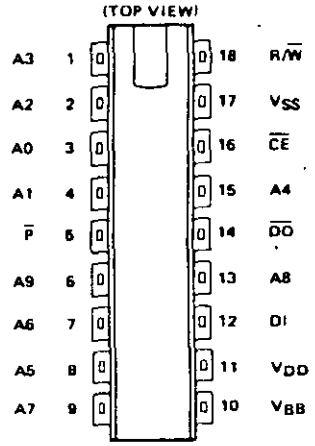
MOS
LSI

TMS 1103 JL, NL; TMS 1103-1 JL, NL
1024-BIT DYNAMIC RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7512234, JANUARY 1975

- 1024 x 1-Bit Organization
- Low Power Dissipation
- Input Interface
  - Fully Decoded, On-Chip Address Decode
  - Static Charge Protection
- Output Interface
  - OR-Tie Capability
- Address Access Time
  - TMS 1103 JL, NL . . . 300 ns
  - TMS 1103-1 JL, NL . . . 150 ns
- P-Channel Silicon-Gate Technology
- 18-Pin 300-Mil Dual-In-Line Packages

18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 1103 JL, NL and TMS 1103-1 JL, NL are monolithic random-access memory devices organized as 1024 one-bit words. Outputs may be OR-tied for simple memory expansion since a particular device can be activated by a chip enable signal. Stored information is read nondestructively and all cells in any row are refreshed by addressing that row at least once every 2 milliseconds for the TMS 1103, 1-millisecond for the TMS 1103-1. These RAMs are fabricated with P-channel silicon-gate enhancement-type technology. Two power supplies and three control clock signals are required with address inputs decoded on the chip. The TMS 1103-1 is a faster-access version of the TMS 1103 with improved cycle times. The TMS 1103 and TMS 1103-1 are offered in both 18-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages.

operation

addresses (A0-A9)

Address terminals are used to activate a particular cell in a 32 x 32 array. Each row address (A0–A4) and each column address (A5–A9) of 5 bits uniquely specify a 10-bit address for a single memory cell. All address signals must be stable during transitions of the chip-enable, read/write, or data-in control signals.

chip enable ($\overline{CE}$)

The chip enable terminal enables one particular device of an array whose outputs are connected to a common data bus. Chip enable must be low during any read or write interval to allow data to enter or exit.

precharge ($\overline{P}$)

The precharge terminal must be low at the start of any read or write cycle and remain low for a specified time interval after chip enable drops to a low. This overlap interval must be maintained between a specified minimum and maximum time in order to maintain the integrity of stored data.

read/write (R/$\overline{W}$)

The read/write input terminal gates data out of or into the addressed memory cell. Read/write is low when data is written and high during a read interval.

data in (DI)

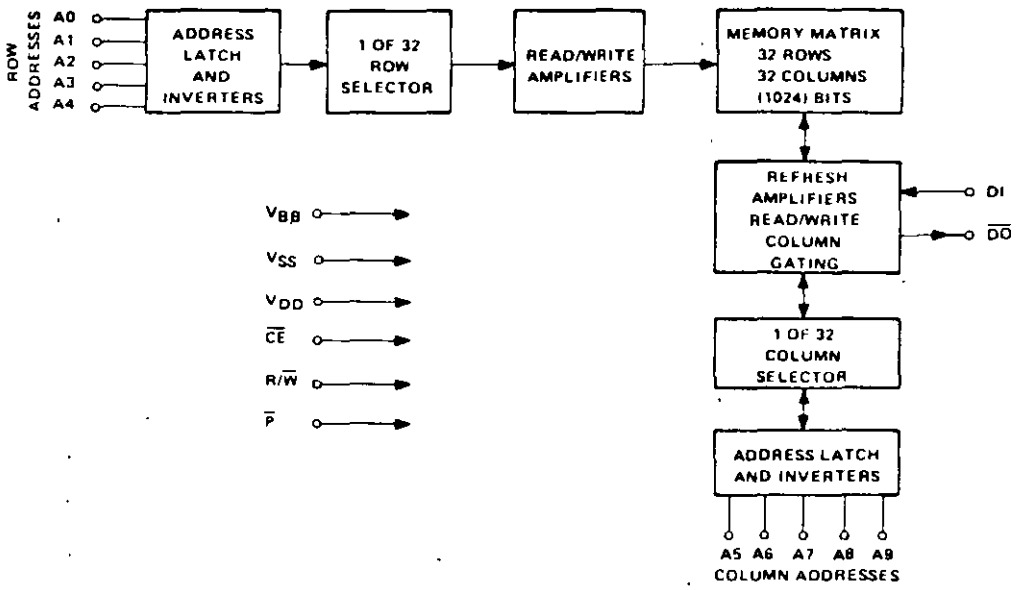
The data-in terminal connects the incoming data bus to the addressed cell for a write operation.

data out ($\overline{DO}$)

Stored data appears at the data out terminal as the complement of the data-in logic level. Information on the data out terminal is sensed just prior to the rise of chip enable in a read only cycle and prior to the fall of read/write in a read-modify-write cycle.

Figure 11-41. Manufacturer's data sheets for TMS 1103 MOS 1024 bit dynamic random access memory (Courtesy Texas Instruments, Inc.)

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)		−25 to 0.3 V
Supply voltage, V_{SS} (see Note 1)		−25 to 0.3 V
Input voltage (any input)		−25 to 0.3 V
Continuous power dissipation		1 W
Operating free-air temperature range	TMS 1103	0°C to 70°C
	TMS 1103-1	0°C to 55°C
Storage temperature range		−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most positive supply voltage V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{DD}.

recommended operating conditions

PARAMETER	TMS 1103			TMS 1103-1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		0			0		V
Supply voltage, V_{SS}	15.2	16	16.8	18	19	20	V
Supply voltage, $V_{BB} - V_{SS}$ (see Note 2)	3		4	3		4	V
Operating free-air temperature, T_A	0		70	0		55	C

NOTE 2: $V_{BB} - V_{SS}$ supply should be applied at the same time as or before V_{SS}.

Figure 11-41 — (*continued*)

Figure 11-41 — (*continued*)

electrical characteristics at specified free-air temperatures
V_{SS} = 16.8 V, ($V_{BB}-V_{SS}$) = 3 V, V_{DD} = 0 V (TMS 1103 JL, NL)
V_{SS} = 20 V, ($V_{BB}-V_{SS}$) = 3 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

PARAMETER			TEST CONDITIONS†		TMS 1103			TMS 1103-1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		T_A = MIN		V_{SS} −1		V_{SS} +1	V_{SS} −1		V_{SS} +1	V
			T_A = MAX		V_{SS} −0.7		V_{SS} +1	V_{SS} −1		V_{SS} +1	
V_{IL}	Low-level input voltage (all addresses and data-in lines)		T_A = MIN		V_{SS} −17		V_{SS} −14.2	V_{SS} −20		V_{SS} −18	V
			T_A = MAX		V_{SS} −17		V_{SS} −14.5	V_{SS} −20		V_{SS} −18	
V_{IL}	Low-level input voltage (precharge, chip enable, and read/write input) (see Note 3)		T_A = MIN		V_{SS} −17		V_{SS} −14.7	V_{SS} −20		V_{SS} −18	V
			T_A = MAX		V_{SS} −17		V_{SS} −15	V_{SS} −20		V_{SS} −18	
V_{OH}	High-level output voltage		R_L = 100 Ω,	T_A = 25°C	60	90	500	115	130	900	mV
			R_L = 100 Ω,	T_A = MAX	50	80	500	90	115	900	
I_I	Input current		V_I = 0 V,	T_A = MIN to MAX			1			10	μA
I_{OH}	High-level output current		R_L = 100 Ω,	T_A = 25°C	600	900	5000	1150	1130	9000	μA
			R_L = 100 Ω,	T_A = MAX	500	800	5000	900	1150	9000	
$I_{O(off)}$	Off-state output current		V_O = 0 V,	T_A = MIN to MAX			1			10	μA
I_{BB}	Supply current from V_{BB}		T_A = MIN to MAX				100			100	μA
$I_{DD(1)}$	Supply current from V_{DD} during precharge pulse width		All addresses = 0 V, $\overline{CE}$ at V_{SS}, V_I = V_{SS} Precharge = 0 V,	T_A = 25°C		37	56		45	60	mA
$I_{DD(2)}$	Supply current from V_{DD} during precharge and chip-enable overlap		All addresses = 0 V, $\overline{CE}$ at 0 V, V_I = V_{SS} Precharge = 0 V,	T_A = 25°C		38	59		50	68	mA
$I_{DD(3)}$	Supply current from V_{DD} during precharge to end of chip enable		Precharge = V_{SS}, T_A = 25°C	$\overline{CE}$ at 0 V, V_I = V_{SS}		5.5	11		8.5	11	μA
$I_{DD(4)}$	Supply current from V_{DD} during chip enable to precharge delay		Precharge = V_{SS}, T_A = 25°C	$\overline{CE}$ at V_{SS}, V_I = V_{SS}		3	4		3	4	mA
$I_{DD(av)}$	Average supply current from V_{DD}	TMS 1103	$t_{w(P)}$ = 190 ns, T_A = 25°C	t_c = 580 ns,		17	25		20	23	mA
		TMS 1103-1	$t_{w(P)}$ = 105 ns, T_A = 25°C	t_c = 340 ns							

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at T_A = 25°C.

NOTE 3: The maximum values for V_{IL} for precharge, chip enable, and read/write of the TMS 1103 may be increased to V_{SS} − 14.2 V at 0°C and V_{SS} − 14.5 V at 70°C (same values as those specified for the address and data-in lines) with a 40 ns degradation (worst case) in $t_{su(a0\ \overline{CE})}$, $t_{d(\overline{P}L\ \overline{CE}L)}$, $t_{c(rd)}$, $t_{c(RW)}$, $t_{a(ad)}$, and $t_{a(\overline{P})}$.

TMS 1103 JL, NL; TMS 1103-1 JL, NL
1024-BIT DYNAMIC RANDOM-ACCESS MEMORIES

dynamic electrical characteristics over operating free-air temperature range (unless otherwise noted)

T_A = 0°C to 70°C, V_{SS} = 16 V ± 5%, ($V_{BB} - V_{SS}$) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103 JL, NL)

T_A = 0°C to 55°C, V_{SS} = 19 V ± 5%, ($V_{BB} - V_{SS}$) = 3 V to 4 V, V_{DD} = 0 V (TMS 1103-1 JL, NL)

capacitance at 25°C free-air temperature

CHARACTERISTICS		TEST CONDITIONS†	PLASTIC PKG		CERAMIC PKG		UNIT
			TYP	MAX	TYP	MAX	
$C_{i(ad)}$	Address input capacitance	$V_I = V_{SS}$	5	7	10	12	pF
$C_{i(\overline{P})}$	Precharge input capacitance	$V_I = V_{SS}$	15	18	16.5	19.5	pF
$C_{i(\overline{CE})}$	Chip-enable input capacitance	$V_I = V_{SS}$	15	18	18	21	pF
$C_{i(R/\overline{W})}$	Read/write input capacitance	$V_I = V_{SS}$	11	15	15.5	19.5	pF
$C_{i(da)}$	Data input capacitance	$\overline{CE}$ at 0 V, $V_I = V_{SS}$	4	5	6.5	7.5	pF
		$\overline{CE}$ at V_{SS}, $V_I = V_{SS}$	2	4	5.6	6.5	
C_o	Data output capacitance	V_O = 0 V	2	3	6	7	pF

†f = 1 MHz, and all unused pins are at ac ground.

read, write, and read, modify write cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rfsh)}$	Refresh cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)		2		1	ms
$t_{su(ad-\overline{CE})}$	Address-to-chip-enable setup time		115		30		ns
$t_{h(\overline{CE}-ad)}$	Chip-enable-to-address hold time		20		10		ns
$t_{d(\overline{P}L-\overline{CE}L)}$	Precharge low to chip-enable low delay time		125		60		ns
$t_{d(\overline{CE}H-\overline{P}L)}$	Chip-enable high to precharge low delay time		85		40		ns
$t_{d(\overline{CE}L-\overline{P}H)1}$	Chip-enable low to precharge high delay time between low reference points		25	75	5	30	ns
$t_{d(\overline{CE}L-\overline{P}H)2}$	Chip-enable low to precharge high delay time between high reference points			140		85	ns

read cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)	480		300		ns
$t_{d(\overline{P}H-\overline{CE}H)}$	Precharge high to chip-enable high delay time		165	500	115	500	ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time			120		75	ns
$t_{a(ad)}$	Access time from address (see Note 4)		300		150		ns
$t_{a(\overline{P})}$	Access time from precharge (see Note 5)		310		180		ns

NOTES

4. $t_{a(ad)} = t_{su(ad\ \overline{CE})} + t_{f(\overline{CE})} + t_{d(\overline{CE}L-\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.
5. $t_{a(\overline{P})} = t_{d(\overline{P}L-\overline{CE}L)} + t_{f(\overline{CE})} + t_{d(\overline{CE}L-\overline{P}H)1} + t_{r(\overline{P})} + t_{p(\overline{P}H)}$.

write or read, modify write cycle

PARAMETER		TEST CONDITIONS	TMS 1103		TMS 1103-1		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	$t_r = t_f$ = 20 ns, C_L = 100 pF (1103), C_L = 50 pF (1103-1), R_L = 100 Ω, v_{ref} = 40 mV (1103), v_{ref} = 80 mV (1103-1)	580		340		ns
$t_{c(R/MW)}$	Read, modify write cycle time		580		340		ns
$t_{d(\overline{P}H-wr)}$	Precharge high to write delay time		165	500	115	500	ns
$t_{w(wr)}$	Write pulse width		50		20		ns
$t_{su(wr)}$	Write setup time		80		20		ns
$t_{su(da)}$	Data setup time		105		40		ns
$t_{h(da)}$	Data hold time		10		10		ns
$t_{p(\overline{P}H)}$	Precharge high to output propagation delay time			120		75	ns
$t_{d(wr-\overline{CE}H)}$	Write to chip-enable high delay time		0		0		ns

Figure 11-41 — (*continued*)

National Semiconductor

DM5401/DM7401 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

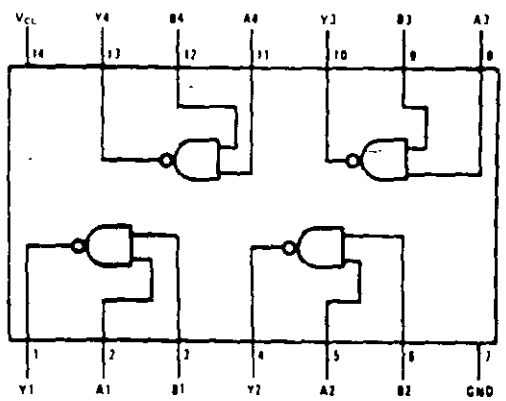
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6814-1

Order Number DM5401J, DM5401W or DM7401N
See NS Package Number J14A, N14A or W14B

Function Table

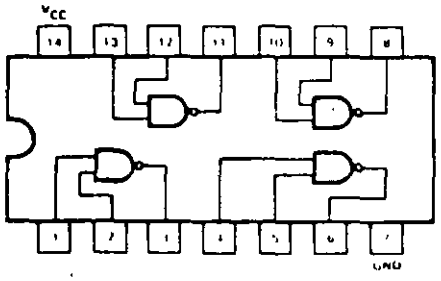
$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS00X	4.5 V	5.0 V	5.5 V	-55°C to 125°C
SN74LS00X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type. W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = -400 µA V_{IN} V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN I_{OL} 4.0 mA V_{IN} 2.0 V
		74		0.35	0.5	V	V_{CC} MIN, I_{OL} 8.0 mA V_{IN} 2.0 V
I_{IH}	Input HIGH Current			1.0	20	µA	V_{CC} MAX V_{IN} 2.7 V
					0.1	mA	V_{CC} MAX V_{IN} = 10 V
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		-15		100	mA	V_{CC} MAX V_{OUT} 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} MAX V_{IN} 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} MAX Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} 5.0 V
t_{PHL}	Turn On Delay Input to Output		5.0	10	ns	C_L = 15 pF

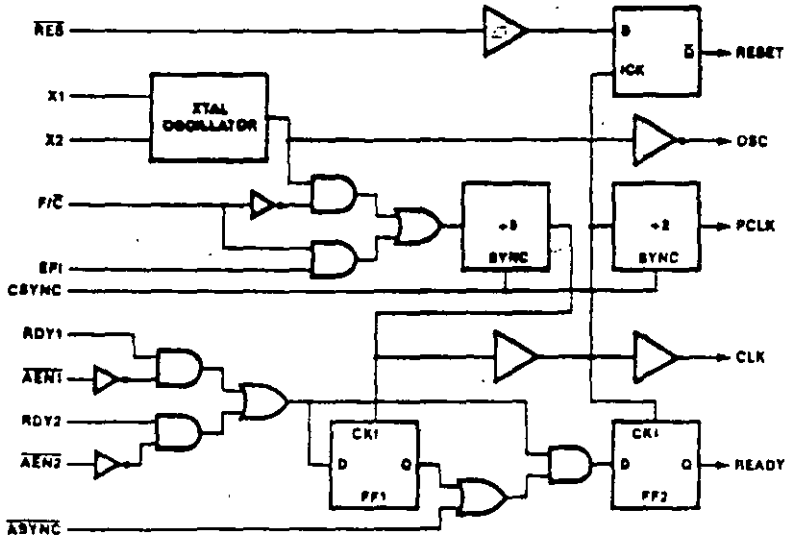
NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C
3. Not more than one output should be shorted at a time.

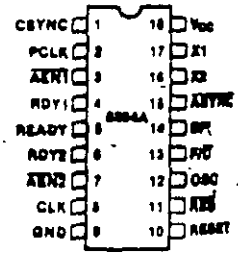
intel

8284A/8284A-1
CLOCK GENERATOR AND DRIVER FOR iAPX 86, 88 PROCESSORS

- Generates the System Clock for the iAPX 86, 88 Processors:
  5 MHz, 8 MHz with 8284A
  10 MHz with 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and MULTIBUS® READY Synchronization
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other 8284As
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range



8284A/8284A-1 Block Diagram



8284A/8284A-1 Pin Configuration

GENERADOR DE RELOJ

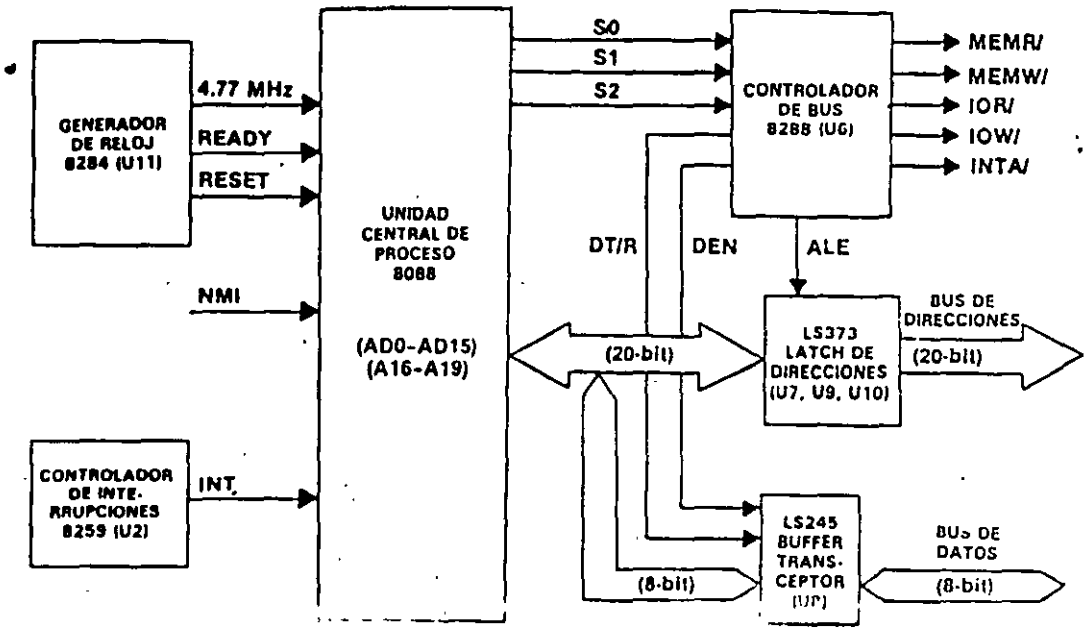


Fig. 2.8. *La UCP 8088 y el circuito asociado.*

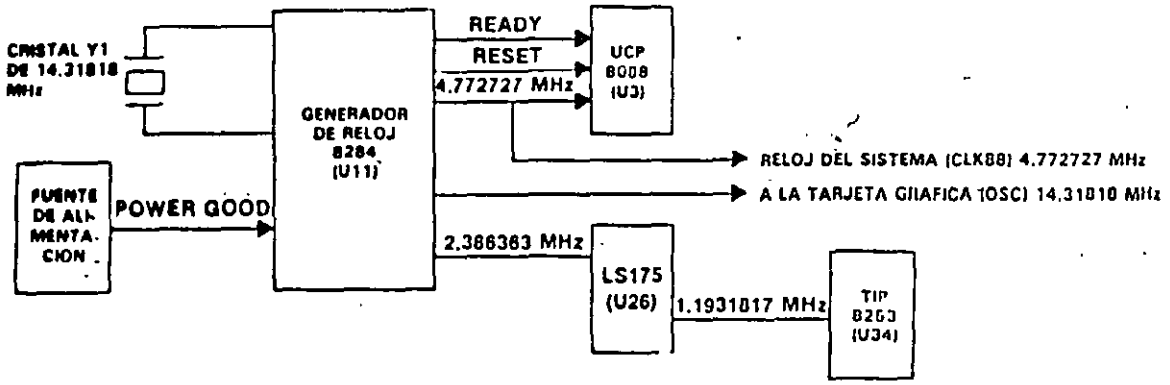


Fig. 2.9. *El circuito de reloj del IBM PC.*

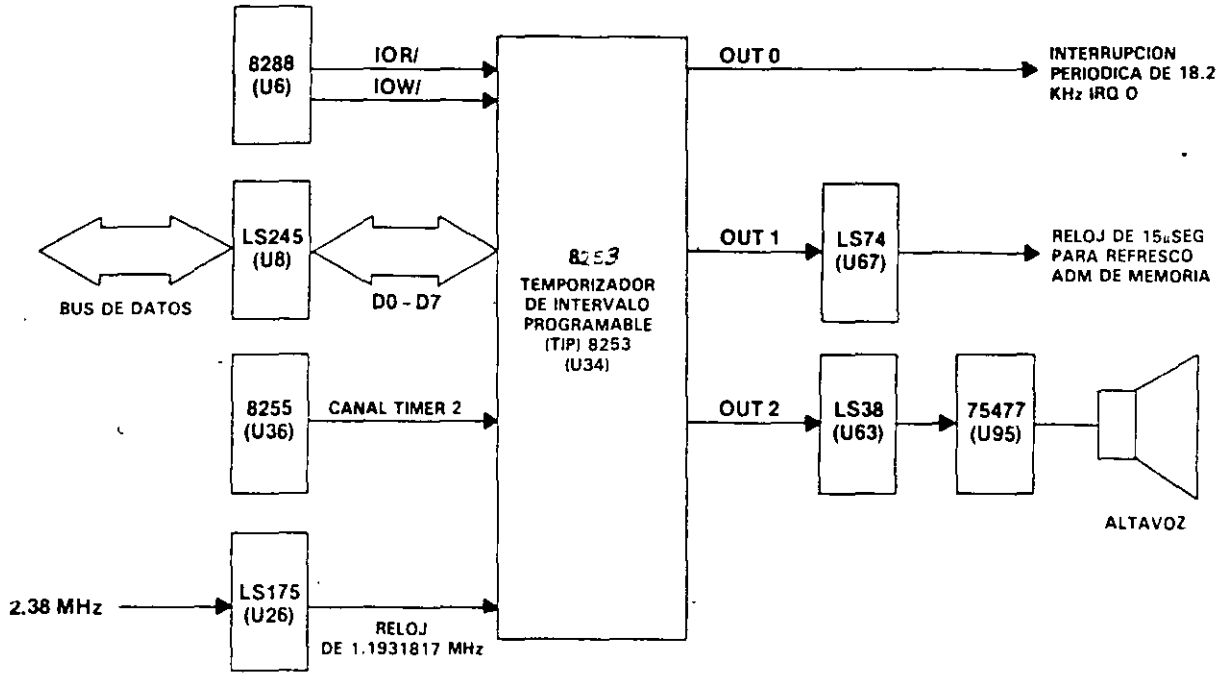
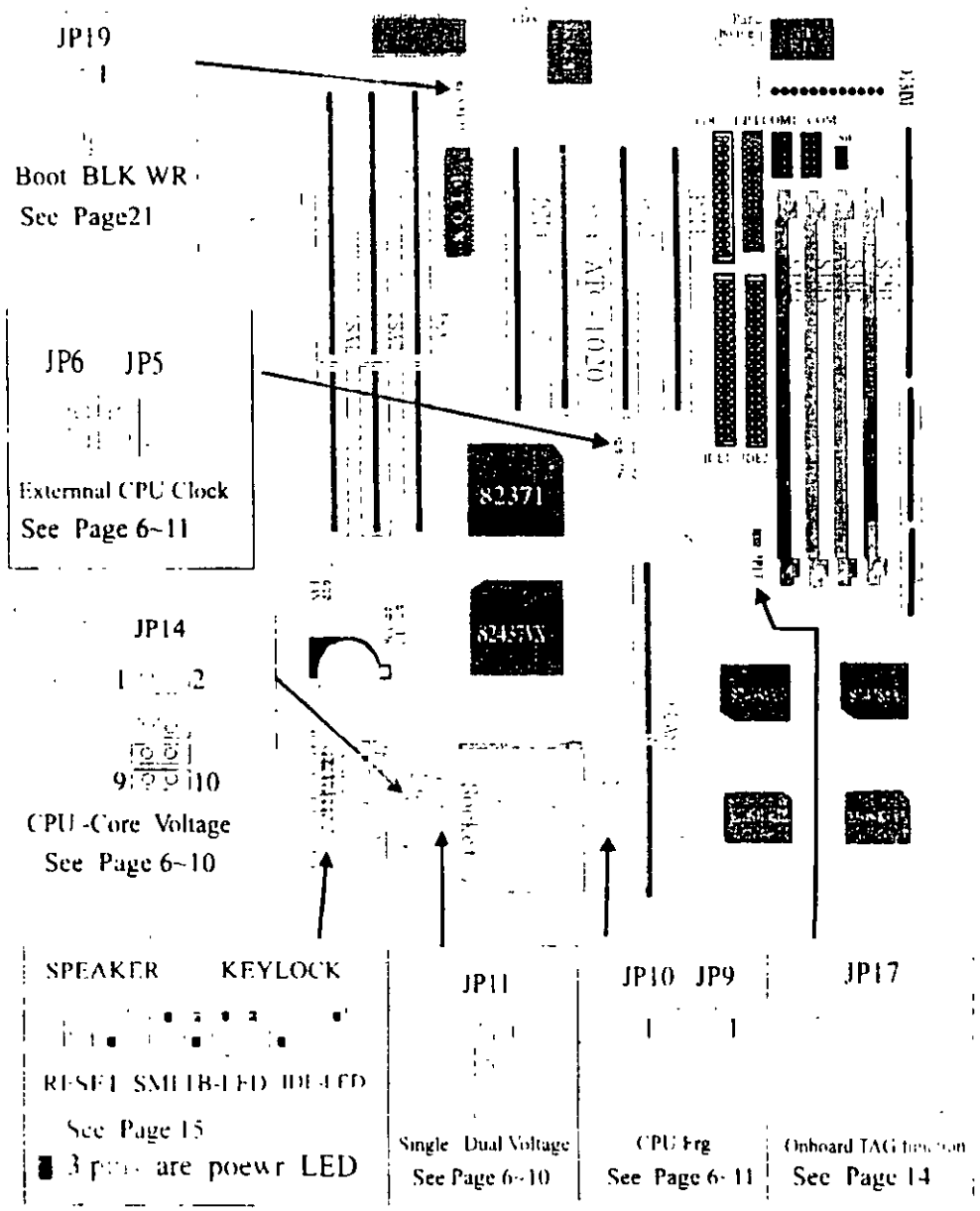


Fig. 2.12. *El circuito del temporizador de intervalo programable (TIP) 8253.*

ATC-1020 Intel 430VX Mainboard
Component Location Diagram



A

1- YSTEM FEATURES

- Pentium level CPU operating at 75 MHz to 200MHz with 321-pin ZIF socket 7 and scalability to accept processor in the future
- INTEL 82430VX PCIset
- Using four 72-pin SIM sockets, provides two banks of 64-bit wide path up to 128MB addressing page mode DRAMs.
- Supporting two types of DRAM including EDO (Extended Data Out), or FPM (Fast Page Mode)
- Supporting four PCI bus master revision 2 1, 5V interface compliant and three 16-bit ISA slots.
- Dual Master IDE connectors support up to four devices in two channels for connection of high capacity hard disk drive, CD-ROM, tape backup etc
- AT style keyboard connector and PS/2 mouse connector
- Winbond 83877 high-speed Multi-I/O chipset.
- Supporting Infrared transfer (IrDA TX/RX) connection
- One FDC port supports two devices up to 2 88MB
- Two 16550A fast UARTs compatiable serial ports
- One EPP/ECP mode parallel port
- Hardware Dimension is 220mm x 280mm (8.66" x 11.02") with four layers designed

2-2 CPU INSTALLATION

ATC-1020 supports Pentium level CPU up to 200MHz For installation, please notice CPU pin 1 must align with the ZIF socket 7 Pin 1 location Before you install or upgrade your CPU, please read CPU guide from CPU manufacturer to make sure the CPU voltage specification. Then choose the right installation in the 2-2-1 based on your CPU type/brand and follow the description to setup jumpers. If your CPU is not in the list of 2-2-1, please refer to 2-2-2 and 2-2-3 for installation

2-2-1 CPU TYPE SELECTION

A. INTEL PENTIUM CPU (P54C)

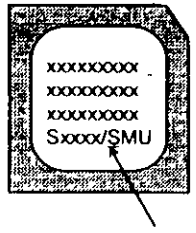
JP11	1-2

CPU Core Voltage	VRE	STD
JP14	1-2**	3-4*

* STD 3 135V ~ 3 600V

** VRE : 3 400V ~ 3 600V
(The fourth line of the mark on the under-side of the processor contains a code that identifies the voltage level type V is VRE, S is standard.)

Intel Pentium CPU, the first letter after '/' denotes voltage type



INTERNAL CPU CLOCK	JP5	JP6	JP9	JP10	Ext x Frq.
75MHz	open	open	1-2	1-2	50x1.5
90MHz	open	close	1-2	1-2	60x1 5
100MHz	close	open	1-2	1-2	66x1 5
120MHz	open	close	1-2	2-3	60x2 0
133MHz	close	open	1-2	2-3	66x2 0
150MHz	open	close	2-3	2-3	60x2 5
166MHz	close	open	2-3	2-3	66x2.5
180MHz	open	close	2-3	1-2	60x3 0
200MHz	close	open	2-3	1-2	66x3.0

B. INTEL PENTIUM CPU (P55C)

Besides CPU clock setting, for P55C (MMX) CPU you have to set JP11,JP14 based on its CPU I/O voltage and core voltage

JP11	2-3

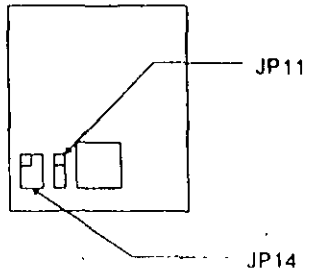
Set 2-3 for dual voltage mode.

CPU Core Voltage	3.5V	3.3V	2.9V	2.8V	2.7V
JP14	1-2	3-4	5-6	7-8	9-10

Currently, Intel P55C is released 2.8V core voltage only. Please confirm this with your system supplier before you install P55C CPU

INTERNAL CPU CLOCK	JP5	JP6	JP9	JP10	Ext.x Frq
166MHz	close	open	2-3	2-3	66x2.5
180MHz	open	close	2-3	1-2	60x3.0
200MHz	close	open	2-3	1-2	66x3.0

※ The location of JP11 and JP14

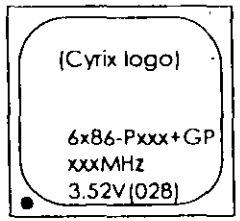


C. Cyrix 6x86/6x86L CPU

※Cyrix 6x86 (028) CPU

CPU	JP11	JP14
Cyrix 6x86 (028)	1-2	1-2

INTERNAL CPU CLOCK	JP5	JP6	JP9	JP10	Ext.x Frq.
PR120+ @ 100MHz	open	.open	1-2	2-3	50x2.0
PR150+ @ 120MHz	open	close	1-2	2-3	60x2.0
PR166+ @ 133MHz	close	open	1-2	2-3	66x2.0

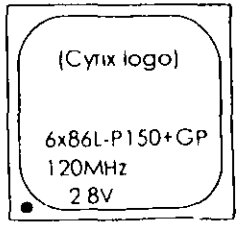


The button line of the mark on the processor contains a code 028 that identifies the voltage level type. If the code is 016 or others, or no marking then please contact your dealer

※Cyrix 6x86L CPU (dual voltage)

CPU	JP11	JP14
Cyrix 6x86L	2-3	7-8

INTERNAL CPU CLOCK	JP5	JP6	JP9	JP10	Ext.x Frq.
PR120+ @ 100MHz	open	open	1-2	2-3	50x2.0
PR133+ @ 110MHz	close	close	1-2	2-3	55x2.0
PR150+ @ 120MHz	open	close	1-2	2-3	60x2.0
PR166+ @ 133MHz	close	open	1-2	2-3	66x2.0



The mark on the processor contains as the sample in the left The code-name 6x86L is dual voltage mode processor, you should set JP11 to 2-3

D. AMD-K5 CPU

CPU	JP11	JP14
AMD K5	1-2	1-2

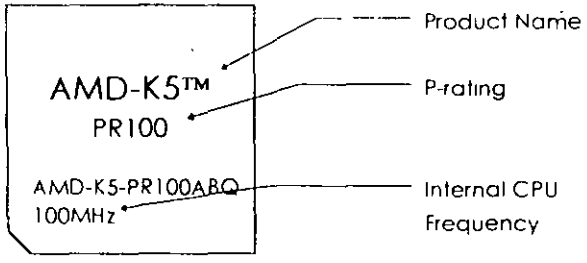
CPU CLOCK RATING	JP5	JP6	JP9	JP10	Ext.x Frq.
PR75ABR 75MHz	open	open	1-2	1-2	50x1 5
PR90ABQ 90MHz	open	close	1-2	1-2	60x1 5
PR100ABQ 100MHz	close	open	1-2	1-2	66x1.5
PR120ABQ 90MHz	open	close	1-2	1-2	60x1.5
PR133ABQ 100MHz	close	open	1-2	1-2	66x1.5
PR166ABQ	close	open	2-3	2-3	66x2.5

E. AMD-K6 CPU

AMD K6-PR166/PR200

JP11	JP14
2-3	5-6

INTERNAL CPU CLOCK	JP5	JP6	JP9	JP10	Ext.x Frq.
AMD K6-PR166	close	open	2-3	2-3	66x2 5
AMD K6-PR200	close	open	2-3	1-2	66x3.0

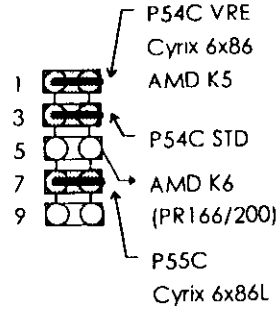


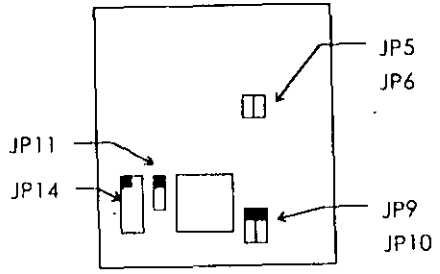
2-2-2 CPU VOLTAGE SETTING

JP11 is for setting single or dual CPU voltage mode. JP14 is used for various CPU voltage value types, please refer to CPU's marking on/under CPU and its user's manual.

CPU MODE	Single	Dual
JP11	 1-2	2-3

CPU CORE VOLTAGE		JP14
INTEL	STD	3-4
(P54C)	VRE	1-2
P55C	2.8V	7-8
Cyrix	6x86(028)	1-2
Cyrix	6x86L	7-8
AMD	K5	1-2
AMD	K6(PR166/200)	5-6



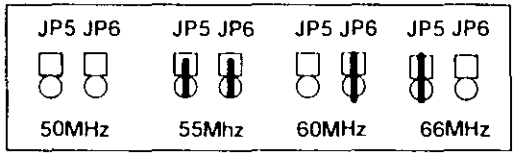


2-2-3 CPU CLOCK SETTING

The following setting is for new release CPUs

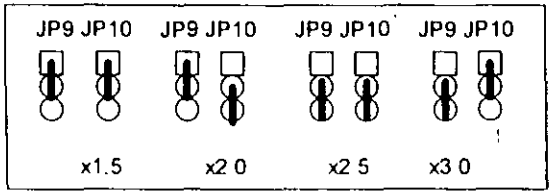
EXTERNAL CPU CLOCK	JP5	JP6
50(MHz)	open	open
55(MHz)	close	close
60(MHz)	open	close
66(MHz)	close	open

External CPU Clock

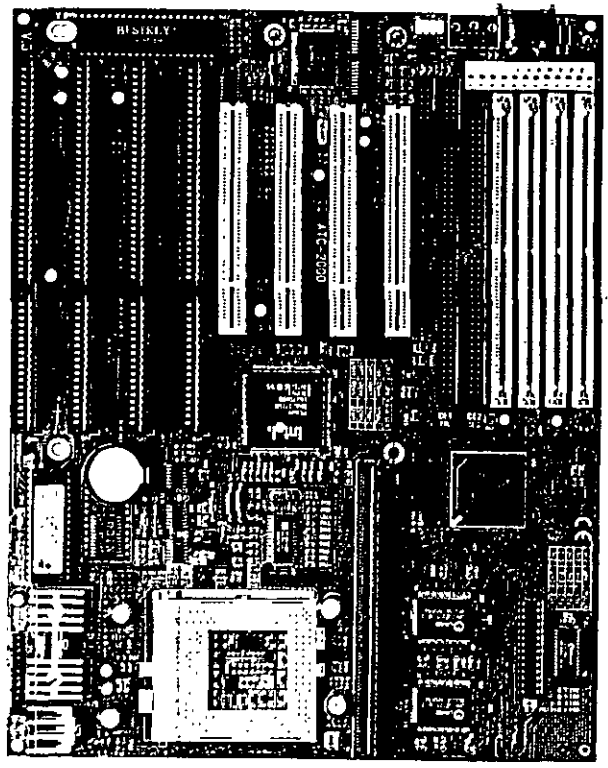


INTERNAL CPU CLOCK	JP9	JP10
INTEL EXTERNAL CLOCK X 1 5	1-2	1-2
INTEL EXTERNAL CLOCK X 2 0	1-2	2-3
INTEL EXTERNAL CLOCK X 2.5	2-3	2-3
INTEL EXTERNAL CLOCK X 3.0	2-3	1-2

Internal CPU Clock :



INTEL 430HX
PCI/ISA Mainboa ·d
User's Manual



P/N : 160-2000R3

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ATC-2000 Intel 430HX Mainboad
Component Location Diagram

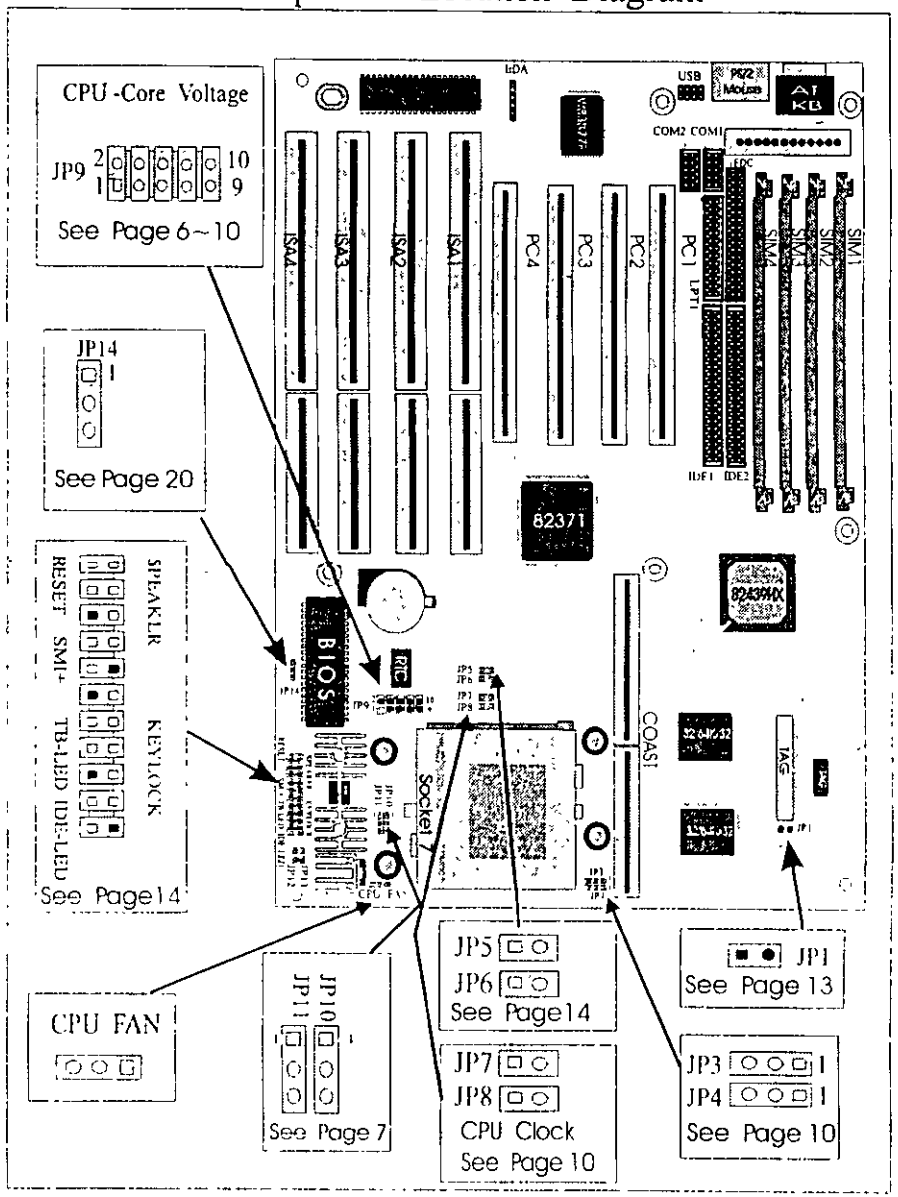

Table of Contents

CHAPTER 1 INTRODUCTION

This manual introduces how to configure the ATC-2000 mainboard for different environments It's an overview of the layout and features of the mainboard, and also provides information for you to change the configuration or system environment.

This manual is divided into two sections .

PART ONE includes page A which contain layout diagram of the mainboard. Please refer it when you configure the system.

PART TWO includes three chapters as following

Chapter 1 is an overview of the mainboard features and packing contents of the mainboard.

Chapter 2 describes how to upgrade and to change hardware configurations such as memory size, CPU type, and lists of jumper settings and connectors

Chapter 3 is the user's guide of AWARD BIOS setup utility, and Flash ROM BIOS update procedure The menu showed in this chapter are default settings.

Your system dealer will set up the mainboard according to your demand of computer. It means that the current settings of your mainboard's current setting may not be the same as the defaults shown in this user's manual. If you need to change your configuration, please ask your dealer firstly, be sure this will not against your system warranty. Or ask for your dealer to do it for you.

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1-1 SYSTEM FEATURES

- P54C, P55C Pentium level CPU operating at 75 MHz to 200MHz with 321-pin ZIF socket 7 and scalability to accept processor in the future.
- INTEL 82430HX PCIset.
- Using four 72-pin SIM sockets, provides two banks of 64-bit wide path up to 256MB addressing page mode DRAMs.
- Supporting all types of DRAM included ECC (Error Checking and Correcting) or parity, EDO (Extended Data Out), BEDO (Burst EDO), or FPM (Fast Page Mode).
- Supporting four PCI bus master revision 2.1, 5V interface compliance and four 16-bit ISA slots.
- Dual Master IDE connectors support up to four devices in two channels for connection of high capacity hard disk drive, CD-ROM drive, tape backup etc..
- Supporting the USB (Universal Serial Bus) connector.
- AT style keyboard connector and PS/2 mouse connector.
- Winbond 83877 high-speed Multi-I/O chipset:
- Supporting Infrared transfer (IrDA TX/RX) connection.
- One FDC port supports two devices up to 2.88MB
- Two 16550A fast UARTs compatiable serial ports
- One EPP/ECP mode parallel port
- Hardware Dimension is 220mm x 280mm (8.66" x 11.02") with four layers designed.

1-2 CHE LIST OF THE PACKING

The mainboard comes securely packed in a durable box and shipping carton. If any of the above items are missed or damaged, please contact your supplier.

Each mainboard containing:

Q'TY	Description	
1	Mainboard	: ATC-2000.
1	Diskette	. Enhanced IDE driver (3.5").
1	Cable	. Enhanced IDE connector
1	Cable	. F.D D connector.
1	Cable	· Serial port.
1	Cable	: Serial/Parallel
1	Manual	: User's manual

NOTE : Leave the mainboard in its original packing until you are ready to install it.

CHAPTER 2 INSTALLATION

2-1 INSTALLATION PROCEDURE

Before installing the computer, please prepare all components such as CPU, DRAM; peripherals such as hard disk drive, keyboard, CD-ROM drive; and accessories such as cables. Then, install the system as following .

1. Plug CPU (w/ heat sink and cooling fan), DRAM modules in the mainboard.
2. Set jumpers based on your configuration.
3. Plug add-on cards in PCI or ISA slots.
4. Connect cables to peripherals, power supply .
5. Make sure all components and devices are well connected, turn on the power and setup System BIOS based on your configuration.
6. Install peripheral, add-on card drivers and test them.
7. If all of above procedures are success, turn-off the power then plug all of them into your computer case.

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2-2 CPU INSTALLATION

ATC-2000 supports P54C and P55C types of CPUs up to 200MHz. For installation, please notice CPU pin 1 must align with the ZIF socket 7 Pin 1 location.

2-2-1 CPU TYPE SELECTION

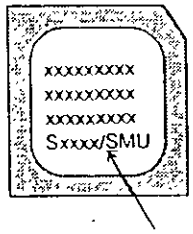
A. INTEL PENTIUM CPU (P54C)

JP10	JP11
1-2	1-2

CPU Core Voltage	3.45V	3.3V
JP9	1-2**	3-4*

* STD set "3-4" ** VRE set " 1-2 "
(The fourth line of the mark on the under-side of the processor contains a code that identifies the voltage level type V is VRE, S is standard)

Intel Pentium CPU, the first letter after '/' denotes voltage type



INTERNAL CPU CLOCK	JP7	JP8	JP3	JP4	Ext x Frq.
75MHz	close	close	1-2	1-2	50x1.5
90MHz	open	close	1-2	1-2	60x1.5
100MHz	close	open	1-2	1-2	66x1.5
120MHz	open	close	2-3	1-2	60x2.0
133MHz	close	open	2-3	1-2	66x2.0
150MHz	open	close	2-3	2-3	60x2.5
166MHz	close	open	2-3	2-3	66x2.5
180MHz	open	close	1-2	2-3	60x3.0
200MHz	close	open	1-2	2-3	66x3.0

B. INTEL PENTIUM CPU (P55C)

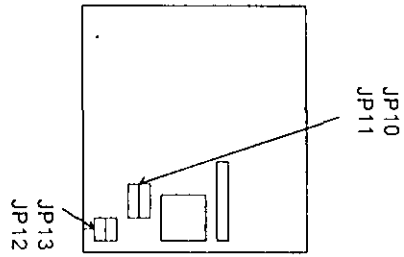
Besides CPU clock setting, for P55C (MMX) CPU you have to set JP10/JP11/JP12/JP13 based on its CPU I/O voltage, and JP9 based on its core voltage.

CPU Core Voltage	3.45V	3.3V	2.9V	2.8V*	2.7V
JP9	1-2	3-4	5-6	7-8	9-10

*Currently, Intel P55C is released 2.8V core voltage only. Please confirm this with your system supplier before you install P55C CPU.

I/O VOLTAGE	JP10	JP11	JP12	JP13
VI/O = 3.3V	2-3	2-3	close	open

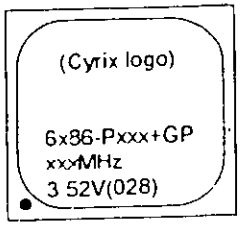
INTERNAL CPU CLOCK	JP7	JP8	JP3	JP4	Ext.x Frq.
166MHz	close	open	2-3	2-3	66x2.5
180MHz	open	close	1-2	2-3	60x3.0
200MHz	close	open	1-2	2-3	66x3.0



C. Cyrix 6x86 CPU

JP9	JP10	JP11
1-2	1-2	1-2

INTERNAL CPU CLOCK	JP7	JP8	JP3	JP4	Ext.x Frq.
P120+ @ 100MHz	close	close	2-3	1-2	50x2.0
P133+ @ 110MHz	open	open	2-3	1-2	55x2.0
P150+ @ 120MHz	open	close	2-3	1-2	60x2.0
P166+ @ 133MHz	close	open	2-3	1-2	66x2.0



The bottom line of the mark on the processor contains a code 028 that identifies the voltage level type. If the code is 016 or others, or no marking then please contact your dealer

D. AMD K5CPU

JP9	JP10	JP11
1-2	1-2	1-2

INTERNAL CPU CLOCK	JP7	JP8	JP3	JP4	Ext.x Frq.
PR75ABR 75MHz	close	close	1-2	1-2	50x1.5
PR90ABQ 90MHz	open	close	1-2	1-2	60x1.5
PR100ABQ 100MHz	close	open	1-2	1-2	66x1.5
PR120ABQ 90MHz	open	close	1-2	1-2	60x1.5
PR133ABQ 100MHz	close	open	1-2	1-2	66x1.5
PR150ABQ 120MHz	open	close	2-3	1-2	60x2.0

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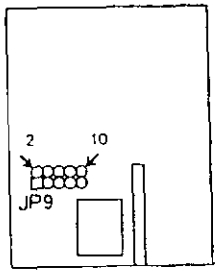
2-2-2 CPU VOLTAGE SETTING

JP9 is used to various CPU core voltage types, please refer to CPU's marking on/under CPU and its user's manual:

CPU		JP9
INTEL (P54C)	STD	3-4
	VRE	1-2
Cyrix	6x86(028)	1-2
AMD	K5	1-2

(※ pin5 ~ pin10 are reserved for dual voltage CPUs)

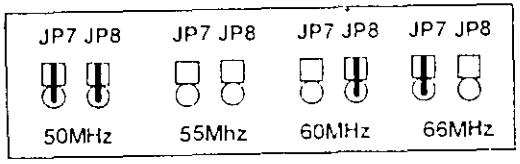


2-2-3 CPU CLOCK SETTING

The following setting is for CPU speed released later than 2-1-1.

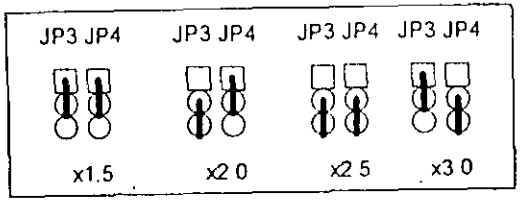
EXTERNAL CPU CLOCK	JP7	JP8
50(MHz)	close	close
55(MHz)	open	open
60(MHz)	open	close
66(MHz)	close	open

External CPU Clock :



INTERNAL CPU CLOCK	JP3	JP4
INTEL EXTERNAL CLOCK X 1 5	1-2	1-2
INTEL EXTERNAL CLOCK X 2.0	2-3	1-2
INTEL EXTERNAL CLOCK X 2 5	2-3	2-3
INTEL EXTERNAL CLOCK X 3 0	1-2	2-3

Internal CPU Clock :



2-3 SYSTEM MEMORY INSTALLATION

ATC-2000 provides four 72-pin SIM sockets for system memory expansion from 4MB to 256MB. These four SIMs are arranged to two banks, Bank0 (SIM 1, 2) and Bank1(SIM 3, 4), please refer to page A. Each bank provides 64-bit wide data path.

The mainboard accepts Fast Page Mode DRAM, and EDO Mode (Extended Data Out) DRAM, with a speed at least 70 nanosecond. You should plug DRAM modules into two sockets (same bank) or four sockets at one time. Each pair of modules must be the same size, type, and speed; no matter single-side or double-side module. Please plug in Bank 0 firstly if you only have 2 modules. The mainboard supports mixing of EDO DRAM SIMMs with fast page mode DRAM SIMMs among different banks; please plug EDO in Bank 0, if you only have 2 EDO modules

If you install more than 64MB DRAM on ATC-2000, and would like to get more than 64MB cacheable size function, you should plug one 16K8 (or 32K8) TAG RAM into U16A socket, and change BIOS value of 'L2 Cache Cacheable Size' to **'512MB'**. (refer to the screen of "CMOS SETUP UTILITY"., page 32)

※ System Memory Combinations Options ※

BANK0 SIM 1, 2	BANK1 SIM 3, 4	Total Memory SIM 1- 4
2MBx2	-	4MB
-	2MBx2	4MB
4MBx2	-	8MB
-	4MBx2	8MB
8MBx2	-	16MB
-	8MBx2	16MB
4MBx2	4MBx2	16MB
4MBx2	8MBx2	24MB

- continue -

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x2	4MBx2	24MB
16MBx2	-	32MB
-	16MBx2	32MB
8MBx2	8MBx2	32MB
4MBx2	16MBx2	40MB
16MBx2	4MBx2	40MB
8MBx2	16MBx2	48MB
16MBx2	8MBx2	48MB
32MBx2	-	64MB
-	32MBx2	64MB
16MBx2	16MBx2	64MB
4MBx2	32MBx2	72MB
32MBx2	4MBx2	72MB
8MBx2	32MBx2	80MB
32MBx2	8MBx2	80MB
16MBx2	32MBx2	96MB
32MBx2	16MBx2	96MB
64MBx2	-	128MB
-	64MBx2	128MB
32MBx2	32MBx2	128MB
4MBx2	64MBx2	136MB
64MBx2	4MBx2	136MB
8MBx2	64MBx2	144MB
64MBx2	8MBx2	144MB
16MBx2	64MBx2	160MB
64MBx2	16MBx2	160MB
32MBx2	64MBx2	192MB
64MBx2	32MBx2	192MB
64MBx2	64MBx2	256MB

2-4 SRAM INSTALLATION

ATC-2000 is built-in 256KB or 512KB Sync. Pipeline Burst SRAM on board and provides a Sync. SRAM module in COAST slot for further expansion. The maximum capacity is 512KB.

※ System Memory Combinations Options ※

SRAM TYPE	SRAM SIZE	DATA SRAM	TAG SRAM
Synchronous on board*	256KB	32K32 x 2pcs	16K8 or 32K8 x 1pcs
	512KB	64K32 x 2pcs	
Synchronous module	256KB	32K32 x 2pcs	16K8 or 32K8 x 1pcs

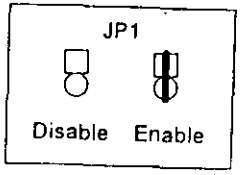
* on board DATA SRAM chips loaction are U24 and U25, TAG SRAM chip location is U16. U16A socket is used for DRAM installed more than 64MB. (refer to 2-3)

※ Upgrade Procedure :

For upgrading your Sync. SRAM from 256KB to 512KB by using COAST Module, you should plug-in the KIT-256 module, then set JP1 to "open" (disable the original TAG on board). You must use KIT-256 for upgrading your system to 512KB Sync. SRAM , please contact your system dealer about this information. It does not need any BIOS value adjustments for upgrading the SRAM size.

On Board TAG	JP1
Disable	open
Enable	close

(If your module is without Tag RAM, please set JP1 "close")



2-5 OTHER JUMPERS AND CONNECTORS DESCRIPTION

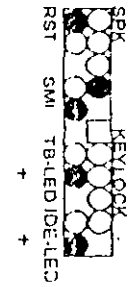
The location of following jumpers please refer to page A

Jumper	Function	Remark
JP5	CMOS	open: Normal * close: Clear CMOS
JP6	ATBUS CLK	open: PCI CLK/3 for external CPU clock 50MHz close: PCI CLK/4 for external CPU clock 60, 66MHz

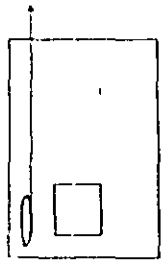
* is default setting

The locations of following connectors are indicated in page A,B When you plug a cable into the following I/O connectors, you should have the pin 1 edge of the cable aligned with the pin 1 end of the connector.

CN8 : Speaker, Keyboard Lock, Reset, SMI, Turbo LED, and IDE LED connectors



SPK : speaker
- Speaker
- GND
- GND
- VCC



KEYLOCK : keyboard lock switch and power LED connector
- Power LED +
- N/C
- GND (power)
- Keylock
- GND (keylock)

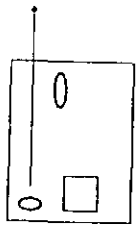
RST : Reset connector
- Reset Signal
- GND

SMI : SMI lead
- GND
- SMI Signal

TB-LED : Turbo LED indicator, LED on when system runs higher speed
- GND
- +5V

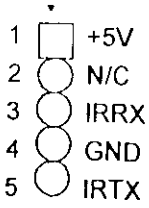
IDE-LED : IDE devices indicator LED connector. IDE-LED stays ON indicates
- GND on-borad IDE devices on operation
- +5V If plug wire into wrong connector, color of LED will be lighter and the IDE devices can still function properly.

1 GND
2 +12V
3 GND



J1 : CPU cooling fan connector. Wire with +12V voltage (most likely red wire) must be plugged into pin2, and GROUND wires (most likely black wires) must be plugged into pin1 and/or pin3. please confirm the wire color represtation with your supplier.

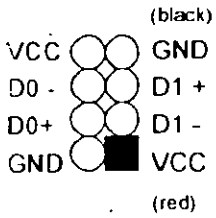
CAUTION: Plug wire into wrong connector will DAMAGE fan and mainboard.

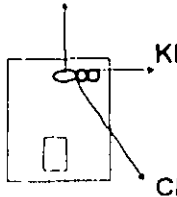


IR1 : Infrared module connector.

(67)

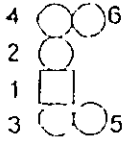
CN9 : Universal Serial Bus connector, this is used to connect USB devices through an optional dual head cable with a iron plane.





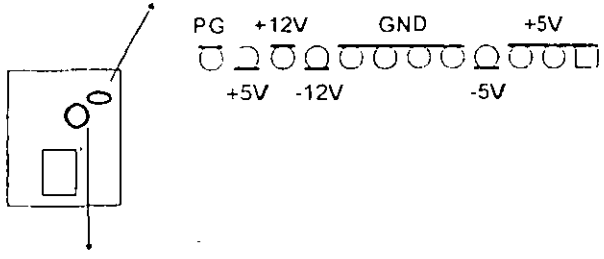
KB1 : 5-pin AT style compatible keyboard connector.

CN1 : PS/2 mouse connector, which is used to connect an optional cable.



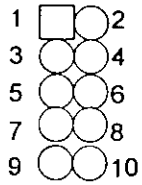
pin1 : data
pin2 : N/C
pin3 GND
pin4 . VCC
pin5 : clock
pin6 : N/C

PW1 : +5 Voltage power supply connector



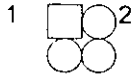
CN2/3:COM1/2

CN2/CN3 : this two connectors are used to connect serial port cables.

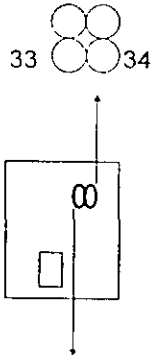


pin	signal name
1	DCD
2	Serial In
3	Serial Out
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	N/C

CN4 : this connector is used to connect floppy disk drive through cable.



pin	signal	pin	signal
2	RWC-	20	STEP-
4	reserved	22	Write Data
6	FDEDIN	24	Write Gate
8	Index-	26	Track 00-
10	Motor EnableA-	28	Write Protect-
12	Drive Sele.B-	30	Read Data-
14	Drive Sele.A-	32	Side 1 Sele.-
16	Motor EnableB-	34	DisketteChange
18	DIR-		
All of odd pins are ground			



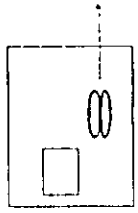
CN5: LPT

CN5 : this connector is used to connect parallel port cable.

pin	signal	pin	signal
1	STROBE-	10	ACK-
2	Data Bit 0	11	BUSY
3	Data Bit 1	12	PE
4	Data Bit 2	13	SLCT
5	Data Bit 3	14	Auto Feed-
6	Data Bit 4	15	ERROR-
7	Data Bit 5	16	INIT-
8	Data Bit 6	17	SLCT IN-
9	Data Bit 7	26	N/C
pin18 -- pin25 are ground			

CN6/CN7 : this two connectors are used to connect IDE devices through IDE cables, total 4 devices.

pin	signal	pin	signal
1	Reset IDE	21	DDRQ0(1)
2	GND	22	GND
3	Host Data 7	23	I/O Write-
4	Host Data 8	24	GND
5	Host Data 6	25	I/O Read-
6	Host Data 9	26	GND
7	Host Data 5	27	IORDY
8	Host Data 10	28	N/C
9	Host Data 4	29	DDAK0-(1)-
10	Host Data 11	30	GND
11	Host Data 3	31	IRQ14*
12	Host Data 12	32	IOCS16-
13	Host Data 2	33	Addr 1
14	Host Data 13	34	N/C
15	Host Data 1	35	Addr 0
16	Host Data 14	36	Addr 2
17	Host Data 0	37	Chip Sele.1P-
18	Host Data 15	38	Chip Sele 3P-
19	GND	39	Activity
20	Key	40	GND



*

IDE1: pin31 is IRQ14;
IDE2: pin31 is IRQ15 or MIRQ0

2-6 IDE DRIVER INSTALLATION

The IDE driver installation procedure is printed on the label of diskette as following :

Setup for DOS/Windows :

1. Starting MS-Windows 3.1 (or 3.11)
2. Select Program Manager, "RUN" a file, then type "A:\setup.exe".
3. Exit MS-Windows, turn power off; then turn power on.

Setup for Windows 95 :

1. Starting Windows 95
2. Select "My Computer"; select "Control Panel"; select "System"; then select "Device Manager", "Hard Disk Controllers".
3. Double-click to remove default driver program, restart computer.
4. Follow the instructions on your screen to install new IDE driver we offer in the 3 5" diskette
5. Exit Windows 95, turn power off; then turn power on.

※ For more information, please refer to Windows 95 manual.

Make sure your HDD should follow ATA standard, and your CD-ROM drive should follow ATAPI standard When you plug-in the IDE devices, please plug your first and second devices into IDE 1 port (Master then Slave), then plug third and forth devices into IDE 2 port. If you have CD-ROM drive, please set it behind hard disk devices as the last device. For example, if you have 2 HDDs and 1 CD-ROM drive, you should set HDD1 and HDD2 in IDE1 Master and Slave, set CD-ROM drive in IDE 2 Master Some of the brands devices combination may not work under this sequence, you can try to re-arrange the device sequence and retry to run it, or contact your vendor.

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CHAPTER 3 AWARD BIOS SETUP

This chapter explains the system BIOS setup, and how to update new BIOS. All BIOS screens showed in the following pages are default values, your system dealer will set up these values according to your demand of computer.

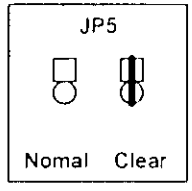
ATC-2000 uses Flash ROM to make BIOS easier to be updated by the floppy disk-based program and to committe Microsoft Windows 95 plug & play feature

- JP5 Setting is for Update System BIOS

open	NORMAL *
close	CLEAR CMOS

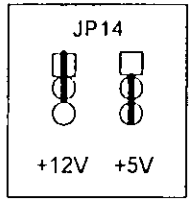
* is default setting

NOTE : If your mainboard is used 'Benchmarq' battery, you should clear CMOS under powering on, otherwise the 'clear' will not work.



- JP14 Setting is for Voltage of Flash ROM

1-2	+12V
2-3	+5V



3-1 UPDATE BIOS PROCEDURES

If the BIOS needs to be updated, it can be obtained on a diskette from your system supplier. The BIOS diskette includes 3 files:

"awdflash.exe" -- BIOS update utility program
"readme.txt"
"(update BIOS filename with version number).rom"

The update procedures are as following:

1. Boot the system to DOS mode in a normal manner.
2. Insert the updated diskette to drive A (or B).
3. Change working directory to floppy drive, A or B, which contains the update BIOS diskette. -- Type "a:\" or "b:\", "ENTER".
4. Run the BIOS update utility -- Type "awdflash", "ENTER".
5. Type "(update BIOS file name with version number).rom", ENTER.
6. Type "N" when the screen displays the message : " Do you want to save BIOS (Y/N) ?".
7. Type "Y" when the screen shows the message : " Are you sure to program (Y/N) ?".
8. Follow instructions displayed on the screen. DO NOT remove the update BIOS diskette from the floppy drive nor turn the system power off until the BIOS update is completed.
9. Exit the utility and turn the system power off, set JP5 to 'close' to clear the CMOS. After about 10 seconds, set JP5 to 'open' (remove the jumper cap), become the normal status.
10. Turn the system power on and test your system working properly or not.

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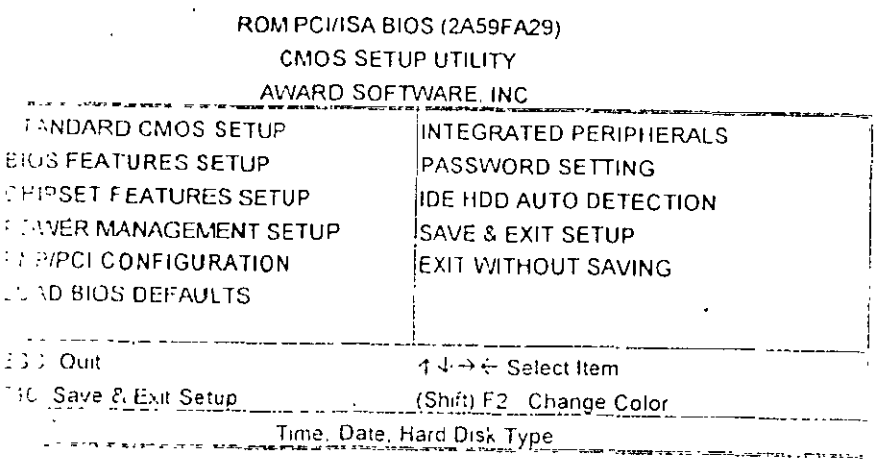
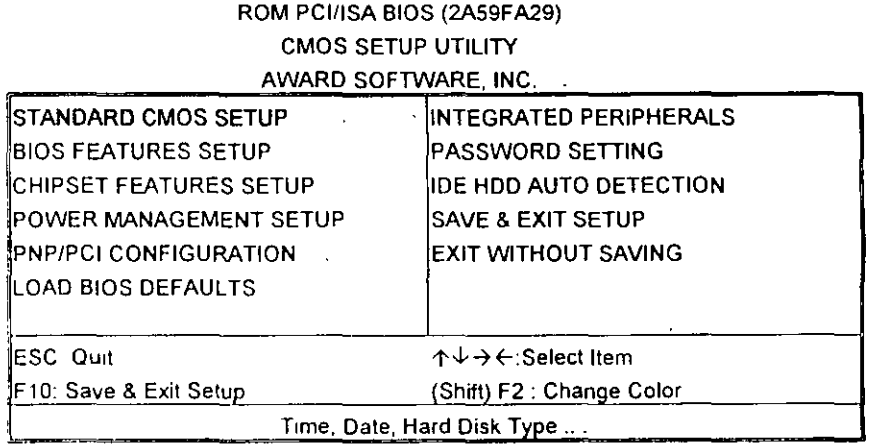
3-2 AWARD SYSTEM BIOS CONFIGURATION SETUP

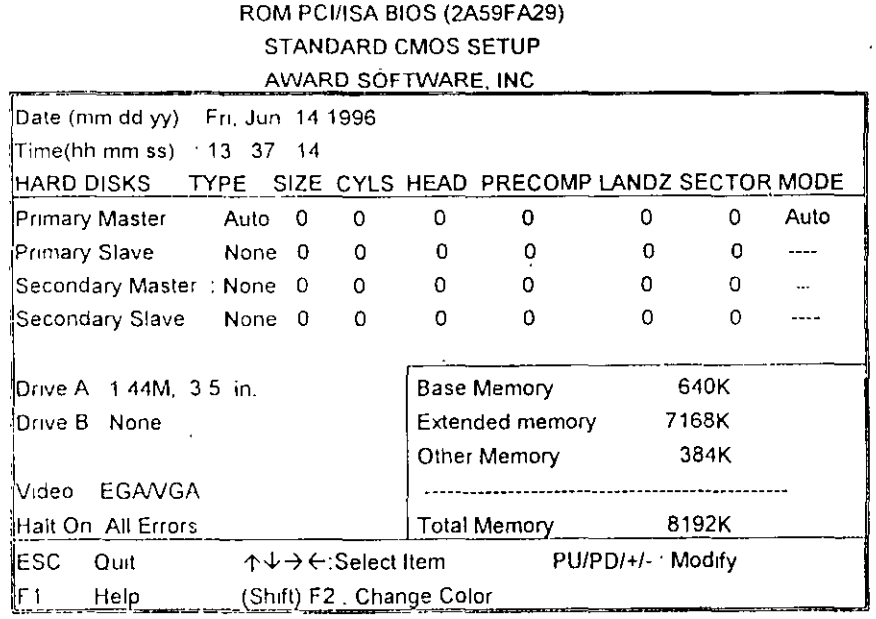
The following pages explain how to set up the system configuration (CMOS) under the AWARD BIOS The SETUP program is stored in the Read-Only-Memory (ROM) on the mainboard To do the SETUP procedure, press the <Del> key when the system is booting up. The following main menu will appear Please select " STANDARD CMOS SETUP" to enter the next screen



The section on the bottom of the main menu explains how to control the screen. The other one section displays the items highlighted in the list

This screen records, some basic hardware information, and set the system clock and error handling. These records can be lost or corrupted if the on-board battery is failed or weak.





Date mm is month, dd is date, yy is year.

date	from 1 to 31
month	from Jan. to Dec.
year	from 1900 to 2099

Time hh is hour, mm is minute, ss is second.

hh	from 0 to 23 (24-hour military -time)
mm	from 0 to 59
ss	from 0 to 59

Primary Master
Primary Slave
Secondary Master
Secondary Slave

These categories identify the types of 2 channels that have been installed in the computer. There are 45 predefined types and 4 user definable types are for Enhanced IDE BIOS Type 1 to 45 are predefined Type **'user'** is user-definable. Press PgUp/PgDn to select a numbered hard disk type or type the number and press<Enter> If you select **'Auto'** BIOS will auto-detect the HDD & CD-ROM Drive at the POST stage and showing the IDE for HDD & CD-ROM Drive. If you select **'user'**, you will need to know the information listed below Enter the information directly from the keyboard and press <Enter> This information should be from your hard disk vender or dealer. If the controller of HDD interface is ESDI, the selection shall be **'Type 1'**: is SCSI, the selection shall be **'None'**. If the device has not been installed select **'NONE'** and press <Enter>.

Type	drive type
SIZE	automatically adjusts
CYLS	number of cylinders
HEAD	number of heads
PRECOMP	write precom
LANDZ	landing zone
SECTOR	number of sectors
MODE	mode type

Drive A
Drive B

This category identifies the types of flop k drive A or drive B that have been installed in the computer.

None	No floppy drive installed
360K, 5.25 in	5.25" PC-type 360KB capacity
1.2M, 5.25 in	5.25" AT-type 1.2MB capacity
720K, 3.5 in	3.5" double-side 720KB capacity
1.44M, 3.5 in	3.5" double-side 1.44MB capacity
2.88M, 3.5 in	3.5" double-side 2.88MB capacity

Video

This category selects the type of video adapter used for the primary system monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

Halt On

This category determines whether the computer will stop if an error is detectd during power up.

No errors	When the BIOS detects a non-fatal error the system will be stopped and you will be prompted
All errors	The system boot will not be stopped for any error that may be detected
All, But Keyboard	The system boot will not stop for a keyboard error, it will stop for all other errors
All, But Diskette	The system boot will not stop for a disk error, it will stop for all other errors
All, But Disk/Key	The system boot will not stop for a disk or keyboard error, it will stop for all other errors

Memory

This category is display-only which is determined by POST (Power On Self Test) of the BIOS. **Base Memory** The value of the base memory is typically 512K or 640K based on the memory installed on the mainboard.

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Extended Memory How much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

Other Memory This refers to the memory located in the 640K to 1024K address space The BIOS is the most frequent user of this RAM area since this is where it shadows RAM.

This screen is a list of system configuration options. Some of them are defaults required by the mainboard's design, others depend on the features of your system.

ROM PCI/ISA BIOS (2A59FA29)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
ESC Quit	↑↓→←.Select Item
F10 Save & Exit Setup	(Shift) F2 : Change Color
Virus, Protection, Boot Sequence	

ROM PCI/ISA BIOS (2A59FA29)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC

Virus Warning	Disabled	Video BIOS Shadow	Enabled
CPU Internal Cache	Enabled	C8000-CBFFF Shadow	: Disabled
External Cache	Enabled	CC000-CFFFF Shadow	Disabled
Quick Power On Self Test	Disabled	D0000-D3FFF Shadow	. Disabled
Boot Sequence	A, C	D4000-D7FFF Shadow	. Disabled
Swap Floppy Drive	Disabled	D8000-DBFFF Shadow	. Disabled
Boot Up Floppy Seek	Enabled	DC000-DFFFF Shadow	. Disabled
Boot Up NumLock Status	On		
Boot Up System Speed	: High		
Gate A20 Option	: Fast		
Typematic Rate Setting	Disabled		
Typematic Rate(Chars/Sec)	6	Esc : Quit	↑↓→←.Select Item
Typematic Delay(Msec)	. 250	F1 Help	PU/PD/+/- : Modify
Security Option	: Setup	F5 Old Values	(SHIFT)F2 : Color
PS/2 mouse function control	Enabled	F6 : Load BIOS Defaults	
PCI/VGA Palette Snoop	Disabled	F7 : Load Setup Defaults	
OS/2 select for DRAM>64MB	Non-OS2		
Report No FDD for WIN 95	No		

Virus Warning

When this item is enabled, the BIOS will monitor the boot sector and partition table of the hard disk drive for any attempt at modification. If an attempt is made, the BIOS will halt the system and the following error message will appear. Many disk diagnostic programs which attempt to access the boot sector table can cause the above warning message. If you will be running such a program, we recommend that you first disable Virus Protection beforehand

```
! WARNING !

Disk boot sector is to be modified
Type 'Y' to accept write or 'N' to abort write
Award Software, Inc
```

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

CPU Internal Cache
External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design. The default value is'enabled'

Quick Power On Self Test

This category speeds up Power On Self Test after you power up the computer. If you set. Enabled, BIOS will shorten or skip some check items during POST.

Boot Sequence

This category determines which drive to se first for the disk operating system (i.e.,DOS).

C,A	System will first search for HDD then FDD
A,C	System will first search for FDD then HDD
CDROM,C, A	System will first search for CDROM then HDD, and next is FDD
C,CDROM, A	System will first search for HDD then CDROM, and next is FDD

Swap Floppy Drive

This item allows you to determine whether enable the swap floppy drive or not.

Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 tracks (360K) or 80 tracks (720K, 1.2M, 1.44M)

Enabled	BIOS searchs for floppy disk drive to determine if it is 40 or 80 tracks
Disabled	BIOS will not search for the type of floppy disk drive by track number

Boot Up NumLock Status

This allows you to determine the default state of the numeric keypad By default, the system boots up with NumLock on.

Boot Up System Speed

Selects the default system speed - the normal operating speed at power up.

Gate A20 Option

This entry allows you to select how the gate A20 is handled The gate A20 is a device used to address memory above 1 MB. Normal is keyboard; Fast is chipset.

Typematic Rate Setting

This determines if the typematic rate is to be used. When disabled, continually holding down a key on your keyboard will generate only one instance.

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Typematic Rate (Chars/Sec)

When the typematic rate is enabled, this section allows you select the rate at which the keys are accelerated.

6	6 characters per second
8	8 characters per second
10	10 characters per second
12	12 characters per second
15	15 characters per second
20	20 characters per second
24	24 characters per second
30	30 characters per second

Typematic Delay (Msec)

When the typematic rate is enabled, this section allows you select the delay between when the key was first depressed and when the acceleration begins.

250	250 msec
500	500 msec
750	750 msec
1000	1000 msec

Security Option

This category allows you to limit access to the system and Setup, or just to Setup

System	The system will not boot and access to Setup will be defined if the correct password is not entered at the prompt
Setup	The system will boot, but access to Setup will be defined if the correct password is not entered at the prompt

To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

PCI/VGA Palette Snoop

It determines whether the MPEG ISA/VESA VGA cards can work with PCI/VGA or not.

Enabled	When PCI/VGA working with MPEG ISA/VESA VGA Card
Disabled	When PCI/VGA not working with MPEG ISA/VESA VGA Card

OS Select for DRAM > 64MB

This item allows you to access the memory that over 64MB in OS/2

Video BIOS Shadow

Determines whether video BIOS will be copied to RAM However it is optional depending on chipset design Video Shadow will increase the vido speed

C8000 - CBFFF Shadow
DC000 - DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of onboard SCSI

Report No FDD For WIN 95

For Windows 3.1x users set 'NO' (default); for Windows 95 users set 'NO' or 'YES'

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This screen cor the setting for the chipset on the mainboard.

ROM PCI/ISA BIOS (2A59FA29)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	

ESC Quit	↑↓→← Select Item
F10 Save & Exit Setup	(Shift) F2 Change Color

AT Clock, DRAM Timmings.

ROM PCI/ISA BIOS (2A59FA29)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC

Auto Configuration	Enabled	Memory Parity/ECC Check	Disabled
DRAM Timing	70 ns	Single Bit Error Report	Enabled
DRAM RAS# Precharge Time	4	L2 Cache Cacheable Size	64MB
DRAM R/W Leadoff Timing	7/6	Chipset NA# Asserted	Enabled
Fast RAS# To CAS# Delay	3	Pipeline Cache Timing	Faster
DRAM Read Burst (EDO/FPM)	x333/x444	Passive Release	Enabled
DRAM Write Burst Timing	x333	Delayed Transaction	Enabled
Turbo Read Leadoff	Disabled		
DRAM Speculative Leadoff	Disabled		
Turn-Around Insertion	Disabled		
ISA Clock	PCICLK/4		
System BIOS Cacheable	Disabled		
Video BIOS Cacheable	Disabled		
8-bit I/O Recovery Time	3		
16-bit I/O Recovery Time	2	Esc Quit	Select Item
Memory Hole At 15M-16M	Disabled	F1 Help	PU/PD/+/- Modify
Peer Concurrency	Enabled	F5 Old Values	(Shift)F2 Color
Chipset Special Features	Disabled	F6 Load BIOS Defaults	
DRAM ECC/PARITY Select	Parity		

Auto Configuration Pre-defined values for DRAM, cache... tin according to CPU type & system clock. When this item is enabled, the pre-defined items will become SHOW-ONLY.

DRAM Timing The DRAM speed is controlled by the DRAM timing Registers. The timings programmed into this register are dependent on the system design.

DRAM RAS# Precharge Time DRAM must continually be refreshed or it will lose its data. Normally, DRAM is refreshed entirely as the result of a single request. This option allows you to determine the number of CPU clocks allocated for the Row Address Strobe to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.

Fast RAS# to CAS# Delay When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS to Column Address Strobe (CAS).

DRAM Read Burst (EDO/FPM) ***DRAM Write Burst Timing*** This sets the timing for burst mode read (or writes) from DRAM. Burst read and write requests are generated by the CPU in four separate parts. The first part provides the location within the DRAM where the read or write is to take place while the remaining three parts provide the actual data. The lower the timing numbers, the faster the system will address memory.

ISA Clock This item allows you to select the PCI clock type. Choices are PCI CLK/3; PCI CLK/4

System BIOS Cacheable When enabled, accesses to the system BIOS ROM addressed at F0000H-FFFFFH are cached, provided that the cache controller is enabled

FACULTAD DE INGENIERIA U.N.A.M.
DIVISION DE EDUCACION CONTINUA

MANTENIMIENTO DE PC'S Y PERIFERICOS

(PARTE II)

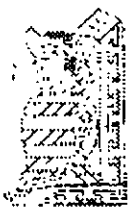
7.- DISCOS DUROS

NOVIEMBRE - DICIEMBRE DE 1998

Palacio de Mineria Calle de Tacuba 5 Primer piso Deleg Cuauhtemoc 06000 Mexico, D F APDO Postal M 2285
Telefonos 512-8955 512-5121 521-7335 521-1987 Fax 510-0573 521-4020 AL 25

MANTENIMIENTO DE PC´S Y PERIFERICOS
PARTE II

7.- DISCOS DUROS



NOVIEMBRE DE 1998

DISCOS DUROS

Formateo Físico: Definición de:
- Cabezas
- Cilindros
- Sectores
- Pistas
- Clusters

Formateo Lógico: Definición de las zonas de:
- Boot
- F.A.T.
- DIR
- Datos

apuntes

METODOS DE REGISTRO

- MFM (modulación de frecuencia modificada)
- RLL (longitud de corrida limitada 2,7)
- ARLL (longitud de corrida avanzada limitada)
- ZBR (registro de bits por zona)

METODOS DE REGISTRO

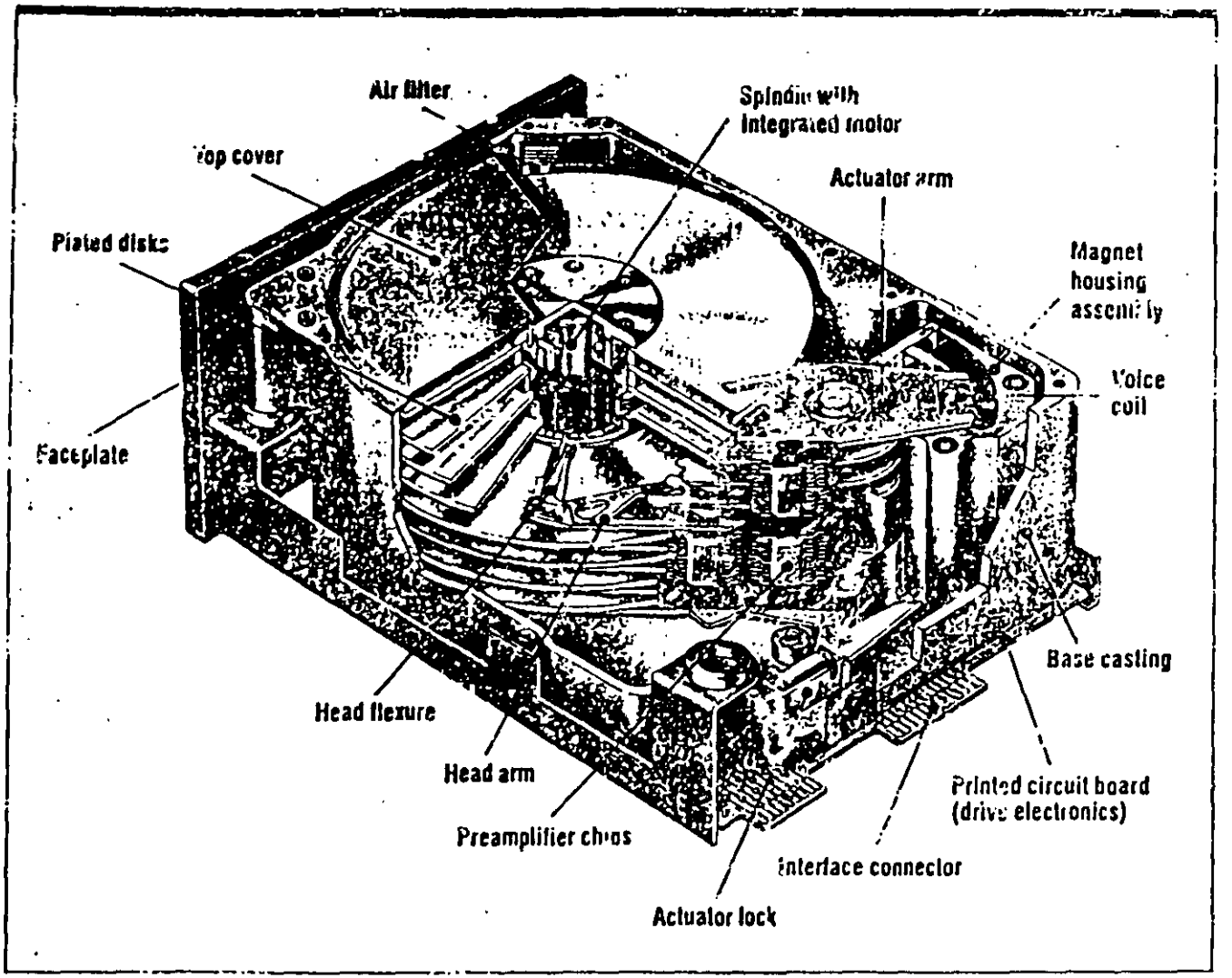
Tipo	Sectores por pista	Velocidad de transferencia Mbits/seg
MFM	17	5
RLL	26	7.5
ARLL	34	10
ZBR	varía	7.5-15

Factores de rendimiento de la unidad de disco

- Tiempo de búsqueda
- Capacidad de cilindro
- Tiempo de conmutación de cabezas
- Tiempo de espera
- Velocidad de transferencia de datos

Factores del rendimiento del controlador

- Factor de intercalación
- Administración de la memoria intermedia
- Administración de defectos
- Administración de errores
- Encabezamiento de mandatos
- Desplazamiento angular de conmutación de cabezas
- Desplazamiento angular de cilindros


Air filter
Spindle with integrated motor
Top cover
Actuator arm
Plated disks
Magnet housing assembly
Voice coil
Faceplate
Base casting
Head flexure
Head arm
Printed circuit board (drive electronics)
Preamplifier chips
Interface connector
Actuator lock

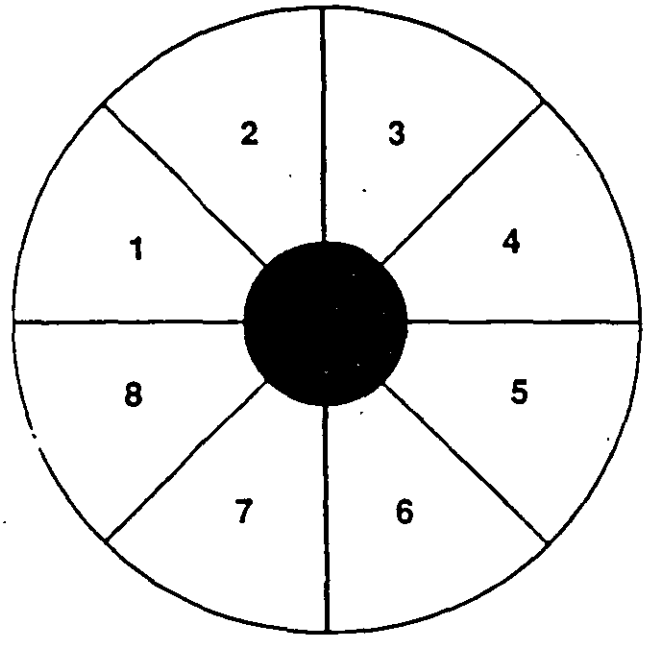
DISCOS DUROS

Formateo Físico: Definición de:
- Cabezas
- Cilindros
- Sectores
- Pistas
- Clusters

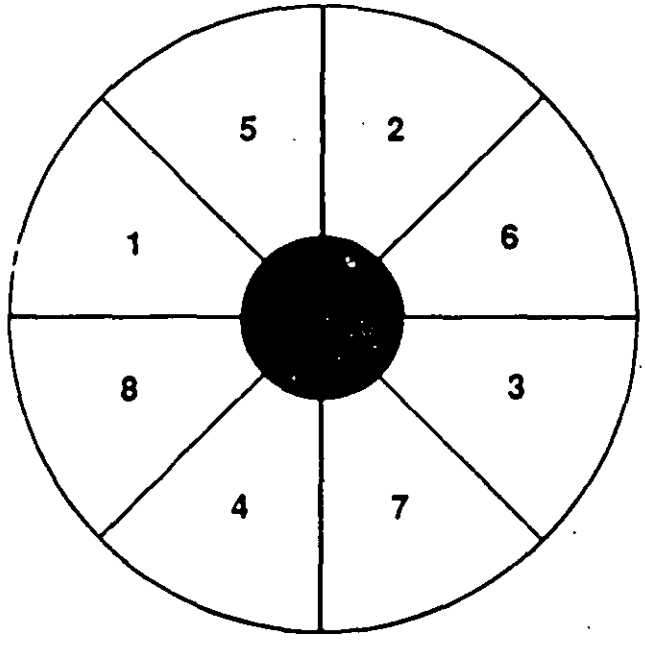
Formateo Lógico: Definición de las zonas de:
- Boot
- F.A.T.
- DIR
- Datos

apuntes

Intercalación de sector

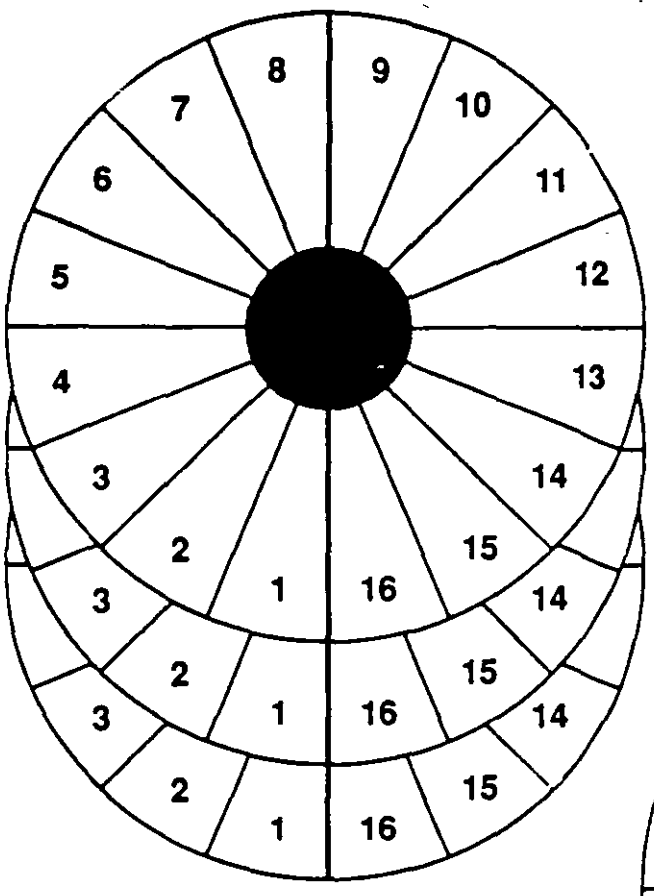


1:1

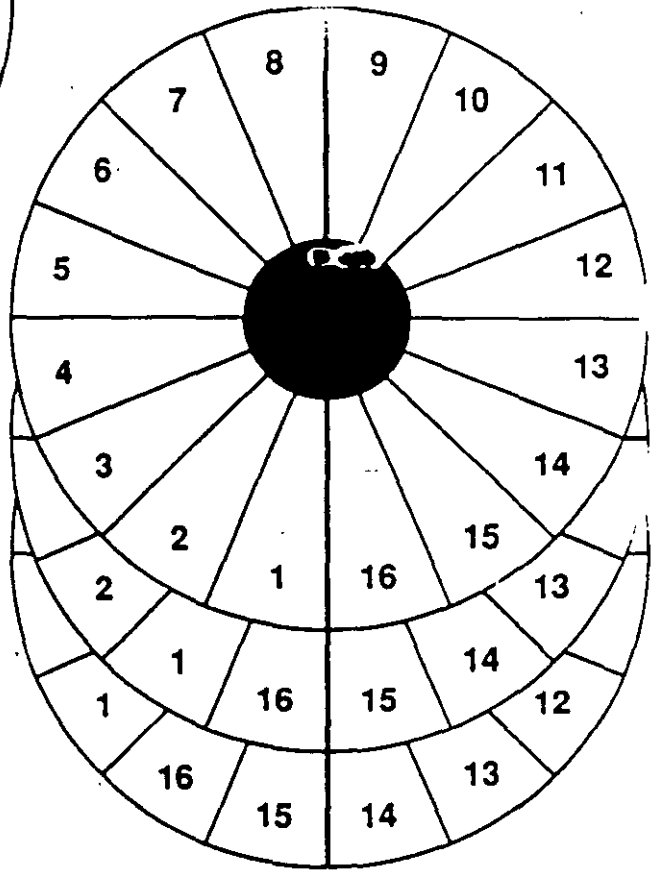


2:1

Desplazamiento angular

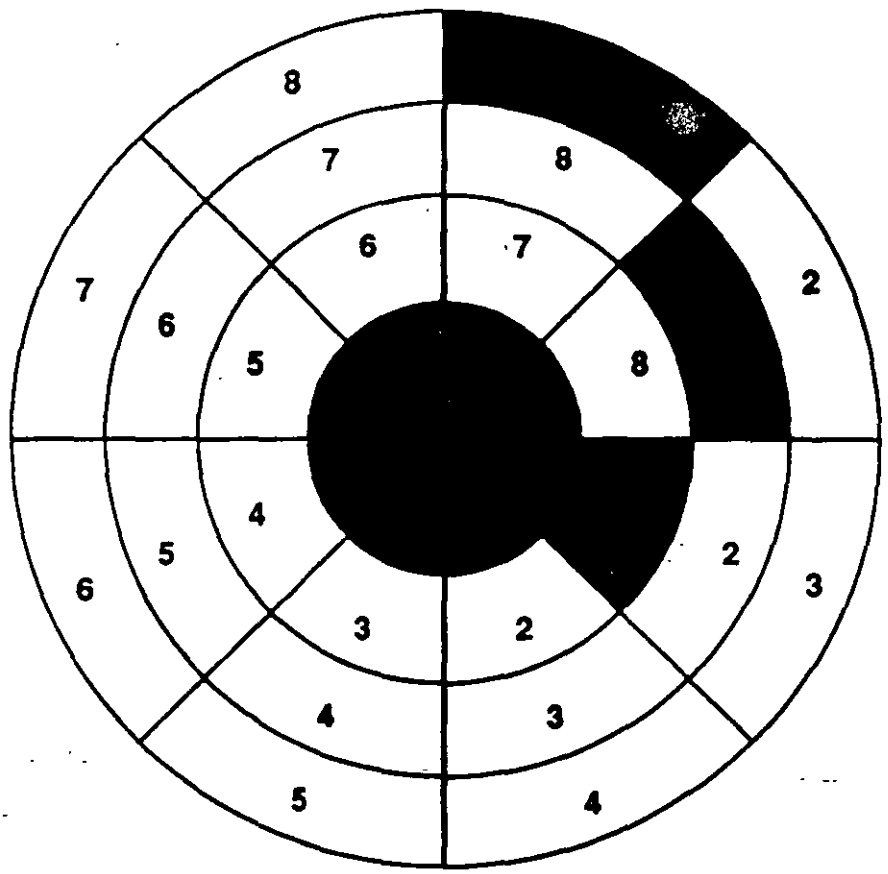


Sin desplazamiento angular de cabeza



Desplazamiento angular de cabeza de 1

Desplazamiento angular de cilindro

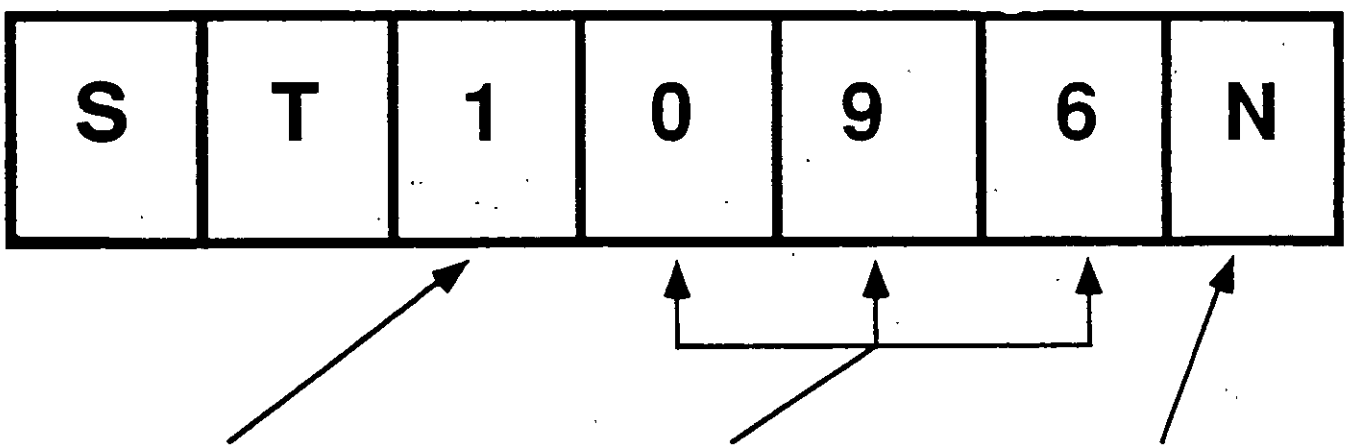


Interfaz SCSI

- Ventajas:
  - Buen rendimiento
  - Respalda la grabación por bites de zona
  - Hasta siete dispositivos
  - Tipos de dispositivos múltiples
  - Capacidades muy grandes
  - Independiente del sistema

- Desventajas:
  - No tiene el respaldo de BIOS IBM
  - No tiene estándares de adaptador de SCSI
  - Se requieren impulsores de software

Números de modelos Seagate



Factor Forma

1XXX = 3.5 pulg

2XX = 5.25 pulg media altura

3XXX = 3.5 pulg altura, 1 pulg

4XXX = 5.25 pulg altura completa

M B

Se especifica sin formatear; v.gr., ST225 es 25 Mbytes sin formatear

Interfaz

No especificada = ST412/MFM

N = SCSI

R = ST412/RLL

A = AT Bus

X = XT Bus

E = ESDI

Video BIOS Cacheable

As with changing the system BIOS above, enabling the Video BIOS cache will cause access to video BIOS addressed at C0000H to C7FFFH to be cached, if the cache controller is also enabled

8 Bit I/O Recovery Time

The recovery time is the length of time, measured in CPU clocks, which the system will delay after the completion of an I/O request This item allows you to determine the recovery time allowed for 8-bit I/O. Choices are from NA, 1 to 8 CPU clocks

16 Bit I/O Recovery Time

This item allows you to determine the recovery time allowed for 16-bit I/O Choices are from NA, 1 to 4 CPU clocks

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards This memory must be mapped into the memory below 16MB

DRAM ECC/ Parity Select

During CPU reads of the DRAM, the 430HX provides error checking and correction or parity of the data.

L2 Cache Cacheable Size

Default value is 64MB, you can get up to 64MB cacheable function based on your DRAM installed size. If you install more than 64MB DRAM and would like to get more than 64MB cacheable size, you should change the value to 512MB, and plug addition one TAG SRAM into U16A socket

This screen controls the 'green' features of this mainboard.

ROM PCI/ISA BIOS (2A59FA29)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
ESC. Quit	↑↓→← Select Item
F10 Save & Exit Setup	(Shift) F2 Change Color
Sleep Timer, Suspend Timer.	

ROM PCI/ISA BIOS (2A59FA29)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC

Power Management	: Disabled	*Power Down & Resume Events*	
PM Control by APM	: Yes	IRQ3 (COM 2)	: OFF
Video Off Method	V/H SYNC	IRQ4 (COM 1)	: OFF
	+Blank	IRQ5 (LPT 2)	OFF
Modem Use IRQ	3	IRQ6 (Floppy Disk)	OFF
		IRQ7 (LPT 1)	: OFF
		IRQ8 (RTC Alarm)	OFF
Doze Mode	Disabled	IRQ9 (IRQ2 Redir)	OFF
Standby Mode	Disabled	IRQ10 (Reserved)	OFF
Suspend Mode	: Disabled	IRQ11 (Reserved)	: OFF
HDD Power Down	Disabled	IRQ12 (PS/2 Mouse)	: OFF
		IRQ13 (Coprocessor)	: OFF
Wake Up Events In Doze & Standby		IRQ14 (Hard Disk)	: OFF
IRQ3 (Wake-Up Event)	OFF	IRQ15 (Reserved)	: OFF
IRQ4 (Wake-Up Event)	OFF		
IRQ8 (Wake-Up Event)	: OFF	Esc Quit	↑↓→← Select Item
IRQ12(Wake-Up Event)	: OFF	F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift) F2: Color
		F6 : Load BIOS Defaults	

Power Management

This category allows you to select the type (or degree) of power saving and is dirctly related to the following modes : **Doze; Standby; Suspend; HDD Power Down.**

Disabled	No power management. Disables all 4 modes
Min. Power Saving	Minimum power management Doze =1hr.; Standby=1hr.; Suspend=1hr.; HDD Power Down=15min
Max. Power Saving	Maximum power management only available for **SL CPU's**.Doze=1min.; Standby=1min ;Suspend=1min.;HD D Power Down=1min
User Defined	Allows you to set each mode indivi-dually When not disabled, each of the ranges are from 1min to 1hr. exect for HDD Power Down which ranges from 1 to 15min and disable

PM Control by APM

When enabled, an Advanced Power Management device will be activated to enhance the Max Power Saving Mode and stop the CPU internal clock If the Max Power Saving is not enabled, this will be present to NO

Video Off Method

This determines the manner in which the monitor is blanked

V/H SYNC + Blank	This selection will cause the system to turn off the vertical and horizontal sync. ports and write blanks to the video buffer
Blank Screen	This option only writes blanks to the video buffer
DPMS	Initial display power management signaling

The Following 4 modes are Green PC power saving function w are only user configuration when 'User Defined' power manage.. ..t has been selected

Doze Mode When enabled and after the set time of system inactivity, the CPU clock will run at slower speed while all other devices still operate at full speed

Standby Mode When enabled and after the set time of system inactivity, the fixed disk drive and the video would be shut off while all other devices still operate at full speed

Suspend Mode When enabled and after the set time of system inactivity, all devices expect the CPU will be shut off

HDD Power Down When enabled and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active

Wake Up Events In Doze & Standby

Power Down & Resume Events

IRQ3 ~ IRQ15 These are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode In effect, the system remains alert for anything which occurs to a device which is configured as **On**, even when the system is in a power down mode. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ (Interrupt ReQuests) to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service. When set off, activity will neither prevent the system from going into a power management mode nor awaken it.

his screen configures the PCI Bus slots.

ROM PCI/ISA BIOS (2A59FA29)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	

ESC: Quit	↑↓→←: Select Item
F10: Save & Exit Setup	(Shift) F2 : Change Color

IRQ Settings, Latency Timers, ...

ROM PCI/ISA BIOS (2A59FA29)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC

Resources Controlled by	Auto	PCI IRQ Actived by	Level
Reset Configuration Data	Disabled	PCI IDE IRQ Map to	PCI-AUTO
		Primary IDE INT#	A
		Secondary IDE INT#	B

Esc. Quit	↑↓→←	Select Item	
F1	Help	PU/PD/+/-	Modify
F5	Old Values	(Shift) F2:	Color
F6	Load BIOS Defaults		

Resource Controlled by — The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play OS such as Windows 95 Choices are Auto and Manual

Reset Configuration Data — This item allows you to determine reset the configuration data or not.

PCI IRQ Actived By — This sets the method by which the PCI bus recognizes that an IRQ service is being requested by a device. Under all circumstances, you should retain the default configuration unless advised otherwise by your system's manufacturer.
Choices are Level and Edge

PCI IDE IRQ Map To — This allows you to configure your system to the type of IDE disk controller in use. If you have equipped your system with a PCI controller, changing this allows you to specify which slot has the controller and which PCI interrupt (A,B,C,D) is associated with the connected hard disk. Select 'PCI Auto' allows the system to automatically determine how your IDE disk system is configured.

This section page des all the items of IDE hard drive and Programmed Input/Output features. See also Section "Chipset FeaturesSetup".

ROM PCI/ISA BIOS (2A59FA29)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	PASSWORD SETTING
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PNP/PCI CONFIGURATION	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
ESC Quit	↑↓→←.Select Item
F10 Save & Exit Setup	(Shift) F2 Change Color

Time, Date, Hard Disk Type .

ROM PCI/ISA BIOS (2A59FA29)
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC

IDE HDD Block Mode	Enabled	
PCI Slot IDE 2nd Channel	Enabled	
On-Chip Primary PCI IDE	Enabled	
On-Chip Secondary PCI IDE	Enabled	
IDE Primary Master PIO	Auto	
IDE Primary Slave PIO	Auto	
IDE Secondary Master PIO	Auto	
IDE Secondary Slave PIO	Auto	
USB Controller	Disabled	
Onboard FDD Controller	Enabled	
Onboard Serial Port 1	Auto	
Onboard Serial Port 2	Auto	
UART 2 Mode	Standard	Esc. Quit ↑↓→← :Select Item
Onboard Parallel Port	378H/IRQ7	F1 Help PU/PD/+/- . Modify
Onboard Parallel Mode	SPP	F5 : Old Values (Shift) F2: Color
		F6 : Load BIOS Defaults

IDE HDD Block Mode This allows your HD controller to use the fast block mode to transfer data to and from your HD drive

Enabled	IDE controller uses block mode
Disabled	IDE controller uses standard mode

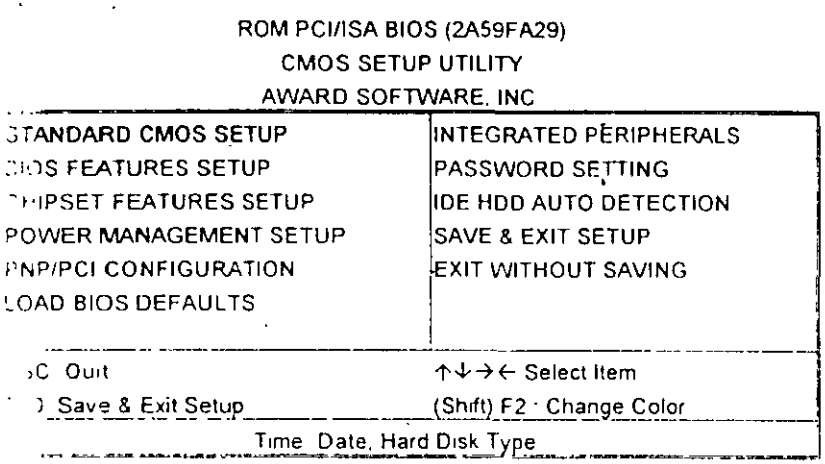
PCI Slot IDE 2nd Channel This item allows you designate an IDE controller board insert into one of the physical PCI slots as your secondary IDE

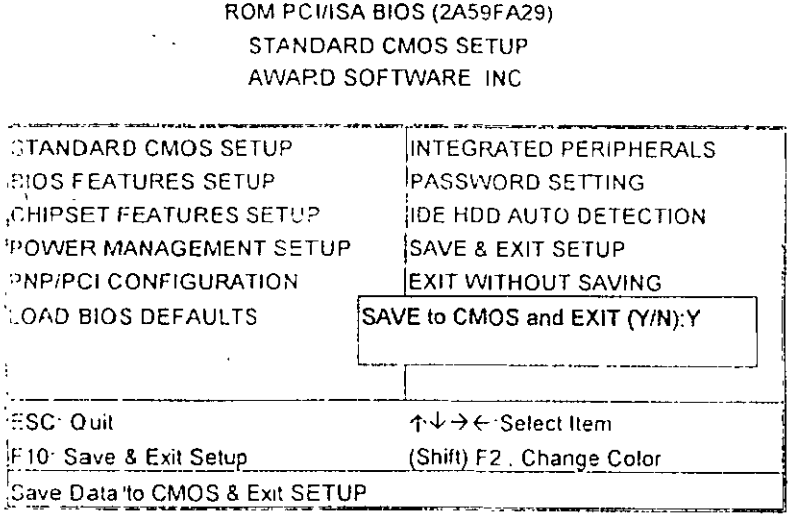
Enabled	External IDE controller designated as the secondary controller
Disabled	No IDE controller occupying a PCI slot

On-Chip Primary PCI IDE / ***On-Chip Secondary PCI IDE*** This setup item allows you either to enable or disable the primary/secondary controller. You might choose to disable the controller if you were to add a higher performance or specialized controller.

IDE Primary Master/Slave PIO / ***IDE Secondary Master/Slave PIO*** PIO - Programmed Input/Output, it allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by themselves. This simpler and more faster. Your system supports five mods, 0 - 4, which primarily differ in timing. When **Auto** is selected, the BIOS will select the best available mode.

The last step is 'save and exit'. If you select this item and press 'Y', then these records will be saved in the CMOS memory on the mainboard. It will be checked every time when you turn your computer on.





LOAD BIOS DEFAULTS

When your mainboard has problems and need to debug or troubleshoot the system, you can use this function.
The default values loaded only affect the BIOS Features Setup, Chipset Features Setup, Power Management Setup and PNP/PCI Configuration Setup. There is no effect on the Standard CMOS Setup. To use this function, select it from main menu and press <Enter>. A line will appear on the screen asking if you want to load the BIOS default values. Press <Yes> and <Enter> then the BIOS default values will be loaded.

LOAD SETUP DEFAULTS

This allows you load optimal settings which are stored in the BIOS ROM. The default values loaded only affect the BIOS Features Setup, Chipset Features Setup, Power Management Setup and PNP/PCI Configuration Setup. There is no effect on the Standard CMOS Setup To use this function, select it from main menu and press <Enter>. A line will appear on the screen asking if you want to load the Setup default values. Press <Yes> and <Enter> then the Setup default values will be loaded.

SUPERVISOR PASSWORD / USER PASSWORD

This allows you to set the password the mainboard defaults password disabled.
Enter/Change password : Enter the current password, at the prompt key-in your new password (up to eight alphanumeric characters), press <Enter>. At the next prompt, confirm the new password by typing it and press <Enter> again.
Disable password : Press <Enter> key instead of entering a new password when the 'Enter Password' dialog box appears A message will appear confirming that the password is disable.

If you set both supervisor and user passwords, only the supervisor password allows you to enter the BIOS SETUP program.

CAUTION :If you forget your password, you must disable the CMOS by turning power off and set JP5 'close'. Then reload the system. Please refer to page 13.

IDD HDD AUTO DETECTION

This allows you to detect IDE hard disk drivers' parameters and enter them into 'Standard CMOS Setup' automatically

If the auto-detected parameters displayed do not match the ones that should be used for your hard drive, do not accept them. Press <N> to reject the values and enter the correct ones manually on the Standard CMOS Setup screen.

SAVE & EXIT SETUP

This allows you to save the new setting values in the CMOS memory and continue with the booting process. Select what you want to do, press <Enter>.

EXIT WITHOUT SAVING

This allows you to exit the BIOS setup utility without recording any new values or changing old ones

※ Control Key Description ※

UP ARROW	↑	Move to previous item
DOWN ARROW	↓	Move to next item
LEFT ARROW	←	Move to the item in the left hand
RIGHT ARROW	→	Move to the item in the right hand
Esc KEY	Esc	Main Menu : Quit and not save changes Setup menu : Exit current page and return to main menu
PgUp KEY		Increase the numeric value or make changes
PgDn KEY		Decrease the numeric value or make changes
F1 KEY	Help	General help
F2 KEY	< Shift > +F2	Change color from total 16 colors
F5 KEY	Old Value	Restore the pervious CMOS value from CMOS
F6 KEY	Load BIOS default	Load the default CMOS value from BIOS default table
F7 KEY	Load setup default	Load Setup default
F10 KEY	Save & Exit Setup	Save all the CMOS changes and Exit setup, only for Main Menu

APPENDIX A

※※ TECHNICAL SUPPORT REQUEST FORM ※※

If the mainboard doesn't function properly, please complete the following informationand return it to your system dealer. If further information is needed to describe the problem, please attach with separate sheets.

Model No . ATC-2000 Date of Purchase : _____

Serial No . _____

HARDWARE .

	BRAND	MODEL	SPEED	Q'TY
CPU				
SIM Module				
TAG SRAM				
Sync Cache				

DRAM _____MB (__ EDO, __FastPage, __ECC)

Hard Disk Interface Controller __ __ IDE, ____ SCSI

Hard Disk Brand _____, Model _____, Capacity _____

Display Controller Brand _____,Model _____

Controller Chip Brand ._____,Model :_____

SOFTWARE:

AWARD SYSTEM BIOS Version _____ Date Code _____

Keyboard BIOS: Brand _____

Other Add-on Cards Information

Add-on Card	Bus Interface	Model	Remark

Error Description